XC7Z020-2CLG484I

AMD / Xilinx Zynq®-7000 Z-7020 SoC · Dual ARM® Cortex®-A9 MPCore 766 MHz · Artix™-7 Equivalent PL · 85K Logic Cells · 220 DSP Slices · 560 KB BRAM · 484-Ball CSPBGA 19×19 · Industrial Grade · Speed Grade −2

1. Quick Description

XC7Z020-2CLG484I is an **AMD/Xilinx Zynq-7000 All Programmable SoC** integrating a dual-core ARM Cortex-A9 MPCore processing system (PS) with 28 nm Artix-7 equivalent programmable logic (PL) on one die, combining CPU firmware/RTOS/Linux with FPGA hardware acceleration. The **Z-7020** fabric provides about **85K logic cells**, **53,200 LUTs**, **106,400 flip-flops**, **220 DSP slices** (18×25 MACCs) and **560 KB** block RAM (140 × 36 Kb blocks); the PS runs the Cortex-A9 at **766 MHz** in the −2 speed grade, with on-chip 256 KB RAM, 32 KB L1 and 512 KB L2 cache, an external DDR2/DDR3/DDR3L/LPDDR2 controller, and USB 2.0 OTG, Gigabit Ethernet, SD/SDIO, CAN, UART, SPI and I²C peripherals. Suffix decoding: **-2** speed grade, **CLG484** 484-ball CSPBGA 19×19 mm, **I** industrial grade. **Procurement focus:** confirm the exact speed/grade and ordering code, on-hand quantity and date code, PS/PL power rails and DDR topology, bank I/O standards, package ball map/MSL, and that this standard XC7Z020 (not the AEC-Q100 qualified XA7Z020 variant) matches the target reliability requirements. **Revision, marking and new-vs-refurbished status must be verified before commitment.**

2. Product Overview

The Zynq-7000 family splits each device into a Processing System (PS) built around a dual-core ARM Cortex-A9 MPCore with CoreSight, on-chip memory, external memory controllers and a rich peripheral set, and a Programmable Logic (PL) fabric equivalent to an Artix-7 or Kintex-7 FPGA, coupled through an AXI interconnect and an 8-channel DMA for efficient PS-to-PL data movement. The Z-7020 (XC7Z020) is the mid-density dual-core member with an Artix-7 equivalent fabric: approximately 85K logic cells, 53,200 LUTs, 106,400 flip-flops, 220 DSP slices and 560 KB of block RAM, supporting custom logic, parallel signal processing and hardware acceleration alongside the CPU subsystem.

The PS integrates on-chip 256 KB RAM, 32 KB L1 cache and 512 KB L2 cache, an external DDR2/DDR3/ DDR3L/LPDDR2 memory controller, USB 2.0 OTG, Gigabit Ethernet, SD/SDIO, CAN, UART, SPI and I²C interfaces, plus secure boot with AES, SHA-256 and RSA authentication. The **−2** speed grade runs the Cortex-A9 at 766 MHz; the −1 grade runs 667 MHz and the −3 grade 866 MHz, with corresponding PL timing differences. The **CLG484** package is a 484-ball CSPBGA/CSBGA with 19×19 mm body; the trailing **I** denotes the industrial temperature grade. This part targets industrial IoT, motor control, embedded vision, industrial networking, control panels, medical and instrumentation designs needing both a CPU subsystem and custom FPGA logic in one component. The standard XC7Z020 line is not automotive-qualified; automotive designs use the AEC-Q100 qualified XA7Z020 variant.

3. Key Attributes

FAMILY / TYPE **Zynq-7000 AP SoC (PS + PL)**	PROCESSOR **Dual Cortex-A9 @ 766 MHz**	PROGRAMMABLE LOGIC **Artix-7 equiv. · 85K LC**
DSP SLICES **220 × 18×25 MAC**	BLOCK RAM **560 KB (140 × 36 Kb)**	ON-CHIP MEMORY **256 KB RAM · L1/L2 cache**
EXTERNAL MEMORY **DDR2/DDR3/DDR3L/LPDDR2**	PACKAGE **484-ball CSPBGA 19×19 mm**	GRADE / SPEED **Industrial I · −2 grade**

4. Technical Specifications

Parameter	Value
Manufacturer	AMD, Inc. (formerly Xilinx, Inc.) — Zynq-7000 SoC family
Part Number	XC7Z020-2CLG484I · Z-7020 dual-core SoC; -2 speed grade, CLG484 484-ball CSPBGA, I industrial grade. Verify full ordering code and tray/reel status against the AMD/Xilinx catalog and BOM.
Product Type	All Programmable System-on-Chip (AP SoC): dual Cortex-A9 processing system + Artix-7 equivalent FPGA programmable logic. Not a standalone FPGA, microcontroller, discrete memory device or analog controller.
Memory Density	On-chip: 256 KB on-chip RAM plus 32 KB L1 cache and 512 KB L2 cache; PL block RAM 560 KB (140 × 36 Kb blocks). External memory is provided through the PS DDR2/DDR3/DDR3L/LPDDR2 controller; verify DRAM size, bus width and device selection against the memory design.
Organization	PS: dual Cortex-A9 MPCore with CoreSight, OCM, L1/L2 cache, DDR memory controller and peripherals. PL: 53,200 LUTs, 106,400 flip-flops, 220 DSP slices, 560 KB BRAM; PS-PL coupling via AXI interconnect and 8-channel DMA. Max user I/O: verify per bank from the package pinout (about 200 I/O for the Z-7020 CLG484).
Data Rate	No fixed digital data-rate rating for a memory device; PL/PS interfaces depend on the design. External DRAM controller supports DDR2/DDR3/DDR3L/LPDDR2 at the speed grades defined in the Zynq-7000 datasheet; this Artix-7 equivalent Z-7020 fabric has no high-speed serial transceivers. Verify interface and DDR rates against the chosen reference design and timing report.
Clock Rate	PS CPU: dual Cortex-A9 at 766 MHz in the −2 speed grade (667 MHz −1, 866 MHz −3). PL clock, DDR clock, peripheral clocks and clocking configuration depend on the design and

	clock manager settings; verify all frequencies against timing analysis and the datasheet. This part has no standalone oscillator rating.
Package	CLG484: 484-ball CSPBGA/CSBGA, 19×19 mm body; verify exact ball pitch, ball map, MSL rating, lead-free finish and top-side marking in the official package drawing. Tray packaging reported in distributor listings; confirm pack type in the ordering code.
Operating Temperature Code	I = industrial grade. Zynq-7000 industrial junction range is −40~+100 °C (verify the exact ambient/junction derating in DS188 / the official datasheet); commercial C is 0~+85 °C and extended E covers the extended range. Confirm the grade and temperature derating against the application environment.
Automotive Requirement	Not AEC-Q100 qualified as a standard XC7Z020. The automotive variant is the XA7Z020 with AEC-Q100 qualification (beyond qualification and PPAP documentation available on request). Do not assign this standard industrial part to an automotive BOM without the qualified XA device and its qualification records.
Revision	Device/die revision and ordering-code revision **must be verified** on the actual shipment; cross-check silicon revision, errata and any required software/firmware baseline for the target design.
RFQ Status	**Verify before commitment:** real on-hand quantity, date code, COO, full ordering code, top-side marking, seal/lead condition, new-vs-refurbished status, RoHS status and remaining lifecycle/lead time. Distributor listings often show zero stock with long factory lead time; confirm authorized-channel availability and lifecycle status against the AMD catalog.

5. Typical Application Areas

- **Industrial IoT & embedded control** — motor drives, PLCs, industrial controllers and gateways combining CPU firmware with custom PL logic and PWM/encoder interfacing.
- **Embedded vision & signal processing** — camera pre-processing, image pipelines, DSP acceleration and parallel filtering using the 220 DSP slices and BRAM fabric.
- **Industrial networking & communication** — Gigabit Ethernet, CAN, UART/SPI/I^2C and protocol bridges with PL-implemented interfaces or hardware offload.
- **Medical, instrumentation & test equipment** — data acquisition, mixed-signal control, user interfaces and custom timing/measurement circuits.
- **Robotics & motion control** — sensor fusion, closed-loop control and real-time signal handling split between the Cortex-A9 PS and the PL fabric.
- **Legacy board support & BOM continuity** — replacements and second-source designs for Zynq-7020-based industrial boards where package, power rails and I/O banks match.

6. RFQ Information to Confirm — Alternative / Cross-Reference Parts

SoC substitution must match PS performance, PL density, I/O count, package, power rails, DDR topology and software/IP compatibility. Same-family Zynq-7000 variants are the closest cross-references; other Zynq or FPGA-only devices require a full design review. Verify availability and the exact ordering code against current listings and the datasheet.

Part Number	Listed Description	Key Parameters	Difference vs Target
XC7Z020-1CLG484I	Same Z-7020 die/package, lower speed grade	85K LC · 220 DSP · 560 KB BRAM; Cortex-A9 667 MHz; CLG484 19×19; industrial I	**Speed grade -1**: 667 MHz CPU and slower PL timing vs the 766 MHz -2 grade. Same fabric, package and pinout; downgrade possible only if timing/headroom and power permit, verify design timing closure.
XC7Z010-2CLG400I	Entry Zynq-7000 dual-core SoC, lower PL density	~28K logic cells · 80 DSP · 240 KB BRAM; 400-ball CSPBGA; fewer I/O; -2 grade	**Smaller fabric and I/O** than the Z-7020: lower LUT/DSP/BRAM count and a 400-ball package. Only a drop-in for designs that fit the smaller resource budget; pinout and power rails differ, require redesign/respin.
XC7Z030-2FBG484I	Mid-high Zynq SoC, Kintex-7 equivalent PL	~125K LC · 400 DSP · 1,060 KB BRAM; FBG484 package; dual Cortex-A9	**Higher PL density and DSP/BRAM** with a Kintex-7 equivalent fabric and FBG484 package. Upward alternative for designs needing more logic/processing; ball map, power and I/O banks differ, not a pin-compatible swap.

Confirm at RFQ: (1) full official ordering code, speed grade, temperature grade and tray/reel pack; (2) real on-hand quantity, date code, COO, silicon revision, marking and new-vs-refurbished condition; (3) PS/PL core and auxiliary power rails, power-up sequencing and current budget; (4) external DDR2/DDR3/DDR3L/LPDDR2 topology, bus width and timing; (5) package ball map, pitch, MSL, bank I/O standards and PCB footprint; (6) RoHS status, lifecycle, lead time and any AEC qualification requirement (use XA7Z020 for automotive).

7. Product FAQ

Q1. What type of device is this?

A1. An AMD/Xilinx Zynq-7000 All Programmable SoC: a dual ARM Cortex-A9 MPCore processing system combined with Artix-7 equivalent programmable logic on one die. It is a CPU+FPGA SoC, not a standalone FPGA, MCU, discrete memory chip or analog controller.

Q2. What do the suffixes -2CLG484I mean?

A2. **-2** is the speed grade (Cortex-A9 766 MHz); **CLG484** is the 484-ball CSPBGA/CSBGA 19×19 mm package; **I** is the industrial temperature grade. Confirm the full ordering code, pack type and grade against the official datasheet and BOM before purchasing.

Q3. What are the main PL and PS resources?

A3. PL: about 85K logic cells, 53,200 LUTs, 106,400 flip-flops, 220 DSP slices and 560 KB BRAM. PS: dual Cortex-A9 at 766 MHz, 256 KB on-chip RAM, 32 KB L1 and 512 KB L2 cache, DDR2/DDR3/DDR3L/LPDDR2 controller, USB 2.0 OTG, GbE, SD/SDIO, CAN, UART, SPI and I^2C. Verify exact counts and I/O banks against DS188.

Q4. What external memory does it support?

A4. The PS memory controller supports DDR2, DDR3, DDR3L and LPDDR2 devices; DRAM size, bus width, speed grade and layout depend on the reference design and timing closure. On-chip memory (256 KB RAM plus cache) is separate from external DRAM; verify the memory schematic and controller configuration.

Q5. What temperature range and grade does it carry?

A5. The trailing I denotes the industrial grade, specified over the Zynq-7000 industrial junction range (−40~+100 °C; verify ambient/junction derating in the official datasheet). Commercial C is 0~+85 °C; do not substitute grades without checking thermal and timing derating.

Q6. Is this part qualified for automotive use?

A6. No. The standard XC7Z020 is an industrial/commercial device without AEC-Q100 qualification. Automotive applications must use the XA7Z020 automotive variant with AEC-Q100 qualification and the available PPAP/qualification documentation; do not claim automotive compliance for this XC part.

Q7. Is this part still in production, and what about lead time?

A7. AMD continues support for 7-series and Zynq-7000 devices through at least 2035, but distributor listings often show zero current stock with long factory lead time for this specific grade/package. Confirm on-hand quantity, date code, COO, silicon revision, RoHS status and new-vs-refurbished condition with the authorized channel before committing to production.

8. RFQ Tip

When sending an RFQ, state explicitly: **(a)** the **full official ordering code** (XC7Z020-2CLG484I), speed/grade and pack type; **(b)** the **real on-hand quantity, date code, COO, silicon revision, marking and new-vs-refurbished condition** you can commit; **(c)** PS/PL core and auxiliary power rails, power-up sequencing and current budget; **(d)** external DDR topology, bus width and timing; **(e)** package ball map, pitch, MSL and bank I/O standards; **(f)** temperature grade, RoHS status, lifecycle and lead time, with a condition report before committing.

Document Description: The content on this page is compiled based on publicly available technical data and authorized channel parameters, intended for RFQ communication and preliminary selection reference. For final procurement, design integration, or replacement confirmation, please refer to the customer's original BOM, official specifications, project certification requirements, and actual supply documentation.