A4B16QH8BNWESW

16GB DDR4-3200 Wide Temperature

VLP Registered ECC DIMM

Datasheet

Version 1.0

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Revision History

Date	Version	Changes compared to previous issue
Mar. 03th, 2021	1.0	1st release.

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1. Product Description

The ATP A4B16QH8BNWESW is a high performance 16GB DDR4-3200 VLP (Very Low Profile) Registered ECC SDRAM memory module. It is organized as 2048M x 72 in a 288-pin Dual-In-Line Memory Module (DIMM) package. The module utilizes eighteen 1024Mx8 DDR4 SDRAMs in FBGA package. The module consists of a 512-byte serial EEPROM, which contains the module configuration information.

2. Key Feature

- Operation Temperature (TA) : -40°C ~ +85°C
- High Density: 16GB (2048M x 72)
- DIMM Rank: 2 Rank
- Cycle Time: 0.62ns (1600MHz)
- CAS Latency: 22(DDR4-3200), 21(DDR4-2933), 19(DDR4-2666), 17(DDR4-2400), 15(DDR4-2133)
- Power supply: V_{DD}=1.2V ±0.06V
  V_{PP}=2.5V -0.125V / +0.250V
  V_{DDSPD}=2.5V ±10%
- PCB Height: 18.75mm (0.74 inches)
- Weight: 25 grams Max.
- Minimum Thickness of Golden Finger: 30 Micro-inch
- Support ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- 16 internal banks(x8); 4 groups of 4 banks each
- Internal self calibration through ZQ
- Temperature controlled refresh (TCR)
- Asynchronous Reset
- 7.8 μs refresh interval at lower than T_{CASE} 85°C, 3.9μs refresh interval at 85°C < T_{CASE} < 95 °C
- Support address and command signals parity function
- Selectable BC4 or BL8 on-the fly(OTF)
- Dynamic On Die Termination
- Fly-by topology
- Targeted Row Refresh supported (TRR)
- RoHS compliant and Halogen-Free

Part No.	Max Freq.	Interface
A4B16QH8BNWESW	1600MHz (0.62ns@CL=22) x2	POD12

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3. PIN Description

Pin Symbol	Description
Ax	Address Inputs.
A10/AP	Address Inputs / Auto precharge
A12/BC_n	Address Input / Burst chop
ACT_n	Command input: ACT_n indicates an ACTIVATE command.
BAx	Bank address inputs.
BGx	Bank group address inputs.
C0,C1,C2 (RDIMM / LRDIMM only)	Chip ID
CKx_t	Register clock input (positive line of differential pair)
CKx_c	Register clocks input (negative line of differential pair)
CKEx	Clock enable
CSx_n	Chip select (DIMM Rank Select Lines input)
ODTx	Register on-die termination control lines input
PARITY	Parity for command and address
RAS_n[1]/A16	Register row address strobe input
CAS_n[2]/A15	Register column address strobe input
WE_n[3]/A15	Register write enable input
RESET_n	Active LOW asynchronous reset
SAx	Serial address inputs
SCL	Serial clock for temperature sensor/SPD EEPROM
DQx	Data Input /Output
CBx	DIMM ECC check bits
DMx_n/DBIx_n/TDQSx_t	Input data mask and data bus inversion, TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
DQMx	Data Mask
SDA	SPD Data Input /Output
DQSx_t	Data strobes, positive line
DQSx_c	Data strobes, negative line
ALERT_n	Alert output
EVENT_n	Temperature sensor event Output
TDQS_t,TDQS_c (x8 DRAM-based RDIMM only)	Termination data strobe
V_{DD}	Power supply
V_{DDQ}	DRAM DQ power supply
V_{PP}	DRAM activating power supply
V_{REFCA}	SDRAM command/address reference supply
V_{SS}	Ground.
V_{TT}	Power supply for termination of address, command, and control VDD/2.
V_{DDSPD}	Power supply used to power the I^2C bus for SPD.
RFU	Reserved for future use.
NC	No connect:
NF	No function

Note : 1. RAS_n is a multiplexed function with A16
2. CAS_n is a multiplexed function with A15.

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3. WE_n is a multiplexed function with A14.

4. PIN Assignment

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	12V[3],NC	145	12V[3], NC	74	CK0_t	218	CK1_t
2	Vss	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	Vss	76	VDD	220	VDD
4	Vss	148	DQ5	77	VTT	221	VTT
5	DQ0	149	Vss	Key			
6	Vss	150	DQ1	78	EVENT_n	222	PARITY
7	TDQS9_t, DQS9_t	151	Vss	79	A0	223	VDD
8	TDQS9_c, DQS9_c	152	DQS0_c	80	VDD	224	BA1
9	Vss	153	DQS0_t	81	BA0	225	A10/AP
10	DQ6	154	Vss	82	RAS_n/A16	226	VDD
11	Vss	155	DQ7	83	VDD	227	RFU
12	DQ2	156	Vss	84	CS0_n	228	WE_n /A14
13	Vss	157	DQ3	85	VDD	229	VDD
14	DQ12	158	Vss	86	CAS_n/A15	230	NC, SAVE_n[2]
15	Vss	159	DQ13	87	ODT0	231	VDD
16	DQ8	160	Vss	88	VDD	232	A13
17	Vss	161	DQ9	89	CS1_n, NC	233	VDD
18	TDQS10_t, DQS10_t	162	Vss	90	VDD	234	NC, A17[5]
19	TDQS10_c, DQS10_c	163	DQS1_c	91	ODT1, NC	235	NC,C2
20	Vss	164	DQS1_t	92	VDD	236	VDD
21	DQ14	165	Vss	93	C0,CS2_n,NC	237	NC,CS3_n,C1
22	Vss	166	DQ15	94	Vss	238	SA2
23	DQ10	167	Vss	95	DQ36	239	VSS
24	Vss	168	DQ11	96	Vss	240	DQ37
25	DQ20	169	Vss	97	DQ32	241	VSS
26	Vss	170	DQ21	98	Vss	242	DQ33
27	DQ16	171	Vss	99	TDQS13_t, DQS13_t	243	VSS
28	Vss	172	DQ17	100	TDQS13_c, DQS13_c	244	DQS4_c
29	TDQS11_t, DQS11_t	173	Vss	101	Vss	245	DQS4_t
30	TDQS11_c, DQS11_c	174	DQS2_c	102	DQ38	246	VSS
31	Vss	175	DQS2_t	103	Vss	247	DQ39
32	DQ22	176	Vss	104	DQ34	248	Vss
33	Vss	177	DQ23	105	Vss	249	DQ35
34	DQ18	178	Vss	106	DQ44	250	Vss
35	Vss	179	DQ19	107	Vss	251	DQ45
36	DQ28	180	Vss	108	DQ40	252	Vss
37	Vss	181	DQ29	109	Vss	253	DQ41
38	DQ24	182	Vss	110	TDQS14_t, DQS14_t	254	Vss
39	Vss	183	DQ25	111	TDQS14_c, DQS14_c	255	DQS5_c
40	TDQS12_t, DQS12_t	184	Vss	112	Vss	256	DQS5_t
41	TDQS12_c, DQS12_c	185	DQS3_c	113	DQ46	257	Vss
42	Vss	186	DQS3_t	114	Vss	258	DQ47
43	DQ30	187	Vss	115	DQ42	259	Vss
44	Vss	188	DQ31	116	Vss	260	DQ43
45	DQ26	189	Vss	117	DQ52	261	Vss
46	Vss	190	DQ27	118	Vss	262	DQ53
47	CB4	191	Vss	119	DQ48	263	Vss
48	Vss	192	CB5	120	Vss	264	DQ49
49	CB0	193	Vss	121	TDQS15_t, DQS15_t	265	Vss
50	Vss	194	CB1	122	TDQS15_c, DQS15_c	266	DQS6_c
51	TDQS17_t, DQS17_t	195	Vss	123	Vss	267	DQS6_t
52	TDQS17_c, DQS17_c	196	DQS8_c	124	DQ54	268	Vss
53	Vss	197	DQS8_t	125	Vss	269	DQ55
54	CB6	198	Vss	126	DQ50	270	Vss
55	Vss	199	CB7	127	Vss	271	DQ51
56	CB2	200	Vss	128	DQ60	272	Vss

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57	Vss	201	CB3	129	Vss	273	DQ61
58	RESET_n	202	Vss	130	DQ56	274	Vss
No.	**Designation**	**No.**	**Designation**	**No.**	**Designation**	**No.**	**Designation**
59	VDD	203	CKE1	131	Vss	275	DQ57
60	CKE0	204	VDD	132	TDQS16_t, DQS16_t	276	Vss
61	VDD	205	RFU	133	TDQS16_c, DQS16_c	277	DQS7_c
62	ACT_n	206	VDD	134	Vss	278	DQS7_t
63	BG0	207	BG1	135	DQ62	279	Vss
64	VDD	208	ALERT_n	136	Vss	280	DQ63
65	A12/BC_n	209	VDD	137	DQ58	281	Vss
66	A9	210	A11	138	Vss	282	DQ59
67	VDD	211	A7	139	SA0	283	Vss
68	A8	212	VDD	140	SA1	284	VDDSPD
69	A6	213	A5	141	SCL	285	SDA
70	VDD	214	A4	142	VPP	286	VPP
71	A3	215	VDD	143	VPP	287	VPP
72	A1	216	A2	144	RFU	288	VPP [4]
73	VDD	217	VDD				

Note:
1. VPP is 2.5V DC.
2. Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs
3. Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4. The 5th VPP is required on all modules. DIMMs
5. Address A17 is only valid for 16Gb x4 based SDRAMs

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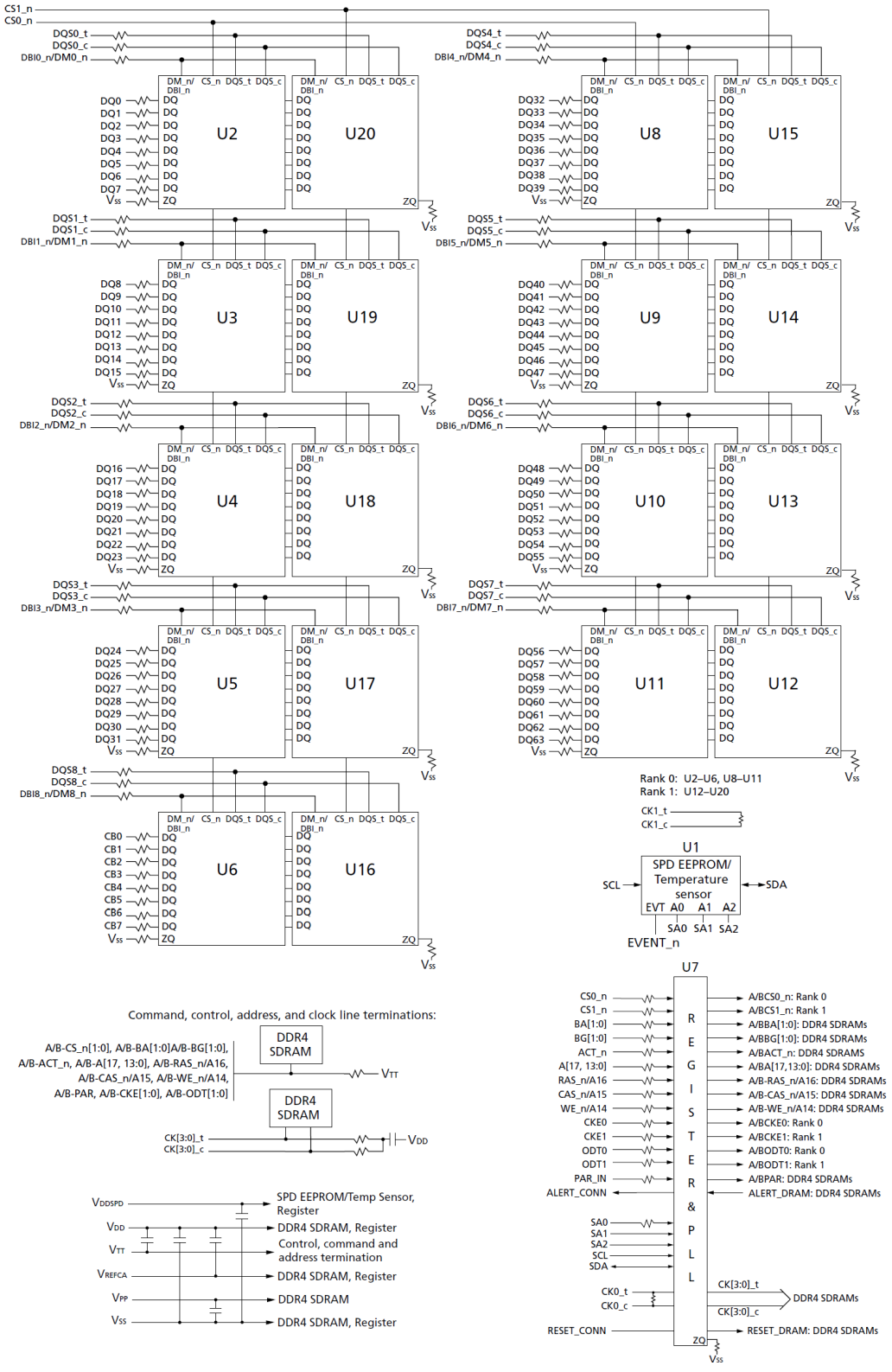
5. Function Block Diagram



Note:

1. Unless otherwise noted, resistor values are 15 ± 5%.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. ZQ resistors are 240 ±1%. For all other resistor values refer to the appropriate wiring diagram.

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4. VDD and VDDSPD also connect to the register.

6. Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.5V	V	1,2
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.5V	V	1,2
Voltage on V_{PP} pin relative to V_{SS}	V_{PP}	-0.4V ~ 3.0V	V	3
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975V	V	1

Note

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
3. VPP must be equal or greater than VDD/VDDQ at all times.

7. DC Operating Voltage[1,2,3] - 1.2V OPERATION

Recommended operating conditions

Item	Symbol	Voltage Rating (Volts)			Maximum Expected Current (AMPs)[4]	Power State
		Min.	Typical[5]	Max.		
Supply Voltage	V_{DD}	1.16	1.21	1.26	11.7	Operational
Activation Supply Voltage	V_{PP}	2.41	2.50	2.75	3.75	Operational
Termination Voltage	V_{TT}[6]	0.565	0.605	0.64	0.75	Operational
SPD-TSE Supply Voltage	V_{DDSPD}	2.41	2.50	2.75	0.75	Operational
Additional Power for non-volatile technologies	V_12 (Optional[7])	10.2	12.0	13.8	1.17	Operational
		5.8	12.0	13.8	0.07	Backup power off
		5.8	12.0	13.8	500u	Idle power off

Note:

1. 20 MHz bandwidth limited measurement for all voltages in the table.
2. Voltages are measured at the DIMM gold fingers.
3. The SDRAM specification must be met and take precedence over this document.
4. Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedances.
5. Typical voltage is platform dependent. This is a suggested value only.
6. At the DIMM interface VTT is the only voltage during normal operating conditions that can both source and sink current.
7. If 12 volts is supplied it must meet these requirements.

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8. Single-Ended AC & DC Input Levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933/3200		Units	Note
		Min.	Max.	Min.	Max.		
DC input logic high	VIH.CA(DC75)	V_{REFCA}+ 0.075	VDD	-	-	V	
DC input logic low	VIL.CA(DC75)	VSS	V_{REFCA}-0.075	-	-	V	
DC input logic high	VIH.CA(DC65)	-	-	V_{REFCA}+ 0.065	VDD	V	
DC input logic low	VIL.CA(DC65)	-	-	V_{SS}	V_{REFCA}-0.065	V	
AC input logic high	VIH.CA(AC100)	V_{REF} + 0.1	Note 1	-	-	V	
AC input logic low	VIL.CA(AC100)	Note 1	V_{REF} - 0.1	-	-	V	
AC input logic high	VIH.CA(AC90)	-	-	V_{REF} + 0.09	Note 1	V	
AC input logic low	VIL.CA(AC90)	-	-	Note 1	V_{REF}- 0.09	V	
Reference Voltage for ADD, CMD inputs	VREFCA(DC)	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V	2

Note:
1. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)
2. For reference: approx. VDD/2 ± 12mV.

9. Environment Parameters

Parameter	Symbol	Rating	Unit	Notes
Storage Temperature	T_{STG}	-55 to +100	°C	1
Operating Temperature	T_{CASE}	-40 to +95	°C	1,2,3
	T_A	-40 to +85	°C	1,3,4

Note:
1. It is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (Refresh interval =3.9 µs) is required, and to enter to self-refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.
3. Both temperature specifications must be satisfied.
4. Operating ambient temperature surrounding the package

10. Electrostatic Discharge Sensitivity

Item	Rating	Units	Notes
HBM (Human-Body Model)	>2000V	V	-
CDM (Charge-Device Model)	>500V	V	-

11. Reliability

MTBF @25 °C (Hours) [1]	FIT @ 25 °C [2]	MTBF @40 °C (Hours) [1]	FIT @ 40 °C [2]
4,517,000	221	2,287,000	437

Note:
1.The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Bellcore Prediction, which based on reliability data of the individual components in the module. It assumes nominal voltage, with all other parameters within specified range.
2. Failures per Billion Device-Hours.

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12. IDD Specification Parameter and Power Consumption

Values are for the DDR4 SDRAM only and are computed from values specified in the vendor's component data sheet)

Symbol	Proposed Conditions	Value	Units
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	820	mA
IPP0	**Operating One Bank Active-Precharge IPP Current** Same condition with IDD0	63	mA
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: sta-ble at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	940	mA
IDD2N	**Precharge Standby Current (AL=0)** CKE: Low; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2); ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit.	720	mA
IDD2NT	**Precharge Standby ODT Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	750	mA
IDD2P	**Precharge Power-Down Current** CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	470	mA
IDD2Q	**Precharge Quiet Standby Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	720	mA
IDD3N	**Active Standby Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	880	mA
IPP3N	**Active Standby IPP Current** Same condition with IDD3N	63	mA
IDD3P	**Active Power-Down Current** CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	590	mA
IDD4R	**Operating Burst Read Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1,700	mA
IDD4W	**Operating Burst Write Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	1,610	mA
IDD5B/ IDD5R	**Burst Refresh Current (1X REF):** IDD5B for Samsung IC module, IDD5R for Micron IC module CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	2,750	mA
IPP5B/ IPP5R	**Burst Refresh Write IPP Current (1X REF)** Same condition with IDD5B / IDD5R	252	mA

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Symbol	Proposed Conditions	Value	Units
IDD6N	**Self Refresh Current: Normal Temperature Range (0˚C to 85˚C)** TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	410	mA
IDD6E	**Self-Refresh Current: Extended Temperature Range** TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: MID-LEVEL	550	mA
IDD6R	**Self-refresh current: Reduced temperature range** TCASE: 0 - 45°C; Low Power Array Self Refresh (LP ASR) : Reduced; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: MID-LEVEL	280	mA
IDD6A	**Auto Self-Refresh Current** TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	380	mA
IDD7	**Operating Bank Interleave Read Current** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	2,120	mA
IPP7	**Operating Bank Interleave Read IPP Current** Same condition with IDD7	126	mA
IDD8	**Maximum Power Down Current**	213	mA
PDIMM	**Power Consumption per DIMM** System is operating at 1600MHz clock with VDD = 1.2V. This parameter is calculated at a common loading.	3,300	mW

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13. Timing Parameter

Parameter	Symbol	DDR4-3200		Notes
		Min.	Max.	
Clock cycle time at CL=22, CWL=16	tCK	0.62	<0.682	ns
Internal read command to first data	tAA	13.75	18	ns
ACT to internal read or write delay time	tRCD	13.75	-	ns
PRE command period	tRP	13.75	-	ns
ACT to ACT or REF command period	tRC	45.75	-	ns
ACTIVE to PRECHARGE command period	tRAS	32	9*tREFI	ns
Average high pulse width	tCH(avg)	0.48	0.52	tCK
Average low pulse width	tCL(avg)	0.48	0.52	tCK
DQS_t, DQS_c to DQ skew, per group, per access	tDQSQ	-	0.22	ps
DQ output hold time from DQS_t,DQS_c	tQH	0.74	-	tCK
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	-250	160	ps
DQ high-impedance time from CK_t, CK_c	tHZ(DQ)	-	160	ps
DQS_t, DQS_c READ Preamble	tRPRE	0.9	-	tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	tCK
DQS_t, DQS_c output high time	tQSH	0.4	-	tCK
DQS_t, DQS_c output low time	tQSL	0.4	-	tCK
DQS_t, DQS_c WRITE Preamble	tWPRE	0.9	-	tCK
DQS_t, DQS_c WRITE Postamble	tWPST	0.33	-	tCK
DQS_t, DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-250	160	ps
DQS_t, DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	160	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge	tDQSS	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time to CK_t, CK_c rising edge	tDSH	0.18	-	tCK
DLL locking time	tDLLK	1024	-	nCK1
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	ns
Delay from start of internal write trans-action to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	ns
Delay from start of internal write trans-action to internal read command for same bank group	tWTR_L	max(4nCK,3.75ns)	-	ns
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	10	-	nCK[1]
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	nCK[1]
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(4 nCK, 5 ns)	-	nCK[1]
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK[1]
Auto precharge write recovery + precharge time	tDAL	Programmed WR + roundup (tRP / tCK(avg))		nCK[1]
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK[1]
ACTIVE to ACTIVE command delay to same bank group for 1KB page size	tRRD	max(4nCK,4.9ns)	-	nCK[1]
Four activate window for 1KB page size	tFAW	max(20nCK,21ns)	-	ns
Command and Address setup time to CK_t, CK_c referenced to VIH(AC) / VIL(AC) levels	tIS(base)	40	-	ps
Command and Address hold time from CK_t, CK_c referenced to VIH(AC) / VIL(AC) levels	tIH(base)	65	-	ps
Power-up and RESET calibration time	tZQinit	1024	-	nCK[1]
Normal operation Full calibration time	tZQoper	512	-	nCK[1]
Normal operation short calibration time	tZQCS	128	-	nCK[1]
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	nCK[1]
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL.	tXP	max(4nCK,6ns)	-	nCK[1]
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	ns
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
8Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	350	-	ns
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	tREFI	-	7.8	us
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	tREFI	-	3.9	us
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	nCK[1]
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK[1]
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	nCK[1]
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE	0	2	ns

Note:
1. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

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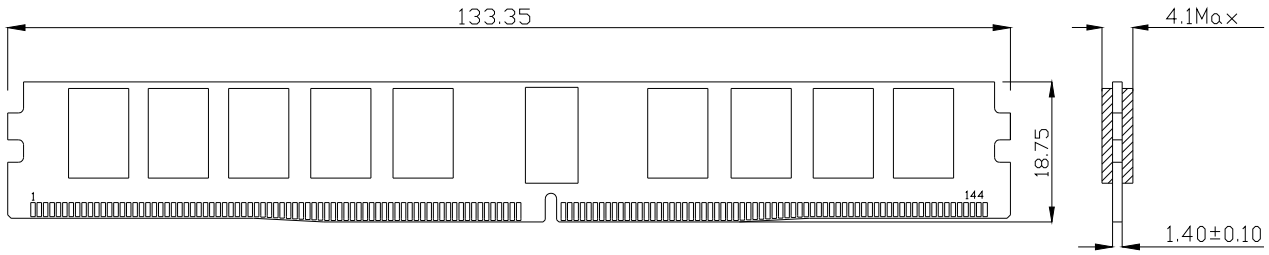
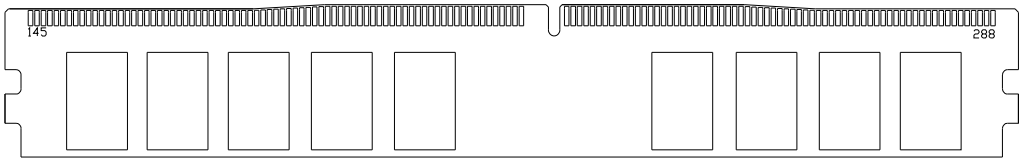
14. Physical Dimensions (Units in Millimeters)

(Drawing not to scale)

Front



Side



Back

Note: Tolerance on all dimensions ±0.15mm (±0.006 inch) unless otherwise noted

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15. Serial Presence Detects

Byte#	Function Described	Hex Value
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	23h
1	SPD Revision	12h
2	Key Byte / DRAM Device Type	0Ch
3	Key Byte / Module Type	01h
4	SDRAM Density and Banks	85h
5	SDRAM Addressing	21h
6	SDRAM Device Type	00h
7	SDRAM Optional Features	08h
8	SDRAM Thermal and Refresh Option	00h
9	Other SDRAM Optional Features	00h
10	Reserved	00h
11	Module Nominal Voltage, VDD	03h
12	Module Organization	09h
13	Module Memory Bus Width	0Bh
14	Module Thermal Sensor	80h
15~16	Reserved	00h
17	Timebases	00h
18	SDRAM Minimum Cycle Time(tckavg min)	05h
19	SDRAM Minimum Cycle Time(tckavg max)	0Dh
20	Cas Latency Supported, First Byte	F8h
21	Cas Latency Supported, Second Byte	FFh
22	Cas Latency Supported, Third Byte	2Fh
23	Cas Latency Supported, Fourth Byte	00h
24	Minimum Cas Latency Time (tAAmin)	6Eh
25	Minimum RAS to CAS Delay Time(tRCD min)	6Eh
26	Minimum Raw Precharge Delay Time(tRP min)	6Eh
27	Upper Nibbles for tRASmin and tRCmin	11h
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	00h
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	6Eh
30	Minimum Refresh Recovery Delay Time (tRFC1min), LSB	F0h
31	Minimum Refresh Recovery Delay Time (tRFC1min), MSB	0Ah
32	Minimum Refresh Recovery Delay Time (tRFC2min), LSB	20h
33	Minimum Refresh Recovery Delay Time (tRFC2min), MSB	08h
34	Minimum Refresh Recovery Delay Time (tRFC4min), LSB	00h
35	Minimum Refresh Recovery Delay Time (tRFC4min), MSB	05h

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Byte#	Function Described	Hex Value
36	Minimum Four Active Window Time (tFAWmin), Most Significant Nibble	00h
37	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte	A8h
38	Minimum Active to Active Delay Time (tRRD_smin), different Bank Group	14h
39	Minimum Active to Active Delay Time (tRRD_Lmin), Same Bank Group	28h
40	Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	28h
41	Upper Nibble for tWRmin	00h
42	Minimum Write Recovery Time(tWRmin)	78h
43	Upper Nibbles for tWTRmin	00h
44	Minimum Write to Read Time(tWTR_smin), different bank group	14h
45	Minimum Write to Read Time(tWTR_Lmin), same bank group	3Ch
46~59	Reserved,	00h
60	Connector to SDRAM Bit Mapping	0Ch
61	Connector to SDRAM Bit Mapping	2Ch
62	Connector to SDRAM Bit Mapping	0Ch
63	Connector to SDRAM Bit Mapping	2Ch
64	Connector to SDRAM Bit Mapping	0Ch
65	Connector to SDRAM Bit Mapping	2Ch
66	Connector to SDRAM Bit Mapping	0Ch
67	Connector to SDRAM Bit Mapping	2Ch
68	Connector to SDRAM Bit Mapping	0Ch
69	Connector to SDRAM Bit Mapping	2Ch
70	Connector to SDRAM Bit Mapping	0Ch
71	Connector to SDRAM Bit Mapping	2Ch
72	Connector to SDRAM Bit Mapping	0Ch
73	Connector to SDRAM Bit Mapping	2Ch
74	Connector to SDRAM Bit Mapping	0Ch
75	Connector to SDRAM Bit Mapping	2Ch
76	Connector to SDRAM Bit Mapping	0Ch
77	Connector to SDRAM Bit Mapping	2Ch
78~116	Reserved	00h
117	Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	00h
118	Fine Offset for Minimum Activate to Activate Delay Time(tRRD_L_min), Same Bank Group	9Ch
119	Fine Offset for Minimum Activate to Activate Delay Time(tRRD_Smin), Different Bank Group	00h
120	Fine Offset for Minimum Activate to Activate/Refresh Delay Time(tRCmin)	00h

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Byte#	Function Described	Hex Value
121	Fine Offset for Minimum Row Precharge Delay Time(tRPmin)	00h
122	Fine Offset for Minimum RAS to CAS Delay Time(tRCD_min)	00h
123	Fine Offset for Minimum CAS Latency Delay Time(tAA_min)	00h
124	Fine Offset for DRAM Maximum Cycle Time(tCKAVG_max)	E7h
125	Fine Offset for DRAM Minimum Cycle Time(tCKAVG_min)	00h
126	Cyclical Redundancy Code	CCh
127	Cyclical Redundancy Code	32h
128	Raw Card Extension, Module Nominal Height	04h
129	Module Maximum Thickness	11h
130	Reference Raw Card Used	47h
131	DIMM Module Attributes	15h
132	RDIMM Thermal Heat Spreader Solution	00h
133	Register Manufacturer ID Code, Least Signficant Byte	86h
134	Register Manufacturer ID Code, Most Signficant Byte	9Dh
135	Register Revision Number	22h
136	Address Mapping from Register to DRAM	01h
137	Register Output Drive Strength for Control	10h
138	Register Output Strength for CK	40h
139~253	Reserved	00h
254	Cyclical Redundancy Code	EBh
255	Cyclical Redundancy Code	C4h
256~319	Reserved	00h
320	Module Manufacturer's ID Code, Least Significant Byte	86h
321	Module Manufacturer's ID Code, Most Significant Byte	E3h
322	Module Manufacturing Location	00h
323	Module Manufacturing Date	00h
324	Module Manufacturing Date	00h
325	Module Serial Number	00h
326	Module Serial Number	00h
327	Module Serial Number	00h
328	Module Serial Number	00h
329	Module Part Number	41h
330	Module Part Number	34h

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Byte#	Function Described	Hex Value
331	Module Part Number	42h
332	Module Part Number	31h
333	Module Part Number	36h
334	Module Part Number	51h
335	Module Part Number	48h
336	Module Part Number	38h
337	Module Part Number	42h
338	Module Part Number	4Eh
339	Module Part Number	57h
340	Module Part Number	45h
341	Module Part Number	53h
342	Module Part Number	45h
343	Module Part Number	00h
344	Module Part Number	00h
345	Module Part Number	00h
346	Module Part Number	00h
347	Module Part Number	00h
348	Module Part Number	00h
349	Module Revision Code	00h
350	DRAM Manufacturer's ID Code, Least Sgnificant Byte	80h
351	DRAM Manufacturer's ID Code, Most Sgnificant Byte	CEh
352	DRAM Stepping	43h
353~380	Module Manufacturer's Specific Data	00h
381	Module Manufacturer's Specific Data	00h
382~383	Reserved	00h
384~511	End User Programmable	00h

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