Advantech

AQD-SD4U8GE24-SE

Datasheet

Rev. 1.0

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Description

DDR4 1.2V ECC SO-DIMM is high-speed, low power memory module that use 1Gx8bits DDR4 SDRAM in FBGA package and a 4096 bits serial EEPROM on a 260-pin printed circuit board. DDR4 1.2V ECC SO-DIMM is a Dual In-Line Memory Module and is intended for mounting into 260-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

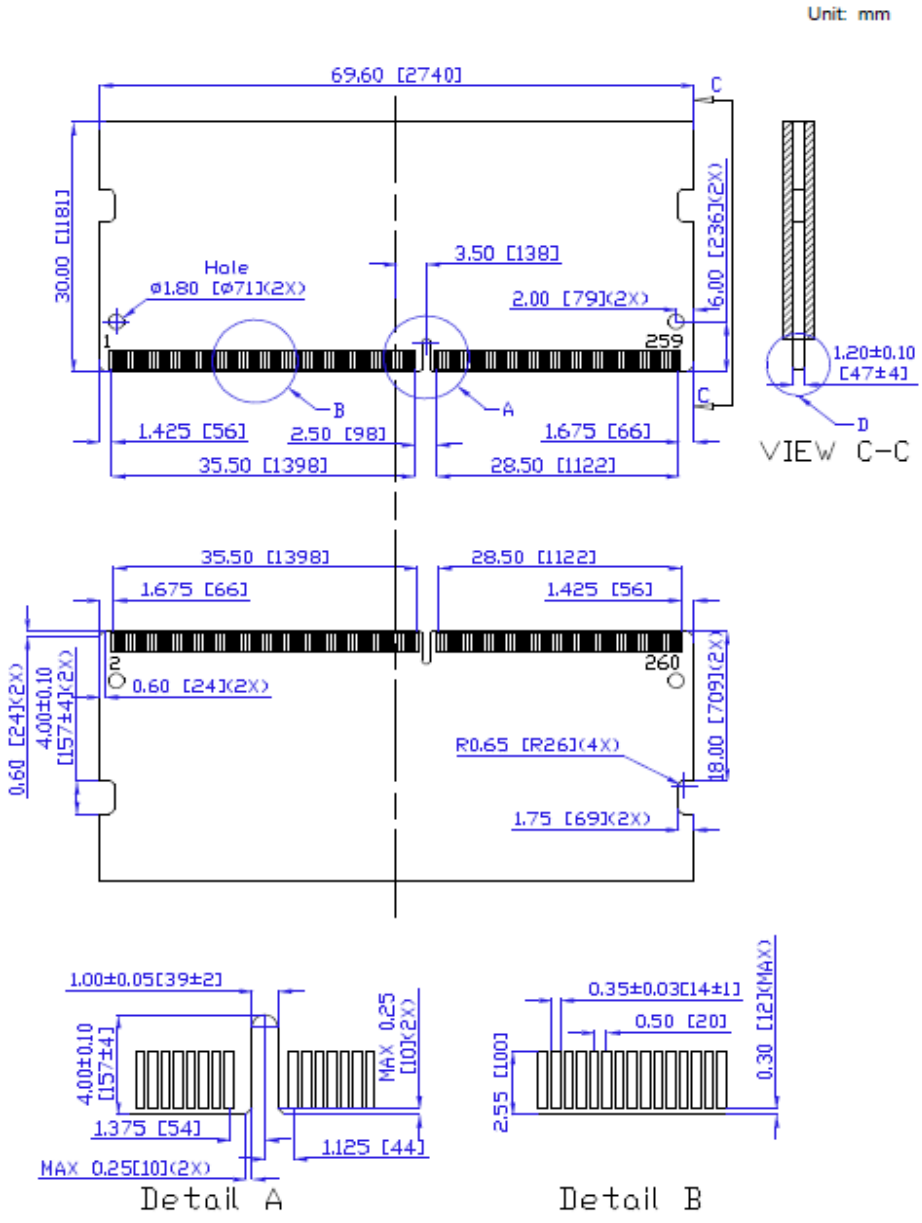
- RoHS compliant products
- JEDEC standard 1.2V (1.14V to 1.26V) Power supply
- VDDQ=1.2V (1.14V to 1.26V)
- Clock Freq: 1200MHZ for 2400Mb/s/Pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10, 11, 12, 13, 14,15,16, 17,18
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 12,16 (DDR4-2400)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset
- PCB: 30µ gold finger

Pin Identification

Symbol	Function
A0–A16	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n1	Register row address strobe input
CAS_n2	Register column address strobe input
WE_n3	Register write enable input
CS0_n, CS1_n,	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register
SA0–SA2	I2C slave address select for SPD/TS and register
PARITY	Register parity input

VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use
NC	No Connection

Dimensions (Unit: millimeter)



30µ gold finger

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Pin Assignments

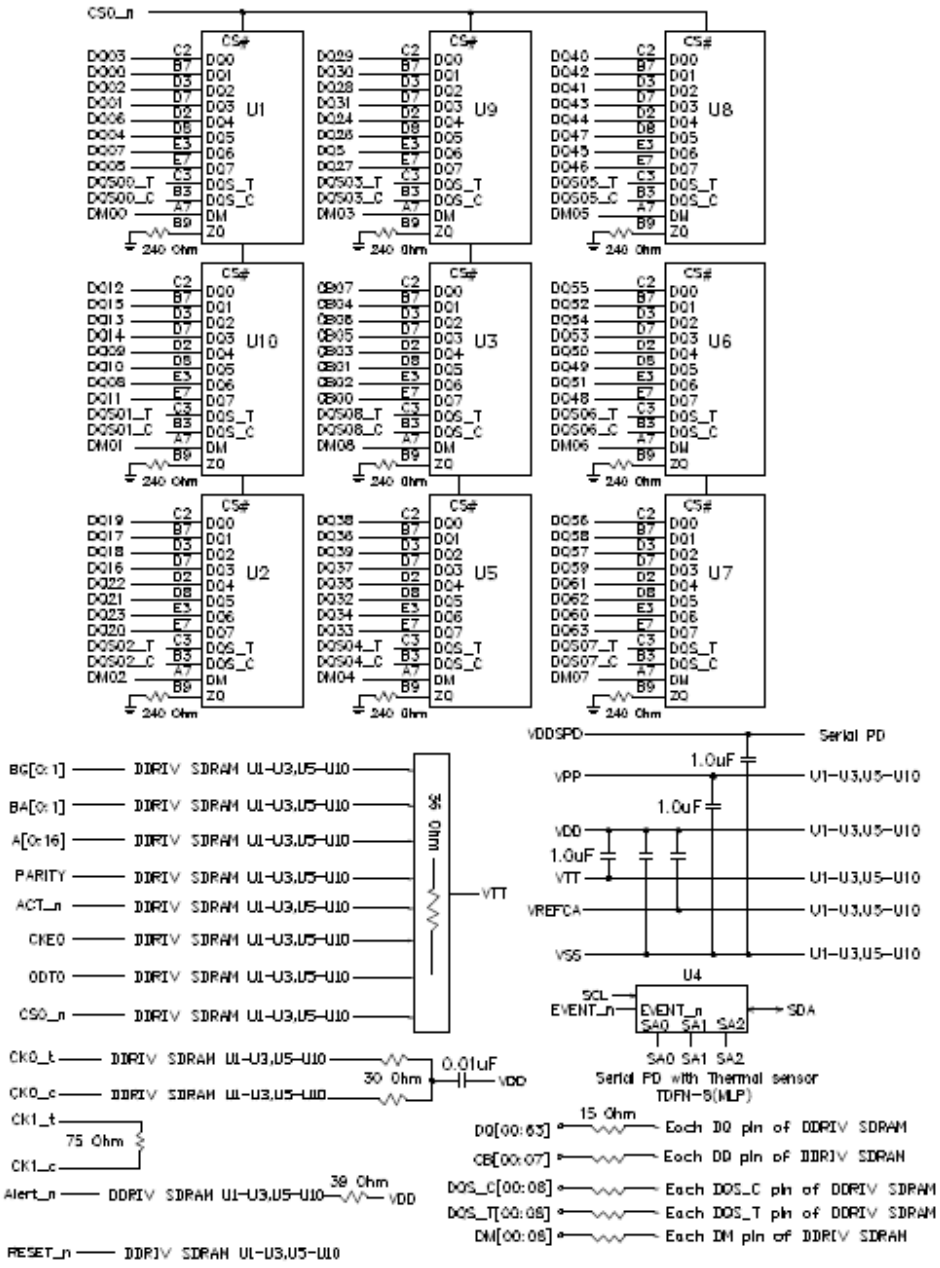
Pin No.	Pin name-Front	Pin No.	Pin name-Back	Pin No.	Pin name-Front	Pin No.	Pin name-Back
1	VSS	2	VSS	133	A1	134	EVENT_n
3	DQ5	4	DQ4	135	VDD	136	VDD
5	VSS	6	VSS	137	CK0_t	138	CK1_t
7	DQ1	8	DQ0	139	CK0_c	140	CK1_c
9	VSS	10	VSS	141	VDD	142	VDD
11	DQS0_c	12	DM0_n, DBI0_n	143	PARITY	144	A0
13	DQS0_t	14	VSS	145	BA1	146	A10/AP
15	VSS	16	DQ6	147	VDD	148	VDD
17	DQ7	18	VSS	149	CS0_n	150	BA0
19	VSS	20	DQ2	151	A14/WE_n	152	A16/RAS_n
21	DQ3	22	VSS	153	VDD	154	VDD
23	VSS	24	DQ12	155	ODT0	156	A15/CAS_n
25	DQ13	26	VSS	157	CS1_n	158	A13
27	VSS	28	DQ8	159	VDD	160	VDD
29	DQ9	30	VSS	161	ODT1	162	C0, CS2_n, NC
31	VSS	32	DQS1_c	163	VDD	164	VREFCA
33	DM1_n, DBI1_n	34	DQS1_t	165	C1, CS3_n, NC	166	SA2
35	VSS	36	VSS	167	VSS	168	VSS
37	DQ15	38	DQ14	169	DQ37	170	DQ36
39	VSS	40	VSS	171	VSS	172	VSS
41	DQ10	42	DQ11	173	DQ33	174	DQ32
43	VSS	44	VSS	175	VSS	176	VSS
45	DQ21	46	DQ20	177	DQS4_c	178	DM4_n, DBI4_n
47	VSS	48	VSS	179	DQS4_t	180	VSS
49	DQ17	50	DQ16	181	VSS	182	DQ39
51	VSS	52	VSS	183	DQ38	184	VSS
53	DQS2_c	54	DM2_n, DBI2_n	185	VSS	186	DQ35
55	DQS2_t	56	VSS	187	DQ34	188	VSS
57	VSS	58	DQ22	189	VSS	190	DQ45
59	DQ23	60	VSS	191	DQ44	192	VSS
61	VSS	62	DQ18	193	VSS	194	DQ41
63	DQ19	64	VSS	195	DQ40	196	VSS
65	VSS	66	DQ28	197	VSS	198	DQS5_c

67	DQ29	68	VSS	199	DM5_n, DBI5_n	200	DQS5_t
69	VSS	70	DQ24	201	VSS	202	VSS
71	DQ25	72	VSS	203	DQ46	204	DQ47
73	VSS	74	DQS3_c	205	VSS	206	VSS
75	DM3_n, DBI3_n	76	DQS3_t	207	DQ42	208	DQ43
77	VSS	78	VSS	209	VSS	210	VSS
79	DQ30	80	DQ31	211	DQ52	212	DQ53
81	VSS	82	VSS	213	VSS	214	VSS
83	DQ26	84	DQ27	215	DQ49	216	DQ48
85	VSS	86	VSS	217	VSS	218	VSS
87	CB5, NC	88	CB4, NC	219	DQS6_c	220	DM6_n, DBI6_n
89	VSS	90	VSS	221	DQS6_t	222	VSS
91	CB1, NC	92	CB0, NC	223	VSS	224	DQ54
93	VSS	94	VSS	225	DQ55	226	VSS
95	DQS8_c	96	DM8_n, DBI8_n	227	VSS	228	DQ50
97	DQS8_t	98	VSS	229	DQ51	230	VSS
99	VSS	100	CB6, NC	231	VSS	232	DQ60
101	CB2, NC	102	VSS	233	DQ61	234	VSS
103	VSS	104	CB7, NC	235	VSS	236	DQ57
105	CB3, NC	106	VSS	237	DQ56	238	VSS
107	VSS	108	RESET_n	239	VSS	240	DQS7_c
109	CKE0	110	CKE1	241	DM7_n, DBI7_n	242	DQS7_t
111	VDD	112	VDD	243	VSS	244	VSS
113	BG1	114	ACT_n	245	DQ62	246	DQ63
115	BG0	116	ALERT_n	247	VSS	248	VSS
117	VDD	118	VDD	249	DQ58	250	DQ59
119	A12	120	A11	251	VSS	252	VSS
121	A9	122	A7	253	SCL	254	SDA
123	VDD	124	VDD	255	VDDSPD	256	SA0
125	A8	126	A5	257	VPP	258	VTT
127	A6	128	A4	259	VPP	260	SA1
129	VDD	130	VDD	–	–	–	–
131	A3	132	A2	–	–	–	–

*IC Component Composition :

256Mx8	A0~A13		
512Mx8	A0~A14,	512Mx4	A0~A14
1024Mx8	A0~A15,	1024Mx4	A0~A15
2048Mx8	A0~A16,	2048Mx4	A0~A16

Block Diagram
8GB, 1Gx72 Module(1 Rank x8)



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Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note:
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At 0 - 85C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.5	V	1,3
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.5	V	1,3
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 3.0	V	4
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.5	V	1,3
Storage temperature	TSTG	-55~+100	°C	1,2

Note:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

AC & DC Operating Conditions

Recommended DC operating conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

NOTE:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

AC & DC Logic Input Levels for Single-Ended Signals

Symbol	Parameter	DDR4-1600/1866/2133/2400		Unit	NOTE
		Min.	Max.		
VIH.CA(DC75)	DC input logic high	VREFCA+ 0.075	VDD	V	
VIL.CA(DC75)	DC input logic low	VSS	VREFCA-0.075	V	
VIH.CA(AC100)	AC input logic high	VREF + 0.1	Note 2	V	1
VIL.CA(AC100)	AC input logic low	Note 2	VREF - 0.1	V	1
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49*VDD	0.51*VDD	V	2,3

NOTE :
1. See “Overshoot and Undershoot Specifications” on section.
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)
3. For reference : approx. VDD/2 ± 12mV

Timing Parameters & Specifications

Speed		DDR4 2400		Unit
Parameter	Symbol	Min	Max	
Average Clock Period	tCK	0.833	<0.938	ns
CK high-level width	tCH	0.48	0.52	tCK
CK low-level width	tCL	0.48	0.52	tCK
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	0.16	tCK(avg) /2
DQ output hold time from DQS, /DQS	tQH	0.76	-	tCK(avg) /2
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-300	150	ps
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	150	ps
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18		tCK
DQS, /DQS Read preamble	tRPRE	0.9	-	tCK
		1.8		tCK
DQS, /DQS differential Read postamble	tRPST	0.33	-	tCK
DQS, /DQS Write preamble	tWPRE	0.9	-	tCK
		1.8	NA	tCK
DQS, /DQS Write postamble	tWPST	0.33	-	tCK
DQS, /DQS differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS, /DQS differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS, /DQS rising edge to CK, /CK rising edge	tDQSS	-0.27	+0.27	tCK
DQS, /DQS falling edge setup time to CK, /CK rising edge	tDSS	0.18	-	tCK
DQS, /DQS falling edge hold time to CK, /CK rising edge	tDSH	0.18	-	tCK
Delay from start of internal write transaction to internal read com-mand for different bank group	tWTR_S	max (2nCK, 2.5ns)	-	
Delay from start of internal write transaction to internal read com-mand for same bank group	tWTR_L	max (4nCK,7.5ns)		
Write recovery time	tWR	15	-	ns
Mode register set command cycle time	tMRD	8	-	nCK
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	nCK

CAS_n to CAS_n command delay for different bank group	tCCD_S	4		nCK
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5 .3ns)	-	nCK
Parameter	**Symbol**	**Min**	**Max**	**Unit**
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	RRD_S(1K)	Max(4nCK,3 .3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK,3 .3ns)		nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6 .4ns)		nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4 .9ns)		nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nCK,4 .9ns)		nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)		ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 13ns)	-	ns
Power-up and RESET calibration time	tZQinitl	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation short calibration time	tZQcs	128	-	nCK
Exit self refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	
Exit self refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	
Internal read to precharge command delay	tRTP	max (4nCK,7.5ns)	-	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+ 1nCK	-	
Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL	tXP	max (4nCK,6ns)	-	
CKE minimum pulse width (high and low pulse width)	tCKE	max (3nCK, 5ns)		
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	ns

SERIAL PRESENCE DETECT SPECIFICATION

8192MB(1024Mx72Bit) Serial Presence Detect for DDR4 ECC SODIMM (PC-19200) 2400 CL=17

BYTE	FUNCTION DESCRIDED	FUNCTION SUPPORTED	HEX VALUE
0	Number of serial PD bytes written/SPD device size/CRC coverage	512B Total, 384B Used	23
1	SPD revision	Revision 1.0	10
2	Key byte/DRAM device type	DDR4 SDRAM	0C
3	Key byte/module type	72b-SO-UDIMM	09
4	SDRAM density and banks	8Gb, 4BG, 4Banks	85
5	SDRAM addressing	16 rows, 10 columns	21
6	SDRAM package type	Monolithic DRAM Device	00
7	SDRAM optional features	Unlimited MAC	08
8	SDRAM thermal and refresh options	—	00
9	Other SDRAM optional feature	sPPR supported	60
10	Reserved	—	00
11	Module Nominal Voltage,VDD	1.2V	03
12	Module organization	1Ranks / x8 bits	01
13	Module memory bus width	72 bits / with ECC	0B
14	Module thermal sensor	Incorporated	80
15	Reserved	—	00
16	Reserved	—	00
17	Timebases	MTB 125ps, FTB 1ps	00
18	SDRAM minimum cycle time(tCKAVG min)	0.833ns	07
19	SDRAM maximum cycle time(tCKAVG max)	1.5ns	0C
20	CAS latencies supported, first byte	CL=10,11,12,13,14,15,16,17,18	F8
21	CAS latencies supported, second byte	CL=10,11,12,13,14,15,16,17,18	0F
22	CAS latencies supported, third byte	CL=10,11,12,13,14,15,16,17,18	00
23	CAS latencies supported, fourth byte	CL=10,11,12,13,14,15,16,17,18	00
24	Minimum CAS latency time(tAA min)	13.75ns	6E
25	Minimum RAS to CAS delay time(tRCD min)	13.75ns	6E
26	Minimum Row precharge delay time(tRP min)	13.75ns	6E

27	Upper nibbles for tRAS min and tRC min	tRAS = 32ns, tRC = 45.75ns	11
28	Minimum active to precharge delay time(tRAS min), least significant byte	32ns	00
29	Minimum active to active/refresh delay time(tRC min), least significant byte	45.75ns	6E
30	Minimum refresh recovery delay time(tRFC1 min), LSB	350ns	F0
31	Minimum refresh recovery delay time(tRFC1 min), MSB	350ns	0A
32	Minimum refresh recovery delay time(tRFC2 min), LSB	260ns	20
33	Minimum refresh recovery delay time(tRFC2 min), MSB	260ns	08
34	Minimum refresh recovery delay time(tRFC3 min), LSB	160ns	00
35	Minimum refresh recovery delay time(tRFC3 min), MSB	160ns	05
36	Minimum four activate window time(tFAW min), most significant nibble	21ns	00
37	Minimum four activate window time(tFAW min), least significant byte	21ns	A8
38	Minimum activate to activate delay time(tRRD_S min), different bank group	3.3ns	1B
39	Minimum activate to activate delay time(tRRD_L min), same bank group	4.9ns	28
40	Minimum CAS to CAS delay time(tCCD_L min), same bank group	5ns	28
41	Upper Nibble for tWR min	15ns	00
42	Minimum Write Recovery Time (tWR min)	15ns	78
43	Upper Nibbles for tWTR min	2.5ns	00
44	Minimum Write to Read Time (tWTR_S min), different bank group	2.5ns	14
45	Minimum Write to Read Time (tWTR_L min), same bank group	7.5ns	3C
46~59	Reserved	—	00
60	Connector to SRAM bit mapping	DQ0 - 3	0C
61	Connector to SRAM bit mapping	DQ4 - 7	2B
62	Connector to SRAM bit mapping	DQ8 - 11	2D
63	Connector to SRAM bit mapping	DQ12 - 15	04
64	Connector to SRAM bit mapping	DQ16 - 19	16
65	Connector to SRAM bit mapping	DQ20 - 23	35
66	Connector to SRAM bit mapping	DQ24 - 27	23
67	Connector to SRAM bit mapping	DQ28 - 31	0D
68	Connector to SRAM bit mapping	CB0 - 3	36

69	Connector to SRAM bit mapping	CB4 - 7	0C
70	Connector to SRAM bit mapping	DQ32 - 35	2C
71	Connector to SRAM bit mapping	DQ36 - 39	0B
72	Connector to SRAM bit mapping	DQ40 - 43	03
73	Connector to SRAM bit mapping	DQ44 - 47	24
74	Connector to SRAM bit mapping	DQ48 - 51	35
75	Connector to SRAM bit mapping	DQ52 - 55	0C
76	Connector to SRAM bit mapping	DQ56 - 59	03
77	Connector to SRAM bit mapping	DQ60 - 63	2D
78~116	Reserved	—	00
117	Fine offset for minimum CAS to CAS delay time (tCCD_L min), same bank group	5ns	00
118	Fine offset for minimum activate to activate delay time (tRRD_L min), same bank group	4.9ns	9C
119	Fine offset for minimum activate to activate delay time (tRRD_S min), different e bank group	3.3ns	B5
120	Fine offset for minimum activate to activate/refresh delay time(tRC min)	45.75ns	00
121	Fine offset for minimum ROW precharge delay time (tRP min)	13.75ns	00
122	Fine offset for minimum RAS to CAS delay time(tRCD min)	13.75ns	00
123	Fine offset for minimum CAS latency time (tAA min)	13.75ns	00
124	Fine offset for SDRAM maximum cycle time(tCKAVG max)	1.6ns	E7
125	Fine offset for SDRAM minimum cycle time(tCKAVG min)	0.833ns	D6
126	CRC for base configuration section section, Least significant byte	CC	CC
127	CRC for base configuration section section, Most significant byte	33	33
128	Raw card extension, module nominal height	R/C D, 30.00 mm	0F
129	Module maximum thickenss	1 < thickness ≤ 2mm	11
130	Reference raw card used	Row Card D	03
131	Address mapping from edge connector to DRAM	Standard = 0	00
132~253	Reserved	—	00
254	CRC for base configuration section section, Least significant byte	14	14
255	CRC for base configuration section section, Most significant byte	5A	5A
256-319	Reserved	—	00

320	Module manufacturer's ID code, least significant byte	Apacer	01
321	Module manufacturer's ID code, least significant byte	Apacer	7A
322	Module manufacturing location		00
323	Module manufacturing date		00
324	Module manufacturing date		00
325	Module serial number		00
326	Module serial number		00
327	Module serial number		00
328	Module serial number		00
329	Module part number	A	41
330	Module part number	Q	51
331	Module part number	D	44
332	Module part number	-	2D
333	Module part number	S	53
334	Module part number	D	44
335	Module part number	4	34
336	Module part number	U	55
337	Module part number	8	38
338	Module part number	G	47
339	Module part number	E	45
340	Module part number	2	32
341	Module part number	4	34
342	Module part number	-	2D
343	Module part number	S	53
344	Module part number	E	45
345	Module part number		20
346	Module part number		20
347	Module part number		20
348	Module part number		20

349	Module revision code		00
350	DRAM manufacturer's ID code, least significant byte		00
351	DRAM manufacturer's ID code, least significant byte		00
352	DRAM stepping		00
353-381	Module manufacturer's specific data		00
382-383	Reserved		00
384-511	End user programmable		00