M.2 2230 PCIe/NVMe SSD 720-D Datasheet

(SQF-C3Axx-xxxGDEDx)

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Revision History

Rev.	Date	History
1.0	2021/11/11	1. Preliminary
1.1	2021/12/21	1. Add performance, consumption and TBW

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1. Overview

Advantech SQFlash 720-D series M.2 2230 (A+E Key) PCIe/NVMe SSD (Solid State Drive) delivers all the advantages of flash disk technology with PCIe Gen3 x2 interface, including being compliant with NGFF M.2 2230 (A+E Key) form factor. The device offers a wide range of capacities up to 512GB and its performance can reach up to 1200 MB/s (for read) and 900 MB/s (for write) based on Kioxia 3D TLC flash. The lower power consumption makes it an ideal storage choice for high performance demanding mobile devices.

2. Features

■ PCIe Interface

- Compliant with NVMe 1.3
- PCI Express Base 3.1
- PCIe Gen 3 x 2 lane & backward compatible to PCIe Gen 2 and Gen 1
- Support up to QD 128 with queue depth of up to 64K
- Support power management (optional)

■ Operating Voltage：3.3V

■ Support LDPC of ECC algorithm

■ Support SMART and TRIM commands

■ Temperature Ranges[1]

- Commercial Temperature
  - 0℃ to 70℃ for operating
  - -40℃ to 85℃ for storage
- Industrial Temperature
  - -40℃ to 85℃ for operating
  - -40℃ to 85℃ for storage

*Note : 1. Based on SMART Attribute (Byte index [2 :1] of PCIe-SIG standard, which measured by thermal sensor

■ Mechanical Specification

- Shock：1,500G / 0.5ms
- Vibration：20G / 80~2,000Hz

■ Humidty

- Humidity：up to 95% under 40℃

■ Acquired RoHS、WHQL、CE、FCC Certificate

■ Acoustic：0 dB

■ Dimension：30.0 mm x 22.0 mm x 3.8 mm

3. Specification Table

■ Performance

		Sequential Performance (MB/sec)		Random Performance (IOPS @4K)	
		Read	**Write**	**Read**	**Write**
3D TLC (BiCS5)	128 GB	1,150	550	95K	125K
	256 GB	1,150	900	150K	200K
	512 GB	1,200	900	130K	210K
3D sTLC (BiCS5)	32 GB	TBD	TBD	TBD	TBD
	64 GB	TBD	TBD	TBD	TBD
	128 GB	TBD	TBD	TBD	TBD

* Subject to change based on firmware migration.

NOTES:

1. The performance was estimated based on Kioxia 3D TLC BICS5 flash.
2. Performance may differ according to flash configuration and platform.
3. The table above is for reference only. The criteria for MP (mass production) and for accepting goods shall be discussed based on different flash configuration

■ Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

TBW = [(NAND Endurance) x (SSD Capacity)] / WAF

- **NAND Endurance**: Program / Erase cycle of a NAND flash.
  - SLC: 100,000 cycles
  - Ultra MLC: 30,000 cycles
  - MLC: 3,000 cycles
  - 3D TLC (BiCS3/BiCS4/BiCS5): 3,000 cycles
  - 3D sTLC (BiCS4): 30,000 cycles
- **SSD Capacit**y: SSD physical capacity in total of a SSD.
- **WAF**: Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

WAF = (Lifetime write to flash) / (Lifetime write to host)

Endurance measurement is based on JEDEC 219A client workload and verified with following workload conditions,

- PreCond%full = 100%
- Trim commands enabled
- Random data pattern.

	WAF	TBW
		3D TLC (BiCS5)
128 GB	3.5	110
256 GB	3.2	240
512 GB	2.9	520

	WAF	TBW
		3D sTLC (BiCS5)
32 GB	TBD	TBD
64 GB	TBD	TBD
128 GB	TBD	TBD

4. General Description

■ Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQF-C3A 720-D applies the LDPC algorithm, which can detect and correct data errors even with the latest 3D TLC technology to ensure data being read correctly, and protects data from corruption.

■ Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, when flash media is not used evenly, some blocks get updated more frequently than others and the lifetime of device would be reduced significantly. Thus, wear leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

SQFlash 720-D series provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static wear leveling algorithms, the life expectancy of the NAND flash is greatly improved.

■ Bad Block Management

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. SQFlash 720-D series implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

■ Power Loss Protection: Flush Manager

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SQFlash SSD applies the Flush Manager technology, only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

In addition, it is critical for a controller to shorten the time the in-flight data stays in the controller internal cache. Thus, SQFlash applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. With Flush Manager, incoming data would only have a “pit stop” in the cache and then move to NAND flash directly. Also, the onboard DDR will be treated as an “organizer” to consolidate incoming data into groups before written into the flash to improve write amplification.

■ TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD so that blocks of data that are no longer in use can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks at all time.

■ SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a solid state drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users impending failures while there is still time to perform proactive actions, such as save data to another device.

■ Over-Provision

Over Provisioning refers to the preserving additional area beyond user capacity in a SSD, which is not visible to users and cannot be used by them. However, it allows a SSD controller to utilize additional space for better performance and WAF. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

■ Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. Thermal Throttling function is for protecting the drive and reducing the possibity of read / write error due to overheat. The temperature is monitored by the thermal sensor. As the operating temperature continues to increase to theshold temperature, the Thermal Throttling mechanism is activated. At this time, the performance of the drive will be significantly decreased to avoid continuous heating. When the operating temperature falls below theshold temperutue, the drive can resume to normal operation.

■ Advanced Device Security Features

- **Advanced Encryption Standard (AES)**

  An AES 256-bit encryption key is generated in the drive's security controller before the data gets stored on the NAND flash. When the controller or firmware fails, the data that is securely stored in the encryption key becomes inaccessible through the NAND flash.

- **OPAL 2.0 support**

  SQFlash 720-D series supports standard OPAL 2.0 function for advance Self-Encryption Drive (SED) feature sets. Advantech provides also user friendly interface for setting disk / system bonding to prevent SSD be used in non-authorized platforms, which is called Flash Lock function.

- **Secure Erase Function**

  SQFlash 720-D series supports standard NVMe command for secure erase function; when the SSD controller receive the secure erase command, the erase process will reset all blocks and erase all of the user data in the SSD.

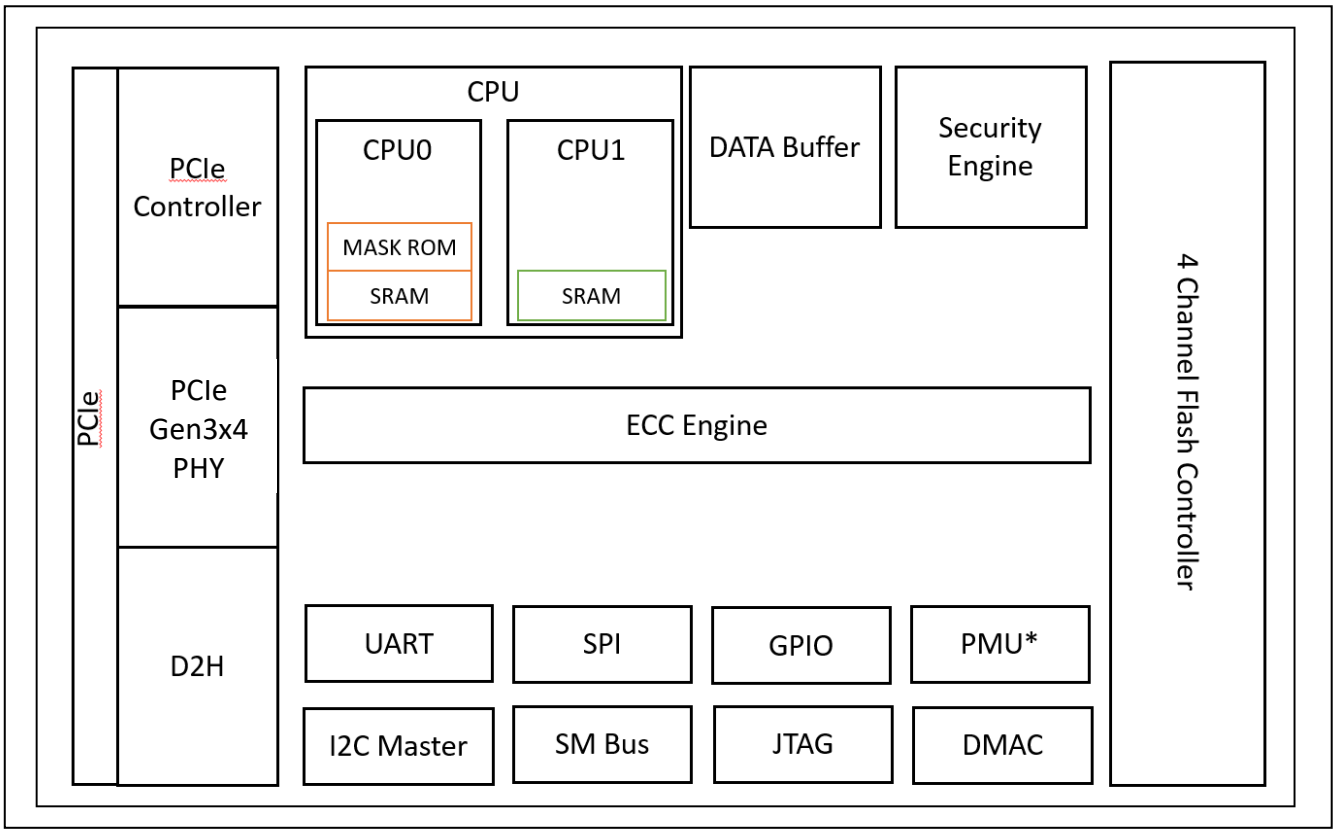
- **Sanitize Fucntion**

  SQFlash 720-D series default implement NVMe Sanitize Device Feature set, which supports the command set of Block Erase, Overwritten and Crypto Scramble. With the internal AES encryption support, the Crypto Scrambel process will start with resetting AES key. By doing so, existing data will be scrambled within 10ms and cannot be recovered anymore. Moreover, erase flag is set when erase function is triggered, which will ensure the whole erase process can be 100% completed. Even there’s power interrupt, after power resume, erase operation will be resume right away as well.

- **Write Protect Function**

  SQFlash 720-D series default support Write Protect function, when the write protect function enabled, all of the write command will carried to a buffer area without real programming to the Flash IC. Therefore, the data won’t be saved in this mode and will be totally discarded upon power shutting down.

■ Block Diagram



■ LBA value

Density	LBA
32 GB	62,533,296
64 GB	125,045,424
128 GB	250,069,680
256 GB	500,118,192
512 GB	1,000,215,216

5. Pin Assignment and Description

■ Interface Pin Assignments

Below table defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.0 of the PCI-SIG.

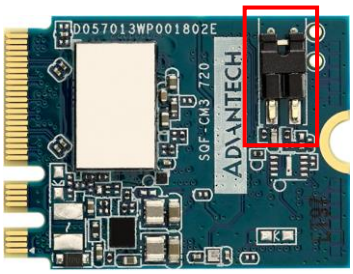
Pin No.	PCIe Pin	Description
1	GND	Ground
2	3.3V	3.3V
3	NC	Not connected
4	3.3V	3.3V
5	NC	Not connected
6	NC	No connect. Reserve for GPIO DAS customized
7	GND	Ground
8	Module Key A	Module Key
9	Module Key A	
10	Module Key A	
11	Module Key A	
12	Module Key A	
13	Module Key A	
14	Module Key A	
15	Module Key A	
16	NC	Not connected
17	NC	Not connected
18	GND	Ground
19	NC	Not connected
20	NC	Not connected
21	NC	Not connected
22	NC	Not connected
23	NC	Not connected
24	Module Key E	Module Key
25	Module Key E	
26	Module Key E	
27	Module Key E	
28	Module Key E	
29	Module Key E	
30	Module Key E	
31	Module Key E	
32	NC	Not connected
33	GND	Ground
34	NC	Not connected
35	PERp0	PERp0
36	NC	Not connected
37	PERn0	PERn0
38	VENDOR DEFINED_1	VENDOR DEFINED_1
39	GND	Ground
40	VENDOR DEFINED_2	VENDOR DEFINED_2
41	PETp0	PETp0
42	NC	No connect. Reserve for GPIO WP customized
43	PETn0	PETn0
44	NC	Not connected
45	GND	Ground
46	NC	Not connected
47	REFCLKp0	REFCLKp0
48	NC	Not connected

49	REFCLKn0	REFCLKn0
50	NC	Not connected
51	GND	Ground
52	PERST0# (I)	PERST0# (I)
53	CLKREQ0# (I/O)	CLKREQ0# (I/O)
54	NC	Not connected
55	NC	Not connected
56	NC	Not connected
57	GND	Ground
58	I2C_DATA (I/O)	Not connected
59	PERp1	PERp1
60	I2C_CLK (I)	Not connected
61	PERn1	PERn1
62	NC	Not connected
63	GND	Ground
64	NC	No connect. Reserve for GPIO Erase customized
65	PETp1	PETp1
66	NC	Not connected
67	PETn1	PETn1
68	NC	Not connected
69	GND	Ground
70	NC	Not connected
71	NC	Not connected
72	3.3V_3	3.3V_3
73	NC	Not connected
74	3.3V	3.3V
75	GND	Ground

■ Hardware Jumper Feature Set

SQFlash 720-D mounted a 2-pin jumper on the PCB, which can control the specific feature enable/disable. Hardware jumper feature set default support Write Protect function, and optionally the pin can be set to Data Erase.

- Short jumper → Data Erase enabled or Write Protect enabled
- Remove jumper → Data Erase disabled or Write Protect disabled



6. NVMe Command List

■ Admin commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
NVM Command Set Specific	
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

■ NVM commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
08h	Write Zeroes
09h	Dataset Management

7. Identify Device Data

The Identity Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

■ Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	SN
63:24	M	Model Number (MN)	Model Number
71:64	M	Firmware Revision (FR)	FW Name
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	0
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0000
83:80	M	Version (VER)	0x00010300
87:84	M	RTD3 Resume Latency (RTD3R)	(TBD)
91:88	M	RTD3 Entry Latency (RTD3E)	(TBD)
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000100
99:96	M	Controller Attributes (CTRATT)	0x00000000
111:100	-	Reserved	0x00
127:112	O	FRU Globally Unique Identifier (FGUID)	0x00
239:128	-	Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0
257:256	M	Optional Admin Command Support (OACS)	0x001F
258	M	Abort Command Limit (ACL)	0x00
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x06
262	M	Error Log Page Entries (ELPE)	0x0F
263	M	Number of Power States Support (NPSS)	0x04
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x01
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	(TBD)
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	(TBD)
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0000
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000(HMB off)0x00080000(HMB on)
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0
295:280	O	Total NVM Capacity (TNVMCAP)	0
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0
315:312	O	Replay Protected Memory Block Support (RPMBS)	0
317:316	O	Extended Device Self-test Time (EDSTT)	0x001E
318	O	Device Self-test Options (DSTO)	0x01
319	M	Firmware Update Granularity (FWUG)	0x1
321:320	M	Keep Alive Support (KAS)	0x0001
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	1
325:324	O	Minimum Thermal Management Temperature (MNTMT)	(TBD)
327:326	O	Maximum Thermal Management Temperature (MXTMT)	(TBD)
331:328	O	Sanitize Capabilities (SANICAP)	0x00000006
511:316	-	Reserved	0

NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x0080
519:516	M	Number of Namespaces (NN)	0x01
521:520	M	Optional NVM Command Support (ONCS)	0x001E
523:522	M	Fused Operation Support (FUSES)	0
524	M	Format NVM Attributes (FNA)	0
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal (AWUN)	0x00FF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x00
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0
533:532	O	Atomic Compare & Write Unit (ACWU)	0x00
535:534	M	Reserved	0
539:536	O	SGL Support (SGLS)	0x00
703:540	M	Reserved	0
IO Command Set Attributes			
2047:704	M	Reserved	0
2079:2048	M	Power State 0 Descriptor	(TBD)
2111:2080	O	Power State 1 Descriptor	PSD1
2143:2112	O	Power State 2 Descriptor	PSD2
2175:2144	O	Power State 3 Descriptor	PSD3
2207:2176	O	Power State 4 Descriptor	PSD4
…	-	(N/A)	0
3071:3040	O	Power State 31 Descriptor	PSD31
Vendor Specific			
4095:3072	O	Vendor Specific (VS)	Vendor Reserved

■ Identify Namespace Data Structure & NVM Command Set Specific

Bytes	Description
7:0	Namespace Size (NSZE)
15:8	Namespace Capacity (NCAP)
23:16	Namespace Utilization (NUSE)
24	Namespace Features (NSFEAT)
25	Number of LBA Formats (NLBAF)
26	Formatted LBA Size (FLBAS)
27	Metadata Capabilities (MC)
28	End-to-end Data Protection Capabilities (DPC)
29	End-to-end Data Protection Type Settings (DPS)
30	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	Reservation Capabilities (RESCAP)
32	Format Progress Indicator (FPI)
33	Deallocate Logical Block Features (DLFEAT)
35:34	Namespace Atomic Write Unit Normal (NAWUN)
37:36	Namespace Atomic Write Unit Power Fail (NAWUPF)
39:38	Namespace Atomic Compare & Write Unit (NAWWU)
41:40	Namespace Atomic Boundary Size Normal (NABSN)
43:42	Namespace Atomic Boundary Offset (NABO)
45:44	Namespace Atomic Boundary Size Power Fail (NABSPF)
47:46	Namespace Atomic Optimal IO Boundary (NOIOB)
63:48	NVM Capacity (NVMCAP)
103:64	Reserved
119:104	Namespace Globally Unique Identifier (NGUID)
127:120	IEEE Extended Unique Identifier (EUI64)
131:128	LBA Format 0 Support (LBAF0)
135:132	LBA Format 1 Support (LBAF1)
139:136	LBA Format 2 Support (LBAF2)
143:140	LBA Format 3 Support (LBAF3)
147:144	LBA Format 4 Support (LBAF4)
151:148	LBA Format 5 Support (LBAF5)
155:152	LBA Format 6 Support (LBAF6)
159:156	LBA Format 7 Support (LBAF7)
163:160	LBA Format 8 Support (LBAF8)
167:164	LBA Format 9 Support (LBAF9)
171:168	LBA Format 10 Support (LBAF10)
175:172	LBA Format 11 Support (LBAF11)
179:176	LBA Format 12 Support (LBAF12)
183:180	LBA Format 13 Support (LBAF13)
187:184	LBA Format 14 Support (LBAF14)
191:188	LBA Format 15 Support (LBAF15)
383:192	Reserved
4095:384	Vendor Specific (VS)

■ List of Device Identification for Each Capacity

Capacity	Byte[7:0]: Namespace Size (NSZE)
128 GB	EE7C2B0
256 GB	1DCF32B0
512 GB	3B9E12B0h

8. SMART Attributes

ID	ATTRIBUTE_NAME	Byte index	
01h	Critical Warning	[0]	-
02h	Composite Temperature	[2:1]	°K
03h	Available Spare	[3]	%
04h	Available Spare Threshold	[4]	%
05h	Percentage Used	[5]	%
06h	Data Units Read	[47:32]	1000 Sectors
07h	Data Units Written(Host Write)	[63:48]	1000 Sectors
08h	Host Read Commands	[79:64]	count
09h	Host Write Commands	[95:80]	count
0Ah	Controller Busy Time	[111:96]	mins
0Bh	Power Cycles	[127:112]	count
0Ch	Power On Hours	[143:128]	hours
0Dh	Unsafe Shutdowns	[159:144]	count
0Eh	Media Errors	[175:160]	times
0Fh	Number of Error Information Log Entries	[191:176]	count
1Ah	Warning Composite Temperature Time	[195:192]	mins
1Bh	Critical Composite Temperature Time	[199:196]	mins
1Ch	Flash Read Sector	[7:0]	sector
1Dh	Flash Write Sector	[15:8]	sector
1Eh	UNC Error	[23:16]	count
1Fh	PHY Error	[27:24]	count
20h	Early Bad Block	[31:28]	count
21h	Later Bad Block	[35:32]	count
22h	Max Erase Count	[39:36]	count
23h	Average Erase Count	[43:40]	count
24h	Current Percent Spares	[51:44]	%
25h	Current Temperature	[53:52]	°K
26h	Lowest Temperature	[55:54]	°K
27h	Highest Temperature	[57:56]	°K
28h	Reserved	[59:58]	-
29h	Current Controller Temperature	[61:60]	°K
2Ah	Spare Blocks	[63:62]	count

9. System Power Consumption

■ Supply Voltage

Parameter	Rating
Operating Voltage	3.3V

■ Power Consumption

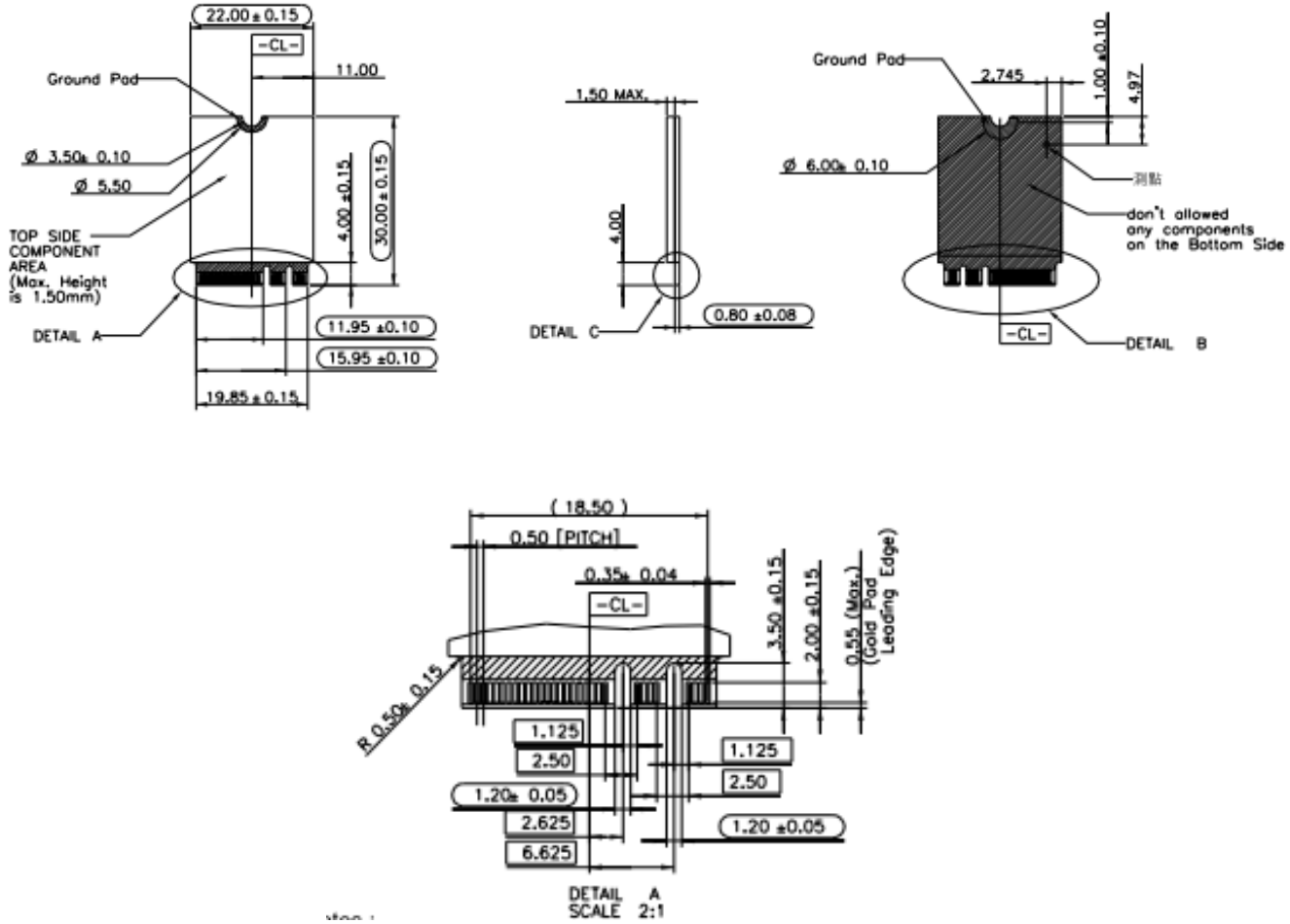
(mW)		Read	Write	Idle
3D TLC (BiCS5)	128 GB	1,700	1,400	800
	256 GB	1,800	1,750	800
	512 GB	1,900	1,850	800

(mW)		Read	Write	Idle
3D sTLC (BiCS5)	32 GB	TBD	TBD	TBD
	64 GB	TBD	TBD	TBD
	128 GB	TBD	TBD	TBD

1. The average value of power consumption is achieved based on 100% conversion efficiency.
2. The measured power voltage is 3.3V.
3. Samples were built of Toshiba 3D TLC (BiCS5) flash and measured under ambient temperature.
4. Sequential R/W is measured while testing 1MB sequential R/W 3 times by IOMeter.
5. Power Consumption may differ according to flash configuration and platform.

10. Physical Dimension

M.2 2230 (A+E key) PCIe/NVMe SSD (Unit: mm)



Appendix: Part Number Table

3D TLC (BiCS5)

Product	Advantech PN
SQF 720-D PCIe/NVMe M.2 2230 128G BiCS5 3D TLC (0~70°C)	SQF-C3AV1-128GDEDC
SQF 720-D PCIe/NVMe M.2 2230 256G BiCS5 3D TLC (0~70°C)	SQF-C3AV1-256GDEDC
SQF 720-D PCIe/NVMe M.2 2230 512G BiCS5 3D TLC (0~70°C)	SQF-C3AV1-512GDEDC