H/S mSATA 640 Datasheet

(SQF-SHMxx-xG-SBx)

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Revision History

Rev.	Date	History
1.0	2017/12/7	1. 1st draft
1.1	2018/5/18	1. Text correction & update information
1.2	2018/8/14	1. Add 3D NAND information
1.3	2018/10/9	1. Update performance data

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1. Overview

Advantech SQFlash 640 series H/S mSATA (SQF-SHM 640) delivers all the advantages of flash disk technology with the Serial ATA I/II/III interface and is fully compliant with MO-300 mSATA specification. The SQF-SHM 640 is designed to operate at a maximum operating frequency of 200MHz with 30MHz external crystal. Its capacity could provide a wide range up to 256GB. Moreover, it can reach up to 550MB/s read as well as 500MB/s write high performance based on MLC flash (with 32MB SDR enabled and measured by CrystalDiskMark v5.0). The power consumption of SQF-SHM 640 is much lower than traditional hard drives, making it the best embedded solution for new platforms.

2. Features

- **Standard SATA interface**
  - Support SATA 1.5 Gbps, 3.0 Gbps, and 6.0 Gbps interface
  - SATA Revision 3.0 compliant
  - Power management supported
- **Operating Voltage：3.3V**
- **TRIM、AHCI supported**
- **Temperature Ranges**
  - Commercial Temperature
    - 0℃ to 70℃ for operating
    - -40℃ to 85℃ for storage
  - Industrial Temperature
    - -40℃ to 85℃ for operating
    - -40℃ to 85℃ for storage
- **Mechanical Specification**
  - Shock：1,500G / 0.5ms
  - Vibration：20G / 80~2,000Hz
- **Humidty**
  - Humidity：5% ~ 95% under 55℃
- **Endurance： > 2,000,000 program/erase cycles**
  - This is a test result of the whole SQFlash drive. The test is to keep writing a fixed logical block address (LBA) and see if any bad blocks occur after 2M cycles. With wear-levelling mechanism, although the disk was kept writing the same LBA but the physical block changes per block writing. So this test also proves that wear-leveling is really working, or the block would be wearout after its designated life cycles.
- **Data Retention**
  - 10 years
- **Acquired RoHS、WHQL、CE、FCC Certificate**
- **Acoustic：0 dB**
- **Dimension：26.88 mm x 29.85 mm x 4.0 mm**

3. Specification Table

■ Performance

		Sequential Performance (MB/sec)		Random Performance (IOPS @4K)	
		Read	Write	Read	Write
SLC	1 GB	TBD	TBD	TBD	TBD
	2 GB	TBD	TBD	TBD	TBD
	4 GB	TBD	TBD	TBD	TBD
	8 GB	TBD	TBD	TBD	TBD
	16 GB	TBD	TBD	TBD	TBD
	32 GB	TBD	TBD	TBD	TBD
Ultra MLC	16 GB	355.83	165.92	36,957	40,056
	32 GB	561.72	313.61	74,856	75,655
	64 GB	561.67	475.19	88.797	80.139
	128 GB	561.36	497.16	87.943	86.088
MLC	32 GB	355.83	165.92	36,957	40,056
	64 GB	561.47	327.99	67,633	76,727
	128 GB	561.30	472.86	82,841	82,765
	256 GB	561.70	498.93	82,376	82,891
3D NAND (BiCS3)	64 GB	554.55	260.29	35,010	61,265
	128 GB	561.15	458.49	65,402	81,994
	256 GB	561.97	498.67	84,850	86,060
	512 GB	561.67	495.34	75,811	68,331

* All performance above are tested with AHCI mode.

Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

TBW = [(NAND Endurance) x (SSD Capacity)] / WAF

- **NAND Endurance**: Program / Erase cycle of a NAND flash.
  - SLC: 100,000 cycles
  - Ultra MLC: 30,000 cycles
  - MLC: 3,000 cycles
  - 3D NAND (BiCS3): 3,000 cycles
- **SSD Capacity**: SSD physical capacity in total of a SSD.
- **WAF**: Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

WAF = (Lifetime write to flash) / (Lifetime write to host)

Endurance measurement is based on JDEC 219 workload and verified with following workload conditions,

- PreCond%full = 100%
- Trim commands enabled
- Random data pattern.

- **SQFlash 640 H/S mSATA TBW**

	WAF	TBW		
		SLC	Ultra MLC	MLC
8 GB	TBD	TBD	--	--
16 GB	TBD	TBD	TBD	--
32 GB	2.13	TBD	TBD	25
64 GB	2.13	TBD	TBD	70
128 GB	1.91	TBD	TBD	133
256 GB	2.64	--	--	320

- **SQFlash 640 H/S mSATA (3D NAND (BiCS3)) TBW**

	WAF	TBW
		3D NAND (BiCS3)
64 GB	2.61	74
128 GB	2.93	131
256 GB	2.44	315
512 GB	2.07	744

- The endurance of SSD could be estimated based on users' behaviors, NAND endurance cycles, and write amplification factor. It is not guaranteed by the flash vendor.
- TBW may vary from flash configuration and platform
- "*" By simulation

4. General Description

Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQFlash 640 series mSATA applies the LDPC (Low Density Parity Check) of ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.
SQFlash provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. SQFlash implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

Power Loss Protection: Flush Manager

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SQFlash SSD applies the Flush Manager technology, only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.
In addition, it is critical for a controller to shorten the time the in-flight data stays in the controller internal cache. Thus, SQFlash applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. With Flush Manager, incoming data would only have a “pit stop” in the cache and then move to NAND flash directly. Also, the onboard DDR will be treated as an “organizer” to consolidate incoming data into groups before written into the flash to improve write amplification.

TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Over-Provision

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

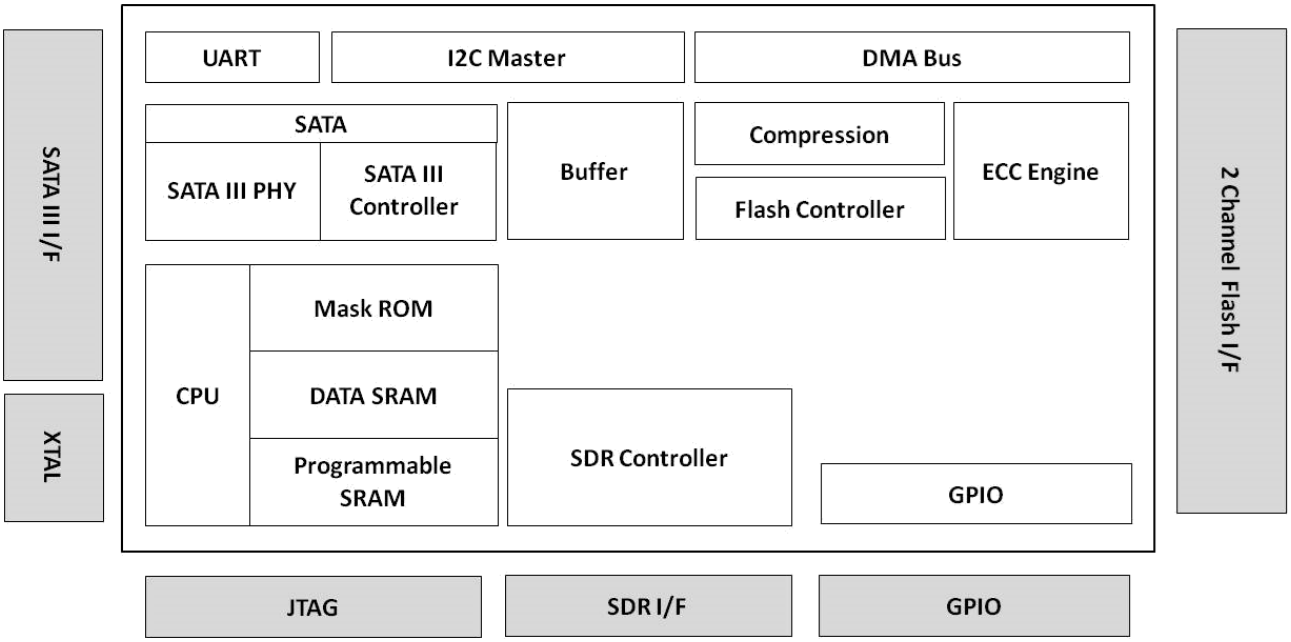
Sophisticate Product Management Systems

Since industrial application require much more reliable devices compare with consumer product, a more sophisticated product management system become necessary for industrial customer requirement. The key to providing reliable devices is product traceability and failure analysis system. By implement such systems end customer can expect much more reliable product.

Thermal Throttling

Thermal Throttling function is for protecting the drive and reducing the possibility of read / write error due to overheat. The temperature is monitored by the thermal sensor. As the operating temperature continues to increase to threshold temperature, the Thermal Throttling mechanism is activated. At this time, the performance of the drive will be significantly decreased to avoid continuous heating. When the operating temperature falls below threshold temperature, the drive can resume to normal operation.

■ Block Diagram



■ LBA value

Density	LBA
16 GB	30,752,064
32 GB	62,008,128
64 GB	125,045,424
128 GB	250,069,680
256 GB	500,118,192
512 GB	1,000,215,216

5. Pin Assignment and Description

5.1 H/S mSATA Interface Pin Assignments

Pin #	Function	Description
1	GPIO_WP	Write Protection GPIO
2	+3.3V	3.3V Source
3	NC	No Connect
4	DGND	Digital GND
5	NC	No Connect
6	NC	No Connect
7	NC	No Connect
8	NC	No Connect
9	DGND	Digital GND
10	NC	No Connect
11	NC	No Connect
12	NC	No Connect
13	NC	No Connect
14	NC	No Connect
15	DGND	Digital GND
16	NC	No Connect
17	GPIO_QE	Quick Erase GPIO
18	DGND	Digital GND
19	NC	No Connect
20	NC	No Connect
21	SATA GND	SATA Ground Return Pin
22	NC	No Connect
23	B+	Host Receiver Differential Signal Pair
24	+3.3V	3.3V Source
25	B-	Host Receiver Differential Signal Pair
26	SATA GND	SATA Ground Return Pin
27	SATA GND	SATA Ground Return Pin
28	NC	No Connect
29	SATA GND	SATA Ground Return Pin
30	NC	No Connect
31	A-	Host Transmitter Differential Signal Pair
32	NC	No Connect
33	A+	Host Transmitter Differential Signal Pair
34	DGND	Digital GND
35	SATA GND	SATA Ground Return Pin
36	NC	No Connect
37	SATA GND	SATA Ground Return Pin
38	NC	No Connect
39	+3.3V	3.3V Source
40	DGND	Digital GND
41	+3.3V	3.3V Source
42	NC	No Connect
43	NC	No Connect
44	DEVSLP	Enter/Exit DevSleep
45	NC	Reserved pin
46	NC	No Connect

47	NC	Reserved pin
48	NC	No Connect
49	DA/DSS	Device Activity Signal
50	DGND	Digital GND
51	GND	Default connect to GND
52	+3.3V	3.3V Source

6. Identify Device Data

The Identity Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

Word	ATA Identify Parameter	Value
0	General configuration bit-significant information	0040h
1	Obsolete	*1
2	Specific configuration	C837h
3	Obsolete	0010h
4-5	Retired	00000000h
6	Obsolete	003Fh
7-8	Reserved for assignment by the Compact Flash Association	00000000h
9	Retired	0000h
10-19	Serial number (20 ASCII characters)	Varies
20-21	Retired	00000000h
22	Obsolete	0000h
23-26	Firmware revision (8 ASCII characters)	Varies
27-46	Model number (xxxxxxxx)	Varies
47	7:0- Maximum number of sectors transferred per interrupt on MULTIPLE commands	8010h
48	Trusted Computing feature set options(not support)	4000h
49	Capabilities	2F00h
50	Capabilities	4000h
51-52	Obsolete	000000000h
53	Words 88 and 70:64 valid	0007h
54	Obsolete	*1
55	Obsolete	0010h
56	Obsolete	003Fh
57-58	Obsolete	*2
59	Sanitize and Number of sectors transferred per interrupt on MULTIPLE commands	5D10h
60-61	Maximum number of sector (28bit LBA mode)	*3
62	Obsolete	0000h
63	Multi-word DMA modes supported/selected	0407h
64	PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time	0078h
67	Minimum PIO transfer cycle time without flow control	0078h
68	Minimum PIO transfer cycle time with IORDY flow control	0078h
69	Additional Supported (support download microcode DMA)	0D00h
70	Reserved	0000h
71-74	Reserved for the IDENTIFY PACKET DEVICE command	0000000000000000h
75	Queue depth	001Fh
76	Serial SATA capabilities	E70Eh
77	Serial ATA Additional Capabilities	0086h
78	Serial ATA features supported	014Ch

79	Serial ATA features enabled	0040h
80	Major Version Number	0FF8h
81	Minor Version Number	0000h
82	Command set supported	706Bh
83	Command set supported	7409h
84	Command set/feature supported extension	6163h
85	Command set/feature enabled	7069h
86	Command set/feature enabled	B401h
87	Command set/feature default	6163h
88	Ultra DMA Modes	007Fh
89	Time required for security erase unit completion	0001h
90	Time required for Enhanced security erase completion	001Eh
91	Current advanced power management value	0000h
92	Master Password Revision Code	FFFEh
93	Hardware reset result. For SATA devices, word 93 shall be set to the value 0000h.	0000h
94	Obsolete	0000h
95	Stream Minimum Request Size	0000h
96	Streaming Transfer Time – DMA	0000h
97	Streaming Access Latency – DMA and PIO	0000h
98-99	Streaming Performance Granularity	0000h
100-103	Maximum user LBA for 48 bit Address feature set	*4
104	Streaming Transfer Time – PIO	0000h
105	Maximum number of 512-byte blocks per DATA SET MANAGEMENT command	0008h
106	Physical sector size/Logical sector size	4000h
107	Inter-seek delay for ISO-7779 acoustic testing in microseconds	0000h
108-111	World Wide Name	Varies
112-115	Reserved	0000000000000000h
116	Reserved	0000h
117-118	Words per logical Sector	00000000h
119	Supported settings	411Ch
120	Command set/Feature Enabled/Supported	401Ch
121-126	Reserved	0h
127	Obsolete	0h
128	Security status	0021h
129-140	Vendor specific	Varies
141	Vendor specific	Varies
142-159	Vendor specific	Varies
160	Reserved for CFA	0h
161-167	Reserved for CFA	0h
168	Device Nominal Form Factor	Varies
169	DATA SET MANAGEMENT command is supported	0001h
170-173	Additional Product Identifier	0h
174-175	Reserved	0h
176-205	Current media serial number	0h
206	SCT Command Transport	0h

207-208	Reserved	0h
209	Alignment of logical blocks within a physical block	4000h
210-211	Write-Read-Verify Sector Count Mode 3 (not support)	0000h
212-213	Write-Read-Verify Sector Count Mode 2 (not support)	0000h
214-216	Obsolete	0000h
217	Non-rotating media device	0001h
218	Reserved	0h
219	NV Cache relate (not support)	0h
220	Write read verify feature set current mode	0h
221	Reserved	0h
222	Transport major version number	10FFh
223	Transport minor version number	0000h
224-229	Reserved	0h
230-233	Extend number of user addressable sectors	0h
234	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h	0001h
235	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h	FFFEh
236-254	Reserved	0h
255	Integrity word (Checksum and Signature)	XXA5h

Capacity (GB)	*1 (Word 1/Word 54)	*2 (Word 57 – 58)	*3 (Word 60 – 61)	*4 (Word 100 – 103)
16	3FFFh	FBFC10h	1DD40B0h	1DD40B0h
32	3FFFh	FBFC10h	3BA2EB0h	3BA2EB0h
64	3FFFh	FBFC10h	7740AB0h	7740AB0h
128	3FFFh	FBFC10h	EE7C2B0h	EE7C2B0h
256	3FFFh	FBFC10h	FFFFFFFh	1DCF32B0h
512	3FFFh	FBFC10h	FFFFFFFh	3B9E12B0h

7. ATA Command Set

[Command Set List]

Op-Code	Command Description	Op-Code	Command Description
00h	NOP	91h	Initialize Device Parameters
06h	Data Set Management	92h	Download Microcode
10h-1Fh	Recalibrate	93h	Download Microcode DMA
20h	Read Sectors	B0h	SMART
21h	Read Sectors without Retry	B4h	Sanitize
24h	Read Sectors EXT	C4h	Read Multiple
25h	Read DMA EXT	C5h	Write Multiple
29h	Read Multiple EXT	C6h	Set Multiple Mode
2Fh	Read Log EXT	C8h	Read DMA
30h	Write Sectors	C9h	Read DMA without Retry
31h	Write Sectors without Retry	CAh	Write DMA
34h	Write Sectors EXT	CBh	Write DMA without Retry
35h	Write DMA EXT	CEh	Write Multiple FUA EXT
38h	CFA Write Sectors Without Erase	E0h	Standby Immediate
39h	Write Multiple EXT	E1h	Idle Immediate
3Dh	Write DMA FUA EXT	E2h	Standby
3Fh	Write Long EXT	E3h	Idle
40h	Read Verify Sectors	E4h	Read Buffer
41h	Read Verify Sectors without Retry	E5h	Check Power Mode
42h	Read Verify Sectors EXT	E6h	Sleep
44h	Zero EXT	E7h	Flush Cache
45h	Write Uncorrectable EXT	E8h	Write Buffer
47h	Read Log DMA EXT	EAh	Flush Cache EXT
57h	Write Log DMA EXT	ECh	Identify Device
60h	Read FPDMA Queued	EFh	Set Features
61h	Write FPDMA Queued	F1h	Security Set Password
70h-76h	Seek	F2h	Security Unlock
77h	Set Date & Time EXT	F3h	Security Erase Prepare
78h	Accessible Max Address configuration	F4h	Security Erase Unit
79h-7Fh	Seek	F5h	Security Freeze Lock
90h	Execute Device Diagnostic	F6h	Security Disable Password

Note: ND = Non-Data Command
PI = PIO Data-In Command
PO = PIO Data-Out Command
DM = DMA Command
DD = Execute Diagnostic Command

[Command Set Descriptions]

1. CHECK POWER MODE (code: E5h);
This command allow host to determine the current power mode of the device.

2. DOWNLOAD MICROCODE (code: 92h);
This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.
All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the content of the LBA Low register and the Sector Count register.
This allows transfer sizes from 0 bytes to 33,553,920 bytes, in 512bytes increments.

3. EXECUTE DEVICE DIAGNOSTIC (code: 90h);
This command performs the internal diagnostic tests implemented by the module.

4. FLUSH CACHE (code: E7h);
This command used by the host to request the device to flush the write cache.

5. FLUSH CACHE EXT (code: EAh);
This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media.

6. IDENTIFY DEVICE (code: ECh);
The IDENTIFY DEVICE command enables the host to receive parameter information from the module.

7. IDLE (code: 97h or E3h);
This command allows the host to place the module in the IDLE mode and also set the Standby timer. INTRQ may be asserted even through the module may not have fully transitioned to IDLE mode. If the Sector Count register is non-"0", then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is "0" then the Standby timer is disabled.

8. IDLE IMMEDIATE (code: E1h);
This command causes the module to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

9. INITIALIZE DEVICE PARAMETERS (code: 91h);
This command enables the host to set the number of sectors per track and the number of heads per cylinder.

10. NOP (code: 00h);
If this command is issued, the module respond with command aborted.

11. READ BUFFER (code: E4h);
This command enables the host to read the current contents of the module's sector buffer.

12. READ DMA (code: C8h or C9h);
This command reads from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

13. READ DMA Ext (code: 25h);
This command allows the host to read data using the DMA data transfer protocol.

14. READ MULTIPLE (code: C4h);

This command performs similarly to the READ SECTORS command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sector per block is defined by the content of word 59 in the IDENTIFY DEVICE response.

15. READ MULTIPLE EXT (code: 29h);

This command performs similarly to the READ SECTORS command. The number of sectors per block is defined by a successful SET MULTIPLE command. If no successful SET MULTIPLE command has been issued, the block is defined by the device's default value for number of sectors per block as defined in bits (7:0) in word 47 in the IDENTIFY DEVICE information.

16. READ NATIVE MAX ADDRESS (code: F8h);

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition.

17. READ NATIVE MAX ADDRESS EXT (code: 27h);

This command returns the native maximum address.

18. READ SECTOR(S) (code: 20h or 21h);

This command reads from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

19. READ SECTOR(S) EXT (code: 24h);

This command reads from "1" to "65536" sectors as specified in the Sector Count register. A sector count of "0" requests "65536" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

20. READ VERIFY SECTOR(S) (code: 40h or 41h);

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

21. READ VERIFY SECTOR(S) EXT (code: 42h);

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

22. RECALIBRATE (code: 1Xh);

This command return value is select address mode by the host request.

23. SECURITY DISABLE PASSWORD (code: F6h);

This command transfers 512 bytes of data from the host. Table defines the content of this information. If the password selected by word 0 match the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password is set.

24. SECURITY ERASE PREPARE (code: F3h);

This command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking.

25. SECURITY ERASE UNIT (code: F4h);

This command transfer 512 bytes of data from the host. Table## defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command.

26. SECURITY FREEZE LOCK (code: F5h);

This command shall set the device to frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen shall be disabled by power-off or hardware reset.

If SECURITY FREEZE LOCK is issued when the drive is in frozen mode, the drive executes the command and remains in frozen mode.

27. SECURITY SET PASSWORD (code: F1h);

This command transfer 512 bytes of data from the host. Table defines the content of this information. The data transferred controls the function of this command. Table defines the interaction of the identifier and security level bits.

28. SECURITY UNLOCK (code: F2h);

This command transfer 512 bytes of data from the host. Table (as Disable Password) defines the content of this information.

If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the identifier bit is set to user then the device shall compare the supplied password with the stored User password.

If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall be decremented for each password mismatch when SECURITY UNLOCK is issued and the device is locked. When this counter reachs zero then SECURITY UNLOCK and SECURITY ERASE UNIT command shall be aborted unitl a power-on or a hardware reset.

29. SEEK (code: 7Xh);

This command performs address range check.

30. SET MAX ADDRESS (code: F9h);

After successful command completion, all read and write access attempts to address greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error. IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

31. SET MAX ADDRESS EXT (code: 37h);

After successful command completion, all read and write access attempts to address greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error. IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

32. SET FEATURE (code: EFh);

This command is used by the host to establish parameters that affect the execution of certain device features.

33. SET MULTIPLE MODE (code: C6h);

This command enables the device to perform READ and Write Multiple operations and establishes the block count for these commands.

34. SLEEP (code: 99h or E6h);

This command causes the module to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

35. SMART READ DATA (code: B0h with Feature register value of D0h);

This command returns the Device SMART data structure to the host.

36. SMART ENABLE/DISABLE AUTO SAVE (code: B0h with Feature register value of D2h);

This command enables and disables the optional attribute autosave feature of the device.

37. SMART EXECUTE OFF_LINE (code: B0h with Feature register value of D4h);
This command cause the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode.

38. SMART READ LOG (code: B0h with Feature register value of D5h);
This command returns the specified log data to the host.

39. SMART ENABLE OPERATION (code: B0h with Feature register value of D8h);
This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device.

40. SMART DISABLE OPERATION (code: B0h with Feature register value of D9h);
This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature. After command acceptance the device shall disable all SMART operations.
After receipt of this command by the device, all other SMART commands including SMART DISABLE OPERATION commands, with exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be command aborted by the device.

41. SMART RETURN STATUS (code: B0h with Feature register value of DAh);
This command causes the device to communicate the reliability status of the device to the host.

42. STANDBY (code: E2h);
This command causes the module to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.

43. STANDBY IMMEDIATE (code: E0h);
This command causes the module to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.

44. WRITE BUFFER (code: E8h);
This command enables the host to overwrite contents of the module's sector buffer with any data pattern desired.

45. WRITR DMA (code: CAh or CBh);
This command writes from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

46. WRITR DMA EXT (code: 35h);
This command writes from "1" to "65536" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "65536" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

47. WRITE MULTIPLE (code: C5h);
This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

48. WRITE MULTIPLE EXT (code: 39h);
This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

49. WRITE SECTOR(S) (code: 30h);

This command writes from “1” to “256” sectors as specified in the Sector Count register. A sector count of “0” requests “256” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

50. WRITE SECTOR(S) EXT (code: 34h);

This command writes from “1” to “65536” sectors as specified in the Sector Count register. A sector count of “0” requests “65536” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

51. WRITE SECTOR(S) W/O ERASE (code: 38h);

This command writes from “1” to “256” sectors as specified in the Sector Count register. A sector count of “0” requests “256” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

52. WRITE VERIFY (code: 3Ch);

This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

8. System Power Consumption

8.1 Supply Voltage

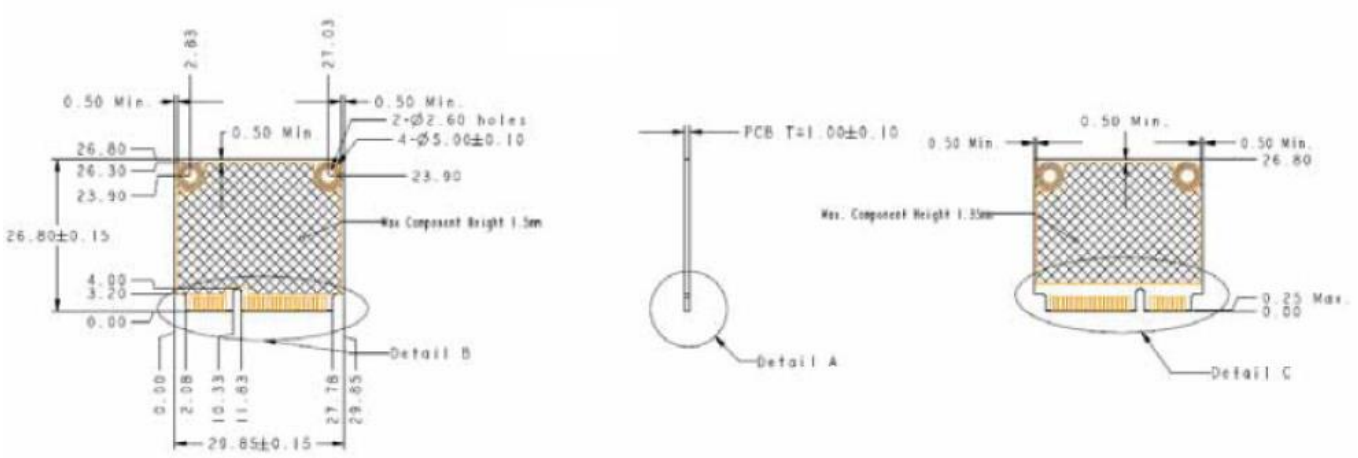
Parameter	Rating
Operating Voltage	3.3V

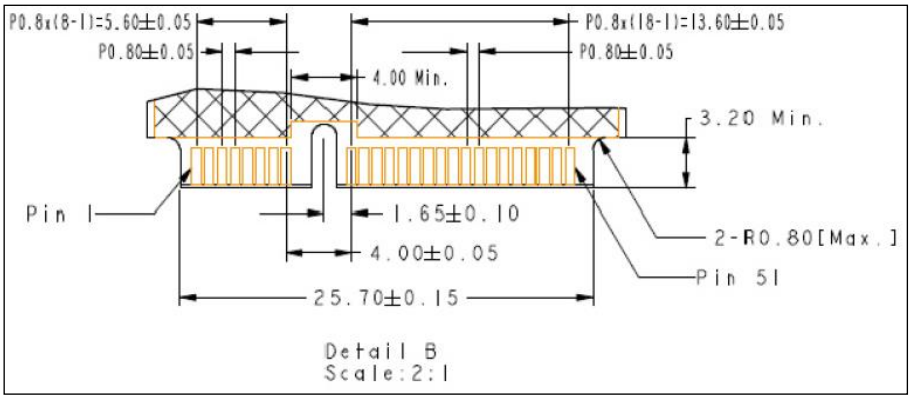
8.2 Power Consumption

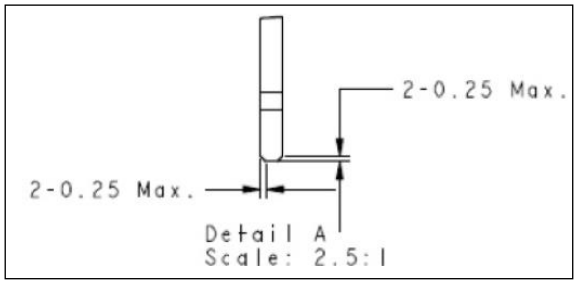
mA		Read	Write	Idle	Slumber
SLC	8 GB	TBD	TBD	TBD	TBD
	16 GB	TBD	TBD	TBD	TBD
	32 GB	TBD	TBD	TBD	TBD
	64 GB	TBD	TBD	TBD	TBD
	128 GB	TBD	TBD	TBD	TBD
Ultra MLC	16 GB	350.12	401.67	67.51	3.09
	32 GB	409.55	562.12	73.12	3.09
	64 GB	430.76	533.33	76.30	3.10
	128 GB	433.79	571.21	76.59	3.10
MLC	32 GB	350.12	401.67	67.51	3.09
	64 GB	409.55	562.12	73.12	3.09
	128 GB	430.76	533.33	76.30	3.10
	256 GB	433.79	571.21	76.59	3.10
3D NAND (BiCS3)	64 GB	363.36	390.90	98.48	4.54
	128 GB	384.84	412.12	98.48	4.54
	256 GB	422.72	448.48	98.48	4.54
	512 GB	412.12	439.39	96.96	4.84

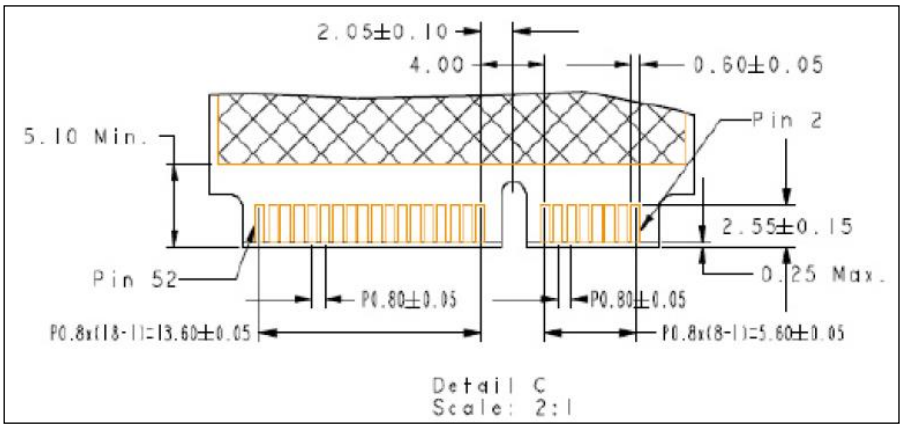
9. Physical Dimension

Half-size mSATA (Unit: mm)









Appendix: Part Number Table

Ultra MLC

Product	Advantech PN
SQF HS mSATA 640 16G U-MLC (0~70°C)	SQF-SHMU1-16G-SBC
SQF HS mSATA 640 32G U-MLC (0~70°C)	SQF-SHMU2-32G-SBC
SQF HS mSATA 640 64G U-MLC (0~70°C)	SQF-SHMU2-64G-SBC
SQF HS mSATA 640 128G U-MLC (0~70°C)	SQF-SHMU2-128G-SBC
SQF HS mSATA 640 16G U-MLC (-40~85°C)	SQF-SHMU1-16G-SBE
SQF HS mSATA 640 32G U-MLC (-40~85°C)	SQF-SHMU2-32G-SBE
SQF HS mSATA 640 64G U-MLC (-40~85°C)	SQF-SHMU2-64G-SBE
SQF HS mSATA 640 128G U-MLC (-40~85°C)	SQF-SHMU2-128G-SBE

MLC

Product	Advantech PN
SQF HS mSATA 640 32G MLC (0~70°C)	SQF-SHMM1-32G-SBC
SQF HS mSATA 640 64G MLC (0~70°C)	SQF-SHMM2-64G-SBC
SQF HS mSATA 640 128G MLC (0~70°C)	SQF-SHMM2-128G-SBC
SQF HS mSATA 640 256G MLC (0~70°C)	SQF-SHMM2-256G-SBC
SQF HS mSATA 640 32G MLC (-40~85°C)	SQF-SHMM1-32G-SBE
SQF HS mSATA 640 64G MLC (-40~85°C)	SQF-SHMM2-64G-SBE
SQF HS mSATA 640 128G MLC (-40~85°C)	SQF-SHMM2-128G-SBE
SQF HS mSATA 640 256G MLC (-40~85°C)	SQF-SHMM2-256G-SBE

3D NAND (BiCS3)

Product	Advantech PN
SQF HS mSATA 640 64G 3D NAND (BiCS3) (0~70°C)	SQF-SHMV1-64G-SBC
SQF HS mSATA 640 128G 3D NAND (BiCS3) (0~70°C)	SQF-SHMV2-128G-SBC
SQF HS mSATA 640 256G 3D NAND (BiCS3) (0~70°C)	SQF-SHMV2-256G-SBC
SQF HS mSATA 640 512G 3D NAND (BiCS3) (0~70°C)	SQF-SHMV2-512G-SBC
SQF HS mSATA 640 64G 3D NAND (BiCS3) (-40~85°C)	SQF-SHMV1-64G-SBE
SQF HS mSATA 640 128G 3D NAND (BiCS3)C (-40~85°C)	SQF-SHMV2-128G-SBE
SQF HS mSATA 640 256G 3D NAND (BiCS3) (-40~85°C)	SQF-SHMV2-256G-SBE
SQF HS mSATA 640 512G 3D NAND (BiCS3) (-40~85°C)	SQF-SHMV2-512G-SBE