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Agilex™ 7 FPGAs and SoCs Device Overview

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1. Overview of the Agilex™ 7 FPGAs and SoCs

The Agilex™ 7 FPGA product family includes the highest performance FPGAs and SoCs in the industry. Comprising of the high-performance F-Series, I-Series, and M-Series FPGAs, the Agilex 7 FPGAs and SoCs provide a range of premium features for the most demanding applications.

- Transceivers with the highest data rate in the industry—up to 116 Gbps
- The industry's first PCI Express* (PCIe*) 5.0 and Compute Express Link* (CXL*) support
- Options to integrate in-package HBM2E memory, delivering the highest memory bandwidth in the industry—over 1 terabytes per second (TBps).
- System-in-package (SiP) chiplet architecture
  - Provides tailored and flexible solutions by integrating heterogeneous technologies in a SiP for highly-specific applications
  - Using advanced 3D packaging technology, such as the Embedded Multi-die Interconnect Bridge (EMIB), Intel combines the traditional FPGA die with purpose-built semiconductor chiplet in a single device package

The Agilex 7 FPGA product family delivers on average 50% higher fabric performance and up to 40% lower total power consumption compared to previous generation Intel® FPGAs. To achieve this improvement, the product family leverages these key innovations and techniques:

- Advanced Intel 10-nm SuperFin and Intel 7 technologies
- Second generation Hyperflex® FPGA architecture
- High level of system integration
- SmartVID standard power devices
- Power islands, power gating, and other power reduction techniques

These capabilities and advanced features enable customized connectivity and acceleration for the most compute-intensive, bandwidth-intensive, and memory-intensive applications. The applications span across many segments including communications, high-performance computing, video and broadcast equipments, high-end test and measurement, medical electronics, data centers, and defense.

Note: The information contained in this document is preliminary and subject to change.

Related Information

Agilex FPGA Portfolio
Provides the latest information about the Agilex FPGA portfolio.

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1.1. Key Features and Innovations in Agilex 7 FPGAs and SoCs

With the power and performance efficiency of industry-leading Intel 10-nm SuperFin and Intel 7 technologies, the Agilex 7 FPGAs and SoCs are available in several series.

Table 1. Agilex 7 FPGAs and SoCs Series

Feature and Innovation	F-Series FPGA	I-Series FPGA	M-Series FPGA
Application optimization	For a wide range of applications that require optimal balance of power and performance	For high performance processor interface and bandwidth-intensive applications	For compute-intensive, high-memory bandwidth applications
Process technology	Intel 10-nm SuperFin	Intel 10-nm SuperFin	Intel 7
Architecture	Chiplet architecture		
Packaging	Rectangular package and hex pattern ball array for more functionality per area		
Core fabric	Second generation Hyperflex core fabric		
Logic elements	573 thousand to 2.7 million	1.9 million to 4 million	3.2 million to 3.9 million
On-chip RAM	MLAB, M20K, and eSRAM	MLAB, M20K, and eSRAM	MLAB and M20K
	287 Mb	431 Mb	370 Mb
Variable precision DSP	Industry-leading digital signal processing (DSP) support with up to 38 TFLOPS		
Clocking and PLL	• Programmable clock tree synthesis for flexible, low power, and low skew clocking • I/O PLL supports integer mode with precise frequency synthesis for general purpose I/O, external memory interfaces, LVDS, and fabric usage • Transmit PLL (TX PLL) supports fractional synthesis and ultra-low jitter with LC tank-based PLL for transceiver usage.		
General purpose I/Os	1.2 V to 1.5 V general-purpose I/O (GPIO)	1.2 V to 1.5 V GPIO	1.05 V to 1.3 V GPIO
External memory interface	Fourth generation scalable integrated hard memory controllers and PHY		
	3,200 Mbps DDR4	3,200 Mbps DDR4	• 820 Gbps with HBM2E • 5,600 Mbps DDR5 • 3,200 Mbps DDR4 • 5,500 Mbps LPDDR5 • Hardened memory NoC
HBM2E	—	—	Yes
Memory NoC	—	—	Yes
Cryptography	High-performance hard crypto blocks(1) supporting Advanced Encryption Standard (AES) and SM4 encryption standards	High-performance hard crypto blocks(1) supporting AES and SM4 encryption standards	SDM supports AES
Transceiver hard IPs	• Multiple Gigabit Ethernet (GbE) network interface connectivity in one device • PCS. PCIe, and CXL(2) hard IPs free up valuable core logic resources, save power, and increase your productivity • Hardened 10, 25, 40, 50, 100, 200, and 400 GbE media access control (MAC), physical coding sublayer (PCS), and forward error correction (FEC) with IEEE 1588 support		

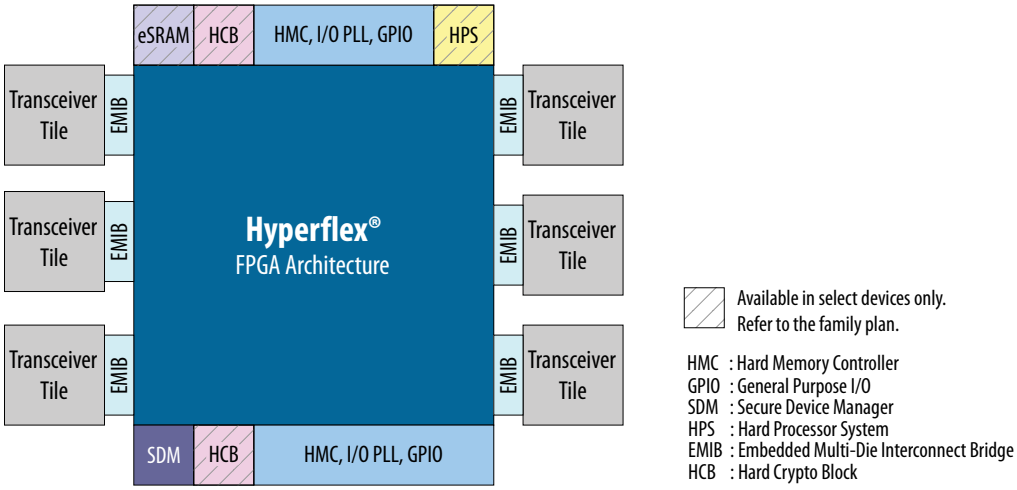
continued...

(1) Only available in select devices. Refer to the family plan.

Feature and Innovation	F-Series FPGA	I-Series FPGA	M-Series FPGA
	• GbE up to 58 Gbps PAM4 or 32 Gbps non-return-to-zero (NRZ) • PCIe 4.0 ×16	• GbE up to 116 Gbps PAM4 • Up to 4 Tbps of transceiver bandwidth • PCIe 5.0(2) ×16 at 32 Gbps data rate • CXL support(2)	• GbE Up to 116 Gbps PAM4 or 58 Gbps NRZ • PCIe 5.0(2) ×16 at 32 Gbps data rate • CXL support(2)
SDM	Dedicated secure device manager (SDM) that: • Manages FPGA configuration process and all security features • Performs authenticated FPGA configuration and HPS boot • Supports FPGA bitstream encryption, secure key provisioning, and physically unclonable function (PUF) key storage • Manages runtime sensors and supports active tamper detection and responses • Supports platform attestation using the security protocol and data model (SPDM) protocol • Provides access to hardened cryptographic engines as a service		
HPS (SoCs only)	Hard processor system (HPS) with embedded quad-core 64-bit Arm* Cortex*-A53 up to 1.4 GHz(3) processors		
Power saving	Comprehensive set of advanced power saving features that deliver up to 40% lower power compared to previous generation high-performance FPGAs		

1.2. Agilex 7 FPGAs and SoCs Block Diagram

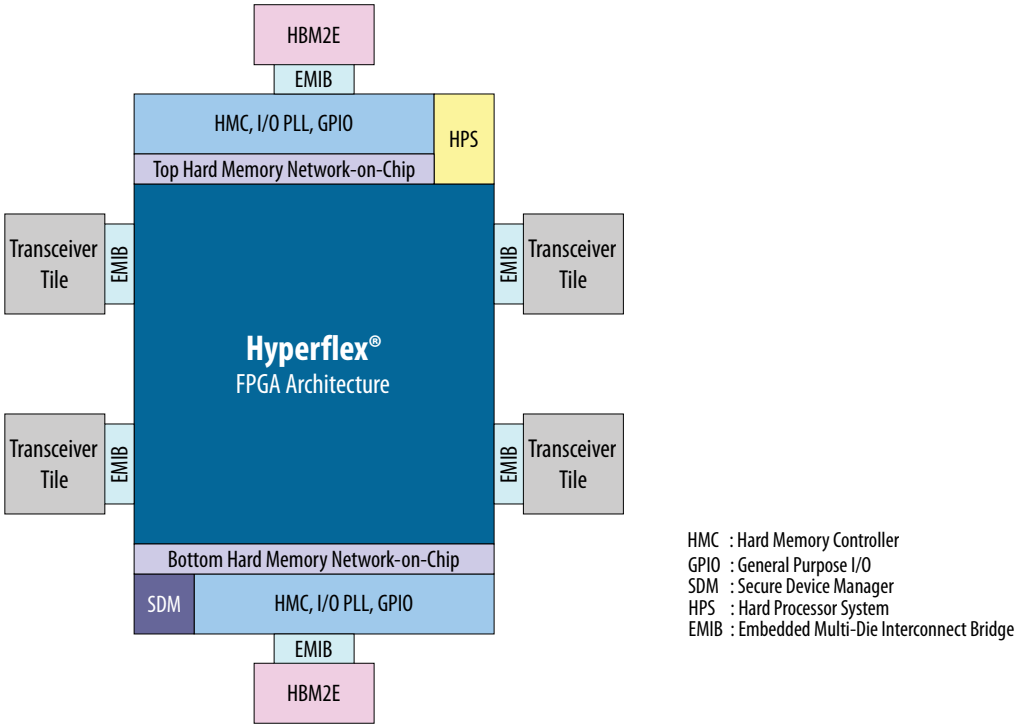
Figure 1. Agilex 7 FPGAs and SoCs F-Series and I-Series Block Diagram



(2) CXL is available only for I-Series and M-Series FPGAs with at least one R-Tile.

(3) Except AGI 035 and AGI 040 devices.

Figure 2. Agilex 7 FPGAs and SoCs M-Series Block Diagram



Related Information

Agilex 7 FPGAs and SoCs Family Plan on page 13

1.3. Agilex 7 FPGAs and SoCs Summary of Features

The Agilex 7 FPGAs and SoCs share the same high performance core fabric and common features.

Table 2. Feature Summary

Feature	Description
Packaging	• Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology • Multiple devices with identical package footprints allow seamless migration across different device densities • Mixture of ball pitch FBGA packages, 1,025 mm, 0.92 mm, and several mixed pitch packages
High performance core fabric	• Second Generation Hyperflex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks • Enhanced adaptive logic module (ALM) • Improved multi-track routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture with programmable clock tree synthesis • Fine-grained partial reconfiguration
Internal memory blocks	• Multi-level on-chip memory hierarchy • M20K—20 kilobits with hard error correction code (ECC) support • MLAB—640-bit distributed LUTRAM

continued...

Feature		Description	
		F-Series I-Series	eSRAM—18 Mb embedded memory block with hard ECC support
Variable precision DSP blocks		• Variable precision DSP blocks with hard IEEE 754-compliant floating-point units, including support for: — Single-precision FP32 (32-bit arithmetic) — Half-precision FP16 (16-bit arithmetic) floating point modes — Tensor floating point FP19 (19-bit arithmetic) floating point modes — BFLOAT16 floating-point format • Supports signal processing with precision ranging from 9×9 up to 54×54 • Native 27×27, 18×19, and 9×9 multiplication modes • 64-bit accumulator and cascade for systolic finite impulse response (FIR) filters • Internal coefficient memory banks • Pre-adder/subtractor improves efficiency • 2× additional pipeline register increases performance and reduces power consumption	
Core clock networks		• Programmable clock tree synthesis—backwards compatible with global, regional and peripheral clock networks • Synthesize clocks where needed only—minimizes dynamic power	
		F-Series I-Series	• 800 MHz LVDS interface clocking—supports 1,600 Mbps LVDS interface through the 1.5 V True Differential Signaling (TDS) standard compatible with LVDS, RSDS, mini-LVDS, and LVPECL standards • 1,600 MHz external memory interface clocking, supports 3,200 Mbps DDR4 interface
		M-Series	• 800 MHz LVDS interface clocking—supports 1,600 Mbps LVDS interface through the 1.3 V TDS standard compatible with LVDS, RSDS, mini-LVDS, and LVPECL standards • 2,800 MHz external memory interface clocking, supports 5,600 Mbps DDR5 interface
General purpose I/Os	General	• Over 700 total GPIOs available • On-chip termination (OCT)	
		F-Series I series	• 1.6 Gbps 1.5 V TDS compatible with LVDS, RSDS, mini-LVDS, and LVPECL standards • 1.2 V single-ended LVCMOS/LVTTL interfacing
		M-Series	• 1.6 Gbps 1.3 V TDS compatible with LVDS, RSDS, mini-LVDS, and LVPECL standards • 1.05 V, 1.1 V, and 1.2 V single-ended single-ended LVCMOS/LVTTL interfacing
	External memory interface (Hard IP)	F-Series I-Series	1,600 MHz (3,200 Mbps) DDR4 external memory interface
		M-Series	• 1,600 MHz (3,200 Mbps) DDR4 external memory interface • 2,800 MHz (5,600 Mbps) DDR5 external memory interface • 2,750 MHz (5,500 Mbps) LPDDR5 external memory interface
Phase locked loops (PLL)	I/O PLL	• Integer PLLs adjacent to general purpose I/Os • Precision frequency synthesis • Clock delay compensation • Zero-delay buffering • Support external memory and LVDS-compatible interface	
	Transmit PLLs (TX PLLs)	• Precise fractional synthesis • Ultra low jitter with LC tank-based PLL • Supports transceiver interfaces	
Memory controller support		Multiple hard IP instantiations in each device	

continued...

Feature		Description	
		F-Series I-Series	• DDR4 hard memory controller • QDR IV using soft memory controller
		M-Series	• DDR5/LPDDR5/DDR4 hard memory controller • QDRIV support using soft memory controller • Hard memory network-on-chip (NoC)
High-bandwidth memory		M-Series	• In-package HBM2E memory options • Up to 32 GB of high bandwidth memory
Memory NoC		M-Series	• Hardened memory network-on-chip (NoC) enabling high bandwidth data flow between the FPGA fabric and the NoC-attached memories without using FPGA resources • Supports over 1 TBps of aggregate memory bandwidth
High-performance crypto blocks(4)		• Supports AES and SM4 encryption standards • Supports GCM and XTS modes of operation	
Transceivers	PCIe	P-Tile F-Tile	PCIe rates up to PCIe 4.0, 16 Gbps NRZ
		R-Tile	• PCIe rates up to PCIe 5.0, 32 Gbps NRZ • Compute Express Link (CXL) support
	Networking	E-Tile	• Continuous operating range of 1 Gbps to 28.9 Gbps NRZ and 2 Gbps to 58 Gbps PAM4 • Insertion loss compliant to 802.3bj, CEI 25G-LR, and CEI 56G-LR • Oversampling capability for data rates below 1 Gbps • ATX transmit PLLs (LC-PLL) with user-configurable fractional synthesis capability • XFP, QSFP-DD, OSFP, QSFP or QSFP28, QSFP56, SFP+, SFP28, SFP56, and CFP or CFP2 or CFP4 optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring)
		F-Tile	• General purpose transceiver block (FGT) with continuous operating range of 1 Gbps to 32 Gbps NRZ and 20 Gbps to 58 Gbps PAM4 • High speed transceiver block (FHT) with operating ranges of: — 24 Gbps to 29 Gbps NRZ and PAM4 — 48 Gbps to 58 Gbps NRZ and PAM4 — 96 Gbps to 116 Gbps PAM4 • The F-Tiles in these devices have the following transceivers: — I-Series—FHT and FGT transceivers — M-Series—FHT and FGT transceivers — F-Series—FGT transceivers only
Transceiver hard IP	PCIe	Multiple hard IP instantiations in each device	
		P-Tile F-Tile	• Up to PCIe 4.0 ×16 EP and RP • Port bifurcation support: 2×8 endpoint or 4×4 root port • TL bypass feature • Single-root I/O virtualization (SR-IOV): 8 physical functions or 2K virtual functions

continued...

(4) Only available in select devices. Refer to the family plan.

Feature			Description
			• VirtIO support • Scalable IOV • Shared virtual memory
		R-Tile	• Up to PCIe 5.0 ×16 EP and RP • Port bifurcation support: 2×8 endpoint or 4×4 root port • TL bypass Feature • SR-IOV: 8 physical functions or 2K virtual functions • VirtIO support • Scalable IOV • Shared Virtual Memory • PIPE Direct mode • Precise Time Management
	CXL	R-Tile	• Up to PCIe 5.0 ×16 EP • Selected features support CXL 1.1 and 2.0 specifications • Soft logic (encrypted) to support CXL Type 1, Type 2, or Type 3 devices • Mix and manage different memory types and controllers
	Other protocols	E-Tile	• Ethernet IP configurations: — 24× 10 or 25 GbE MAC, PCS, and RS-FEC — 4× 100 GbE MAC, PCS, and RS-FEC • CPRI and fibre channel FECs • CR/KR (AN/LT) • 1588 PTP • MAC, PCS, and FEC bypass options • PMA Direct Mode
		F-Tile	• Ethernet IP Configurations: — 16× 10 or 25 GbE MAC, PCS, and FEC — 8× 50 GbE MAC, PCS, and FEC — 8× 40 GbE MAC, PCS, and FEC — 4× 100 GbE MAC, PCS, and FEC — 1× 400 GbE MAC, PCS, and FEC • KP FEC support • Flex-O FEC, FlexE PCS and FEC, Ethernet over OTN Mode, SyncE, fibre channel, and CPRI FEC • CR/KR (AN/LT) • 1588 PTP • MAC, PCS, and FEC bypass options • PMA Direct Mode
Configuration			• Dedicated SDM • Software-programmable device configuration • Fine-grained partial reconfiguration of core fabric—add or remove system logic while the device is operating • Dynamic reconfiguration of transceivers and PLLs • PUF service • Platform attestation • Anti-tamper features

continued...

Feature	Description	
	F-Series	• Serial and parallel flash interface • Configuration via protocol (CvP) using PCIe 1.0, 2.0, 3.0, or 4.0 • Comprehensive set of security features including AES-256, SHA-256/384, ECDSA-256/384 accelerators, and multi-factor authentication
	I-Series M-Series	• Serial and parallel flash interface • Configuration via protocol (CvP) using PCIe 1.0, 2.0, 3.0, 4.0, or 5.0 • Comprehensive set of security features including AES-256, SHA-256/384, ECDSA-256/384 accelerators, and multi-factor authentication
Software and tools	• Quartus® Prime Pro Edition design suite with new compiler and Hyper-Aware design flow • New compile innovations in each Intel oneAPI release • Transceiver toolkit • Platform Designer IP integration tool • Intel DSP Builder for Intel FPGAs advanced blockset • Arm Development Studio for Intel SoC FPGA (Arm DS for Intel SoC FPGA)	

1.4. Additional Features for Agilex 7 SoCs

In addition to the common features of Agilex 7 devices, the Agilex 7 SoCs provide additional features.

Table 3. Features Specific to Agilex 7 SoCs

SoC Subsystem	Feature	Description
HPS	Multiprocessor unit core	• Quad-core Arm Cortex-A53 MPCore processor with Arm CoreSight* debug and trace technology • Scalar floating-point unit supporting single and double precision • Arm Neon* media processing engine for each processor
	System controllers	• System memory management unit (SMMU) • Cache coherency unit (CCU)
	Cache	• Arm Cortex-A53: — Level 1 cache per core: • 32 kilobytes (KB) L1 instruction cache with parity • 32 KB L1 data cache with ECC • 1 megabyte (MB) shared L2 cache with ECC
	On-chip memory	256 KB on-chip RAM
	Direct memory access (DMA)	Eight-channel DMA controller
	Ethernet media access controller (EMAC)	Three 10 Mbps/100 Mbps/1 Gbps EMAC with integrated DMA
	USB	Two USB 2.0 On-The-Go (OTG) with integrated DMA
	UART	Two UART 16550-compatible controllers
	Serial peripheral interface (SPI) controller	Four SPI (two masters and two slaves)
	I^2C	Five I^2C controllers

continued...

SoC Subsystem	Feature	Description
	SD/SDIO/MMC controller	• One eMMC version 4.5 with DMA and CE-ATA support • SD, including eSD, version 3.0 • SDIO, including eSDIO, version 3.0 • CE-ATA version 1.1
	NAND flash controller	• One ONFI 1.0 • 8 bit and 16 bit support
	GPIO	Maximum of 48 software-programmable GPIOs
	Timers	• Four general-purpose timers • Four watchdog timers
SDM		• Secure boot • AES encryption • Secure Hash Algorithms (SHA) and Elliptic Curve Digital Signature Algorithm (ECDSA) authentications
External memory interface		Hard memory controllers: • F-Series and I-Series—DDR4 • M-Series—DDR4, DDR5, and LPDDR5

2. Agilex 7 FPGAs and SoCs Family Plan

The Agilex 7 FPGAs and SoCs are available as FPGAs with different features to fit your application requirements.

Note:

- The tables in the following sections are preliminary and subject to change.
- The resource counts vary by package options.
- The performance specifications vary by speed grades.
- The HPS and transceivers are available only for specific ordering part numbers.

Related Information

Agilex 7 FPGAs and SoCs Family Plan on page 13

2.1. Agilex 7 FPGAs and SoCs F-Series

Table 4. F-Series FPGA Family Plan—Core Features

The values in this table are maximum resources or performance.

Device	Logic Element	Adaptive Logic Module	eSRAM		M20K		MLAB		DSP		Crypto Block
			Count	Size (Mb)	Count	Size (Mb)	Count	Size (Mb)	Count	18×19 Multiplier	
AGF 006	573,480	194,400	—	—	2,844	56	9,720	6	1,640	3,280	—
AGF 008	764,640	259,200	—	—	3,792	74	12,960	8	2,296	4,592	—
AGF 012	1,178,525	399,500	2	36	5,900	115	19,975	12	3,743	7,486	—
AGF 014	1,437,240	487,200	2	36	7,110	139	24,360	15	4,510	9,020	—
AGF 019	1,918,975	650,500	1	18	8,500	166	35,525	20	1,354	2,708	2
AGF 023	2,308,080	782,400	1	18	10,464	204	39,120	24	1,640	3,280	2
AGF 022	2,208,075	748,500	—	—	10,900	212	37,425	23	6,250	12,500	—
AGF 027	2,692,760	912,800	—	—	13,272	259	45,640	28	8,528	17,056	—

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Table 5. F-Series FPGA Family Plan—Transceivers and HPS

The values in this table are maximum resources or performance.

Device	F-Tile				P-Tile	E-Tile			HPS Option
	FGT Transceiver Channel (5)		Ethernet Block (6)	PCIe Controller (7)	PCIe Controller (7)	Transceiver Channel (8)		Ethernet Block (9)	
	32 Gbps NRZ	58 Gbps PAM4				28.9 Gbps NRZ	58 Gbps PAM4		
AGF 006	32	24	2	2	—	—	—	—	Yes
AGF 008	32	24	2	2	—	—	—	—	Yes
AGF 012	32	24	2	2	1	16	8	4	Yes
AGF 014	32	24	2	2	1	16	8	4	Yes
AGF 019	64	48	4	4	2	24	12	4	Yes
AGF 023	64	48	4	4	2	24	12	4	Yes
AGF 022	64	48	4	4	2	24	12	4	Yes
AGF 027	64	48	4	4	2	24	12	4	Yes

Table 6. F-Series FPGA Packages with F-Tile

Table reading example: In package 1546A of AGF 006, there are 384 GPIOs, of which, 192 are LVDS. There are two F-Tiles supporting a maximum total of 32× 32 Gbps NRZ or 24× 58 Gbps PAM4.

Device	Package (Grid Array: Hexagonal)													
	1546A (37.5 mm × 34 mm) 0.92 mm pitch				2340A (45 mm × 42 mm) 0.92 mm pitch						3184C (56 mm × 45 mm) 0.92 mm pitch			
	GPIO	LVDS	F-Tile ×2		GPIO	LVDS	F-Tile ×2 (10)		F-Tile ×1 (11)		GPIO	LVDS	F-Tile ×4	
			32 Gbps NRZ	58 Gbps PAM4			32 Gbps NRZ	58 Gbps PAM4	32 Gbps NRZ	58 Gbps PAM4			32 Gbps NRZ	58 Gbps PAM4
AGF 006	384	192	32	24	576	288	32	24	16	12	—	—	—	—
AGF 008	384	192	32	24	576	288	32	24	16	12	—	—	—	—

continued...

(5) Maximum F-Tile general purpose transceiver (FGT) RS and KP FEC NRZ up to 32 Gbps, or PAM4 up to 58 Gbps.

(6) Maximum 10, 25, 40, 50, 100, 200, or 400 GbE MAC and FEC hard IP blocks.

(7) Maximum PCIe hard IP blocks (PCIe 4.0 ×16) or bifurcatable two PCIe 4.0 ×8 (EP) or four PCIe 4.0 ×4 (RP).

(8) Maximum RS and KP FEC NRZ up to 28.9 Gbps, or PAM4 up to 58 Gbps.

(9) Maximum 100 GbE MAC and FEC hard IP blocks

(10) Applicable to package code R24C only.

(11) Applicable to package code R24D only.

Device	Package (Grid Array: Hexagonal)													
	1546A (37.5 mm × 34 mm) 0.92 mm pitch				2340A (45 mm × 42 mm) 0.92 mm pitch						3184C (56 mm × 45 mm) 0.92 mm pitch			
	GPIO	LVDS	F-Tile ×2		GPIO	LVDS	F-Tile ×2 (10)		F-Tile ×1 (11)		GPIO	LVDS	F-Tile ×4	
			32 Gbps NRZ	58 Gbps PAM4			32 Gbps NRZ	58 Gbps PAM4	32 Gbps NRZ	58 Gbps PAM4			32 Gbps NRZ	58 Gbps PAM4
AGF 012	—	—	—	—	744	372	32	24	16	12	—	—	—	—
AGF 014	—	—	—	—	744	372	32	24	16	12	—	—	—	—
AGF 019	—	—	—	—	480	240	32	24	—	—	480	240	64	48
AGF 023	—	—	—	—	480	240	32	24	—	—	480	240	64	48
AGF 022	—	—	—	—	744	372	32	24	—	—	720	360	64	48
AGF 027	—	—	—	—	744	372	32	24	—	—	720	360	64	48

Table 7. F-Series FPGA Packages with P-Tile and E-Tile

Table reading example: In package 2581A of AGF 019, there are 480 GPIOs, of which, 240 are LVDS. There is one E-Tile supporting a maximum of 24× 28.9 Gbps NRZ or 12× 58 Gbps PAM4. There are two P-Tiles supporting a maximum total of 32× PCIe at up to 16 Gbps per lane.

Device	Package (Grid Array: Hexagonal)									
	2486A (55 mm × 42.5 mm) 1.0 mm pitch					2581A (52.5 mm × 40.5 mm) 0.92 mm or 0.94 mm pitch				
	GPIO	LVDS	E-Tile ×1		P-Tile ×1	GPIO	LVDS	E-Tile ×1		P-Tile ×2
			28.9 Gbps NRZ	58 Gbps PAM4	16 Gbps PCIe			28.9 Gbps NRZ	58 Gbps PAM4	16 Gbps PCIe
AGF 006	—	—	—	—	—	—	—	—	—	—
AGF 008	—	—	—	—	—	—	—	—	—	—
AGF 012	768	384	16	8	16	—	—	—	—	—
AGF 014	768	384	16	8	16	—	—	—	—	—
AGF 019	—	—	—	—	—	480	240	24	12	32
AGF 023	—	—	—	—	—	480	240	24	12	32
AGF 022	—	—	—	—	—	624	312	24	12	32
AGF 027	—	—	—	—	—	624	312	24	12	32

(10) Applicable to package code R24C only.

(11) Applicable to package code R24D only.

2.2. Agilex 7 FPGAs and SoCs I-Series

Table 8. I-Series FPGA Family Plan—Core Features

The values in this table are maximum resources or performance.

Device	Logic Element	Adaptive Logic Module	eSRAM		M20K		MLAB		DSP		Crypto Block
			Count	Size (Mb)	Count	Size (Mb)	Count	Size (Mb)	Count	18x19 Multiplier	
AGI 019	1,918,975	650,500	1	18	8,500	166	35,525	20	1,354	2,708	2
AGI 023	2,308,080	782,400	1	18	10,464	204	39,120	24	1,640	3,280	2
AGI 022	2,208,075	748,500	—	—	10,900	212	37,425	23	6,250	12,500	—
AGI 027	2,692,760	912,800	—	—	13,272	259	45,640	28	8,528	17,056	—
AGI 035	3,540,000	1,200,000	3	54	14,931	292	60,000	37	9,594	19,188	4
AGI 040	4,047,400	1,372,000	3	54	19,908	389	68,600	42	12,792	25,584	4
AGI 041	4,000,672	1,356,160	2	36	17,136	335	67,808	42	—	—	4

Note: Agilex 7 FPGAs and SoCs support PCIe blocks in tile locations 15A, 14C, and 15C. CXL is supported in tile locations 14C and 15C in the 2957A package only.

Table 9. I-Series FPGA Family Plan—Transceivers and HPS

The values in this table are maximum resources or performance.

Device	CXL Lane	F-Tile						R-Tile	HPS
		Transceiver Channel				Ethernet Block (12)	PCIe Controller (13)	PCIe (14)/ CXL (15) Controller	
		FGT (16)		FHT (17)					
		32 Gbps NRZ	58 Gbps PAM4	58 Gbps NRZ	116 Gbps PAM4				
AGI 019	16	64	48	8	8	4 (18)	4 (19)	1	Yes
AGI 023	16	64	48	8	8	4 (18)	4 (19)	1	Yes
AGI 022	32	64	48	8	8	4 (18)	4 (19)	3	Yes
AGI 027	32	64	48	8	8	4 (18)	4 (19)	3	Yes
AGI 035	—	96	72	24	24	6 (20)	6 (21)	—	—
AGI 040	—	96	72	24	24	6 (20)	6 (21)	—	—
AGI 041	32	64	48	8	8	4	4	3	Yes

(12) Maximum 10, 25, 40, 50, 100, 200, or 400 GbE MAC and FEC hard IP blocks.

(13) Maximum PCIe hard IP blocks (PCIe 4.0 ×16) or bifurcatable two PCIe 4.0 ×8 (EP) or four PCIe 4.0 ×4 (RP).

(14) Maximum PCIe hard IP blocks (PCIe 5.0 ×16) or bifurcatable two PCIe 5.0 ×8 (EP) or four PCIe 5.0 ×4 (RP).

(15) Maximum CXL hard IP blocks (PCIe 5.0 ×16) endpoint.

(16) Maximum F-Tile general purpose transceiver (FGT) RS and KP FEC NRZ up to 32 Gbps, or PAM4 up to 58 Gbps.

(17) Maximum F-Tile high speed transceiver (FHT) RS and KP FEC NRZ up to 58 Gbps, or PAM4 up to 116 Gbps.

(18) Maximum of four F-Tiles in package 3184B.

(19) Maximum of four PCIe controllers in package 3184B.

(20) Maximum of six F-Tiles in package 3948A.

(21) Maximum of six PCIe controllers in package 3948A.

Table 10. I-Series FPGA Packages with F-Tile

Table reading example: In package 3184B of AGI 022, there are 720 GPIOs, of which, 360 are LVDS. There are four F-Tiles with FGT channels supporting a maximum total of 64× 32 Gbps NRZ or 48× 58 Gbps PAM4, and FHT channels supporting a maximum total of 8× 58 Gbps NRZ or 8× 116 Gbps PAM4.

Device	Package (Grid Array: Hexagonal)											
	3184B (56 mm × 45 mm) 0.92 mm pitch						3948A (56 mm × 56 mm) 0.92 mm pitch					
	GPIO	LVDS	F-Tile ×4				GPIO	LVDS	F-Tile ×6			
			FGT		FHT				FGT		FHT	
			32 Gbps NRZ	58 Gbps PAM4	58 Gbps NRZ	116 Gbps PAM4			32 Gbps NRZ	58 Gbps PAM4	58 Gbps NRZ	116 Gbps PAM4
AGI 019	480	240	64	48	8	8	—	—	—	—	—	—
AGI 023	480	240	64	48	8	8	—	—	—	—	—	—
AGI 022	720	360	64	48	8	8	—	—	—	—	—	—
AGI 027	720	360	64	48	8	8	—	—	—	—	—	—
AGI 035	—	—	—	—	—	—	576	288	96	72	24	24
AGI 040	—	—	—	—	—	—	576	288	96	72	24	24
AGI 041	732	366	64	48	8	8	—	—	—	—	—	—

Table 11. I-Series FPGA Packages with F-Tile and R-Tile—1805A and 2957A

Table reading example: In package 2957A of AGI 022, there are 720 GPIOs, of which, 360 are LVDS. There is one F-Tile with FGT channels supporting a maximum of 16× 32 Gbps NRZ or 12× 58 Gbps PAM4, and FHT channels supporting a maximum of 4× 58 Gbps NRZ or 4× 116 Gbps PAM4. There are three R-Tiles supporting a maximum total of 48× PCIe at up to 32 Gbps per lane, or 32× CXL lanes.

Device	Package (Grid Array: Hexagonal)													
	1805A (42.5 mm × 42.5 mm) 1.025 mm pitch						2957A (56 mm × 45 mm) 1.0 or 0.92 mm pitch							
	GPIO	LVDS	F-Tile ×1		R-Tile ×1		GPIO	LVDS	F-Tile ×1				R-Tile ×3	
			FGT		32 Gbps PCIe	CXL			FGT		FHT		32 Gbps PCIe	CXL (22)
			32 Gbps NRZ	58 Gbps PAM4					32 Gbps NRZ	58 Gbps PAM4	58 Gbps NRZ	116 Gbps PAM4		
AGI 019	480	240	16	12	16	16	—	—	—	—	—	—	—	—
AGI 023	480	240	16	12	16	16	—	—	—	—	—	—	—	—
AGI 022	—	—	—	—	—	—	720	360	16	12	4	4	48	32
AGI 027	—	—	—	—	—	—	720	360	16	12	4	4	48	32
AGI 041	—	—	—	—	—	—	720	360	16	12	4	4	48	32

(22) For options to increase available CXL lanes, contact Intel Premier Support and quote ID #15012021851.

Table 12. I-Series FPGA Packages with F-Tile and R-Tile—3184A and 3184E

Table reading example: In package 3184A of AGI 022, there are 720 GPIOs, of which, 360 are LVDS. There are three F-Tiles with FGT channels supporting a maximum total of 48× 32 Gbps NRZ or 36× 58 Gbps PAM4, and FHT channels supporting a maximum of 8× 58 Gbps NRZ or 8× 116 Gbps PAM4. There is one R-Tile supporting a maximum of 16× PCIe at up to 32 Gbps per lane, or 16× CXL lanes.

Device	Package (Grid Array: Hexagonal)															
	3184A (56 mm × 45 mm) 0.92 mm pitch								3184E (56 mm × 45 mm) 0.92 mm pitch							
	GPIO	LVDS	F-Tile ×3				R-Tile ×1		GPIO	LVDS	F-Tile ×2				R-Tile ×2	
			FGT		FHT		32 Gbps PCIe	CXL			FGT		FHT		32 Gbps PCIe	CXL
			32 Gbps NRZ	58 Gbps PAM 4	58 Gbps NRZ	116 Gbps PAM 4					32 Gbps NRZ	58 Gbps PAM 4	58 Gbps NRZ	116 Gbps PAM 4		
AGI 022	720	360	48	36	8	8	16	16	—	—	—	—	—	—	—	—
AGI 027	720	360	48	36	8	8	16	16	—	—	—	—	—	—	—	—
AGI 041	—	—	—	—	—	—	—	—	744	372	32	24	8	8	32	32

2.3. Agilex 7 FPGAs and SoCs M-Series

Table 13. M-Series FPGA Family Plan—Core Features

The values in this table are maximum resources or performance.

Device	Logic Element	Adaptive Logic Module	M20K		MLAB		HBM2E DRAM (GB)	DSP		Crypto Block
			Count	Size (Mb)	Count	Size (Mb)		Count	18x19 Multiplier	
AGM 032	3,245,000	1,100,000	15,932	311	55,000	33	16 / 32	9,375	18,750	—
AGM 039	3,851,520	1,305,600	18,960	370	65,280	40	16 / 32	12,300	24,600	—

Table 14. M-Series FPGA Family Plan—Transceivers and HPS

The values in this table are maximum resources or performance.

Device	CXL Lane	F-Tile						R-Tile	HPS
		Transceiver Channel				Ethernet Block (23)	PCIe Controller (24)	PCIe (25)/ CXL (26) Controller	
		FGT (27)		FHT (28)					
		32 Gbps NRZ	58 Gbps PAM4	58 Gbps NRZ	116 Gbps PAM4				
AGM 032	16(29)	64	48	8	8	4 (30)	4 (31)	1	Yes
AGM 039	16(29)	64	48	8	8	4 (30)	4 (31)	1	Yes

Table 15. M-Series FPGA Package with F-Tile

Table reading example: In package 3184B of AGM 032, there are 720 GPIOs, of which, 360 are LVDS. There are four F-Tiles with FGT channels supporting a maximum total of 64× 32 Gbps NRZ or 48× 58 Gbps PAM4, and FHT channels supporting a maximum total of 8× 58 Gbps NRZ or 8× 116 Gbps PAM4.

Device	Package (Grid Array: Hexagonal)					
	3184B (56 mm × 45 mm) 0.92 mm pitch					
	GPIO	LVDS	F-Tile ×4			
			FGT		FHT	
			32 Gbps NRZ	58 Gbps PAM4	58 Gbps NRZ	116 Gbps PAM4
AGM 032	720	360	64	48	8	8
AGM 039	720	360	64	48	8	8

(23) Maximum 10, 25, 40, 50, 100, 200, or 400 GbE MAC and FEC hard IP blocks.

(24) Maximum PCIe hard IP blocks (PCIe 4.0 ×16) or bifurcatable two PCIe 4.0 ×8 (EP) or four PCIe 4.0 ×4 (RP).

(25) Maximum PCIe hard IP blocks (PCIe 5.0 ×16) or bifurcatable two PCIe 5.0 ×8 (EP) or four PCIe 5.0 ×4 (RP).

(26) Maximum CXL hard IP blocks (PCIe 5.0 ×16) endpoint.

(27) Maximum F-Tile general purpose transceiver (FGT) RS and KP FEC NRZ up to 32 Gbps, or PAM4 up to 58 Gbps.

(28) Maximum F-Tile high speed transceiver (FHT) RS and KP FEC NRZ up to 58 Gbps, or PAM4 up to 116 Gbps.

(29) Available in package 4700A.

(30) Maximum of four F-Tiles in package 3184B.

(31) Maximum of four PCIe controllers in package 3184B.

Table 16. M-Series FPGA Package with F-Tile and HBM2E

Table reading example: In package 4700B of AGM 032, there are 768 GPIOs, of which, 384 are LVDS. There are three F-Tiles with FGT channels supporting a maximum total of 64× 32 Gbps NRZ or 48× 58 Gbps PAM4, and FHT channels supporting a maximum total of 8× 58 Gbps NRZ or 8× 116 Gbps PAM4. The devices are available with 16 GB or 32 GB in-package HBM2E memory.

Device	Package (Grid Array: Hexagonal)						
	4700B (56 mm × 66 mm) 0.92 mm pitch						
	GPIO	LVDS	F-Tile ×4				HBM2E (GB)
			FGT		FHT		
			32 Gbps NRZ	58 Gbps PAM4	58 Gbps NRZ	116 Gbps PAM4	
AGM 032	768	384	64	48	8	8	32
AGM 039	768	384	64	48	8	8	32

Table 17. M-Series FPGA Package with F-Tile, R-Tile, and HBM2E

Table reading example: In package 4700A of AGM 032, there are 768 GPIOs, of which, 384 are LVDS. There are three F-Tiles with FGT channels supporting a maximum of 48× 32 Gbps NRZ or 36× 58 Gbps PAM4, and FHT channels supporting a maximum of 8× 58 Gbps NRZ or 8× 116 Gbps PAM4. There is one R-Tile supporting a maximum of 16× PCIe at up to 32 Gbps per lane. The devices are available with 16 GB or 32 GB in-package HBM2E memory.

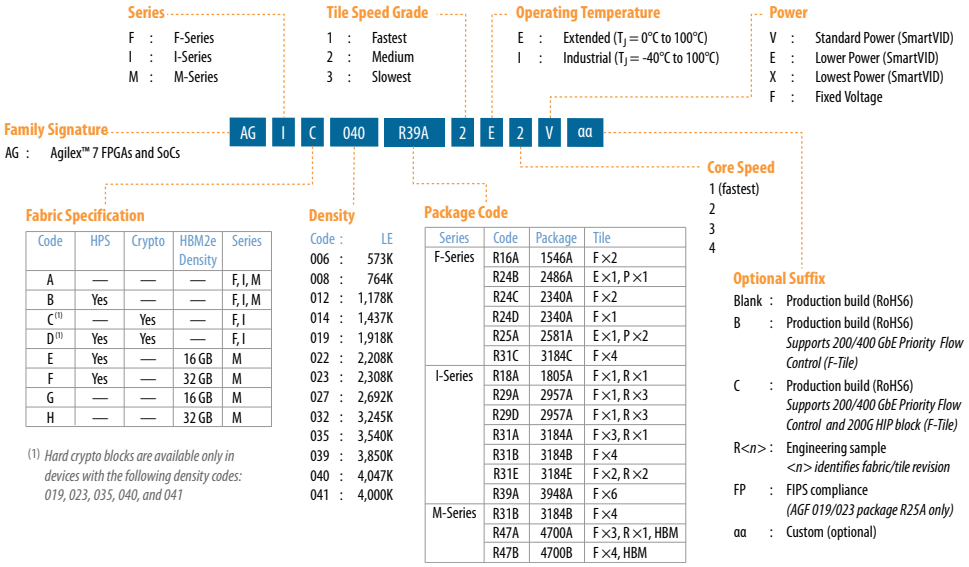
Device	Package (Grid Array: Hexagonal)								
	4700A (56 mm × 66 mm) 0.92 mm pitch								
	GPIO	LVDS	F-Tile ×3				R-Tile ×1		HBM2E (GB)
			FGT		FHT		32 Gbps PCIe	CXL	
			32 Gbps NRZ	58 Gbps PAM4	58 Gbps NRZ	116 Gbps PAM4			
AGM 032	768	384	48	36	8	8	16	16	16 / 32
AGM 039	768	384	48	36	8	8	16	16	16 / 32

Related Information

Heterogeneous 3D Stacked HBM2E DRAM Memory in Agilex 7 FPGAs and SoCs M-Series on page 45

2.4. Part Number Decoder

Figure 3. Agilex 7 FPGAs and SoCs Ordering Part Number



Fabric Specification

Code	HPS	Crypto	HBM2e Density	Series
A	—	—	—	F, I, M
B	Yes	—	—	F, I, M
C(1)	—	Yes	—	F, I
D(1)	Yes	Yes	—	F, I
E	Yes	—	16 GB	M
F	Yes	—	32 GB	M
G	—	—	16 GB	M
H	—	—	32 GB	M

(1) *Hard crypto blocks are available only in devices with the following density codes: 019, 023, 035, 040, and 041*

Density

Code	LE
006	573K
008	764K
012	1,178K
014	1,437K
019	1,918K
022	2,208K
023	2,308K
027	2,692K
032	3,245K
035	3,540K
039	3,850K
040	4,047K
041	4,000K

Package Code

Series	Code	Package	Tile
F-Series	R16A	1546A	F ×2
	R24B	2486A	E ×1, P ×1
	R24C	2340A	F ×2
	R24D	2340A	F ×1
	R25A	2581A	E ×1, P ×2
	R31C	3184C	F ×4
I-Series	R18A	1805A	F ×1, R ×1
	R29A	2957A	F ×1, R ×3
	R29D	2957A	F ×1, R ×3
	R31A	3184A	F ×3, R ×1
	R31B	3184B	F ×4
	R31E	3184E	F ×2, R ×2
	R39A	3948A	F ×6
M-Series	R31B	3184B	F ×4
	R47A	4700A	F ×3, R ×1, HBM
	R47B	4700B	F ×4, HBM

Related Information

- Agilex 7 FPGAs and SoC FPGAs F-Series
  Provides an updated list of the available F-Series devices.
- Agilex 7 FPGAs and SoC FPGAs I-Series
  Provides an updated list of the available I-Series devices.
- Agilex 7 FPGAs and SoC FPGAs M-Series
  Provides an updated list of the available M-Series devices.

3. Second Generation Hyperflex Core Architecture

The Agilex 7 FPGAs and SoCs are based on a core fabric featuring the second generation Hyperflex core architecture.

Table 18. Advantages of the Hyperflex Core Architecture

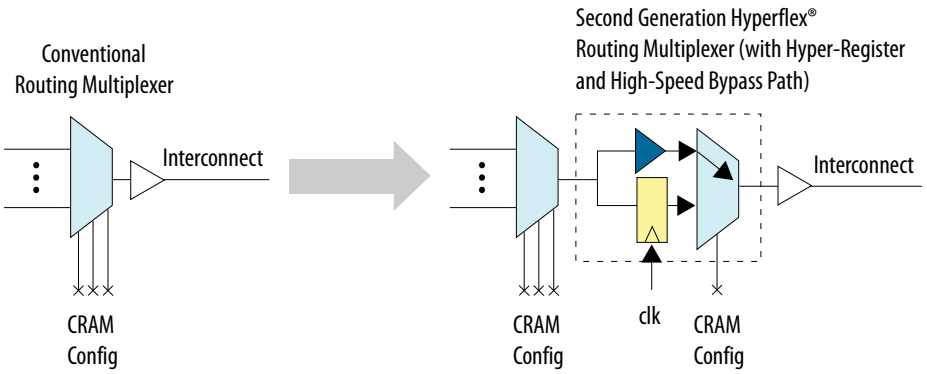
This table lists some of the advantages of the Hyperflex core architecture.

Advantage	Description
Higher throughput	Delivers, on average, 50% higher core clock frequency performance in designs from previous generation high-end FPGAs to obtain throughput breakthroughs.
Improved power efficiency	Uses reduced IP size to consolidate designs that previously spanned multiple devices into a single device. This consolidation reduces power requirement by up to 40% compared to previous generation devices.
Greater design functionality	Uses faster clock frequency to reduce bus widths and reduce IP size. The reduced bus widths and IP size free up additional FPGA resources to add greater functionality.
Increased designer productivity	Boosts performance with less routing congestion and fewer design iterations using the Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure.

Additional to traditional ALM user registers, the Hyperflex core architecture adds bypassable registers called Hyper-Registers:

- Distributed throughout the FPGA fabric.
- Available on every interconnect routing segment and at the inputs of all functional blocks.

Figure 4. Bypassable Hyper-Register



In the second generation Hyperflex core architecture, Altera optimized the number of registers to improve timing closure time and fabric area utilization.

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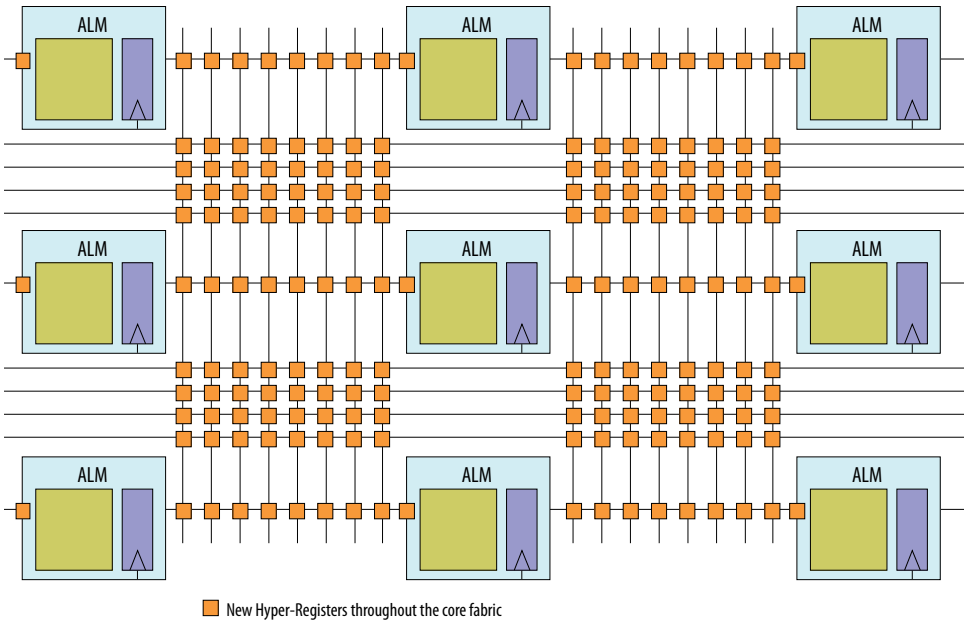
Figure 5. Hyperflex Core Architecture



The Hyper-Registers enable you to achieve core performance increases using key design techniques. If you implement these design techniques, the Hyper-Aware design tools automatically utilizes the Hyper-Registers to achieve maximum core clock frequency:

- Fine grain Hyper-Retiming to eliminate critical paths
- Zero-latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

4. Adaptive Logic Module in Agilex 7 FPGAs and SoCs

The Agilex 7 FPGAs and SoCs use an enhanced adaptive logic module (ALM) similar to the previous generation FPGAs such as the Arria® 10 and Stratix® 10 FPGAs. The enhanced ALM allows for efficient implementation of logic functions and easy IP conversion between Agilex 7 FPGAs and Arria 10 and Stratix 10 FPGAs.

Figure 6. ALM Block Diagram

This figure shows the ALM with 8-input fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

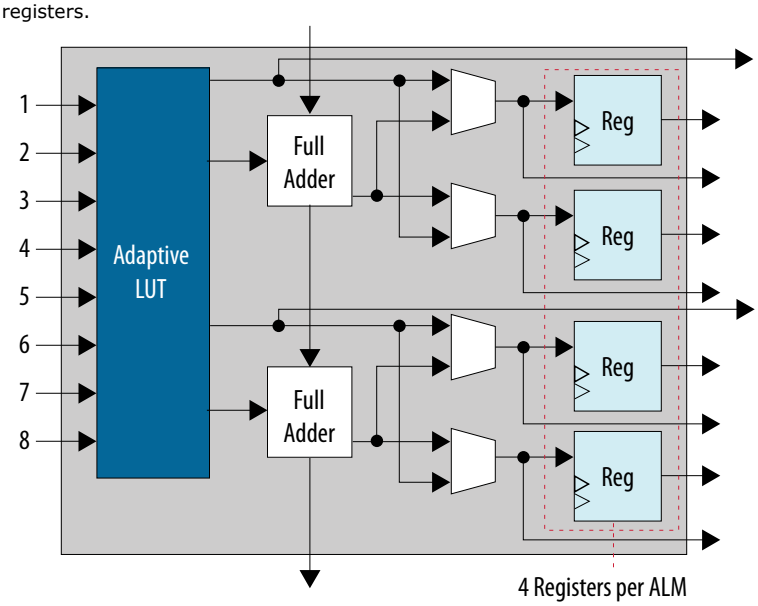


Table 19. Key Features and Capabilities of the ALM

Key Feature	Capability
High register count	Together with the second generation Hyperflex architecture, the four registers per 8-input fracturable LUT enables maximized core performance at very high core logic utilization.
ALM operating modes	Optimize core logic utilization by implementing an extended 7-input logic function, a single 6-input logic function, or two smaller independent functions (for example, two 4-input functions).
Two clock sources	Two clock sources per ALM generate two normal clocks and two delayed clocks to drive the ALM registers, resulting in more clock domains and time-borrowing capability.
Additional LUT outputs	Additional fast 6-LUT and 5-LUT outputs for combinatorial functions improve critical path for logic cascade.
Improved register packing	The improved register packing, including 5-input LUT with two packed register paths, results in more efficient usage of the fabric area and improved critical path.
Latch mode support	The ALM supports latch mode in the address latch enable.

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The Quartus Prime software capitalizes on the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Quartus Prime software simplifies design reuse as the software automatically maps legacy designs into the ALM architecture of the Agilex 7 FPGAs and SoCs.

5. Internal Embedded Memory in Agilex 7 FPGAs and SoCs

The MLAB and M20K embedded memory blocks in Agilex 7 FPGAs and SoCs are similar to the embedded memory of previous generation FPGAs. Additionally, some Agilex 7 FPGAs also feature eSRAM blocks with stitching support.

Table 20. Embedded Memory Block Types and Features for Agilex 7 FPGAs and SoCs

Feature	MLAB	M20K	eSRAM(32)
Usage	For wide and shallow memory configurations	For supporting larger memory configurations	For large memory configurations with fast path, low latency, and high bandwidth on-chip memory
Block size	640 bits	20 kilobits	18 Megabits
Configurations	• 64×10 (emulated) • 32×20	• 2,048×10 (or ×8) • 1,024×20 (or ×16) • 512×40 (or ×32)	• 8 channels of 2.25 Mb (18 Mb) • Each channel contains 32 banks of 72×1K memory
Hard ECC	—	Yes	Yes
Modes	Single-port RAM, dual-port RAM, FIFO, ROM, and shift register		—

(32) Available in F-Series and I-Series FPGAs.

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6. Variable-Precision DSP in Agilex 7 FPGAs and SoCs

The Agilex 7 FPGAs and SoCs carry over the variable-precision DSP architecture from previous FPGAs with hard fixed point and IEEE 754-compliant floating point capabilities.

In fixed point mode, you can configure the DSP blocks to support signal processing with precisions from 9×9 up to 54×54:

- Increased 9×9 multipliers count, with three 9×9 multipliers for every 18×19 multiplier
- A pipeline register increases the maximum DSP block operating frequency and reduces the power consumption
- Dynamically switch multiplier inputs through `scanin` and `chainout` signals
- Compile each DSP block independently as four 9×9, two 18×19, or one 27×27 multiply-accumulate

The variable-precision DSP supports floating point addition, multiplication, multiply-add, and multiply-accumulate:

- Single-precision 32-bit arithmetic FP32 floating point mode
- Half-precision 16-bit arithmetic FP16 and FP19 floating point modes, and BFLOAT16 floating point format

With a dedicated 64-bit cascade bus, you can cascade multiple variable-precision DSP blocks to efficiently implement even higher-precision DSP functions.

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Figure 7. Low Precision Fixed Point Mode

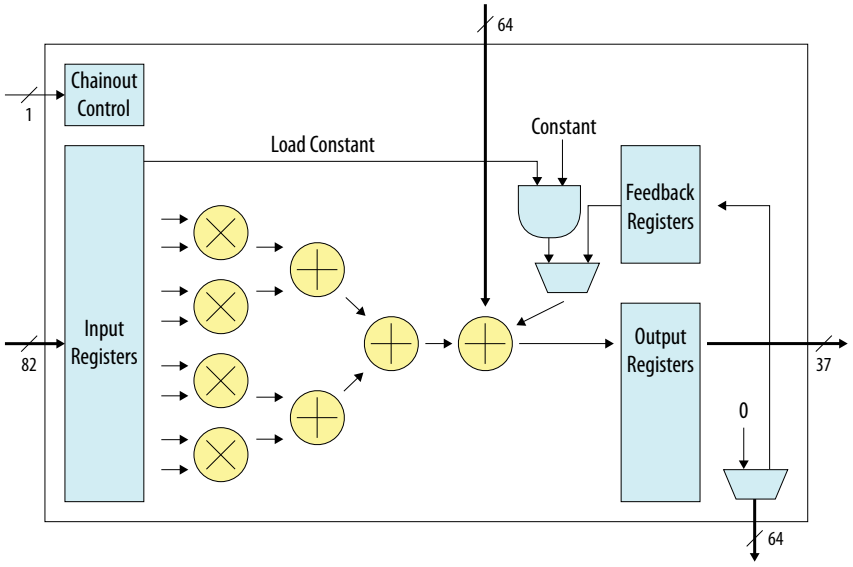

Figure 8. Standard Precision Fixed Point Mode

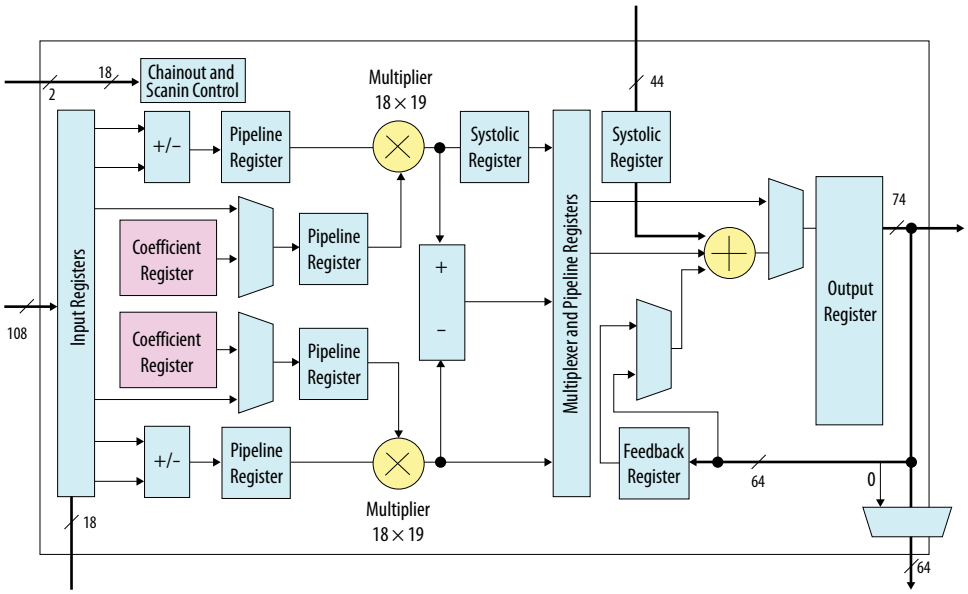

Figure 9. High Precision Fixed Point Mode

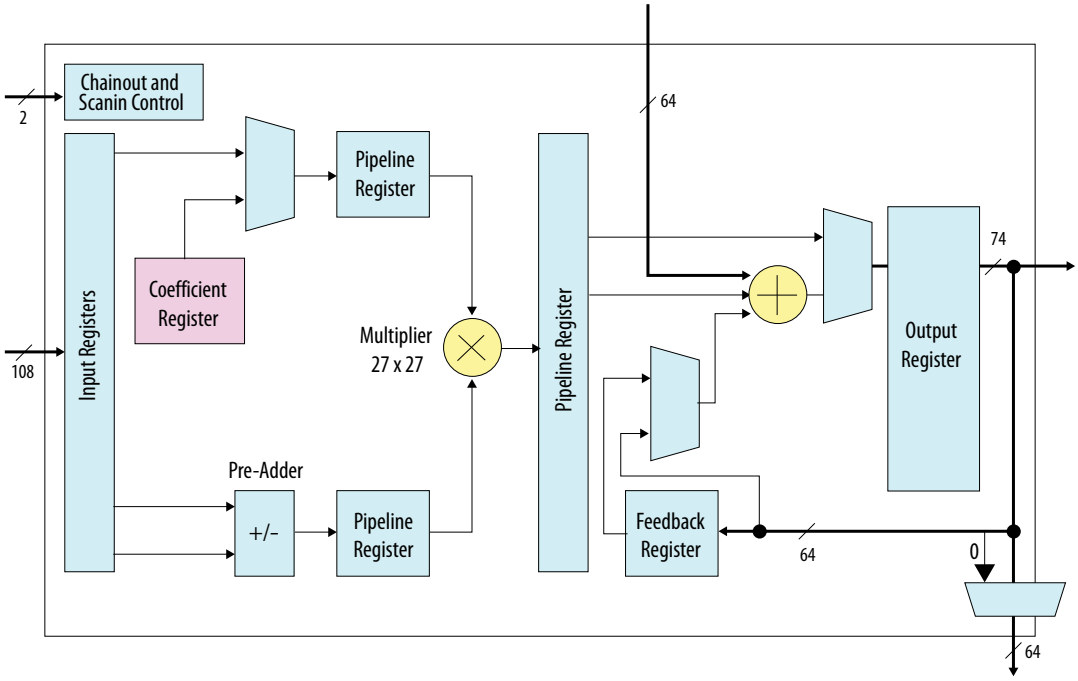

Figure 10. Half Precision 16-bit Arithmetic Floating Point

This block diagram shows the functional representation of the DSP block. The pipeline registers are embedded within the various circuits of the DSP block.

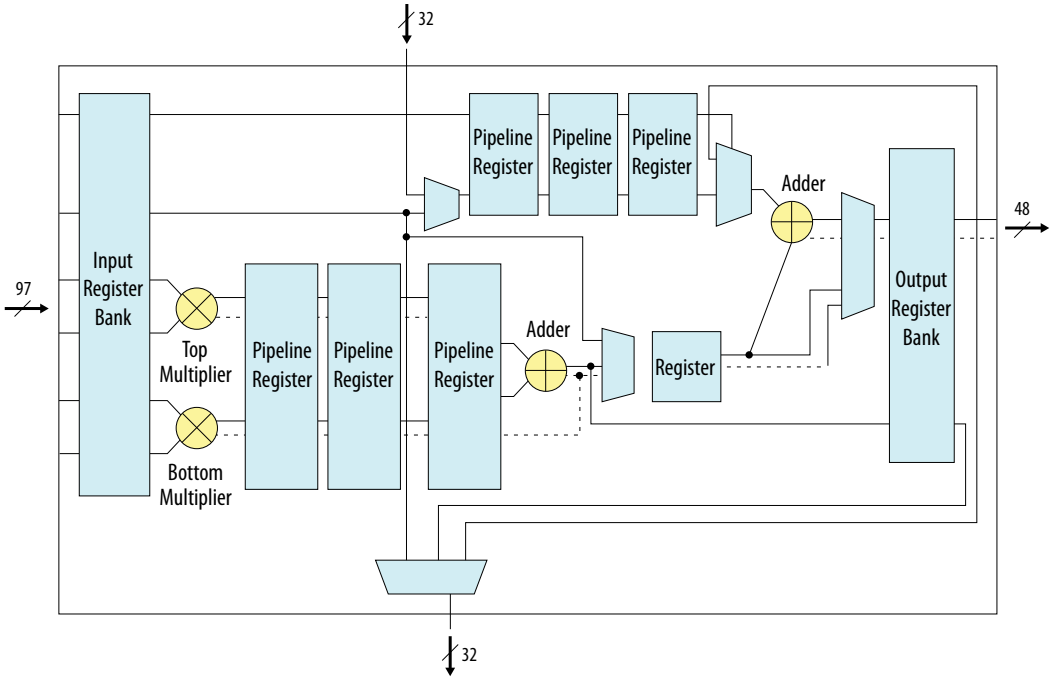

Figure 11. Single Precision 32-bit Arithmetic Floating Point

This block diagram shows the functional representation of the DSP block. The pipeline registers are embedded within the various circuits of the DSP block.

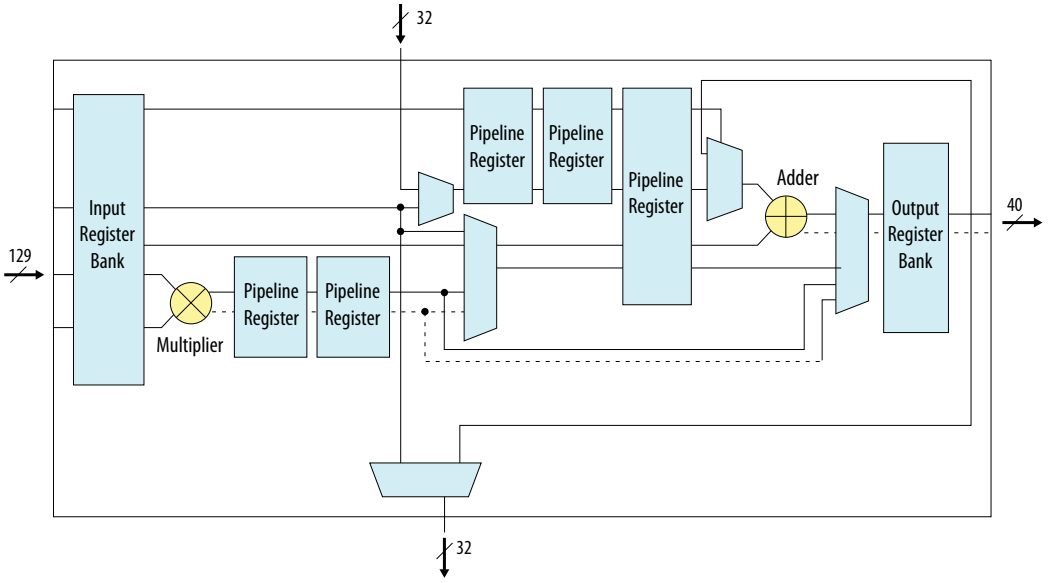

Table 21. Variable-Precision DSP Block Configurations in Agilex 7 FPGAs and SoCs

This table lists the way Agilex 7 FPGAs and SoCs accommodate the different precisions within a DSP block or by utilizing multiple DSP blocks.

Multiplier	DSP Block Resource Usage	Expected Application
9×9 bits	One-fourth of a variable-precision DSP block (One DSP block can support four 9×9)	Low-precision fixed point
18×19 bits	Half of a variable-precision DSP block	Medium-precision fixed point
27×27 bits	One variable-precision DSP block	High-precision fixed point
19×36 bits	One variable-precision DSP block with external adder	Fixed point fast Fourier transform (FFT)
36×36 bits	Two variable-precision DSP blocks with external adder	Very high-precision fixed point
54×54 bits	Four variable-precision DSP blocks with external adder	Double-precision fixed point
Half-precision floating point	One variable-precision DSP block (Contains adder for two FP16 multipliers with one accumulator)	Half-precision floating point
Single-precision floating point	One variable-precision DSP block (Contains one FP32 multipliers with one accumulator)	Single-precision floating point

7. Core Clock Network in Agilex 7 FPGAs and SoCs

Agilex 7 FPGAs and SoCs use programmable clock tree synthesis for its core clocking function.

Programmable clock tree synthesis uses dedicated clock tree routing and switching circuits. These dedicated circuits enable the Quartus Prime software to create the exact clock trees that your design requires.

Advantages of using programmable clock tree synthesis:

- Minimizes clock tree insertion delay
- Reduces dynamic power dissipation in the clock tree
- Allows greater flexibility of clocking in the core
- Maintains backwards compatibility with legacy global and regional clocking schemes

Features of the core clock network of Agilex 7 FPGAs and SoCs:

- Supports the second-generation Hyperflex core architecture
- Supports the hard memory controllers[33] for:
  - DDR4—up to 3,200 Mbps with a quarter-rate transfer to the core
  - DDR5—up to 5,600 Mbps
  - LPDDR5—up to 5,500 Mbps
- Supported by dedicated clock input pins and integer I/O PLLs

Related Information

- Key Features and Innovations in Agilex 7 FPGAs and SoCs on page 5
  Provides more information about memory interface performance in different Agilex 7 FPGA series.
- Agilex 7 FPGAs and SoCs Summary of Features on page 7
  Provides more information about hard memory controller support in different Agilex 7 FPGA series.

(33) Each Agilex 7 FPGA series has different hard memory controller support. For more information, refer to the related information.

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8. General Purpose I/Os in Agilex 7 FPGAs and SoCs

The Agilex 7 FPGAs and SoCs are equipped with general purpose I/Os (GPIO) that support various I/O standards from 1.05 V to 1.5 V.

In each GPIO bank, there are two 48-pin sub-banks, providing a total of 96 pins per bank. In the M-Series FPGAs, each sub-bank has its own V_{CCIO}.

Table 22. I/O Standards Support and Performance in Agilex 7 FPGAs and SoCs

I/O Standard	Series	Specification	Notes
LVCMOS/LVTTL	F-Series I-Series	1.2 V single-ended	—
	M-Series	1.05 V, 1.1 V, and 1.2 V single-ended	
TDS	F-Series I-Series	• 1.5 V • Up to 1.6 Gbps	Works with the LVDS SERDES Intel FPGA IP
	M-Series	• 1.3 V • Up to 1.6 Gbps	

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9. I/O PLLs in Agilex 7 FPGAs and SoCs

The I/O banks of the Agilex 7 FPGAs and SoCs contain I/O PLLs for use in I/O interfacing or fabric clocking.

Table 23. I/O PLLs in I/O Banks

Series	Bank I/O PLL	Fabric-Feeding I/O PLL
F-Series	2	1
I-Series	2	1
M-Series	2	1

You can use the I/O PLLs for general purpose applications in the core fabric, such as clock network delay compensation and zero-delay clock buffering.

The I/O PLLs are situated adjacent to the hard memory controllers and LVDS serializer/deserializer (SERDES) blocks in the I/O bank. This placement creates a tight coupling of the PLLs with the I/Os that need them. The architecture simplifies designing external memory and high-speed LVDS interfaces, and eases timing closure.

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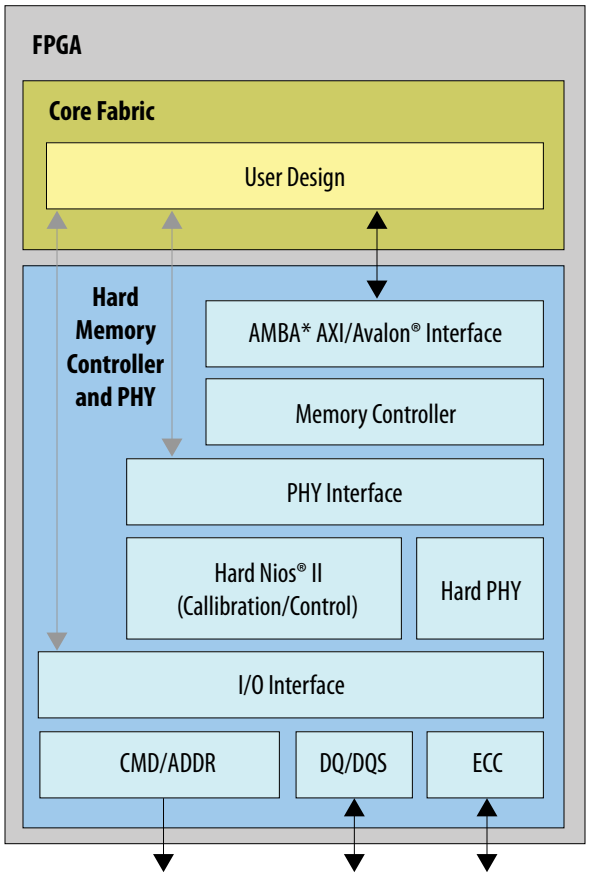
10. External Memory Interface in Agilex 7 FPGAs and SoCs

The Agilex 7 FPGAs and SoCs feature a substantial external memory bandwidth. This bandwidth is accompanied by the ease-of-design, lower power, and resource efficiencies of high-performance hard memory controllers. Using the hard or soft memory controller, you can configure external memory interfaces width up to a maximum of 72 bits.

Figure 12. Hard Memory Controller



Each I/O bank contains 96 general purpose I/Os and two high-efficiency hard memory controllers. The hard memory controllers support various memory types, each with different performance capabilities. You can bypass the hard memory controller and implement a soft memory controller in user logic.

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Each I/O contains a hard DDR read and write path (PHY) capable of performing key memory interface functions such as:

- Read and write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

Hard microcontrollers aid the timing calibration. Altera customized these hard microcontrollers to control the calibration of multiple memory interfaces. The calibration enables the Agilex 7 device to compensate for process, voltage, and temperature (PVT) variance within the Agilex 7 device or the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

10.1. External Memory Interface Performance

Table 24. F-Series and I-Series FPGAs External Memory Interface Performance

Interface Protocol	Memory Controller	Interface Performance (Mbps)	Maximum Width (Bits)
DDR4	Hard	3,200	64 / 72
QDRIV	Soft	2,133	36

Table 25. M-Series FPGAs External Memory Interface Performance

Interface Protocol	Memory Controller	Interface Performance (Mbps)	Maximum Width (Bits)	
DDR4	Hard	3,200	Component	40
			DIMM	72
DDR5	Hard	5,600	Component	40
			DIMM	2×40
LPDDR5	Hard	5,500	4×16	
QDRIV	Soft	2,133	36	

10.2. Features of the Hard Memory Controller

Table 26. Hard Memory Controller Features

Feature	Description
Protocol	• LPDDR5—two dynamic frequency scaling (DFS) frequencies • DDR4 and DDR5—up to two chip selects and up to two 3D stacks
Interface	• Fully pipelined command, read, and write data interfaces to the controller • Arm AMBA* 4 AXI compliance including AXI ordering rules: — Four priority quality of service (QoS) levels — Programmable address mapping — Exclusive monitors

continued...

Feature	Description
Scheduling	• Software-configurable priority scheduling on individual SDRAM bursts • Advanced bank look-ahead features for high memory throughput • Configurable for one of these placement orders: — Out-of-order placement for writes — In-order placement for writes from the same port — In-order placement for writes from the same AXI master • Configurable for in-order scheduling for reads and writes • Support read or write grouping
Timing	Fully programmable timing parameter support for all JEDEC*-specified timing parameters
Refresh	• All bank refresh or per bank refresh (if supported by memory) • Refresh management for DDR5
ECC	• Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters • Hardened ECC support including configurations for various ECC types with programmable single-bit and double-bit error reporting and automatic correction: — In-line ECC, out-of-band ECC, link ECC, end-to-end (user) ECC, or no ECC — Supports standard single bit error correction and double bit error detection — Support for ECC passthrough for fabric ECC with 8 bits of ECC per 64 bits of data — Supports scrubbing
Power states	Low power DRAM states including active power down, precharge power down, and self-refresh power down states for DRAM: • Under register control; or • Based on idle times
Training	Initial and periodic ZQ calibration (LPDDR4, LPDDR5, DDR5)
Verification	• Performance monitoring statistics • Memory test for DDR memories through register control

11. Hard Processor System in Agilex 7 SoCs

The Agilex 7 SoCs hard processor system (HPS) consists of multicore Arm processors. Additionally, the HPS adds a system memory management unit that enables system-wide hardware virtualization.

With the HPS architecture improvements, the Agilex 7 SoCs fulfill the requirements of current and future embedded markets, including:

- Wireless and wireline communications
- Datacenter acceleration
- Numerous military applications
- Various industrial applications

The HPS of the F-Series, I-Series, and M-Series SoCs consists a quad-core Arm Cortex-A53, allowing you to easily migrate existing SoC designs from Stratix 10 SoCs.

Figure 13. Agilex 7 SoCs HPS Block Diagram

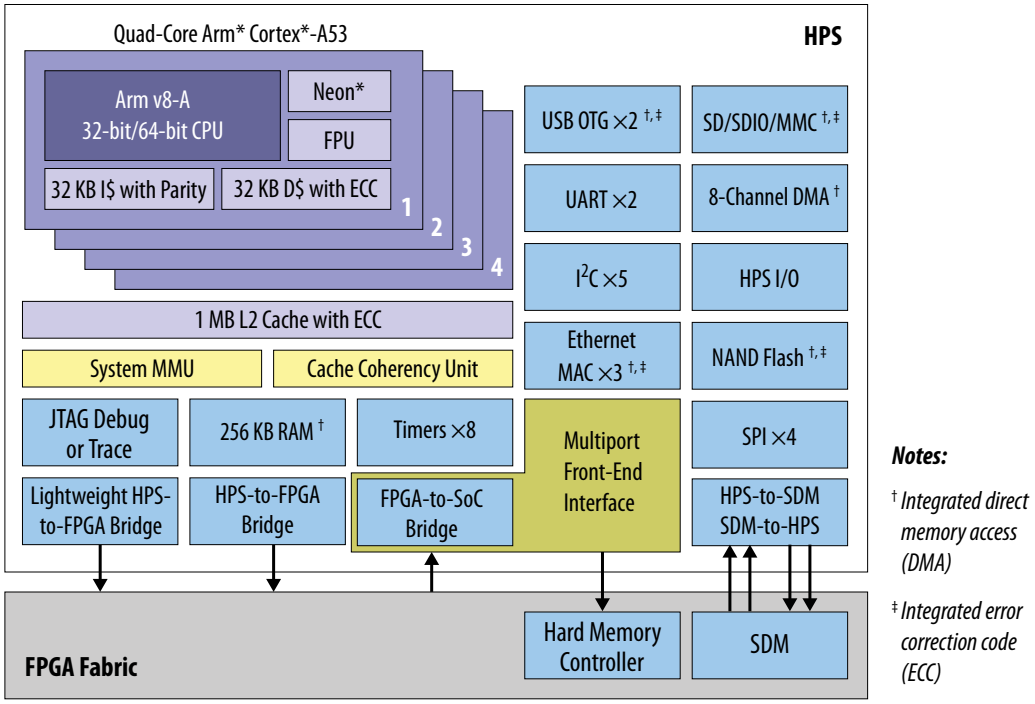

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Table 27. Summary of Agilex 7 SoCs Key Features

Feature		Description
Processor units		• Quad-core Arm Cortex-A53 MPCore processor unit — CPU frequency up to 1.4 GHz • 2.3 MIPS/MHz instruction efficiency • At 1.4 GHz, total performance of 13,800 MIPS — Arm v8-A architecture • Run 64-bit and 32-bit Arm instructions • 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint • Arm Jazelle* runtime compilation target (RCT) execution architecture with 8-bit Java* bytecodes • Superscalar, variable-length, out-of-order pipeline with dynamic branch prediction • Improved Arm Neon media processing engine • Single-precision and double-precision floating-point unit • Arm CoreSight debug and trace technology
System memory management unit		• Enables a unified memory model • Extends hardware virtualization into peripherals implemented in the FPGA fabric
Cache coherency unit		Propagates changes in shared data stored in cache throughout the system to provide I/O coherency for co-processing elements
Cache memory		• L1 cache: — 32 KB L1 I-cache with parity check — 32 KB of L1 D-cache with ECC — Parity checking • L2 cache: — Shared 1 MB — 8-way set associative — SEU protection with parity on TAG ram and ECC on data RAM — Cache lockdown support
On-chip memory		256 KB on-chip RAM
External SDRAM and flash memory Interfaces for HPS	Hard memory controller	• Supports DDR4, up to 3200 Mbps • 40-bit (32-bit + 8-bit ECC) • Some packages support 72-bit (64 bit + 8 bit ECC) • ECC support including calculation, error correction, write-back correction, and error counters • Software-configurable priority scheduling on individual SDRAM bursts • Fully programmable timing parameter support for all JEDEC-specified timing parameters • Multi-port front end (MPFE) interface to the hard memory controller, supporting AMBA 4 AXI QoS for interface to the FPGA fabric
	NAND flash controller	• Integrated descriptor-based controller with DMA • Programmable hardware ECC support • Support for 8-bit and 16-bit flash devices • Supports the ONFI 1.0 specification
	SD/SDIO/MMC controller	• Integrated descriptor-based DMA controller • Supports CE-ATA digital commands • Supports eMMC version 5.0 • 50 MHz operating frequency
	DMA controller	• Eight channels • Supports up to 32 peripheral handshake interfaces

continued...

Feature		Description
Communication interface controllers	Ethernet MAC	• Three Ethernet MACs supporting 10 Mbps, 100 Mbps, and 1 Gbps with integrated DMA • Ethernet standards: — IEEE 1588-2002 and IEEE 1588-2008 standards for precise networked clock synchronization — IEEE 802.1Q VLAN tag detection for reception frames • Ethernet interfaces: — Supports RGMII and RMII external PHY Interfaces — Supports MII and GMII operating modes through standard FPGA I/O — Supports RMII operating mode using MII to RMII adapter — Supports RGMII operating mode using GMII to RGMII adapter — Supports SGMII operating mode using GMII to SGMII adapter
	USB 2.0 OTG	• Two USB OTG controllers with DMA • Dual-role device (device and host functions) — High-speed (480 Mbps) — Full-speed (12 Mbps) — Low-speed (1.5 Mbps) — Supports USB 1.1 (full-speed and low-speed) • Integrated descriptor-based scatter-gather DMA • Support for external ULPI PHY • Up to 16 bidirectional endpoints, including control endpoint • Up to 16 host channels • Supports generic root hub • Configurable to USB OTG 1.3 and USB OTG 2.0 modes
	I^2C	• Five I^2C controllers, three can be used by the Ethernet MAC for MIO to external PHY • Support 100 Kbps and 400 Kbps modes • Support 7-bit and 10-bit addressing modes • Support master and slave operating modes
	UART	• Two UART 16550-compatible controllers • Programmable baud rate up to 115.2 kilobaud
	SPI	• Four SPI (two masters, two slaves) • Supports full duplex and half duplex
Timers		• Four general-purpose timers • Four watchdog timers
I/O		• 48 HPS direct I/Os allow HPS peripherals to connect directly to the I/Os • Up to two FPGA fabric I/O banks assignable to the HPS for HPS DDR access
Interconnect to logic core	HPS–to–FPGA bridge	• Allows HPS bus masters to access bus slaves in FPGA fabric • Configurable 32-, 64-, or 128-bit AMBA AXI data interface allows high-bandwidth HPS master transactions to FPGA fabric
	HPS–to–SDM and SDM–to–HPS bridges	Allows the HPS to reach the SDM block and the SDM to bootstrap the HPS
	Lightweight HPS–to–FPGA bridge	Lightweight 32-bit AMBA AXI interface suitable for low bandwidth register access from HPS to soft peripherals in the FPGA fabric
	FPGA–to–HPS bridge	• Configurable 128, 256, or 512 bits ACE-Lite interface • Up to 256-bit FPGA–to–HPS interface targeting the HPS • Up to 512-bit FPGA–to–HPS interface targeting the DDR

12. Heterogeneous 3D SiP Transceivers in Agilex 7 FPGAs and SoCs

The Agilex 7 FPGA product family offers low-latency power-efficient transceivers optimized for a wide variety of applications. These FPGA transceivers support bandwidth capacities ranging from 1 Gbps to 32 Gbps NRZ, 2 Gbps to 58 Gbps PAM4, and 116 Gbps PAM4.

Intel implements the Agilex 7 FPGA transceivers on heterogeneous 3D system-in-package (SiP) tiles, providing flexibility and scalability for current and future data rates, modulation schemes, and protocol IPs.

Figure 14. Core Fabric and Heterogeneous 3D SiP Transceiver Tiles

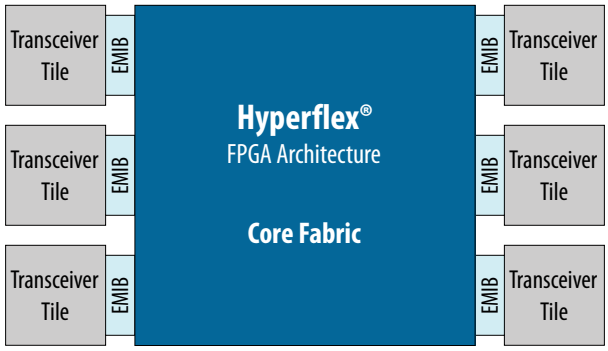

Table 28. Availability of Transceiver Types in Agilex 7 FPGAs and SoCs

Series	Transceiver Type			
	E-Tile	P-Tile	F-Tile	R-Tile
F-Series	Yes	Yes	Yes	—
I-Series	—	—	Yes	Yes
M-Series	—	—	Yes	Yes

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Table 29. Capabilities of the Different FPGA Transceiver Types

Tile Type	General Description	Maximum Data Rate and Channel Count	Hardened IP	Applications
E-Tile	General purpose transceiver	12× 58 Gbps PAM4 or 24× 28.9 Gbps NRZ	• 10/25/100 GbE MAC, PCS and RS-FEC (528,514) • RS-FEC (544,514)	• General purpose transceivers • Multi-protocol support for CEI, Ethernet, CPRI, FlexE, Interlaken, Fibre Channel, SRIO, Serial Lite, OTN, JESD204B/C, FlexO, IEEE1588
P-Tile	PCIe 4.0 transceiver	16× 16 Gbps NRZ	16× PCIe 4.0 with 8 PF/2K VF SR-IOV EP/RP	• PCIe 4.0 x16 • Port bifurcation support for 2×8 EP or 4×4 RP • CvP, autonomous HIP, SR-IOV 8PF/2kVF, VirtIO, scalable IOV, and shared virtual memory
F-Tile	General purpose and PCIe 4.0 transceiver	4×116 Gbps PAM4, 12× 58 Gbps PAM4, or 16× 32 Gbps NRZ	• 10/25/40/50/ 100/200/400 GbE MAC, PCS, and KR/KP RS-FEC • 16× PCIe 4.0 with 8 PF/2K VF SR-IOV EP/RP	• General purpose transceivers • Multi-protocol support for CEI, Ethernet, CPRI, FlexE, 300G Interlaken, fibre channel, SRIO, Serial Lite, OTN, JESD204B/C, IEEE1588, FlexO, GPON, SDI, Vby1, HDMI, CvP, Display Port • Includes P-Tile PCIe 4.0 features plus precise time management and PMA direct mode
R-Tile	PCIe 5.0 and CXL transceiver	16×32 Gbps NRZ	• 16× PCIe 5.0 with 8 PF/2K VF SR-IOV EP/RP • 16× CXL	• PCIe 5.0 x16 • Port bifurcation support for 2x8/4×4 EP or 4x4 RP • CvP, autonomous HIP, SR-IOV 8PF/2kVF, VirtIO, scalable IOV, and shared virtual memory • Separate header and payload interfaces on user interface • Precise time management and PIPE direct • CXL 1.1 and 2.0 support for applications that need cache and memory coherency to achieve low latency and high bandwidth for FPGA-based discrete accelerator use-cases

12.1. E-Tile Transceivers

The E-Tile transceivers provide continuous data rates from 1 Gbps to 28.9 Gbps NRZ and 2 Gbps to 58 Gbps PAM4. For longer-reach backplane driving applications, the E-Tile transceivers use advanced adaptive equalization circuits to equalize system loss.

All E-Tile transceiver channels are equipped with these blocks:

- Dedicated PMA—provides primary interfacing capabilities to physical channels
- Hardened PCS—typically handles encoding and decoding, word alignment, and other preprocessing functions before transferring data to the FPGA core fabric

A single PMA–PCS channel with independent clock domains forms each transceiver within the transceiver tile. Using a highly configurable clock distribution network, you can configure various bonded and non-bonded data rate within each transceiver bank and within each transceiver tile.

12.1.1. PMA Features in E-Tile Transceivers

The transmitter, receiver, and high speed clocking resources form the PMA channels. The transmit features deliver exceptional signal integrity at data rates up to 58 Gbps PAM4 or 28.9 Gbps NRZ. Additionally, each PMA features advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

Table 30. Transceiver PMA Features in E-Tile Transceivers

Feature	Capability
Data rates	Up to 58 Gbps
Optical module support	XFP, QSFP-DD, OSFP, QSFP/QSFP28, QSFP56, SFP+, SFP28, SFP56, CFP/CFP2/CFP4 optical modules support
Cable driving support	SFP+ Direct Attach, eSATA
Transmit pre-emphasis	• One post-tap and three pre-tap for PAM4 • One post-tap and one pre-tap for NRZ
Dynamic reconfiguration	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility
Multiple PCS–PMA and PCS–Core to FPGA fabric interface widths	16, 20, 32, 40, or 64 bits interface width for flexible deserialization width, encoding, and reduced latency

12.1.2. PCS Features in E-Tile Transceivers

The E-Tile PCS includes the following features:

- 64B/66B encoder/decoder
- Scrambler/descrambler
- Block distribution/block synchronization
- Lane reorder

12.2. P-Tile Transceivers

The P-Tile transceivers are exclusively PCIe transceivers.

Features of the P-Tile transceivers:

- Support up to PCIe 4.0 ×16 at 16 Gbps
- Port bifurcation support—2×8 endpoint or 4x×4 root port
- TL bypass features
- Configuration via protocol (CvP)
- Autonomous hard IP
- Single-root I/O virtualization (SR-IOV)—8 physical functions or 2K virtual functions
- VirtIO support
- Scalable IOV
- Shared Virtual Memory

12.3. F-Tile Transceivers

The F-Tile transceivers are general purpose transceivers.

Features of the F-Tile transceivers:

- Speed options:
  - Four channels of 116 Gbps PAM4 or 58 Gbps NRZ
  - 12 channels of 58 Gbps PAM4 or 16 channels of 32 Gbps NRZ
- Hard IP support for Ethernet and PCIe
- Other protocols support:
  - Multiprotocol support for CEI, Ethernet, CPRI, FlexE, 300 Gbps Interlaken, fibre channel, SR-IOV, SerialLite IV, OTN, JESD204B, JESD204C, FlexO, IEEE1588, GPON, SDI, Vby1, HDMI, and Display Port
  - PCIe 4.0 ×16 support with P-Tile feature set, Precise Time Management, and PMA Direct mode
  - Configuration via protocol (CvP)

12.4. R-Tile Transceivers

The R-Tile transceivers are PCIe transceivers with hardened CXL IP.

Features of the R-Tile transceivers:

- Support up to PCIe 5.0 ×16 at 32 Gbps
- Port bifurcation support—2×8 endpoint or 4×4 root port
- TL bypass features
- Configuration via protocol (CvP)
- Autonomous hard IP
- Separate header and payload interfaces on the user interface
- Single-root I/O virtualization (SR-IOV)—8 physical functions or 2K virtual functions
- VirtIO support
- Scalable IOV
- Shared Virtual Memory
- Precise time management
- PIPE direct
- Hardened CXL IP, up to PCIe 5.0 ×16 endpoint
- Selected features support CXL 1.1 and 2.0 specifications
- Soft logic (encrypted) to support CXL Type 1, Type 2, or Type 3 devices
- Mix and manage different memory types and controllers

13. Heterogeneous 3D Stacked HBM2E DRAM Memory in Agilex 7 FPGAs and SoCs M-Series

Agilex 7 FPGAs and SoCs M-Series offer options for integrated HBM2E DRAM memory. The HBM2E memory blocks are inside the package together with the high-performance FPGA core fabric, transceiver tiles, and HPS.

The in-package inclusion of the HBM2E memory results in a near-memory compute implementation that allows up to 820 GBps total aggregate memory bandwidth. This aggregate bandwidth is an increase of over ten times compared to DDR5 memory bandwidth. A near-memory configuration also reduces system power by reducing traces between the FPGA and memory, while also reducing board area.

Some M-Series FPGAs have two integrated HBM2E DRAM memory stacks inside the package. Each DRAM stack contains:

- 8 GB or 16 GB density per stack with 16 GB or 32 GB total density per device
- 410 GBps memory bandwidth per stack with 820 GBps total aggregate memory bandwidth per device
- Eight 128-bits wide independent channels or sixteen 64-bits wide independent pseudo channels
- Data transfer rates of up to 3.2 Gbps per signal between the core fabric and the HBM2E DRAM memory

The core fabric of the M-Series FPGAs can interface with the HBM2E directly or through the hardened memory NoC.

Related Information

Agilex 7 FPGAs and SoCs M-Series on page 19

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14. High-Performance Crypto Blocks in Agilex 7 FPGAs and SoCs F-Series and I-Series

Select Agilex 7 FPGAs contain multiple instances of the crypto block. The 200 Gbps half-duplex crypto block consists of hardened logic that performs both encryption and decryption functions in a single circuit. The crypto blocks reside in the top and bottom periphery of the device next to the I/O cells.

The crypto block supports these encryption standards:

- AES standard, used worldwide
- SM4 standard, used primarily in China

The crypto block supports these different modes of operation:

- Galois counter mode (GCM)
- XTS mode, built on top of XOR-encrypt-XOR

The Ethernet MACsec soft IP supports each crypto block, providing a complete MACsec solution for 100 Gbps full-duplex or 200 Gbps half-duplex throughput rates. You can also use the crypto block with a third-party or your own IPsec soft IP.

Related Information

- Part Number Decoder on page 22
  List the ordering part number of devices with the cryptographic block option.
- Agilex 7 FPGAs and SoCs F-Series on page 13
  List the available cryptographic blocks in F-Series FPGAs.
- Agilex 7 FPGAs and SoCs I-Series on page 16
  List the available cryptographic blocks in I-Series FPGAs.

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15. Configuration via Protocol Using PCIe for Agilex 7 FPGAs and SoCs

Configuration via protocol (CvP) using PCIe allows you to configure the Agilex 7 FPGAs and SoCs across the PCIe bus. This capability simplifies board layout and increases system integration.

The embedded PCIe hard IP operates in autonomous mode before the FPGA is configured. Using this hard IP, you can power up and activate the PCIe bus within the 100 ms time allowed by the PCIe specification.

The Agilex 7 FPGAs and SoCs also support partial reconfiguration across the PCIe bus. This capability reduces system downtime by keeping the PCIe link active during device reconfiguration.

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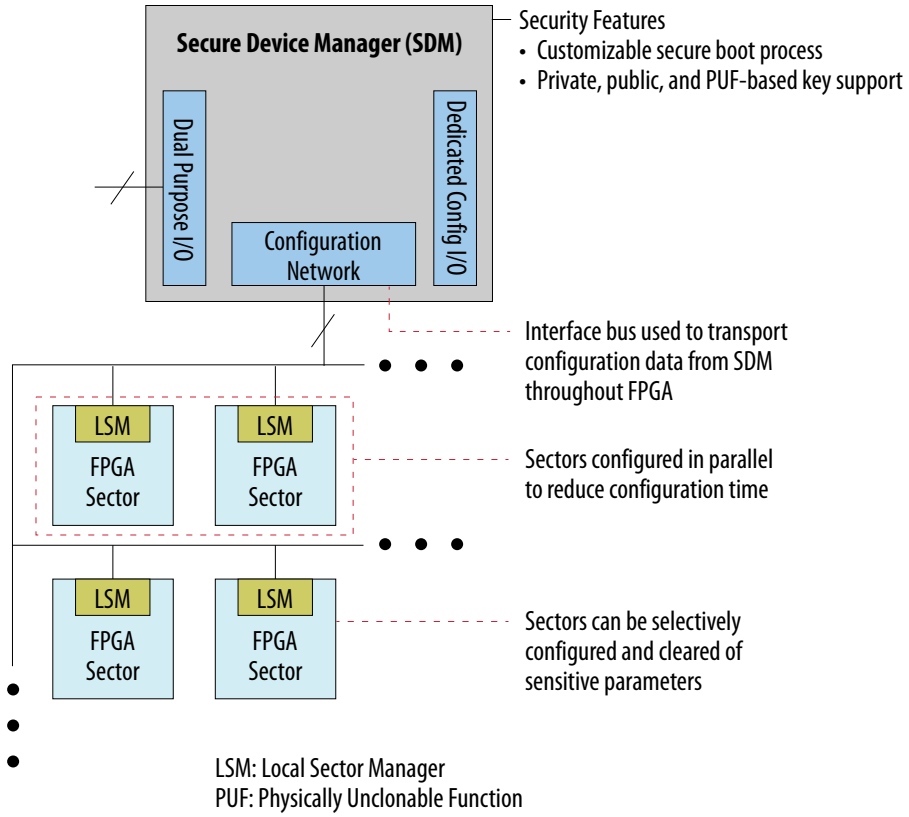
16. Device Configuration and the SDM in Agilex 7 FPGAs and SoCs

All Agilex 7 FPGAs and SoCs contain an SDM. The SDM is a triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. Additionally, the SDM in the Agilex 7 FPGAs and SoCs enables system certification to FIPS140-3 layer 2 compliance(34).

The SDM bootstraps the HPS in Agilex 7 SoCs. This bootstrapping ensures that the HPS boots using the same security features available to the FPGA.

Figure 15. SDM Block Diagram



(34) Applicable devices: AGF 019, AGF 023, AGI 019, AGI 023, AGI 035, AGI 040, AGI 041, AGM 032, and AGM 039.

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During configuration, the Agilex 7 FPGA or SoC divides into logical sectors. A local sector manager (LSM) manages each logical sector. The SDM passes configuration data to each LSMs across the on-chip configuration network.

Advantages of the sector-based approach:

- Enables independent configuration of the sectors—one at a time or in parallel
- Achieves simplified sector configuration and reconfiguration
- Reduces overall configuration time caused by inherent parallelism.

The Agilex 7 FPGAs and SoCs use the same sector-based approach to respond to SEUs and security attacks.

Although the sectors provide a logical separation for device configuration and reconfiguration, the sectors overlay the normal rows and columns of FPGA logic and routing:

- No impact to the Quartus Prime software place and route
- No impact to the timing of logic signals that cross the sector boundaries

The SDM enables robust, secure, and fully-authenticated device configuration. Additionally, the SDM allows you to customize the configuration scheme, enhancing device security.

Advantages of the SDM-based device configuration approach:

- Provides a dedicated secure configuration manager
- Reduces device configuration time because sectors are configured in parallel
- Enables an updatable configuration process
- Supports partial reconfiguration
- Allows remote system update
- Supports zeroization of whole device or individual sectors

Table 31. Supported Configuration Schemes for Agilex 7 FPGAs

Configuration Scheme	Data Width	Maximum Data Rate
Active Serial (AS) normal and fast modes	4 bits	4 bits × 166 MHz = 664 Mbps
Avalon® streaming interface ×32	32 bits	32 bits × 125 MHz = 4 Gbps
Avalon streaming interface ×16	16 bits	16 bits × 125 MHz = 2 Gbps
Avalon streaming interface ×8	8 bits	8 bits × 125 MHz = 1 Gbps
JTAG	1 bit	1 bit × 30 MHz = 30 Mbps
Configuration via Protocol (CvP)	×8 and ×16 lanes	The maximum data rate depends on the PCIe generation and number of lanes. Typically, the configuration data width is limited by the data rate of the device's internal configuration data path instead of the PCIe link width.

17. Partial and Dynamic Configuration of Agilex 7 FPGAs and SoCs

Altera built the partial reconfiguration process on top of the proven incremental compile design flow in the Quartus Prime design software. With partial reconfiguration, you can reconfigure parts of the FPGA while other sections continue to run. In systems with critical uptime requirement, you can update or adjust functions without disrupting service provision.

Apart from lowering power usage and cost, partial configuration effectively increases the logic density. Instead of placing all functions in the FPGA from the start, you can store functions that do not have to operate simultaneously in external memory. You can load these function into the FPGA when needed. Using this technique, you can run multiple applications on a single FPGA and reduce the requirements for FPGA size, board space, and power.

With dynamic reconfiguration, Agilex 7 FPGAs and SoCs can dynamically change data rates, protocols, and analog settings of a transceiver channel without affecting data transfer on adjacent transceiver channels. This capability is ideal for applications that require on-the-fly multi-protocol or multi-rate support.

You can dynamically reconfigure both the PMA and PCS blocks within the transceiver. You can also use dynamic reconfiguration together with partial reconfiguration to partially reconfigure the FPGA core and transceivers simultaneously.

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18. Device Security for Agilex 7 FPGAs and SoCs

Agilex 7 FPGAs and SoCs are built with robust security features and managed by the SDM. The devices prioritize the operations of the SDM over fabric and other microprocessor tasks.

The dedicated SDM manages and supports the following critical security features:

- Manages FPGA configuration process and all security features
- Performs authenticated FPGA configuration and HPS boot
- Supports FPGA bitstream encryption, secure key provisioning, and PUF key storage
- Supports platform attestation using the SPDM protocol
- Manages runtime sensors and supports active tamper detection and responses
- Provides access to hardened cryptographic engines as a service

In addition to the preceding list, the following table summarizes the three pillars of security with the advanced security features that Agilex 7 FPGAs and SoCs support.

Table 32. Agilex 7 FPGAs and SoCs Advanced Security Features

Pillar of Security	Device Security Features
Confidentiality, integrity, and availability	• Encryption • Authentication • Attestation • Secure boot • User access to cryptographic functions • Secure debug • Vendor authorized boot
Key protection	• Side channel mitigation • Physical anti-tamper detection and response
Secure manufacturing	• Black key provisioning • Secure returned merchandise authorization (RMA)

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19. SEU Error Detection and Correction in Agilex 7 FPGAs and SoCs

Agilex 7 devices feature a robust SEU error detection and correction circuitry that protects the configuration RAM (CRAM) programming bits and M20K user memories.

To protect the CRAM, a parity checker circuit with integrated ECC runs continuously to automatically correct single-bit or double-bit errors and detect higher order multi-bit errors. The optimized physical layout of the CRAM array makes most multi-bit upsets appear as independent single-bit or double-bit errors. Therefore, the CRAM ECC circuitry can automatically correct these errors.

The user memories also has integrated ECC circuitry and are also layout-optimized for error detection and correction.

To provide a complete SEU mitigation solution, a soft IP and the Quartus Prime software support the SEU error detection and correction hardware. The following components make up the complete solution:

- Hard error detection and correction for CRAM and M20K user memory blocks
- Optimized memory cells physical layout to minimize the probability of an SEU
- Sensitivity processing soft IP that reports if a CRAM upset affects a used or unused bit
- Fault injection soft IP with Quartus Prime software support to change CRAM bits state for testing
- Hierarchy tagging feature in the Quartus Prime software
- Triple modular redundancy (TMR) for the SDM and critical on-chip state machines

Furthermore, Agilex 7 FPGAs and SoCs are built on the FinFET-based Intel 10-nm SuperFin or Intel 7 technology. FinFET transistors are less susceptible to SEUs compared to conventional planar transistors.

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20. Power Management for Agilex 7 FPGAs and SoCs

The Agilex 7 FPGA product family offers standard power devices that support SmartVID and fixed core voltage devices with limited core speed options.

The Agilex 7 FPGAs and SoCs achieve up to 40% total power reduction compared to the previous generation Stratix 10 FPGAs.

To achieve the total power reduction, the Agilex 7 FPGAs and SoCs capitalizes on:

- Advanced Intel 10-nm SuperFin or Intel 7 technology
- Second generation Hyperflex core architecture
- Other power reduction techniques such as power island and power gating

Table 33. Agilex 7 FPGAs and SoCs Power Options

Device Type	Series	Designation	Description
SmartVID	F-Series I-Series M-Series	-V	• The devices operate at the optimum core voltage that meets the VID power limit and required device performance for various FPGA applications. • A factory-programmed code allows a PMBus voltage regulator to operate at the optimum core voltage to meet the device VID power limit and performance specifications. Therefore, you must mandatorily drive the V_{CC} and V_{CCP} core voltage supplies of the SmartVID device with a dedicated PMBus voltage regulator.
Fixed voltage	F-Series	-F	• The devices support 0.8 V. • Using a fixed low core voltage, the devices further reduce the total power consumption. • These fixed voltage devices have lower static power than the SmartVID standard power devices while maintaining device performance.

The power island and power gating feature powers down unused resources in Agilex 7 devices to reduce static power consumption. During configuration, the Quartus Prime software automatically powers down specific unused resources such as the DSP or M20K blocks.

Furthermore, Agilex 7 devices feature industry-leading low power transceivers and include a number of hard IP blocks. The hard IP blocks not only reduce logic resources utilization but also deliver substantial power savings compared to soft implementations. The hard IP blocks generally consume up to 50% less power than equivalent soft logic implementations.

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21. Software and Tools for Agilex 7 FPGAs and SoCs

The Quartus Prime Pro Edition design suite supports the Agilex 7 FPGAs and SoCs with a new compiler and the Hyper-Aware design flow.

Together with the Intel oneAPI toolkit, software developers can develop acceleration solutions using Agilex 7 FPGAs and SoCs. The Intel oneAPI toolkit provides a unified, single-sourced, software-friendly, and heterogeneous programming environment for a diverse set of computing engines. The toolkit includes a comprehensive and unified portfolio of developer tools you can use to map software to hardware and accelerate your code.

To improve the efficiency and quality of your designs, Altera also provides the following tools for the Agilex 7 FPGAs and SoCs:

- Transceiver toolkit
- Platform Designer IP integration tool
- Intel DSP Builder for Intel FPGAs advanced blockset
- Arm Development Studio for Intel SoC FPGA (Arm DS for Intel SoC FPGA)

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22. Revision History for the Agilex 7 FPGAs and SoCs Device Overview

Document Version	Changes
2024.10.09	Updated information about PCS features in E-Tile transceivers.
2024.04.01	• Updated the ethernet MAC row in the table listing the features specific to Agilex 7 SoCs. • Added package 3184E with F-Tile ×2 and R-Tile ×2 (package code R31E) for the AGI 041 device. • Removed package 3695A. • Retitled "Available Options" to "Part Number Decoder". • Updated the figure showing the ordering part number: — Added package 3184E to I-Series FPGAs. — Removed package 3695A from M-Series FPGAs. — Added optional suffixes B and C. • Added links to updated lists of available Agilex 7 FPGAs and SoCs. • In the summary of Agilex 7 SoCs key features, updated the eMMC support from version 4.5 to 5.0.
2023.10.31	• Added package 2340A with F-Tile ×1 (package code R24D) for AGF 006, AGF 008, AGF 012, and AGF 014 devices. • Added package 3184B to M-Series FPGAs. • Removed package 3695B from M-Series FPGAs.
2023.09.07	Removed Ethernet AVB from the list of Ethernet standards that the HPS supports.
2023.07.05	Corrected typographical error in the table summarizing the device family features.
2023.04.19	• Added package 3184B to the AGI 041 device. • Removed packages 3184B and 3687A from M-Series FPGAs. • Added packages 3695A and 3695B to M-Series FPGAs.
2023.02.20	Added the AGI 041 device.
2023.01.10	• Moved all D-Series information to new *Intel Agilex 5 FPGAs and SoCs Device Overview* • Updated product family name to "Intel Agilex 7 FPGAs and SoCs" • Updated the I-Series FPGA packages — Added CXL column to package 1085A — Added package 3184A • Updated the figure showing the ordering part numbers • Updated the table that lists the tile types, hardened IPs, and applications
2022.09.26	• Added the D-Series FPGAs and SoCs • Restructured and rewrote the document
2022.06.09	• Updated the ordering part numbers • Removed the 3184A package • Added information about FHT and FGT transceivers • Added M-Series FPGAs with F-Tile and HBM2E package options • Updated the figure showing the hard memory controller
2022.04.06	Updated package code "R19A" to "R18A" in the ordering part number.

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Document Version	Changes
2022.03.06	• Revised key innovations in Agilex 7 FPGAs and SoCs: — DDR5 supports up to 5600 Mbps per pin — Intel 7 technology in the M-Series • Added *Agilex 7 SoC FPGAs M-Series* • Added M-Series in the *Agilex 7 Ordering Part Number (OPN)* figure • Added block diagram for the M-Series in the *Agilex 7 FPGA and SoC Block Diagram* • Added support for the M-Series FPGAs and SoCs including the AGM 032 and AGM 039 devices • Added *Heterogeneous 3D Stacked HBM2E DRAM Memory*
2021.12.05	• Updated *Agilex 7 FPGA and SoC Device Overview* • Globally revised key innovations in Agilex 7 FPGAs and SoCs: — Device densities of up to 4 million equivalent logic elements — Configurable networking support is up to 6 x 400G or 12 x 200G in a single device — Over 25K of 18x19 multipliers, or over 50K of 9x9 multipliers in a single device — Over 389 Mb of embedded RAM in the largest device • Updated description of the following features in the *Feature Summary* table: — Technology — General purpose I/Os — Core clock networks — Packaging • Globally added AGI 035 and AGI 040 devices support for the I-Series
2021.07.22	Added Adaptive Logic Modules (ALM) count in the *Agilex 7 FPGAs and SoCs F-Series Family Plan* and *Agilex 7 FPGAs and SoCs I-Series Family Plan* tables.
2021.06.21	• Updated *Agilex 7 FPGA and SoC Device Overview* • Renamed 10nm FinFET process Technology to 10nm SuperFin Technology • Updated specification and package code in the *Agilex 7 FPGAs and SoCs Ordering Part Number (OPN)* figure • Added new high-performance crypto blocks feature • Globally added AGF 014 and AGF 022 devices support for the F-Series FPGAs • Globally added AGI 019 and AGI 023 devices support for the I-Series FPGAs • Added new topic: *High-Performance Crypto Block* • Revised figures and diagrams.
2021.04.19	Sections Updated: • *Available Options* • *Agilex 7 FPGA and SoC Family Plan*
2021.03.23	Sections Updated: • *Agilex 7 SoC FPGAs M-Series* • *Available Options* • *Agilex 7 FPGA and SoC Summary of Features* • *Agilex 7 FPGA and SoC Family Plan* • *Heterogeneous 3D SiP Transceiver Tile* • *Agilex 7 FPGA Transceivers* • *External Memory and General Purpose I/O*
2020.09.30	Sections Updated: • *Agilex 7 FPGA and SoC Device Overview* • *Agilex 7 FPGA and SoC Summary of Features* • *Agilex 7 FPGA and SoC Family Plan* • *Hyperflex Core Architecture* • *Agilex 7 FPGA Transceivers*
2019.07.02	Sections Updated:

continued...

Document Version	Changes
	• *Agilex 7 FPGA and SoC Device Overview* • *Agilex 7 FPGA and SoC Family Variants* • *Agilex 7 SoC FPGAs F-Series* • *Agilex 7 SoC FPGAs* I-Series • *Agilex 7 SoC FPGAs M-Series* • *Common Features* • *Available Options* • *FPGA and SoC Summary of Features* • *FPGA and SoC Family Plan* • *Hyperflex Core Architecture* • *Heterogeneous 3D SiP Transceiver Tile* • *PCS Features* • *P-Tile Transceivers* • *External Memory and General Purpose I/O* • *Adaptive Logic Module (ALM)* • *Internal Embedded Memory* • *Variable Precision DSP* • *Device Security*
2019.04.02	Initial Release