EC2650QI 6A Voltage Divider

High Efficiency 12V to 6V (33W) Intermediate Bus Converter

DESCRIPTION

The EC2650QI is an Intel® Enpirion® DC-DC intermediate voltage bus converter with extremely high efficiency. It integrates low ON-resistance MOSFET switches and small-signal control circuits in an advanced 5.5mm x 5.5mm x 0.9mm 36-pin QFN package.

The EC2650QI generates an output voltage that tracks one-half of the input voltage and is designed to power the other Intel Enpirion 6V DC-DC converters. By using a highly efficient 2-stage approach with the EC2650QI, smaller size and lower cost converters may be used without sacrificing total system efficiency. When multiple rails are involved, this can greatly reduce precious PCB board space needed for power regulation.

Intel Enpirion Power Solutions significantly help in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of components required for the complete power solution helps to enable an overall system cost saving.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

FEATURES

- High Efficiency (Up to 94%)
- Very Thin 12V to 6V Converter Solution
- 150mm^2 Optimized Total Solution Size
- 5.5mm x 5.5mm x 0.9mm Package
- 8V to 13.2V Input Voltage Range
- Up to 6A Continuous Operating Current
- Adjustable Switching Frequency
- Master/Slave Parallel Operation (up to 144W)
- Input Power OK Indicator
- Over-Current, Short Circuit, Thermal Shutdown, Input OVP and UVLO Protection
- RoHS Compliant, MSL Level 3, 260°C Reflow

APPLICATIONS

- 12V Applications Requiring High Efficiency, Small Solution Size and High Power Density
- Systems with FPGA, ASICs, or ASSPs that Require Multiple Power Rails
- Applications with Multiple Power Rails such as Industrial, Networking, embedded Computing and PCIe Cards
- 12V Industrial and Consumer Applications in Audio/Video, Home Theater and Tuners

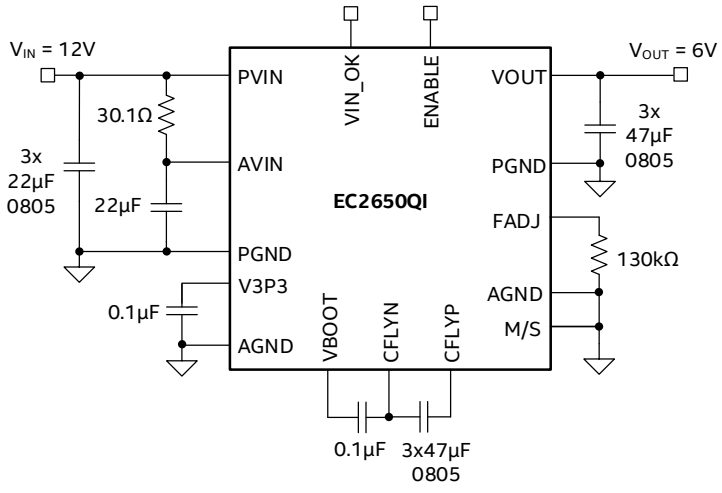


Figure 1: Simplified Applications Circuit

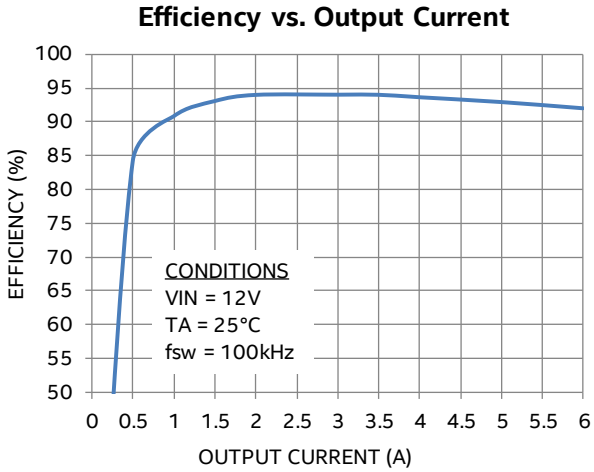


Figure 2: Efficiency vs. Output Current

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EC2650QI	EC2650QI	-40°C to +125°C	36-pin (5.5mm x 5.5mm x 0.9mm) QFN
EVB-EC2650QI	EC2650QI	QFN Evaluation Board	

Packing and Marking Information:

https://www.intel.com/content/www/us/en/programmable/support/quality-and-reliability/packing.html

PIN FUNCTIONS

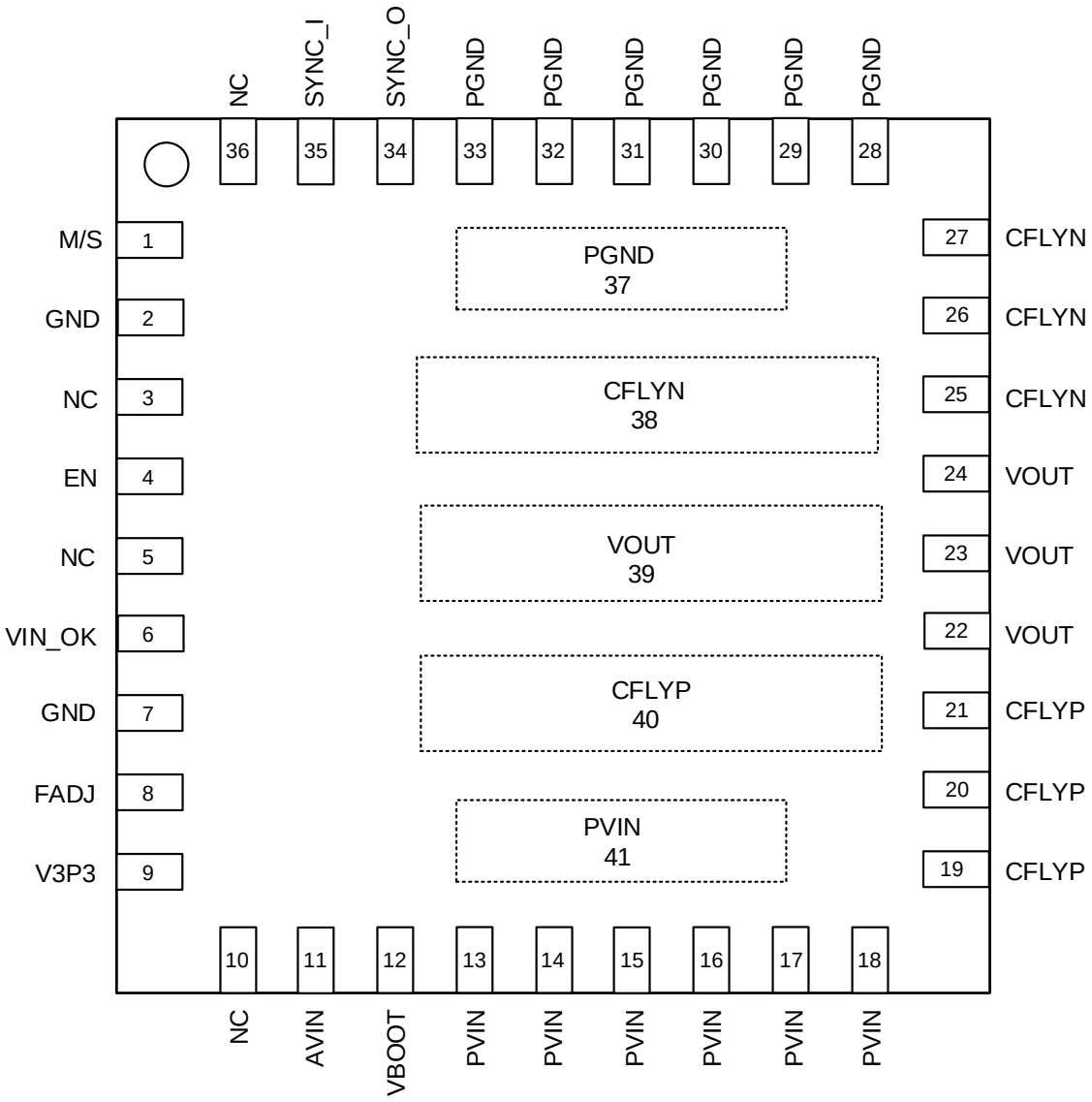


Figure 3: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1	M/S	Input	Master/Slave pin for Parallel Operation. Logic low = Master. Logic High = Slave. Use Master mode for standalone operation. Recommended to connect to V3P3 for High and to GND for Low.
2, 7	GND	Ground	Internally Regulated Supply Ground. Must tie directly to ground plane with a via right next to each pin.
3, 5, 10, 36	NC	No Connect	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION: May be internally connected.
4	EN	Input	Output Enable. Applying logic high on the ENABLE pin will enable the device and initiate a soft-start. Applying logic low or floating ENABLE disables the output and switching stops.
6	VIN_OK	Output	Open drain transistor for power system state indication for nominal 12V operation. VIN_OK is logic high when Vin is greater than 9V. This pin can be used to control the ENABLE signals of downstream converters powered by the EC2650QI.
8	FADJ	Input/Output	Frequency Adjust pin used to set the switching frequency. Connect a 130kΩ resistor from FADJ pin to GND for 100kHz switching frequency.
9	V3P3	Output	Internal Regulated Supply Output. Connect 0.1µF bypass capacitor from V3P3 to GND.
11	AVIN	Power	Quiet Input Supply for Controller. Connect to PVIN through an RC filter.
12	VBOOT	Input/Output	Internal power Supply for high-side drive. Connect a 0.1uF/25V boot-strap capacitor from VBOOT to CFLYN.
13-18	PVIN	Power	Main Input Supply
19-21	CFLYP	Input/Output	Positive Terminal of Flying Capacitor
22-24	VOUT	Output	Converter Output Voltage
25-27	CFLYN	Input/Output	Negative Terminal of Flying Capacitor
28-33	PGND	Ground	Power ground for the switching voltage divider
34	SYNC_O	Output	Synchronizing Clock Output. Provides clock input to EC2650s in Slave Mode from the Master Mode device.
35	SYNC_I	Input	External Synchronizing Clock Input. Input accepted in Slave Mode from an EC2650QI operating in Master Mode. May be left floating when used in Master mode.
37	PGND Pad	Ground	Not a perimeter pin. PGND pad under the device.

PIN	NAME	TYPE	FUNCTION
38	CFLYN Pad	Input/Output	Not a perimeter pin. Negative Terminal of Flying Capacitor.
39	VOUT Pad	Output	Not a perimeter pin. Converter Output Voltage.
40	CFLYP Pad	Input/Output	Not a perimeter pin. Positive Terminal of Flying Capacitor
41	PVIN Pad	Input	Not a perimeter pin. PVIN pad under the device.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage – PVIN, AVIN		-0.5	14	V
Input Voltage – VIN_OK, CFLYN, CFLYP, VOUT		-0.5	VIN	V
Input Voltage – V3P3, FADJ, M/S, SYNC_I, SYNC_O		-0.5	3.5	V
Input Voltage – VBOOT		-0.5	VIN + 8	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	8	13.2	V
Output Voltage Range	V_{OUT}	V_{IN} / 2	V_{IN} / 2 (1)	V
Output Current Range	I_{OUT}		6	A
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	160	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	20	°C
Thermal Resistance: Junction to Ambient (0 LFM) (2)	θ_{JA}	11	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1	°C/W

(1) V_{OUT} is equal to half of V_{IN} at the VOUT pin and is subject to voltage drop across the VOUT power plane as the load current increases.

(2) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{IN} = PVIN = 12V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	PVIN, AVIN		8	12	13.2	V
Operating Boot Strap Voltage	VBOOT	@ Vin =12V, with 0.1uF capacitor between VBOOT and CFLYN		17		V
Internal Regulated Supply Output	V3P3	@ Vin =12V	3.1	3.3	3.5	V
Input Under Voltage Lockout Rising	V_{UVLO_R}		6.6	7.2	7.7	V
Input Under Voltage Lockout Falling	V_{UVLO_F}		6.2	6.7	7.3	V
VIN_OK Rising	VIN_OK_R			8		V
VIN_OK Falling	VIN_OK_F			7.7		V
VIN_OK Sink Capability	VIN_OK_I			1		mA
Over Voltage Lockout	OVP		13.8	14.2	15	V
No-Load Operating Current	I_{OP}	$12V_{IN}$; I_{OUT} = 0A; fsw=100kHz		50		mA
Shutdown Current	I_{SD}			270		µA
Switching Frequency (Internal Oscillator)	F_{OSC}	R_{FADJ}= 130 KΩ	80	100	120	kHz
Output Voltage Range	V_{OUT}	10V ≤ V_{IN} ≤ 13.2V, 0A ≤ I_{LOAD} ≤ 6A	$0.42V_{IN}$		$0.5V_{IN}$	-
Output Impedance	R_{OUT}	$\Delta V_{OUT}/\Delta I_{LOAD}$ R_{FADJ}= 100 KΩ,		70		mΩ
Output Under Voltage Trip Level	V_{OCP}	V_{IN}=12V; When V_{OUT} is below 90% of $0.5V_{IN}$		5.4		V
Over-Current Trip Level	I_{OCP}	V_{IN} = 12V; Based on 70mΩ Output Impedance		8.5		A
EN Low Threshold	EN_L		1.2	1.58	2	V
EN High Threshold	EN_H		1.22	1.62	2.02	V

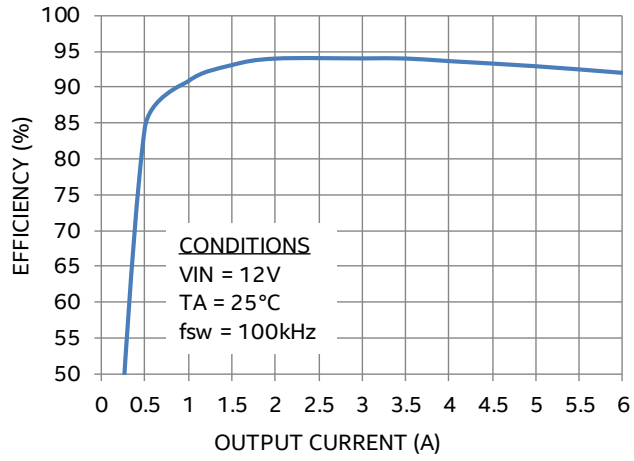
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
EN Hysteresis	EN_HYS			20		mV
M/S Input Logic Low	M/S_I_VIL		-0.3		0.3	V
M/S input Logic High	M/S_I_VIH		V3P3-0.6	V3P3	V3P3 + 0.3	V
SYNC_I Logic Low	SYNC_I_L				0.3	V
SYNC_I Logic High	SYNC_I_H		1.8		3.3	V
SYNC_O Logic Low	SYNC_O_L				0.3	V
SYNC_O Logic High	SYNC_O_H	@ 1mA	V3P3-0.6			V
Current Balance (3) (4)	ΔI_{OUT}	With 2 to 4 Converters in Parallel, the Difference Between Nominal and Actual Current Levels.		+/-10		%

(3) Parameter not production tested but is guaranteed by design.

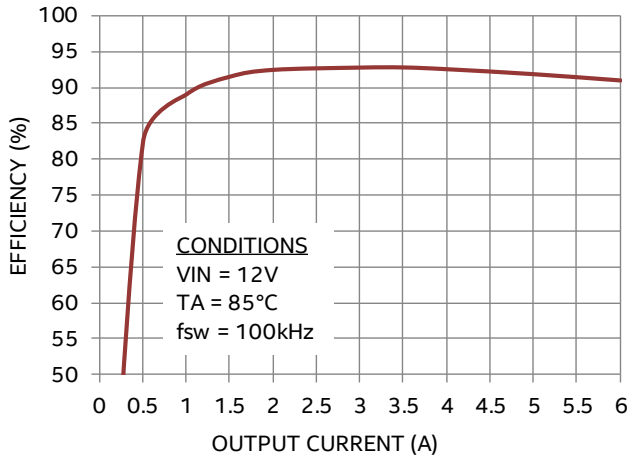
(4) Current Balance in Master/Slave parallel operation is dependent on layout and closeness of PVIN, PGND and VOUT.

TYPICAL PERFORMANCE CURVES

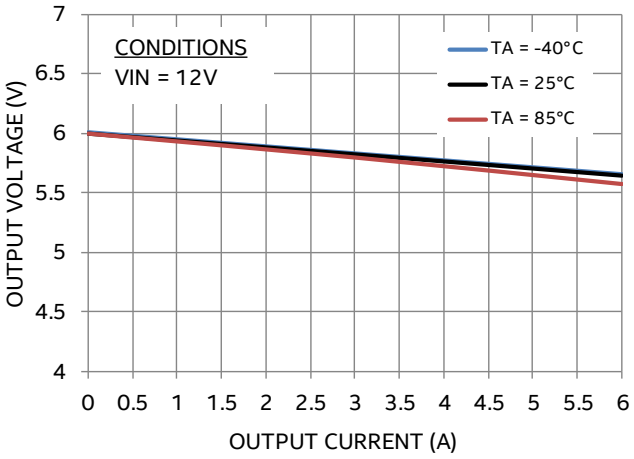
Efficiency vs. Output Current



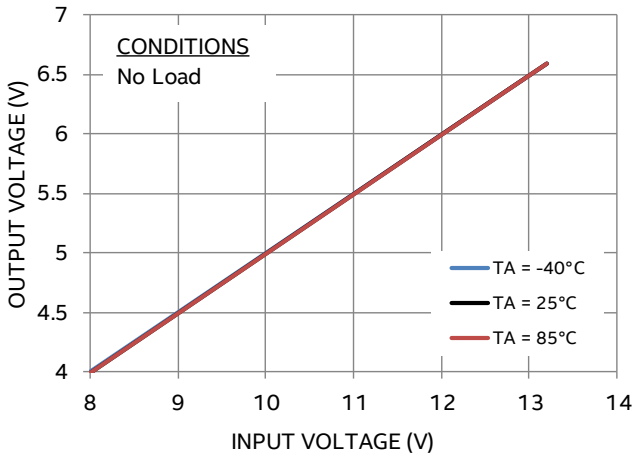
Efficiency vs. Output Current



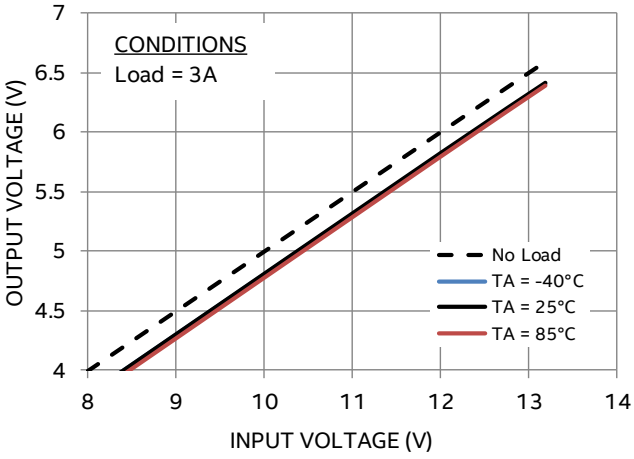
VOUT vs IOUT



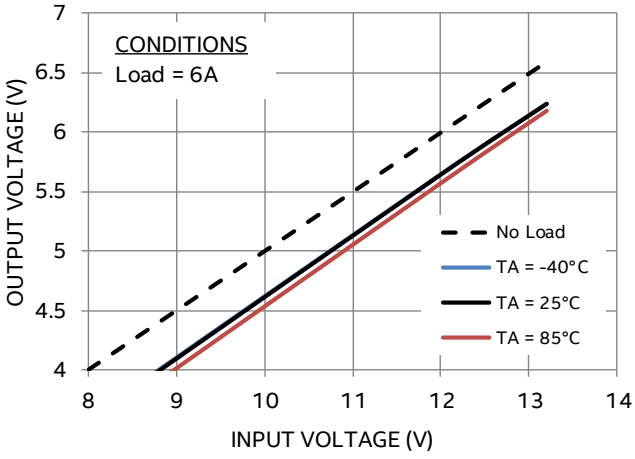
VOUT vs VIN



VOUT vs VIN

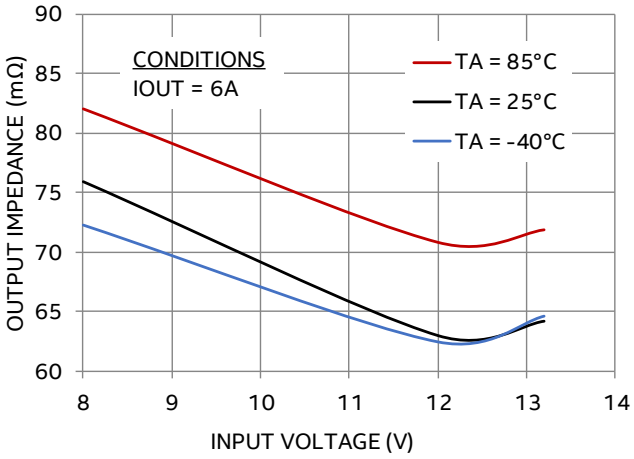


VOUT vs VIN

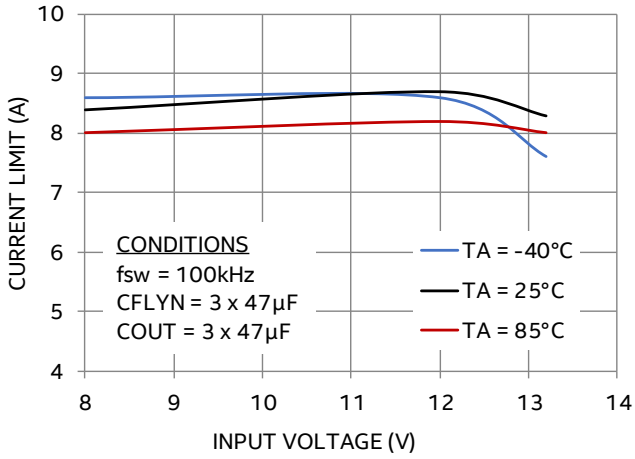


TYPICAL PERFORMANCE CURVES (CONTINUED)

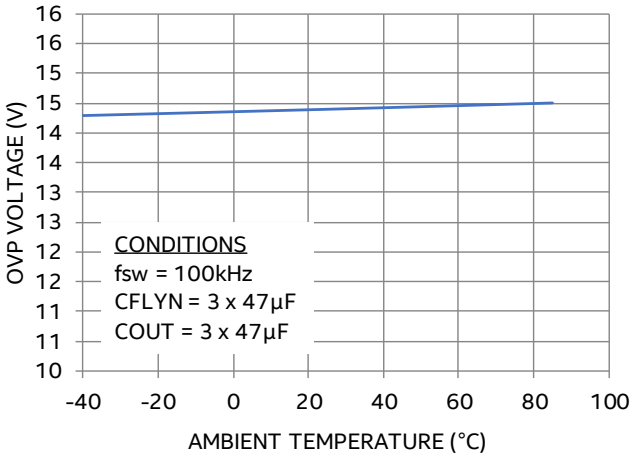
Output Impedance vs. Input Voltage



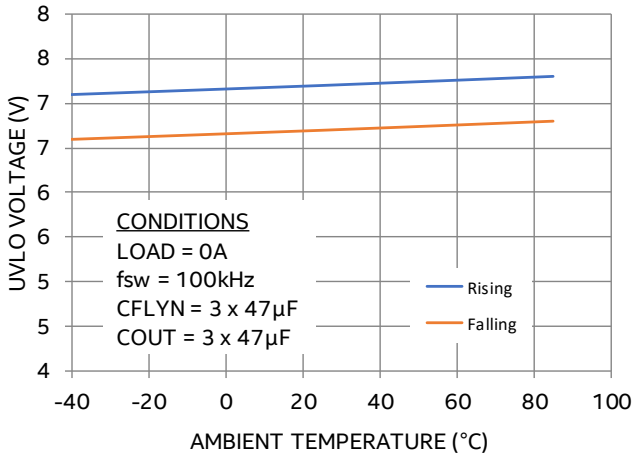
Current Limit vs. Input Voltage



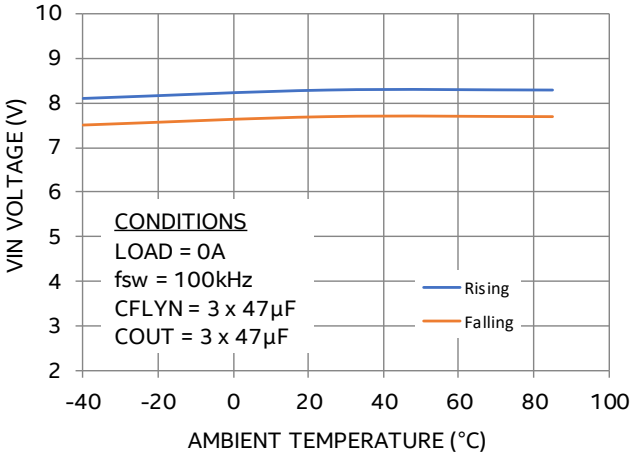
OVP Threshold vs. Temperature



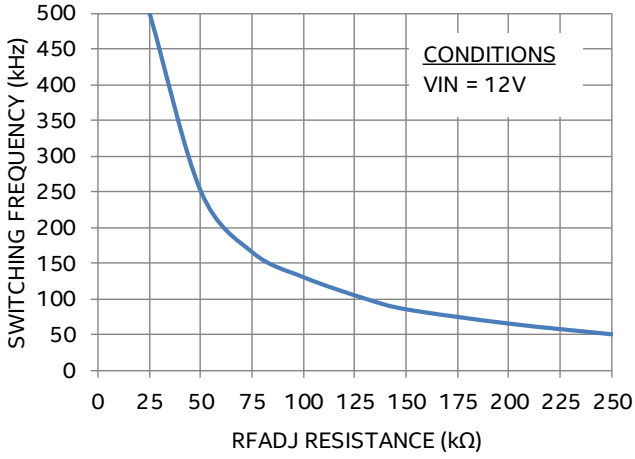
UVLO Threshold vs. Temperature



VIN_OK Threshold vs. Temperature

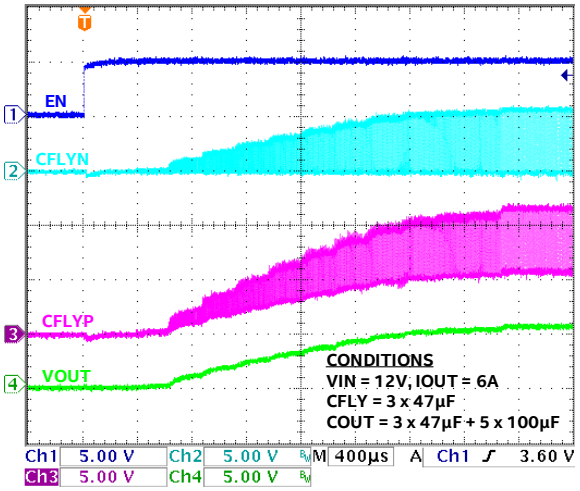


Switching Frequency vs. RFADJ

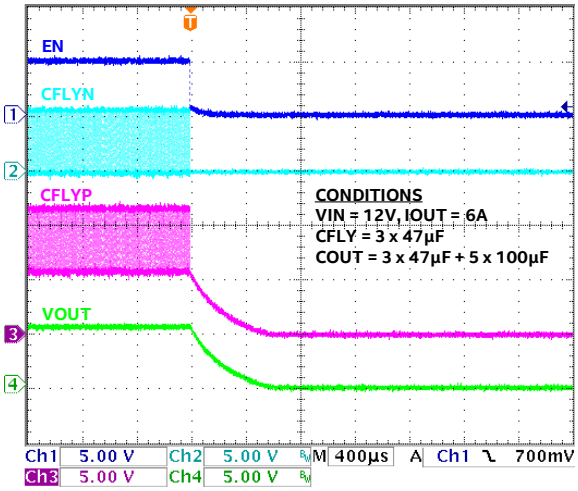


TYPICAL PERFORMANCE CHARACTERISTICS

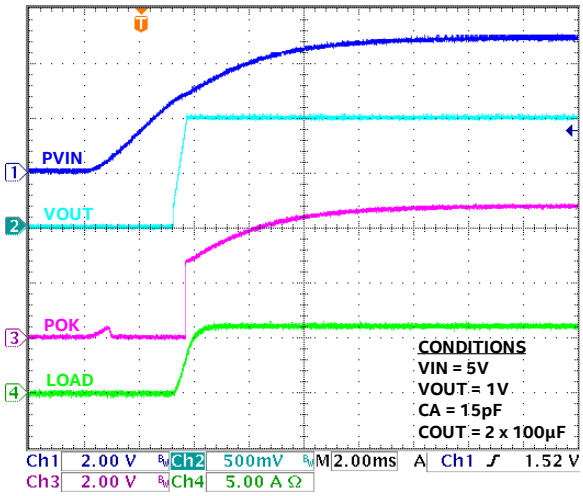
Enable Startup with 6A Load



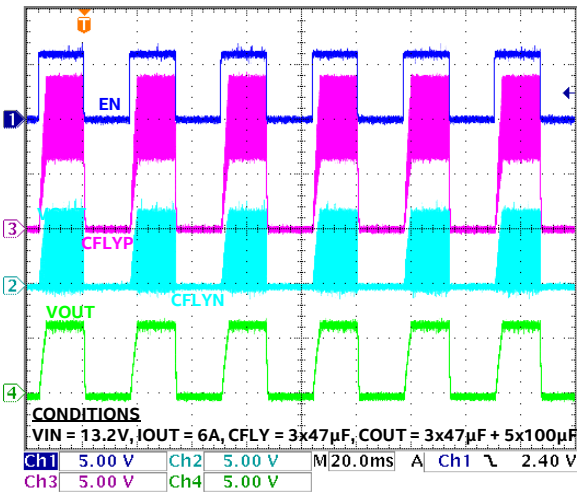
Enable Shutdown with 6A Load



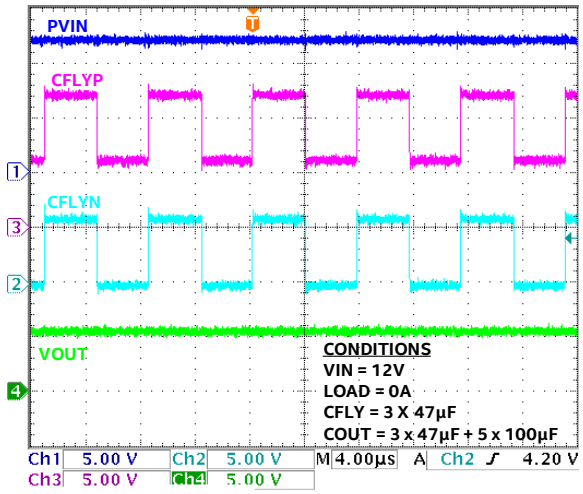
PVIN Startup at 6A Load



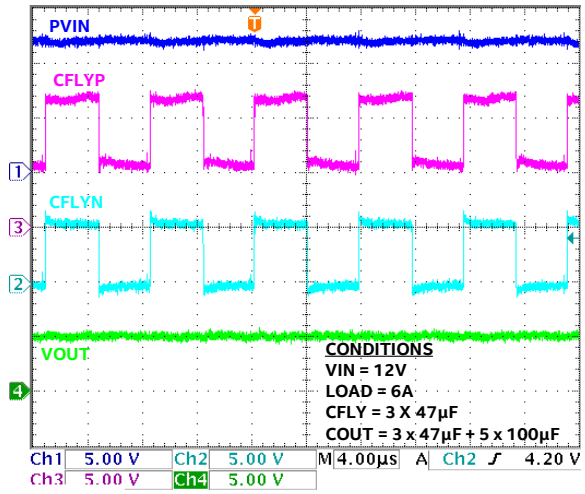
Startup and Shutdown at 6A Load



Switching Waveforms at 0A Load

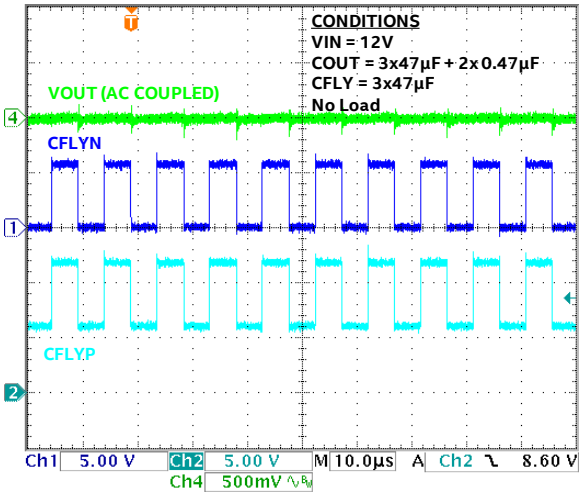


Switching Waveforms at 6A Load

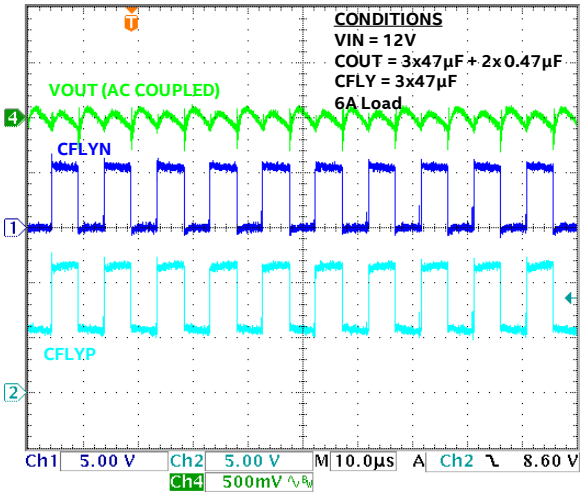


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

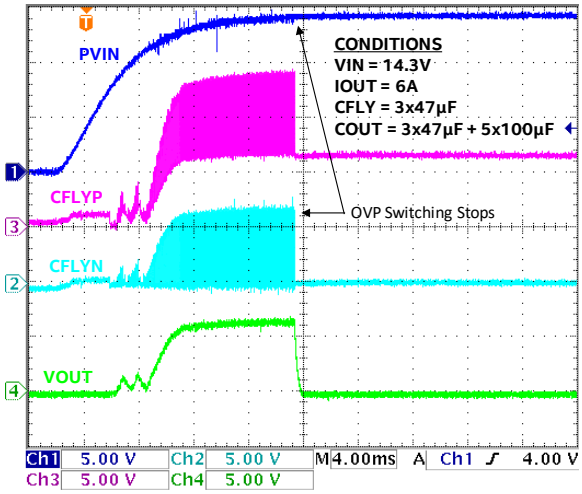
Output Ripple at 20MHz Bandwidth



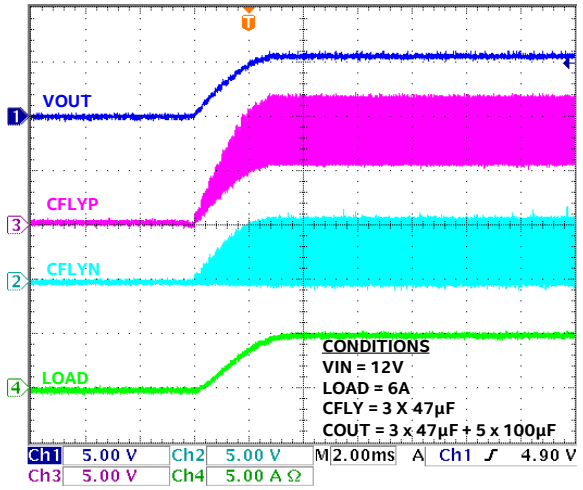
Output Ripple at 20MHz Bandwidth



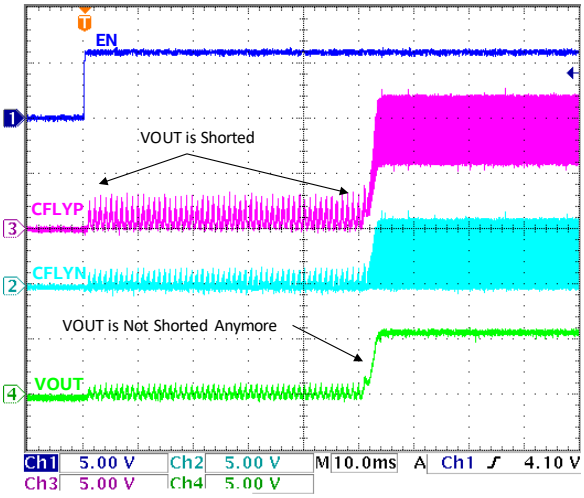
Input Over-Voltage Protection



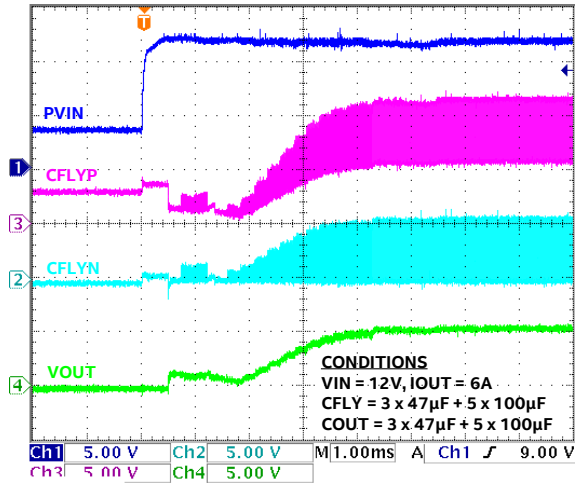
Thermal Shutdown Recovery



Short Circuit Recovery

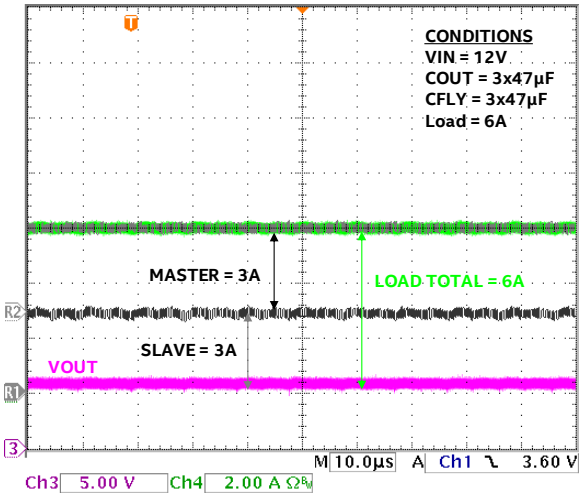


Fast PVIN Startup into 6A Load

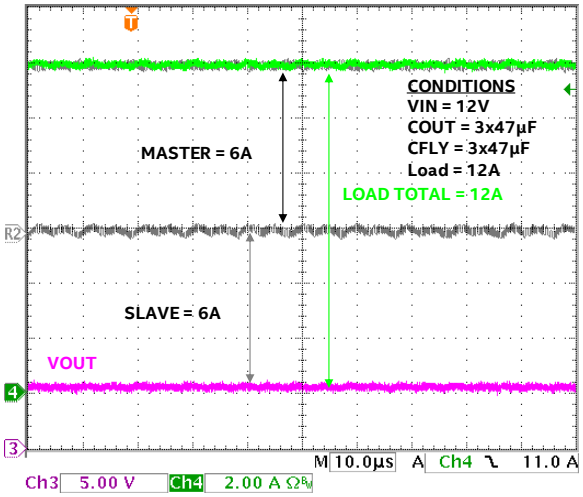


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

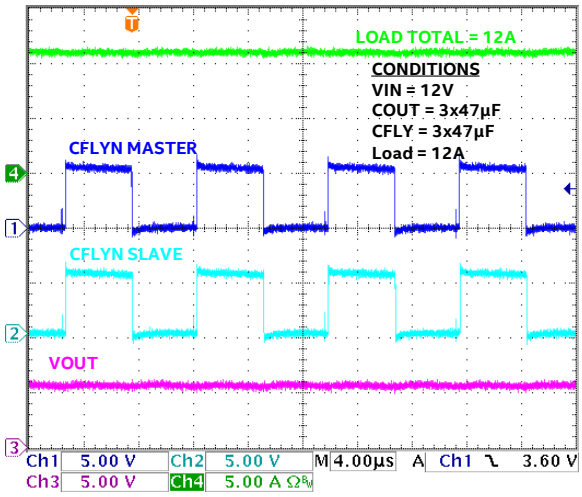
Parallel Operation with Load = 6A



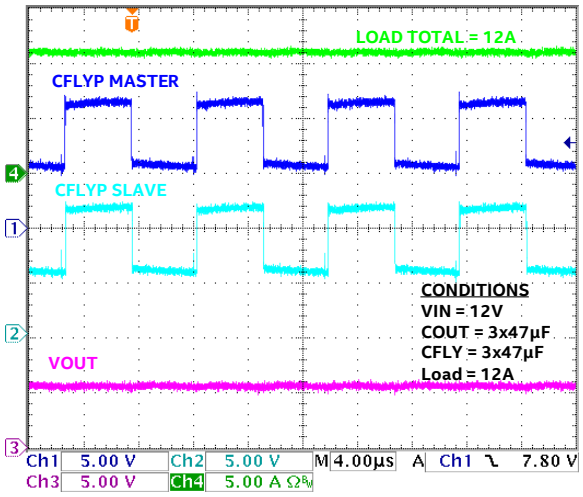
Parallel Operation with Load = 12A



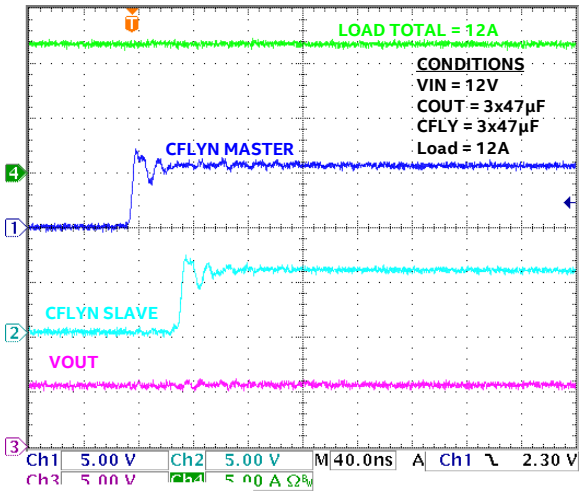
Parallel Operation CFLYN Waveform



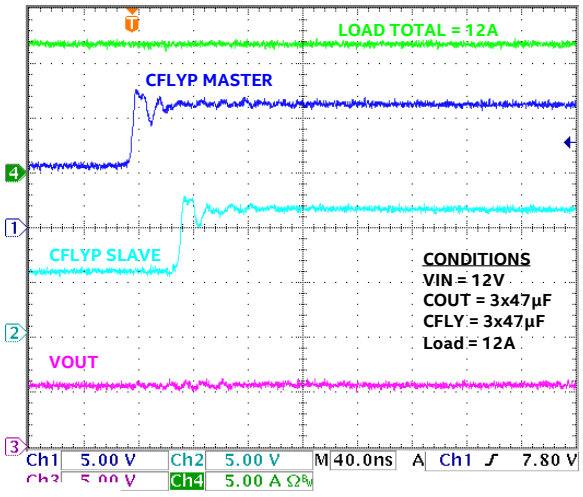
Parallel Operation CFLYP Waveform



Parallel Operation CFLYN Delay



Parallel Operation CFLYP Delay



FUNCTIONAL BLOCK DIAGRAM

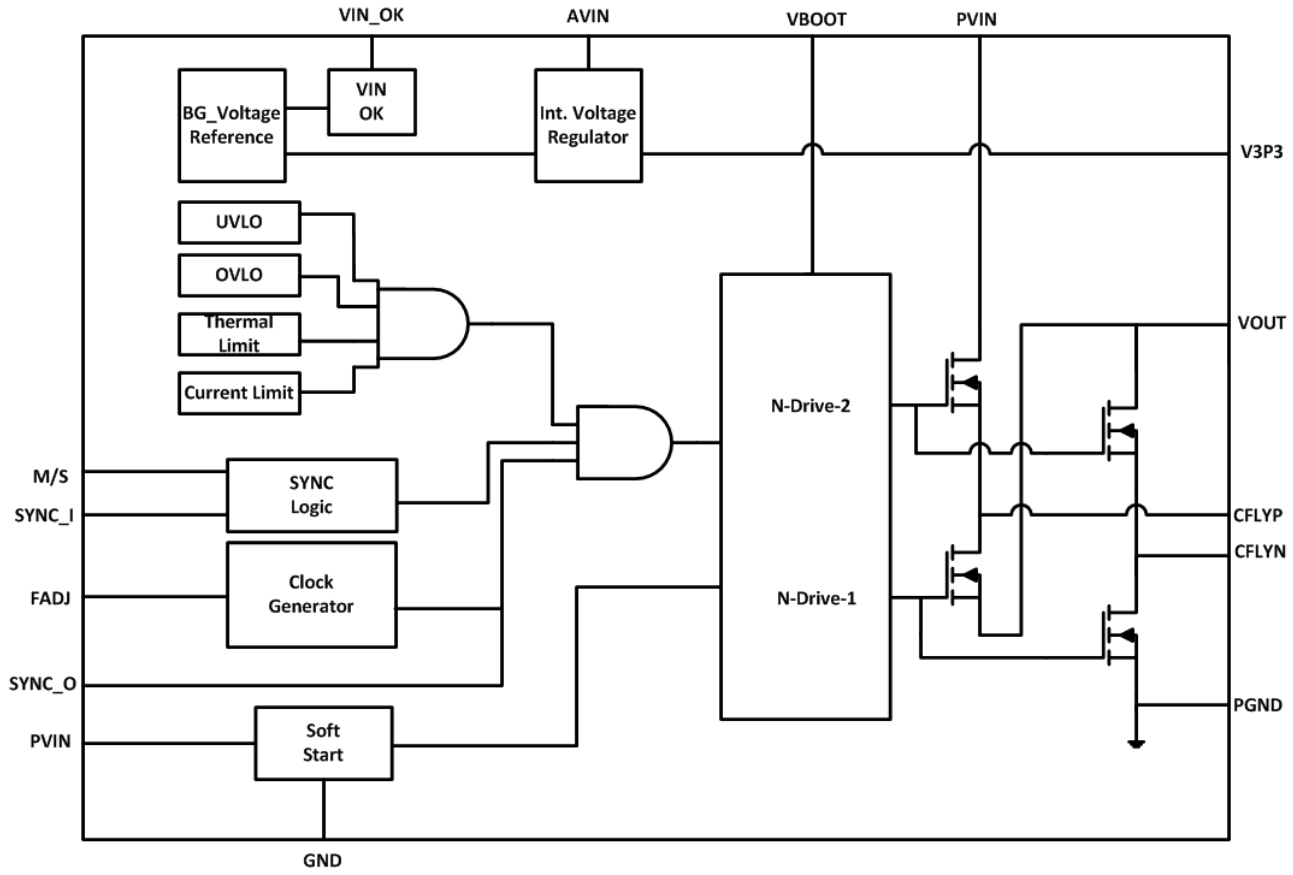


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Bus Voltage Divider

The EC2650QI is an open loop bus voltage divider. It generates an output voltage which is approximately half the input voltage value. The device uses switched capacitors to divide the input voltage by a factor of 2. External capacitors are charged in series during one half of a clock cycle and the capacitors are then connected in parallel during the second half of the clock cycle. The output voltage depends on the input voltage and the load current. The EC2650QI will divide the input voltage by 2 at very high efficiency up to 6A. It can also be paralleled together with other EC2650QI devices to support higher currents (4 devices can parallel to support up to 24A). This device has been designed specifically for use with Intel Enpirion point-of-load products for output voltage regulation.

The Voltage Divider has the following features:

- Output voltage soft-start
- Over-current and short circuit protection
- Thermal shutdown with hysteresis
- Input under-voltage lockout
- VIN_OK indicator signal
- Parallel operation with 2 or more devices to support higher currents

Theory of Operation

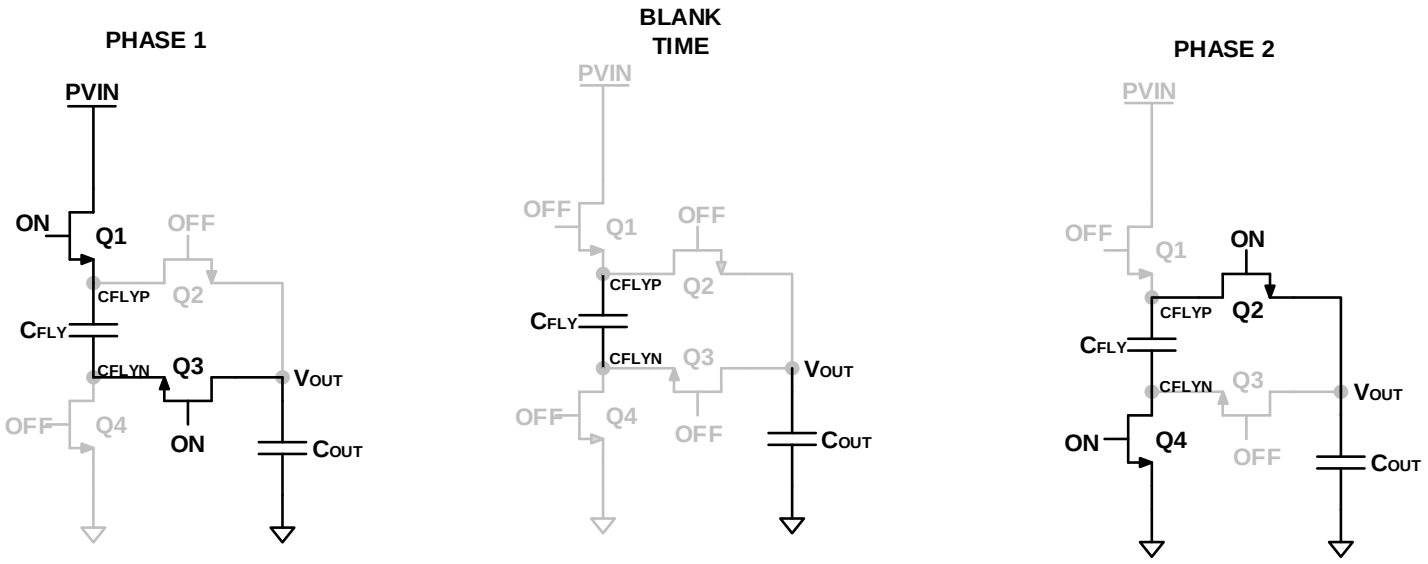


Figure 5: Operational Switching Scheme

The EC2650 uses external capacitors C_{FLY} and C_{OUT} to divide down the input voltage by alternately switching Q1 and Q3, then Q2 and Q4. This alternately configures C_{OUT} and C_{FLY} between series and in parallel connections. The switches Q1 and Q3 are closed during the first phase of each cycle arranging the capacitors in series. A blank time is then asserted to ensure no cross conduction happens. During the second phase, Q2 and Q4 are closed and the capacitors are configured in parallel, thus disconnecting from the input. By connecting the CFLY and COUT capacitors in series and then in parallel at 50% duty cycle, the output voltage will be 50% of the input voltage (at no load).

Soft-Start Operation

Soft start is a means to reduce the in-rush current when the device is enabled. When the device is enabled by ramping up the input voltage, and the output capacitors are discharged, a large current flow is averted by modulating the gate drive of the NFET during the soft-start interval. This interval is pre-programmed and not user programmable. Once enabled, the device will achieve its nominal output voltage in around 3.2ms.

Over-Current Protection

The over-current function is achieved by sensing the output voltage with respect to its input voltage. Due to inherent output impedance (R_{OUT} ~ 70mΩ), the output voltage is a function of the input voltage and the output current. As output current increases, the output voltage will decrease. An over-current state is entered when the device is out of soft-start and the output voltage drops below ~90% of the expected voltage ($V_{OUT_EXPECTED}$ = 0.5V_{IN}). The expected current limit is around 8.5A.

$$V_{OUT_OCP} = 0.9V_{OUT_EXPECTED} = 0.45V_{IN}$$

The controller will disable switching during this over-current state and then initiate a fresh soft-start. The device will continue cycling through soft-start as long as the over-current or short circuit condition exists. Proper layout and decoupling should be followed to ensure output current limit is within specifications in the Electrical Characteristics table. Figure 6 shows the simplified over-current protection circuit.

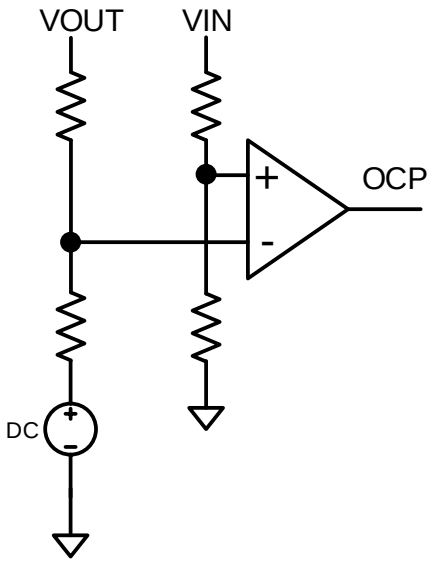


Figure 6: OCP Detection Circuit

Thermal Shutdown Protection

Thermal shutdown will disable operation when the junction temperature exceeds 160°C. Once the junction temperature drops by its hysteresis of 20°C, the converter will re-start with a normal soft-start. This ensures protection for the device in case of elevated temperature levels. Note that operating at temperature levels higher than its maximum operating range may reduce reliability of the device and is not recommended.

Input Under-Voltage Lock-Out (UVLO)

When the device's input voltage falls below UVLO, switching is disabled to prevent operation at insufficient voltage levels. During startup, the UVLO circuit ensures that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis and input de-glitch circuits are incorporated in order to ensure high noise immunity and prevent a false trigger in the UVLO voltage region.

Input Power OK Flag (VIN_OK)

The VIN_OK is an open drain signal to indicate that the input voltage is sufficient for operation. VIN_OK may be tied high to the 3.3V voltage rail (V3P3) of the device or tied to other external rails through a 100k resistor. VIN_OK is asserted high when the rising input voltage reaches approximately 8V.

Parallel Operation (Master/Slave)

The EC2650QI may be paralleled together to support higher output currents. For parallel operation, the device may be configured to Master Mode or Slave Mode by pulling the M/S pin low (Master) or high (Slave). In Master mode, the internal switching frequency of the Master device is output through the SYNC_O pin, which can be connected to the SYNC_I pin(s) of other Slave device(s). The Master's clock signal is used to synchronize the gate drives of other EC2650QI devices for parallel operation. Slaves do not have an output signal on their SYNC_O pin(s). There is no limit to how many EC2650QI may be used in parallel, but since the devices do not actively current balance, the current distribution depends on board layout. Some devices will incur higher or lower current depending on trace impedance. Due to this restriction, careful attention would need to be paid when using more than 4 devices in parallel operation.

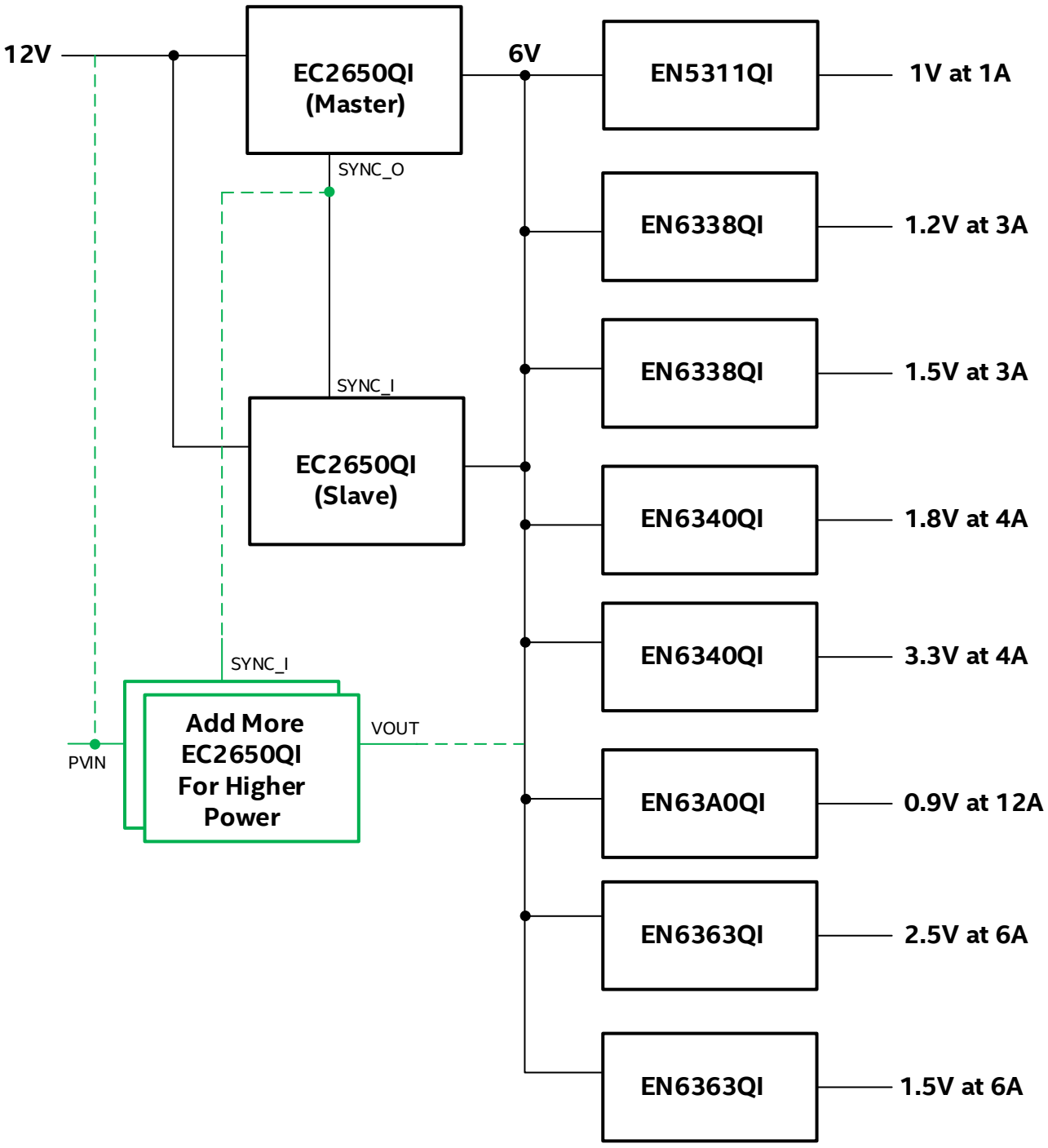


Figure 7: $12V_{IN}$ Parallel Operation with 66W Capability

(Up to 132W when using 4 devices)

EMI Performance

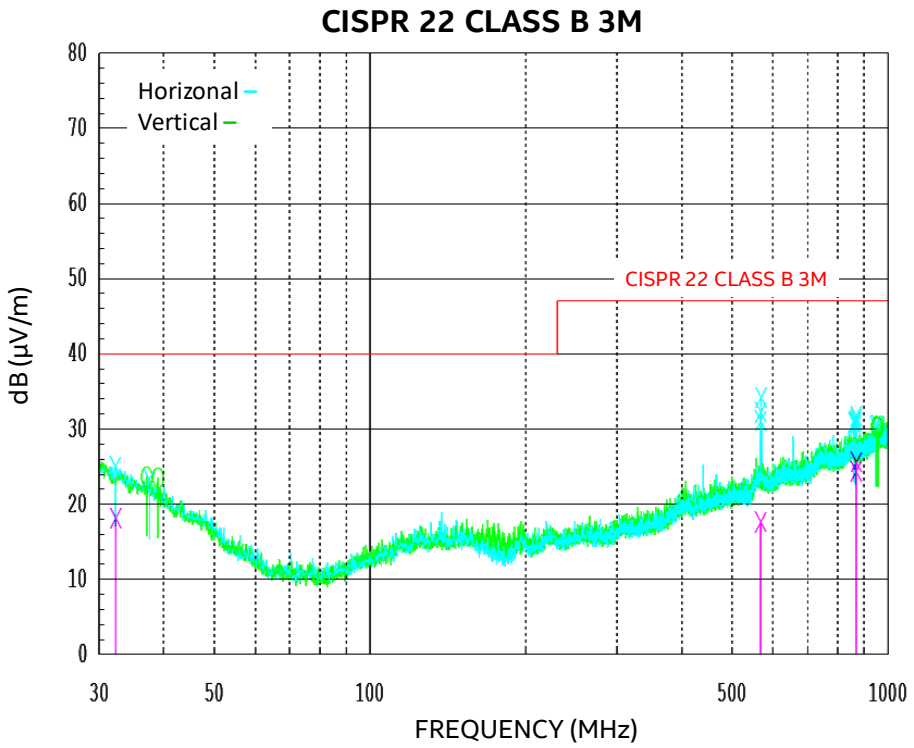


Figure 8: Output Voltage vs. Output Current

Due to changing voltage signals within switching voltage converters, electromagnetic interference (EMI) may cause interference to other circuits in a system. As a result, the EMI performance should be measured. The EC2650QI EMI performance graph is compared to the CISPR 22 Class B 3M specification in Figure 8. Due to edge softening switching technology within the EC2650QI, voltage over-shoots are minimized. As a result, the EMI performance is well within the specification of CISPR 22 Class B at 3 meters.

APPLICATION INFORMATION

Output Voltage Regulation

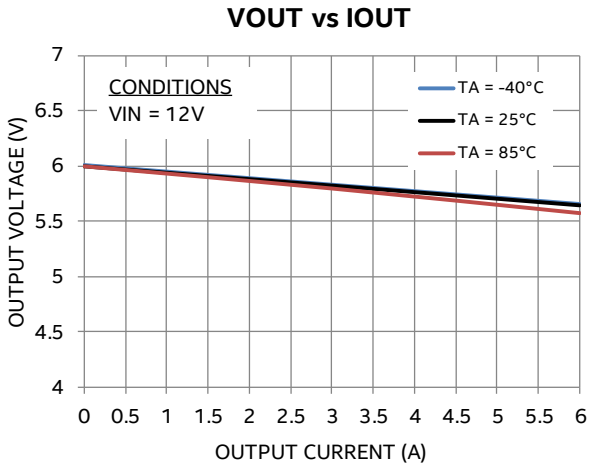


Figure 9: Output Voltage vs. Output Current

The output voltage is a function of the input voltage and output current. The device has an inherent output impedance of (R_{OUT} ~ 70mΩ). As output current increases, the output voltage will decrease. Since the impedance increases with temperature, the output voltage drop at higher temperatures will be higher than at lower temperatures. The EC2650QI has a fixed duty cycle of 50%.

$$V_{OUT_EXPECTED} = 0.5V_{IN} – I_{OUT} \times R_{OUT}$$

Frequency Adjustment

The device is optimized to run at 100 kHz switching frequency (with R_{FADJ}= 130 kΩ) independent of load current. The internal oscillator frequency can be adjusted by altering the value of the resistor between the FADJ pin and AGND (see chart below). Higher switching frequency can reduce output ripple at the cost of lower efficiency. Since current limit is based on output voltage level, the current limit will increase slightly with higher switching frequency, due to lower output ripple.

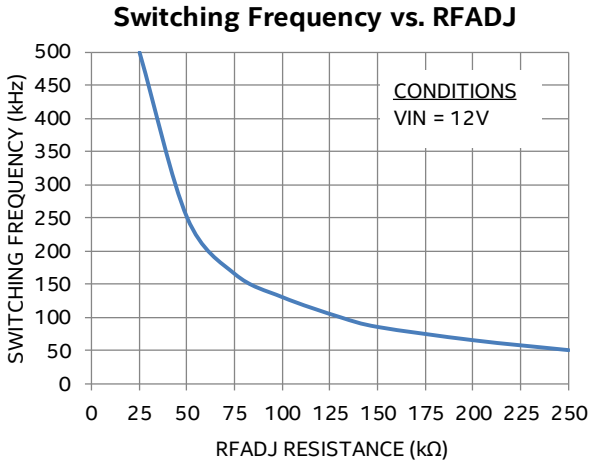


Figure 10. Recommended R_{FADJ} vs. Switching Frequency

Input Capacitor Selection

The input of EC2650QI voltage divider can be noisy and should be decoupled properly in order to reduce switching voltage ripple. In addition, input parasitic line inductance can attribute to higher input voltage ripple. The EC2650QI requires a minimum of 3 x 22µF 0805 input capacitors. As the distance of the input power source to the input of the EC2650QI is increased, it is recommended to increase input capacitance in order to mitigate the line inductance from the source. Input bulk capacitors, such as electrolytic or tantalum, has significant capacitance for their size and will help reduce system level noise. For applications where the input power source is far away, bulk capacitors should be in consideration. Low-ESR ceramic capacitors should be used near the input pin. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. In general, larger case size offers higher effective capacitance over the same DC bias. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger capacitors in order to provide high frequency decoupling. Larger electrolytic or tantalum bulk capacitors may be used in conjunction to increase total input capacitance but should not be used solely as a replacement for the ceramic capacitors.

Table 1: Recommended Input Capacitors

DESCRIPTION	MFG	P/N
22µF ±20%, 16V X5R, 0805	Taiyo Yuden	EMK212BBJ226MG-T
	Murata	GRM21BR61C226ME44
	TDK	C2012X5R1C226M
22µF ±20%, 16V X5R, 1206	Taiyo Yuden	EMK316ABJ226MD-T
	Murata	GRM31CR61C226ME15
	TDK	C3216JB1C226M160AB

Output Capacitor Selection

The output ripple of the EC2650QI voltage divider can be attributed to its switching frequency and output decoupling. The lower the frequency, the higher the output ripple and the higher the output capacitance, the lower the output ripple. The EC2650QI requires a minimum of 3 x 47µF/10V 0805 output capacitors. Additional output capacitance will reduce output ripple; however, excessive output capacitance may cause the current limit protection to activate during soft-start operation. It is recommended to keep the total output capacitance under 600µF. Low ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. In general, larger case size offers higher effective capacitance over the same DC bias. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

Table 2: Recommended Output Capacitors

DESCRIPTION	MFG	P/N
47µF ±20%, 10V, X5R, 0805	Taiyo Yuden	LMK212BBJ476MG-T
	Murata	GRM21BR61A476ME15
47µF ±20%, 10V, X5R, 1206	Taiyo Yuden	LMK316ABJ476ML-T
	Murata	GRM31CR61A476ME15
	TDK	C3216X5R1A476M160AB

CFLY Capacitor Selection

The CFLY capacitors are placed between the CFLYP and CFLYN pins. The EC2650QI requires a minimum of 3 x 47µF/10V 0805 output capacitors. Low ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. In general, larger case size offers higher effective capacitance over the same DC bias. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

Table 3: Recommended CFLY Capacitors

DESCRIPTION	MFG	P/N
47µF ±20%, 10V, X5R, 0805	Taiyo Yuden	LMK212BBJ476MG-T
	Murata	GRM21BR61A476ME15
47µF ±20%, 10V, X5R, 1206	Taiyo Yuden	LMK316ABJ476ML-T
	Murata	GRM31CR61A476ME15
	TDK	C3216X5R1A476M160AB

THERMAL CONSIDERATIONS

Thermal considerations are important elements of power supply design. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be taken into account. The Intel Enpirion PowerSoC technology helps alleviate some of those concerns.

The EC2650QI DC-DC converter is packaged in a 5.5mm x 5.5mm x 0.9mm 36-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 160°C.

The following example and calculations illustrate the thermal performance of the EC2650QI with the following parameters:

V_{IN} = 12V

V_{OUT} = 6V (drops to ~5.5V at I_{OUT} = 6A)

I_{OUT} = 6A

First, calculate the output power.

$P_{OUT} = V_{OUT} \times I_{OUT} = 5.5V \times 6A = 33W$

Next, determine the input power based on the efficiency (η) shown in Figure 11.

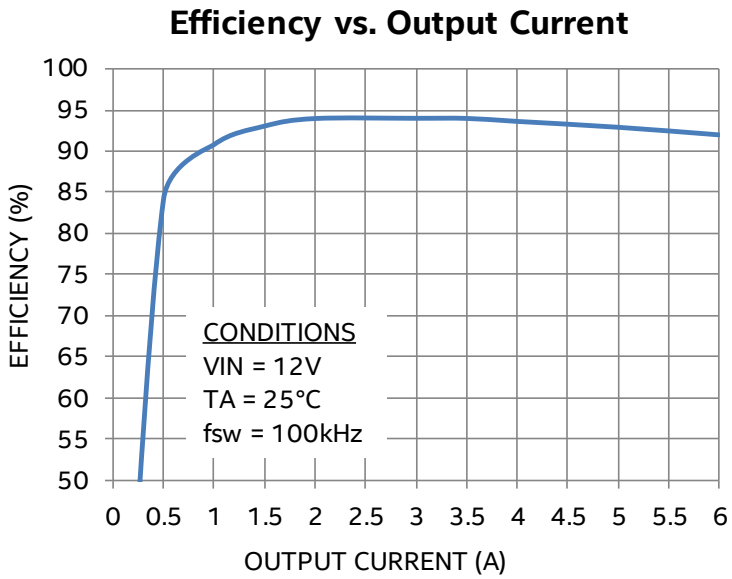


Figure 11: Efficiency vs. Output Current

For V_{IN} = 12V, V_{OUT} = 5.5V at 6A, η ≈ 92%

$\eta = P_{OUT} / P_{IN}$ = 92% = 0.92

$P_{IN} = P_{OUT} / \eta$

$P_{IN} \approx 33W / 0.92 \approx 35.9W$

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

$P_D = P_{IN} – P_{OUT}$

$= 35.9W – 33W \approx 2.9W$

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EC2650QI has a θ_{JA} value of 11°C/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

$\Delta T = P_D \times \theta_{JA}$

$\Delta T \approx 2.9W \times 11°C/W \approx 31.9°C$

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$T_J = T_A + \Delta T$

$T_J \approx 25°C + 31.9°C \approx 56.9°C$

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

$T_{AMAX} = T_{JMAX} – P_D \times \theta_{JA}$

$\approx 125°C – 31.9°C \approx 93.1°C$

The maximum ambient temperature the device can reach is 93°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

APPLICATION CIRCUIT

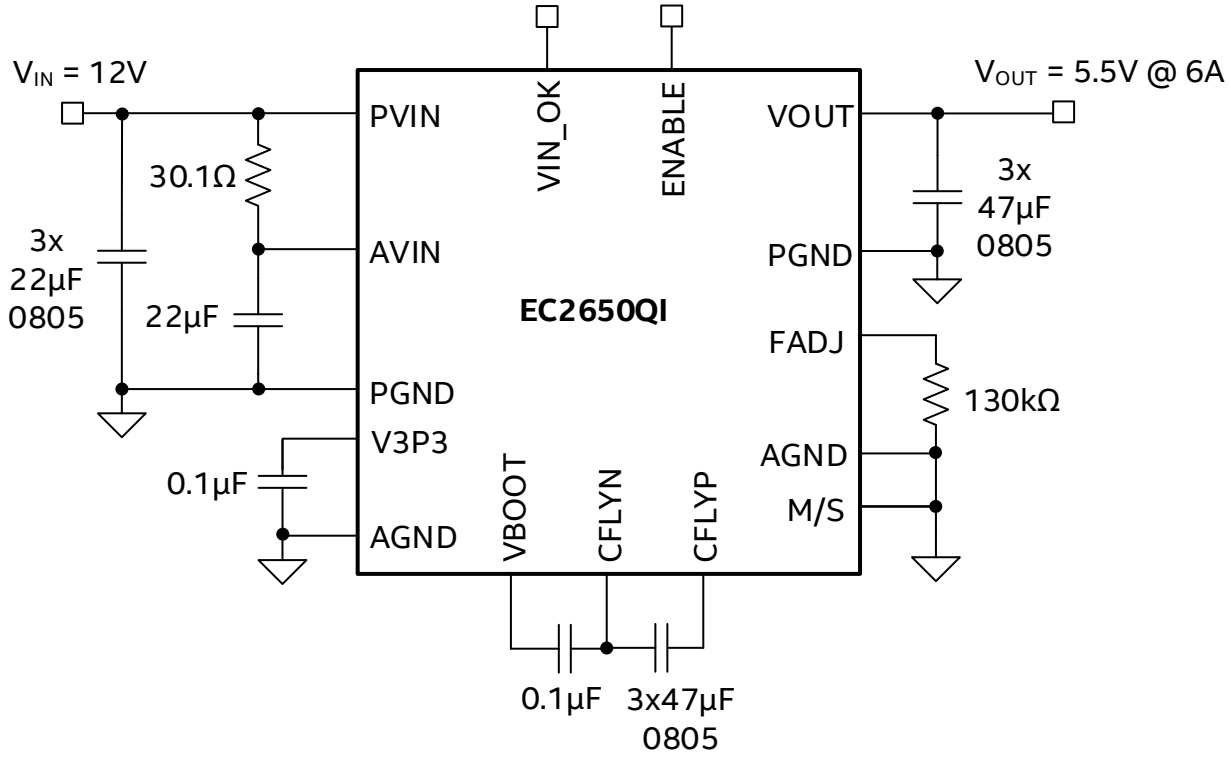


Figure 12: Typical Standalone Application Circuit (~33W, 5.5V_{OUT} @ 6A)

APPLICATION CIRCUIT

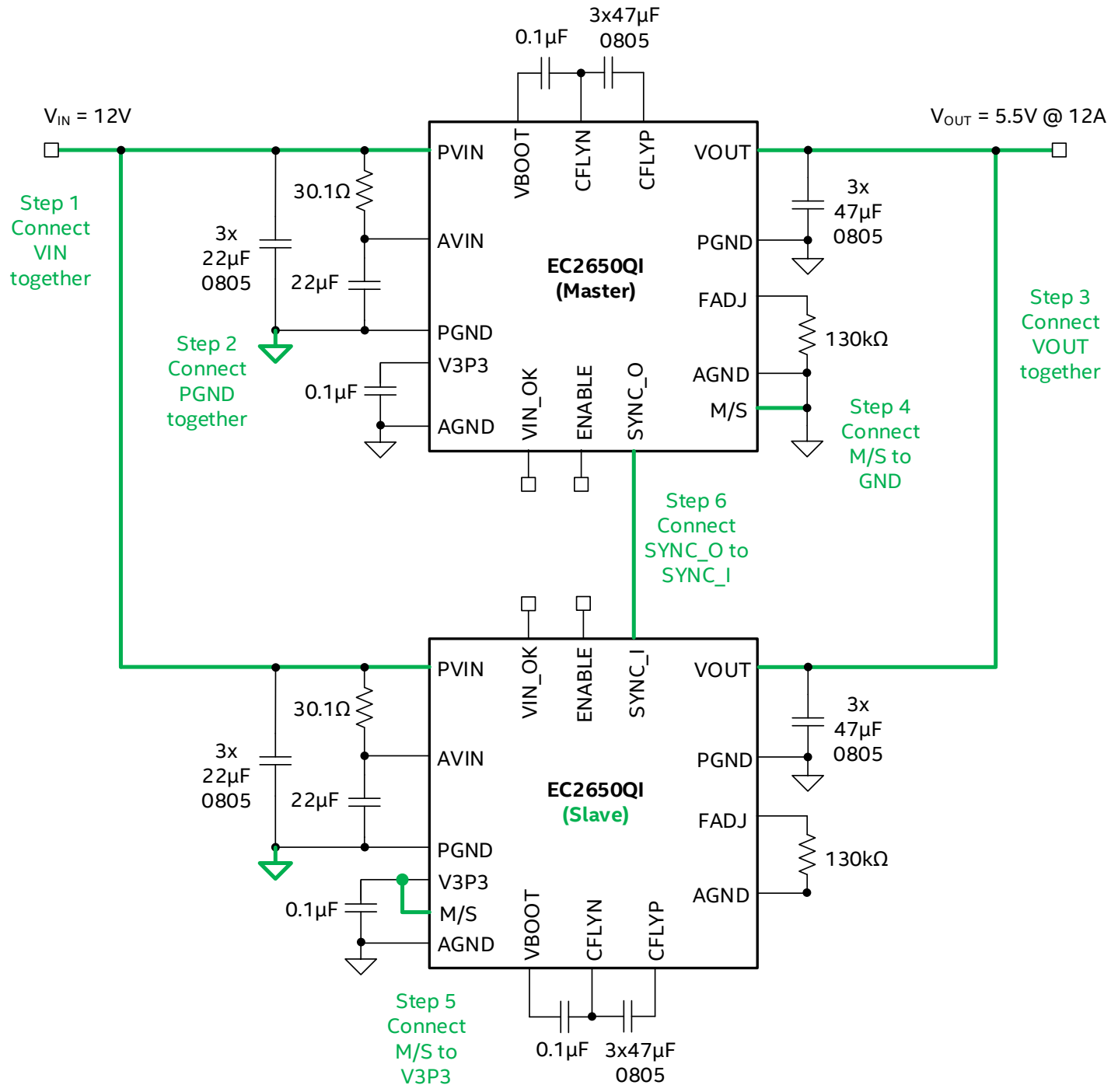


Figure 13: Parallel Operation Typical Circuit (~66W, 5.5V$_{OUT}$ @ 12A)

LAYOUT RECOMMENDATIONS

Figure 14 shows critical components and layer 1 traces of a recommended minimum footprint EC2650QI layout. ENABLE and other small signal pins need to be connected and routed according to specific customer application. Visit the Enpirion Power Solutions website at www.intel.com/enpirion for more information regarding layout. Please refer to this Figure 14 while reading the layout recommendations in this section.

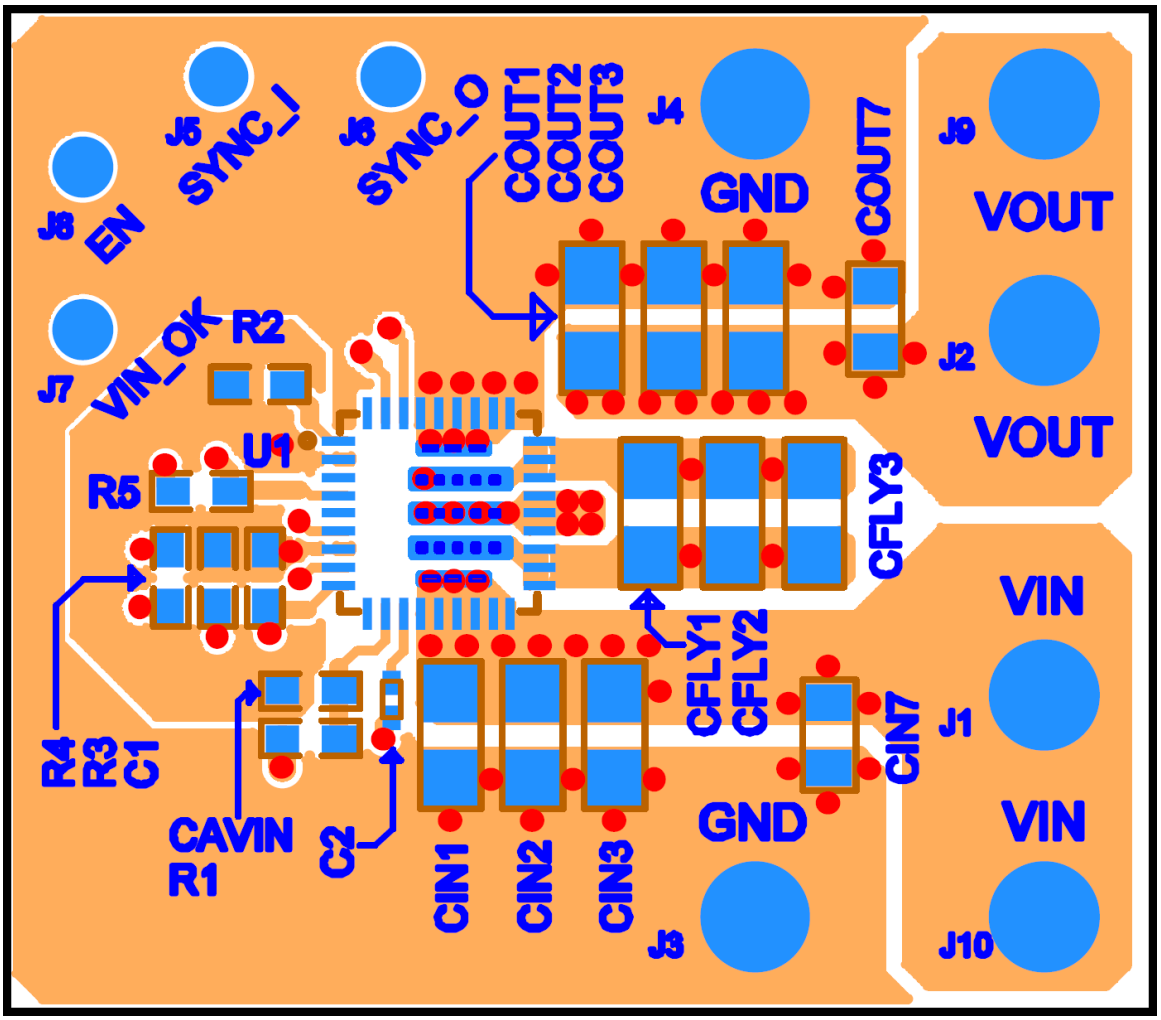


Figure 14: Top PCB Layer Critical Components and Copper for Minimum Footprint (Top View)

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EC2650QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EC2650QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to be wide traces and filled with vias to the 2nd layer ground plane. This ensures lowest impedance possible between input and output ground.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 4: The large pads (PGND, CFLYN, VOUT, CFLYP, PVIN) underneath the component should be connected to their respective pins with as many vias as possible. In order to reduce excessive solder from bridging between the large pads, follow the stencil size as shown by the blue boxes inside the large pads in Figure 14. The large pads provides lower impedance from inside the package to the outside connections as well as help with power dissipation due to the amount of metal present.

Recommendation 5: As shown in Figure 14, VOUT is brought out from its pins on another layer. Be sure that the connection from VOUT pin to the output caps is as thick and wide as possible in order to reduce resistance.

Recommendation 6: As shown in Figure 14, the input ground is connected to the PGND pins through the 2nd layer ground plane with as many vias as possible. This ensures that the input and output ground connections have as low resistance as possible while also minimizing the total solution layout.

Recommendation 7: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 14, this connection is made at the input capacitor furthest away from the PVIN pins. The AVIN also has a RC filter (30.1Ω and 10µF) close to its pin.

Recommendation 8: Follow all the layout recommendations as close as possible to optimize performance. Not following layout recommendations can complicate designs and create anomalies different than the expected operation of the product.

DESIGN CONSIDERATIONS FOR LEAD-FRAME BASED MODULES

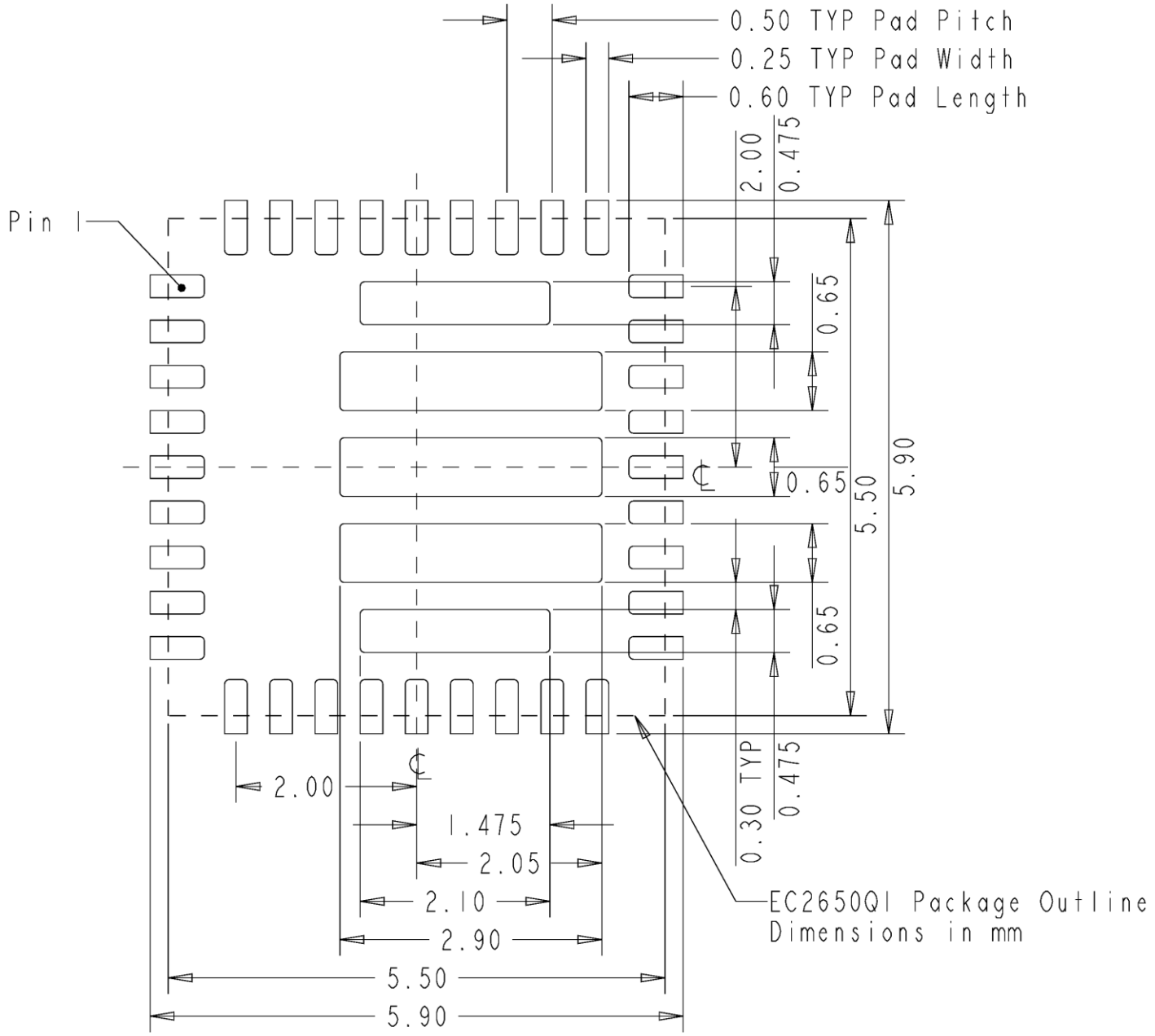


Figure 15: Landing Pattern with Solder Stencil (Top View)

The solder stencil aperture for the thermal PGND pad is shown in Figure 15 and is based on Enpirion power product manufacturing specifications.

PACKAGE DIMENSIONS

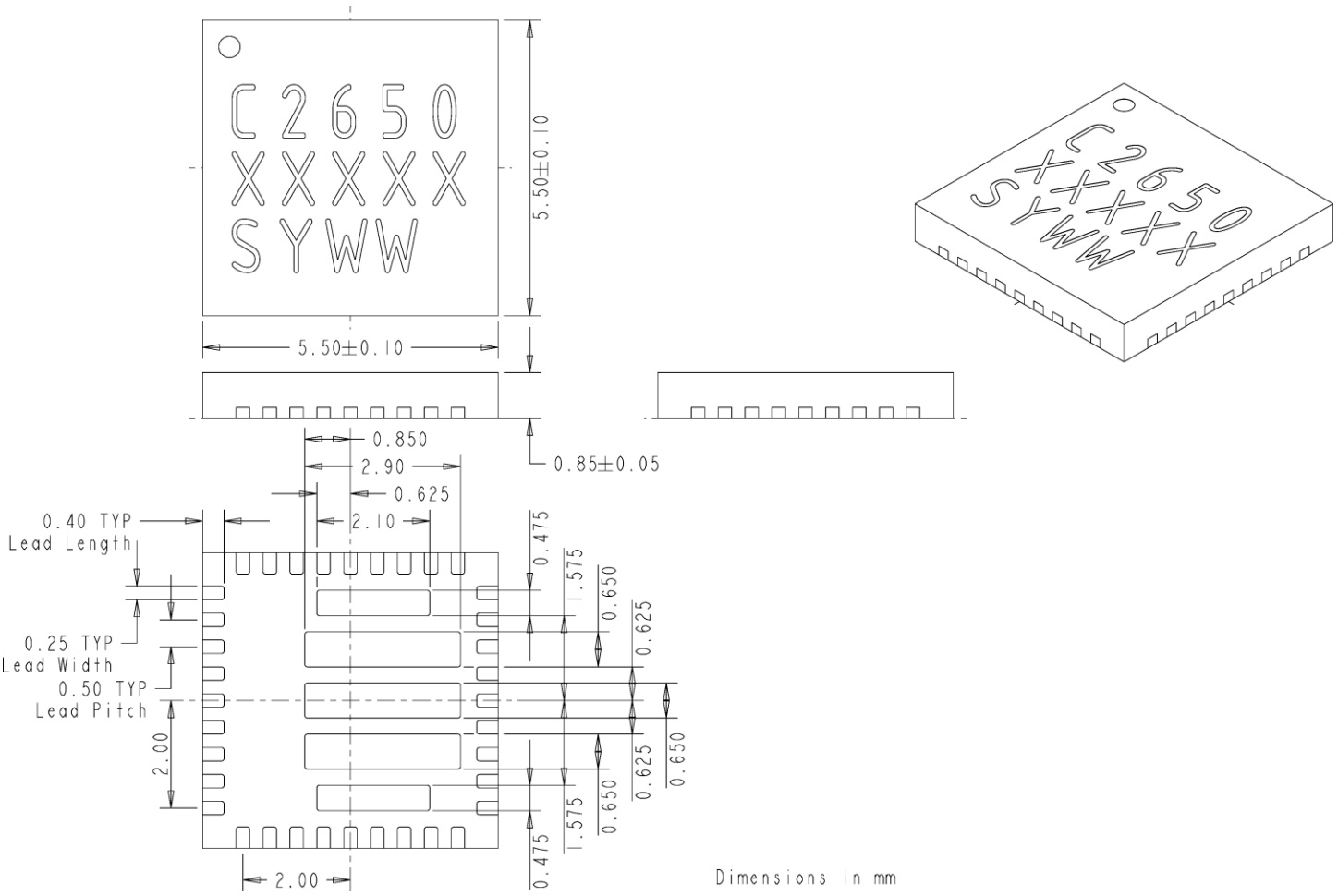


Figure 16: EC2650QI Package Dimensions

Packing and Marking Information:

https://www.intel.com/content/www/us/en/programmable/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
A	March, 2019	Initial Datasheet

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

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