EP5368QI 600mA PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EP5368QI is a synchronous buck converter with integrated Inductor, PWM controller, MOSFETS, and Compensation providing the smallest possible solution size. The EP5368QI requires only two small MLCC capacitors to make a complete solution. Integration of the inductor greatly simplifies design, contains noise, reduces part count, and reduces solution footprint. Low output ripple ensures compatibility with RF systems.

The EP5368QI operates at a switching frequency of 4 MHz, enabling this unprecedented level of integration and small external components. Type III voltage mode control is used to provide high noise immunity and wide control loop bandwidth. The device can source 600mA of current over the industrial temperature range and up to 700mA over the commercial temperature range.

The small footprint makes this part ideal for space constrained applications. Output voltage is programmed via a 3-pin VID selector providing seven pre-programmed output voltages along with an option for external resistor divider.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

FEATURES

- Integrated Inductor
- 3mm x 3mm x 1.1mm QFN package
- Only two low cost MLCC caps required
- 4 MHz switching frequency
- High efficiency, up to 94%
- Up to 700mA continuous output current
- Wide 2.4V to 5.5V input range
- V_{OUT} Range 0.603V to V_{IN} – 0.4V
- 100% duty cycle capable
- Less than 1 µA standby current
- Low V_{OUT} ripple for RF compatibility
- Short circuit and over current protection
- UVLO and thermal protection
- Stable over entire operating range
- RoHS compliant; MSL 3 260°C reflow

APPLICATIONS

- Noise sensitive RF applications
- Area constrained applications
- Smart phones and PDAs
- Personal Media Players
- Advanced Mobile Processors, DSP, IO, Memory, Video, Multimedia Engines

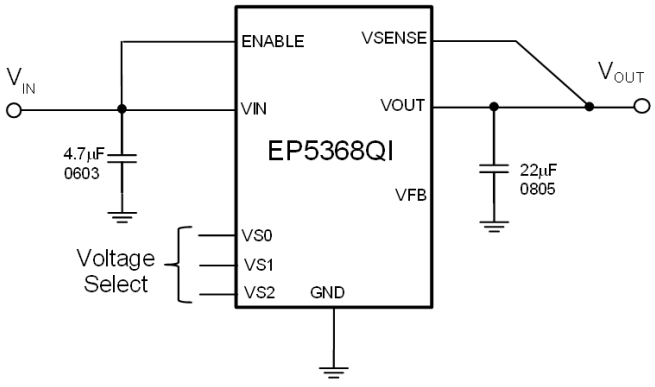


Figure 1. Typical Application Schematic

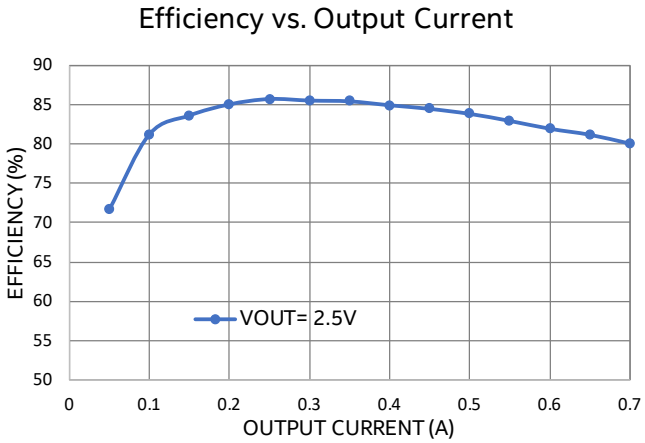


Figure 2. Efficincy at V_{IN} =5V

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EP5368QI	AAXX	-40°C to +125°C	16-pin (3mm x 3mm x 1.1mm) QFN
EP5368QI-E		QFN Evaluation Board	

Packing and Marking Information: https://www.Intel.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

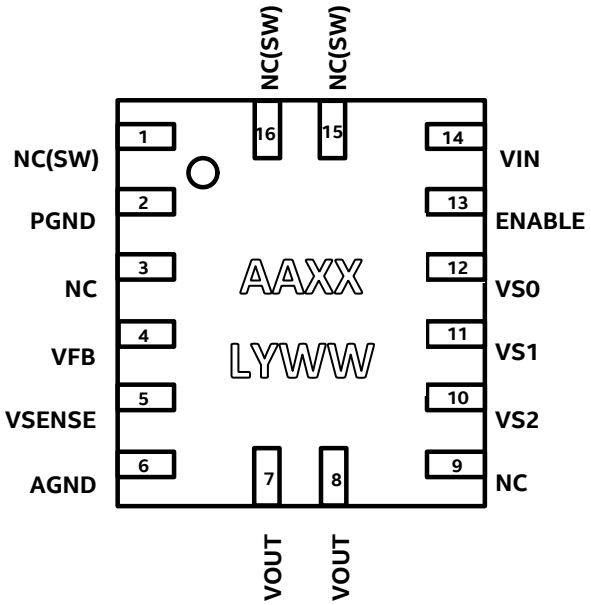


Figure 3. EP5368QI Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1, 15, 16	NC(SW)	-	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. NC (SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage to the device.
2	PGND	Ground	Power ground. Connect this pin to the ground electrode of the Input and output filter capacitors.
3, 9	NC	-	NO CONNECT - These pins are not electrically connected internally. They may be connected to ground externally if necessary to increase trace width in layout. These pins must be soldered to the PCB.
4	VFB	Analog	Feedback pin for external divider option. When using the external divider option (VS0=VS1=VS2= high) connect this pin to the center of the external divider. Set the divider such that VFB = 0.603V. The “ground” side of the external divider should be connected to AGND. This pin may be left unconnected when using VID mode.
5	VSENSE	Analog	Sense pin for preset output voltages. Connect to the output capacitor. Must be left unconnected when operating at 700mA load current. (Refer to section on operation at 700mA output current for more detail.)
6	AGND	Power	Analog ground. This is the quiet ground for the internal control circuitry
7, 8	VOUT	Power	Regulated Output Voltage.
10, 11, 12	VS2, VS1, VS0	Analog	Output voltage select. VS2=pin10, VS1=pin11, VS0=pin12. Selects one of seven preset output voltages or choose external divider by connecting pins to logic high or low. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate. (Refer to section on output voltage select for more detail.)
13	ENABLE	Analog	Output enable: Enable = logic high, disable = logic low. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate.
14	VIN	Power	Input voltage pin. Supplies power to the IC.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.3	7.0	V
ENABLE, V_{SENSE}, $V_{SO} – V_{S2}$		-0.3	V_{IN}+0.3	V
V_{FB}		-0.3	2.7	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Resistance: Junction to Ambient –0 LFM (1)	θ_{JA}	85	°C/W
Thermal Overload Trip Point	T_{J-TP}	+150	°C
Thermal Overload Trip Point Hysteresis		15	°C

(1) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.6V

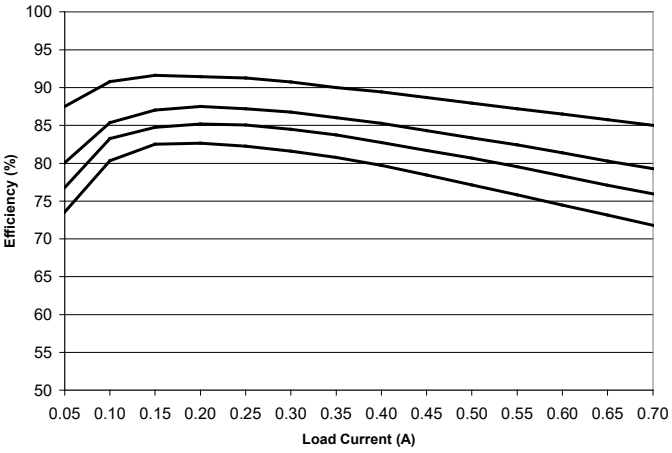
C_{IN} = 4.7µF 0603 MLCC, C_{OUT} = 22µF 0805 MLCC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Under Voltage Lock-Out – V_{IN} Rising	V_{UVLOR}			2.2	2.3	V
Under Voltage Lock-Out – V_{IN} Falling	V_{UVLOF}			2.1	2.2	V
Drop Out Resistance	R_{DO}	Input to Output Resistance in 100% duty cycle operation.		400	500	mΩ
Output Voltage Range[2]	V_{OUT}	External Feedback Mode VID Mode	0.603 0.8		V_{IN}-V_{DO} 3.3	V
Dynamic Voltage Slew Rate (VID Change)	V_{SLEW}		0.975	1.5	2.025	V/ms
V_{OUT} Initial Accuracy (VID Preset Mode)	$\Delta V_{OUT_INITIAL}$	T_A = 25°C, V_{IN} = 3.6V; I_{LOAD} = 100mA ; 0.8V ≤ V_{OUT} ≤ 3.3V	-2		+2	%
V_{OUT} Accuracy (VID Preset Mode) over line, load and temperature variation	ΔV_{OUT_ALL}	-40°C ≤ T_A ≤ +85°C 2.4V ≤ V_{IN} ≤ 5.5V; 0.8V ≤ V_{OUT} ≤ 3.3V 0A ≤ I_{LOAD} ≤ 700A	-3		+3	%
Feedback Pin Voltage Initial Accuracy	$\Delta V_{FB_INITIAL}$	T_A = 25°C, V_{IN} = 3.6V; I_{LOAD} = 100mA ; 0.8V ≤ V_{OUT} ≤ 3.3V	0.591	0.603	0.615	V
Feedback Pin Voltage Accuracy over line, load, and temperature variations	ΔV_{FB_ALL}	-40°C ≤ T_A ≤ +85°C 2.4V ≤ V_{IN} ≤ 5.5V; 0.8V ≤ V_{OUT} ≤ 3.3V 0A ≤ I_{LOAD} ≤ 700A	0.585	0.603	0.621	V
Feedback Pin Input Current	I_{FB}				100	nA

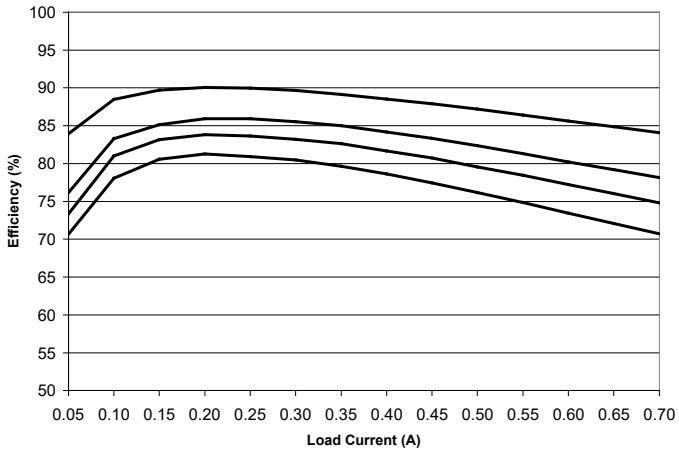
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Output Current	I_{OUT}	V_{IN} = 5V, 0.603V <V_{OUT} < 3.3V, T_A = -40°C to +85°C	600			mA
Continuous Output Current	I_{OUT}	V_{IN} = 5V, 0.603V <V_{OUT} < 3.3V, T_A = -10°C to +85°C (Application Circuit Figure 6)	700			mA
Shut-Down Current	I_{SD}	Enable = Low		0.75		µA
PFET OCP Threshold	I_{ILM}	2.4V ≤V_{IN} ≤5.5V, 0.6V ≤ V_{IN} ≤ 3.3V	1.4	2		A
VS0-VS2, Enable Voltage Threshold	V_{TH}	Pin = Low Pin = High	0.0 1.4		0.4 V_{IN}	V
VS0-VS2 Pin Input Current	I_{VSX}			1		nA
Operating Frequency	F_{OSC}			4		MHz
Soft-Start Slew Rate	V_{SS}	VID programming mode	0.975	1.5	2.025	V/ms
V_{OUT} Rise Time	T_{SS}	VFB programming mode	0.784	1.2	1.628	ms

(2) $V_{DO} = I_{OUT} \times R_{DO}$

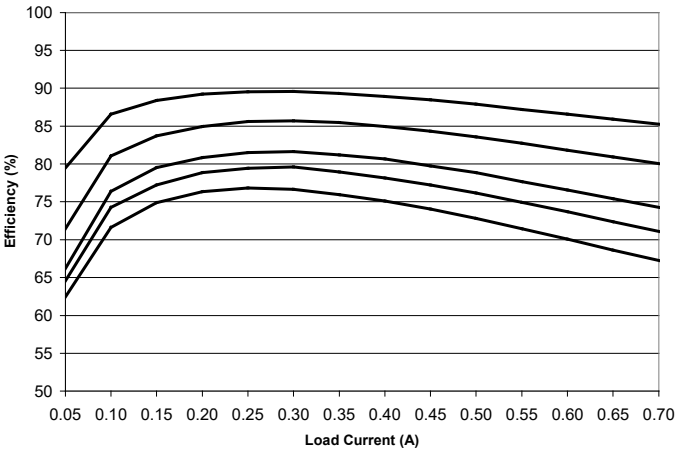
TYPICAL PERFORMANCE CURVES



Efficiency Versus Load; V_{IN} = 3.3V,
V_{OUT} (from top to bottom) 2.5V, 1.8V, 1.5V, 1.2V

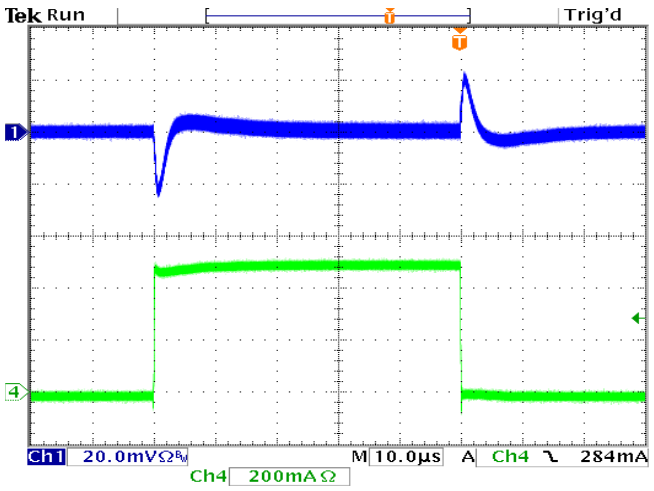


Efficiency Versus Load; V_{IN} = 3.7V,
V_{OUT} (from top to bottom) 2.5V, 1.8V, 1.5V, 1.2V

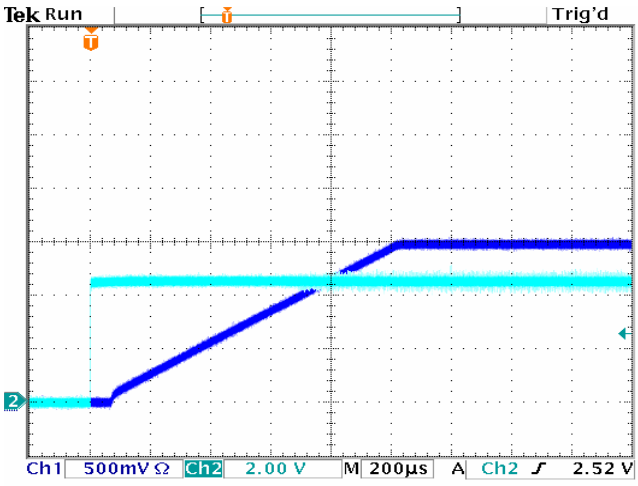


Efficiency Versus Load; V_{IN} = 5V,
V_{OUT} (from top to bottom) 3.3V, 2.5V, 1.8V, 1.5V, 1.2V

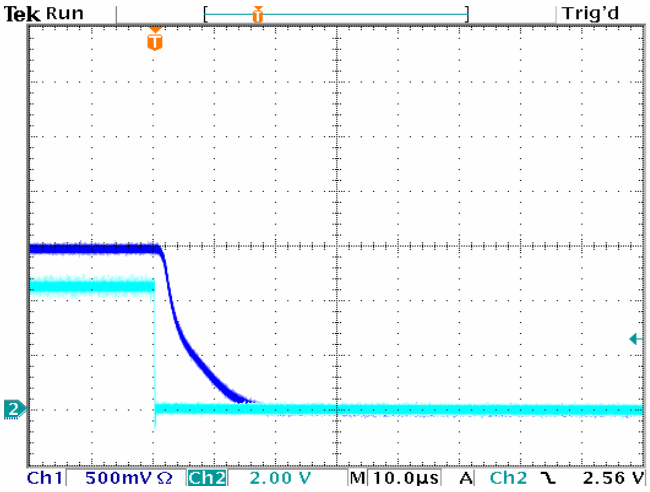
TYPICAL PERFORMANCE CHARACTERISTICS



Transient, V_{IN} = 3.6V, V_{OUT} = 1.2V, Load = 0-500mA

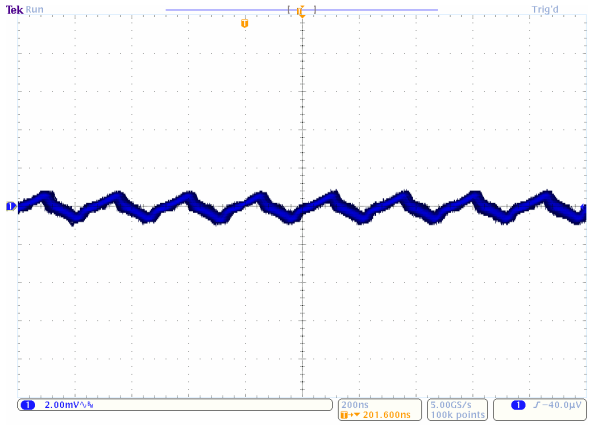


Startup, V_{IN} = 3.6V, V_{OUT} = 1.5V, Load = 500mA

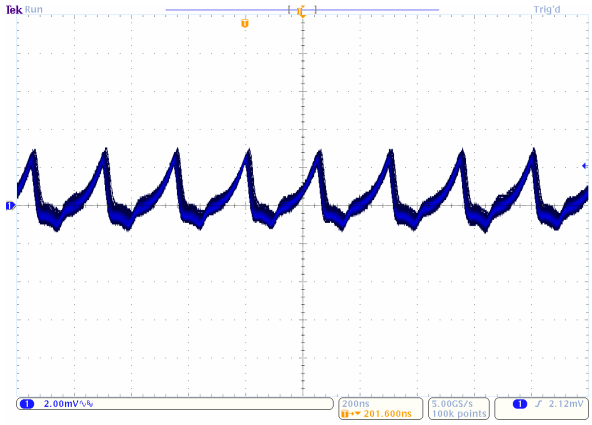


Shutdown, V_{IN} = 3.6V, V_{OUT} = 1.5V, Load = 500mA

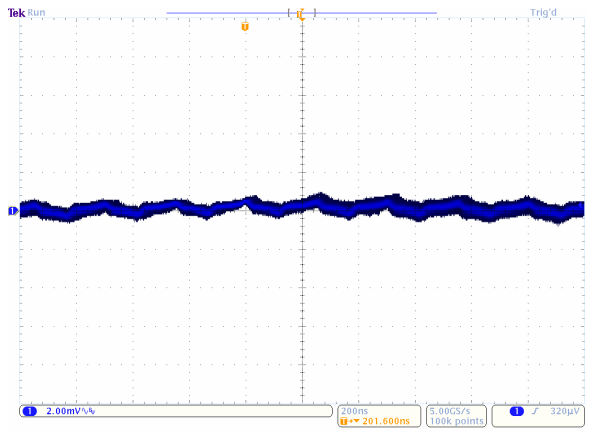
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



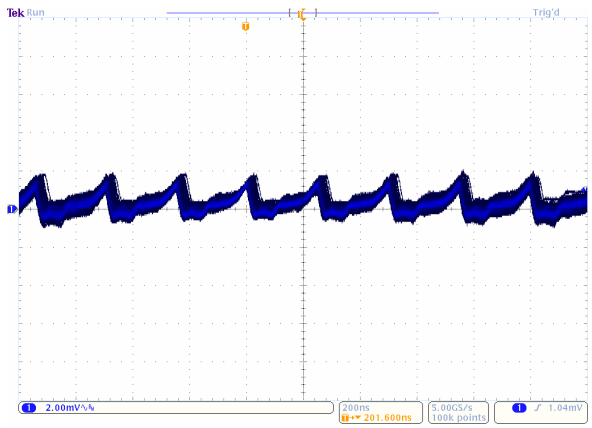
Voltage Ripple, V_{IN} = 3.3V, V_{OUT} = 1.8V, Load = 0mA C_{OUT} = 1x 22µF, 0805, 2.0mV/Div.



Voltage Ripple, V_{IN} = 3.3V, V_{OUT} = 1.8V, Load = 600mA C_{OUT} = 1x 22µF, 0805, 2.0mV/Div.



Voltage Ripple, V_{IN} = 3.3V, V_{OUT} = 1.8V, Load = 0mA C_{OUT} = 2x 10µF, 0805, 2.0mV/Div.



Voltage Ripple, V_{IN} = 3.3V, V_{OUT} = 1.8V, Load = 600mA C_{OUT} = 2x 10µF, 0805, 2.0mV/Div.

FUNCTIONAL BLOCK DIAGRAM

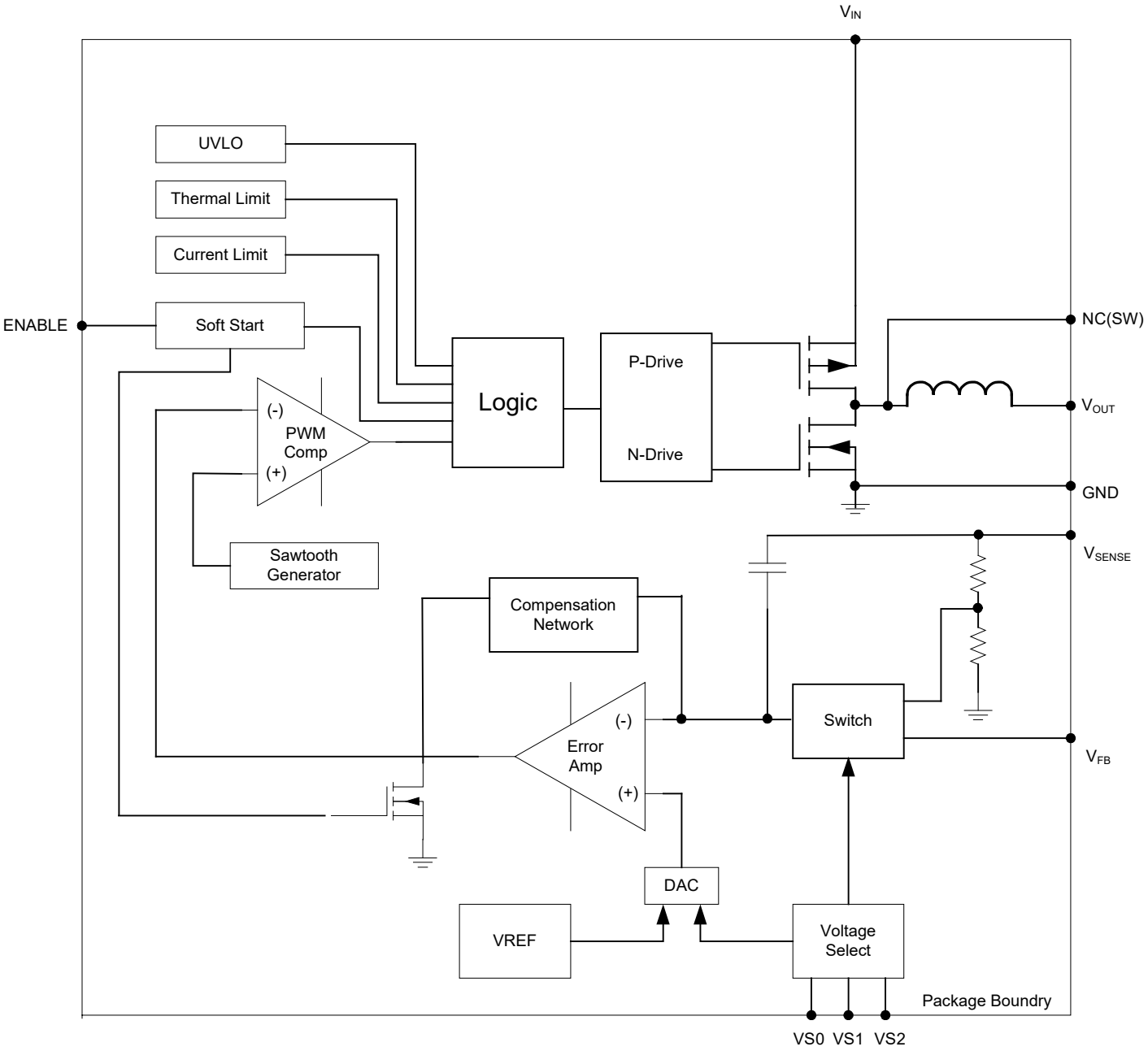


Figure 4. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EP5368QI is a complete DC-DC converter solution requiring only two low cost MLCC capacitors. MOSFET switches, PWM controller, Gate-drive, compensation, and inductor are integrated into the tiny 3mm x 3mm x 1.1mm package to provide the smallest footprint possible while maintaining high efficiency, low ripple, and high performance. The converter uses voltage mode control to provide the simplest implementation and high noise immunity. The device operates at a 4MHz switching frequency. The high switching frequency allows for a wide control loop bandwidth providing excellent transient performance. The high switching frequency further enables the use of very small components making possible this unprecedented level of integration.

Intel Enpirion's proprietary power MOSFET technology provides very low switching loss at frequencies of 4 MHz and higher, allowing for the use of very small internal components, and high performance. Integration of the magnetics virtually eliminates the design/layout issues normally associated with switch-mode DC-DC converters. All of this enables much easier and faster incorporation into various applications to meet demanding EMI requirements.

Output voltage is chosen from seven preset values via a three pin VID voltage select scheme. An external divider option enables the selection of any voltage in VIN to 0.603V range. This reduces the number of components that must be qualified and reduces inventory burden. The VID pins can be toggled on the fly to implement glitch free dynamic voltage scaling.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor

Intel has introduced the world's first product family featuring integrated inductors. The EP5368QI utilizes a proprietary low loss integrated inductor. The use of an internal inductor localizes the noises associated with the output loop currents. The inherent shielding and compact construction of the integrated inductor reduces the radiated noise that couples into the traces of the circuit board. Further, the package layout is optimized to reduce the electrical path length for the AC ripple currents that are a major source of radiated emissions from DC-DC converters. The integrated inductor significantly reduces parasitic effects that can harm loop stability, and makes layout very simple.

Stable Over Wide Range of Operating Conditions

The EP5368QI utilizes an internal type III compensation network and is designed to provide a high degree of stability over a wide range of operating conditions. The device operates over the entire input and output voltage range with no external modifications required. The very high switching frequency allows for a very wide control loop bandwidth.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EP5368QI has two soft start operating modes. When VOUT is programmed using a preset voltage in VID mode, the device has a constant slew rate. When the EP5368QI is configured in external resistor divider mode, the device has a constant VOUT ramp time. Output voltage slew rate and ramp time is given in the Electrical Characteristics Table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. Maximum allowable output capacitance depends on the device's minimum current limit, the output current at startup, the minimum soft-start time and the output voltage (all are listed in the Electrical Characteristics Table). The total maximum capacitance on the output rail is estimated by the equation below:

$C_{OUT_MAX} = 0.7 * (I_{LIMIT} - I_{OUT}) * t_{SS} / V_{OUT}$

C_{OUT_MAX} = maximum allowable output capacitance

I_{LIMIT} = minimum current limit = 0.8A

I_{OUT} = output current at startup

V_{OUT} = output voltage

0.7 = margin factor

$t_{SS(VFB)}$ = min soft-start time

= 0.784ms ← External feedback setting

$t_{SS(VID)} = V_{OUT}$ [V] / 2.025 [V/ms] ← VID setting

The soft-start time in VID setting is different than External Feedback (VFB) setting, so be sure to use the correct value when calculating the maximum allowable output capacitance.

NOTE: Do not use excessive output capacitance since it may affect device stability. The EP5368QI has high loop bandwidth and 80µF is all that is needed for transient response optimization.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for a period of 1ms and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat in a "hiccup" mode.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold, the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. In shutdown mode, the device quiescent current will be less than 1µA. At extremely cold conditions below -30°C, the controller may not be properly powered if ENABLE is tied directly to AVIN during startup. It is recommended to use an external RC circuit to delay the ENABLE voltage rise so that the internal controller has time to startup into regulation (see circuit below). The RC circuit may be adjusted so that AVIN and PVIN are above UVLO before ENABLE is high. The startup time will be delayed by the extra time it takes for the capacitor voltage to reach the ENABLE threshold.

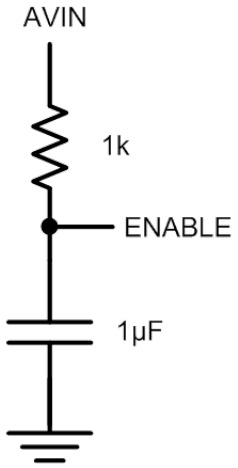


Figure 5. ENABLE Delay Circuit

NOTE: This pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases to a safe operating level, the device will go through the normal startup process. The specific thermal shutdown junction temperature and hysteresis can be found in the thermal characteristics table.

APPLICATION INFORMATION

Output Voltage Programming

To provide the highest degree of flexibility in choosing output voltage, the EP5368QI uses a 3 pin VID, or Voltage ID, output voltage select arrangement. This allows the designer to choose one of seven preset voltages, or to use an external voltage divider. Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected.

shows the various VS0-VS2 pin logic states and the associated output voltage levels. A logic "1" indicates a connection to VIN or to a "high" logic voltage level. A logic "0" indicates a connection to ground or to a "low" logic voltage level. These pins can be either hardwired to VIN or GND or alternatively can be driven by standard logic levels. Logic low is defined as VLOW ≤ 0.4V. Logic high is defined as VHIGH ≥ 1.4V. Any level between these two values is indeterminate. These pins must not be left floating.

Table 1: VID Voltage Select Settings

VS2	VS1	VS0	V_{OUT}
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V
1	1	1	User Selectable

External Voltage Divider

As described above, the external voltage divider option is chosen by connecting the VS0, VS1, and VS2 pins to V_{IN} or logic "high". The EP5368QI uses a separate feedback pin, VFB, when using the external divider. VSENSE must be connected to VOUT as indicated in Figure 6.

The output voltage is selected by the following formula:

$$V_{OUT} = 0.603V\left(1+\frac{Ra}{Rb}\right)$$

R_a must be chosen as 200kΩ to maintain loop gain. Then R_b is given as:

$$R_b = \frac{1.206x10^5}{V_{OUT}-0.603}\Omega$$

V_{OUT} can be programmed over the range of 0.603V to V_{IN}-0.4V.

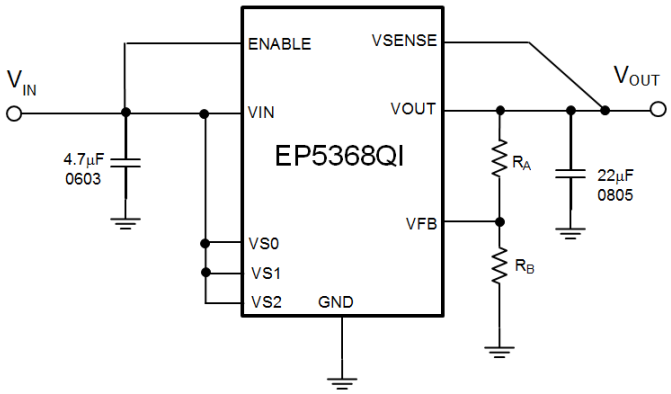


Figure 6. External Divider Application Circuit

Dynamically Adjustable Output

The EP5368QI is designed to allow for dynamic switching between the predefined VID voltage levels. The inter-voltage slew rate is optimized to prevent excess undershoot or overshoot as the output voltage levels transition. The slew rate is identical to the soft-start slew rate and is provided in the electrical characteristics table.

Dynamic transitioning between internal VID settings and the external divider is not allowed.

Input and Output Capacitors

The input capacitance requirement is 4.7µF 0603 MLCC. The input capacitor must be a X5R/X7R MLCC. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, and are not suitable for switch-mode DC-DC converter input filter applications.

The output capacitance requirement is approximately 20µF. Intel recommends a single 22µF 0805 MLCC. Ripple performance can be improved by using 2 x 10µF 0805 MLC capacitors.

As described in the Soft Start section, there is a limitation on the maximum bulk capacitance that can be placed on the output of this device. Please refer to that section for more details.

The output capacitor must be a X5R/X7R or equivalent MLCC. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter output filter applications.

Operation at 700mA Output Current

Operation at 700mA is supported by using the application circuit shown in Figure 7. The modification in the compensation is to ensure stability over the entire set of input and output voltage conditions.

For 700mA operation, use the following component values:

1) R_a = 249kΩ

2) C_a = 15pF 0402 MLCC capacitor.

3) Then R_b is given as:

$$R_b = \frac{1.501x10^5}{V_{OUT} - 0.603}\Omega$$

V_{OUT} can be programmed over the range of 0.603V to V_{IN}-0.4V.

4) Do not connect the sense line.

NOTE: Stability cannot be assured if these guidelines are not followed.

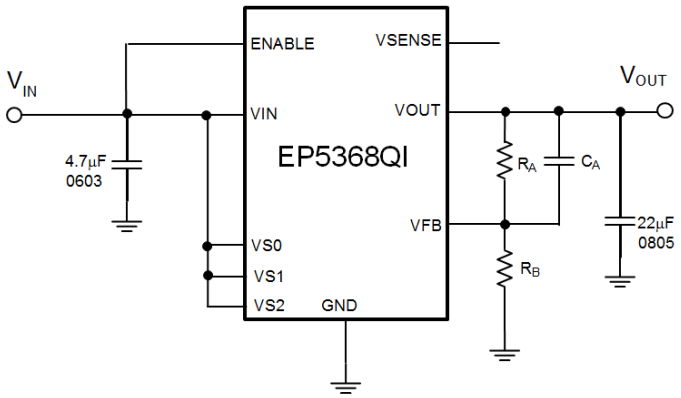


Figure 7. Applications Circuit for Operation at 700mA

Startup into Pre-Bias

The EP5368QI supports startup into a pre-biased output of up to VOUT. The output of the EP5368QI can be pre-biased with a voltage up to VOUT when it is first enabled.

LAYOUT RECOMMENDATIONS

Figure 8 shows critical components and layer 1 traces of a recommended minimum footprint EP5368QI layout. ENABLE configurations and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Intel website www.Intel.com/enpirion for exact dimensions and other layers. Please refer to Figure 8 while reading the layout recommendations in this section.

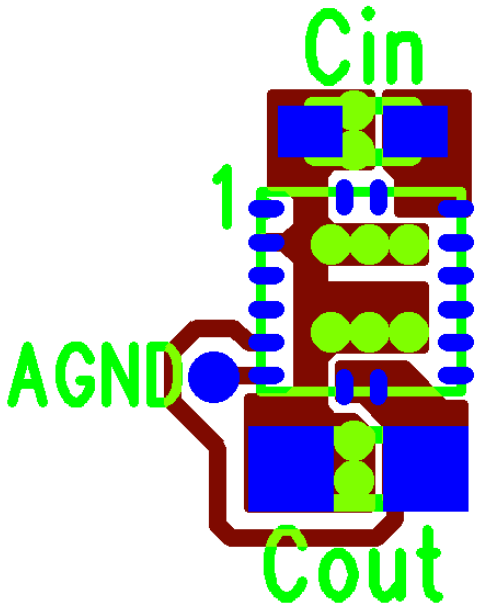


Figure 8: Top PCB Layer Critical Components and Copper for Minimum Footprint (Top View)

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EP5368QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EP5368QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Input and output grounds are separated until they connect at the PGND pins. The separation shown on Figure 8 between the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Intel website www.Intel.com/enpirion.

Recommendation 4: Multiple small vias should be used to connect the ground traces under the device to the system ground plane on another layer for heat dissipation. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 8. These vias connect the input/output filter capacitors to the GND plane and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

RECOMMENDED PCB FOOTPRIN

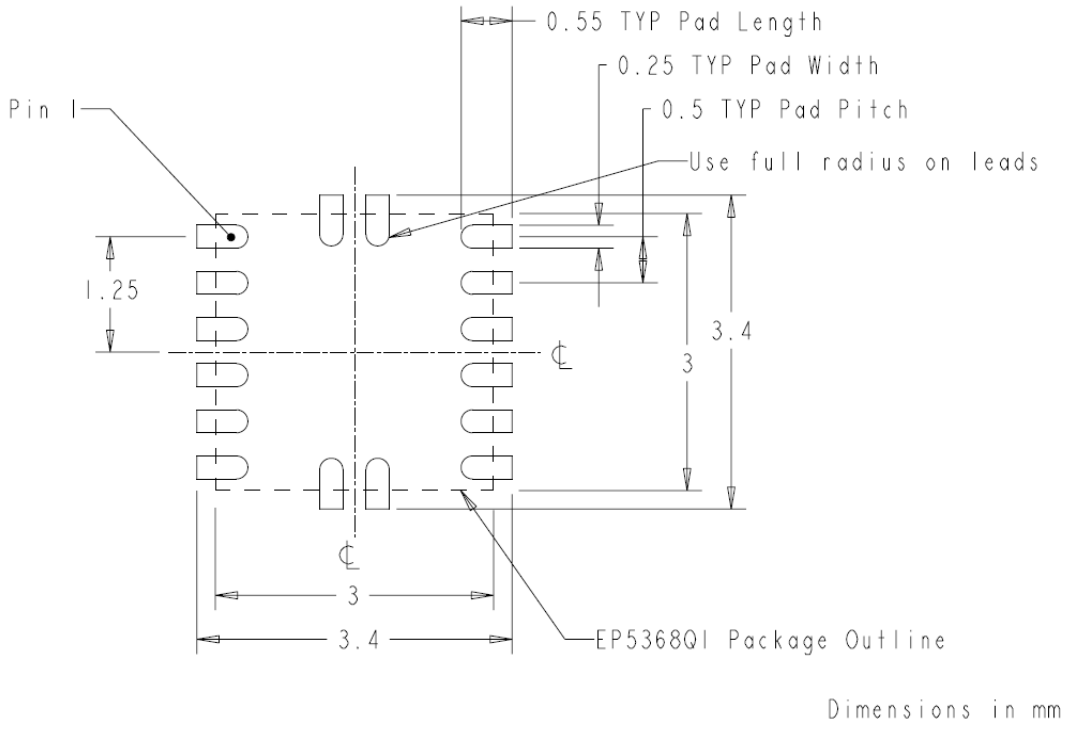


Figure 9: EP5368QI PCB Footprint (Top View)

PACKAGE DIMENSIONS

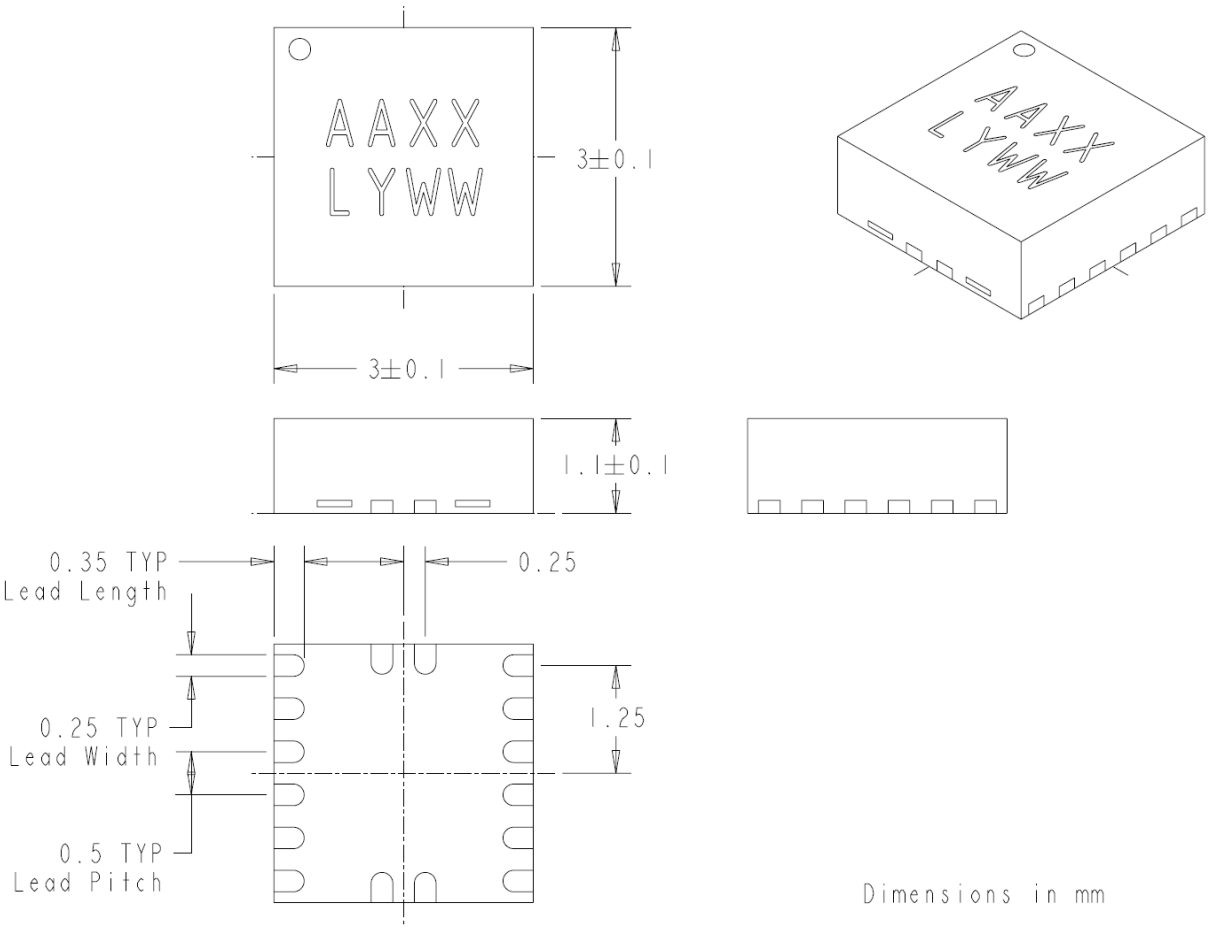


Figure 10: EP5368QI Package Dimensions

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
J	Dec, 2018	Changed datasheet into Intel format.
K	Jun, 2019	Max Bulk Cap (C_{OUT_MAX}) equation updated to reflect loading and startup time (with margin added)

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

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