REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Convert to military drawing format. Add vendor CAGE 01295. Changes to table I. Delete subgroup 9 from final electrical test parameters. Add case outline X. Added four devices 09 - 12.	87-07-06	M. A. Frye
D	Update part numbers for vendor CAGE number 01295. Correction on page 18, terminal connections. Editorial changes throughout. Add vendor CAGE numger 01295 as a supplier of the K package for device types 01 through 08. Changes to pages 5 and 6 table I. Changes to pages 10 and 11 terminal connections. Changes on pages 21 - 28.	88-05-06	M. A. Frye
E	Correct figure 1 device types 02 and 04 for case outline X. Boilerplate updated. ksr	04-08-06	Raymond Monnin
F	Update drawing to current requirements. Editorial changes throughout. ksr.	09-11-30	Charles F. Saffle
G	Update drawing to reflect current MIL-PRF-38535 requirements. – llb	17-09-27	Charles F. Saffle

REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30				

REV STATUS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Greg Pitz

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http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
84-08-24

MICROCIRCUIT, MEMORY, DIGITAL, BIPOLAR, PROGRAMMABLE LOGIC, MONOLITHIC SILICON

REVISION LEVEL

SIZE	CAGE CODE	
A	**67268**	**84129**

SHEET 1 OF 30

DSCC FORM 2233
APR 97

5962-E602-17

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

84129	01	J	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit
01, 09	PAL20L8A, L8A-2	20-input 8-output AND-OR invert gate array
02, 10	PAL20R8A, R8A-2	20-input 8-output registered AND-OR gate array
03, 11	PAL20R6A, R6A-2	20-input 6-output registered AND-OR gate array
04, 12	PAL20R4A, R4A-2	20-input 4-output registered AND-OR gate array
05	PAL20L10A	20-input 10-output AND-OR invert gate array
06	PAL20X8A	20-input 8-output registered AND-OR-XOR gate array
07	PAL20X10A	20-input 10-output registered AND-OR-XOR gate array
08	PAL20X4A	20-input 4-output registered AND-OR-XOR gate array

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	dual-in-line package
K	GDFP2-F24 or CDFP3-24	24	flat package
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line package
X	CQCC1-N28	28	square chip carrier package 1/
3	CQCC1-N28	28	square chip carrier package 1/

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +12.0 V dc
Input voltage range	-1.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θJ_C): 2/ 3/	
Cases J, K, L, X, and 3	(See MIL-STD-1835)
Output voltage applied	-1.5 V dc to +12 V dc
Output sink current	100 mA
Maximum power dissipation(P_D) 3/	1.2 W
Maximum junction temperature (T_J)	+175°C

1/ See figure 1.
2/ Heat sinking is recommended to reduce the junction temperature.
3/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ---------- 4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH}) ---------- 2.0 V dc
Maximum low level input voltage (V_{IL}) ---------- 0.8 V dc
Case operating temperature range (T_C) ---------- -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth tables for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_I = -18 mA	1	All		-1.5	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V, $V_{IL} \le$ 0.8 V, $V_{IH} \ge$ 2.0 V, I_{OH} = -2 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, $V_{IL} \le$ 0.8 V, $V_{IH} \ge$ 2.0 V, I_{OH} = 12 mA	1, 2, 3	All		0.5	V
High level input voltage	V_{IH}	V_{CC} = 5.5 V 2/	1, 2, 3	All	2.0		V
Low level input voltage	V_{IL}	V_{CC} = 5.5 V 2/	1, 2, 3	All		0.8	V
High level input current	I_{IH}	V_{CC} = 5.5 V, VI = 2.4 V 3/ $\overline{OE}$	1, 2, 3	All		40	µA
		others				25	
Low level input current	I_{IL}	V_{CC} = 5.5.V, V_I = 0.4 V 3/	1, 2, 3	All		-0.25	mA
Output short circuit current	I_{OS}	V_{CC} = 5.5.V, V_O = 0.4 V 3/	1, 2, 3	01-08	-30	-250	mA
				09,10, 11,12		-130	
Input current	I_I	V_{CC} = 5.5 V, V_I = 5.5. V	1, 2, 3	All		1.0	mA
Off-state output current	I_{OZL}	V_{CC} = 5.5 V, V_{IL} = 0.8 V, V_{IH} = 2.4 V, V_O = 0.4 V 3/	1, 2, 3	All		-250	µA
Off-state output current	I_{OZH}	V_{CC} = 5.5 V, V_{IL} = 0.8 V, V_{IH} = 2.4 V, V_O = 2.4 V 3/	1, 2, 3	All		100	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	01,02, 03,04		210	mA
				05		165	
				06,07, 08		180	
				09,10, 11,12		105	
Functional testing		See 4.3.1c	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay data input to output	t_{PHL}	V_{CC} = 5.0 V, C_L = 50 pF ±10%, R_1 = 390Ω, ±5%, R_2 = 750Ω ±5% (or equivalent load circuit) Unless otherwise specified	9, 10, 11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		50	
Propagation delay data input to output	t_{PLH}		9, 10, 11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		50	
Propagation delay high impedance to output high	t_{PZH}		9, 10, 11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		45	
Propagation delay high impedance to output low	t_{PZL}		9, 10, 11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		45	
Propagation delay output high to high impedance 5/	t_{PHZ}		9, 10, 11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		45	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

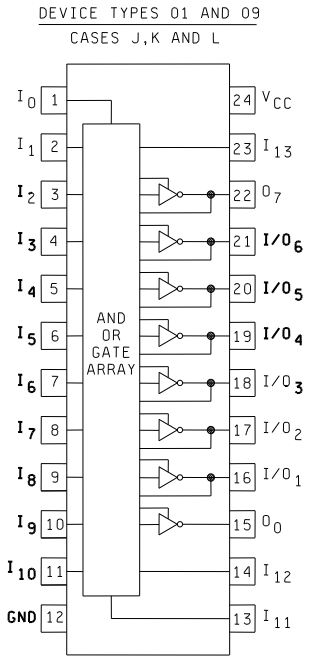
Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay output low to high impedance 5/	t_{PLZ}	V_{CC} = 5.0 V, C_L = 50 pF ±10%, R_1 = 390Ω, ±5%, R_2 = 750Ω ±5% (or equivalent load circuit) Unless otherwise specified	9, 10, 11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		45	
Propagation delay high impedance to output high $\overline{OE}$ to all output pins	t_{PZH}		9, 10, 11	02,03, 04,06, 07,08, 10,11, 12		25	ns
Propagation delay high impedance to output low $\overline{OE}$ to all output pins	t_{PZL}		9, 10, 11	02,03, 04,06, 07,08, 10,11, 12		25	ns
Propagation delay output high to high impedance $\overline{OE}$ to all output pins 5/	t_{PHZ}		9, 10, 11	02,03, 04,06, 07,08, 10,11, 12		25	ns
Propagation delay output low to high impedance $\overline{OE}$ to all output pins 5/	t_{PLZ}		9, 10, 11	02,03, 04,06, 07,08, 10,11, 12		25	ns
Clock to output	t_{PCH}		9, 10, 11	02,03, 04		20	ns
	t_{PCL}			06,07, 08,09, 10,11, 12		25	
Minimum clock pulse width	$t_{p(CL)}$		9, 10, 11	02,03, 04	20		ns
				06,07, 08	35		
				09,10, 11,12	25		
Minimum setup time 2/	t_{su}		9, 10, 11	02,03, 04	30		ns
				06,07, 08	40		
				09,10, 11,12	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Minimum hold time 2/	t_H	V_{CC} = 5.0 V, C_L = 50 pF ±10%, R_1 = 390Ω, ±5%, R_2 = 750Ω ±5% (or equivalent load circuit) Unless otherwise specified	9, 10, 11	03,03, 04,06, 07,08, 09,10, 11,12	0		ns
Maximum clock frequency 2/	f_{MAX}		9, 10, 11	02,03, 04	20		MHz
				06,07, 08,09, 10,11, 12	15.3		

1/ Unless otherwise specified V_{CC} is 4.5 V to 5.5 V.
2/ Tested only initially and after any design change, or used as setup condition, therefore guaranteed if not tested.
3/ I/O terminal leakage is the worst case of I_{IX} or I_{OZX}.
4/ Only one output shorted at a time.
5/ C_L = 5 pF.



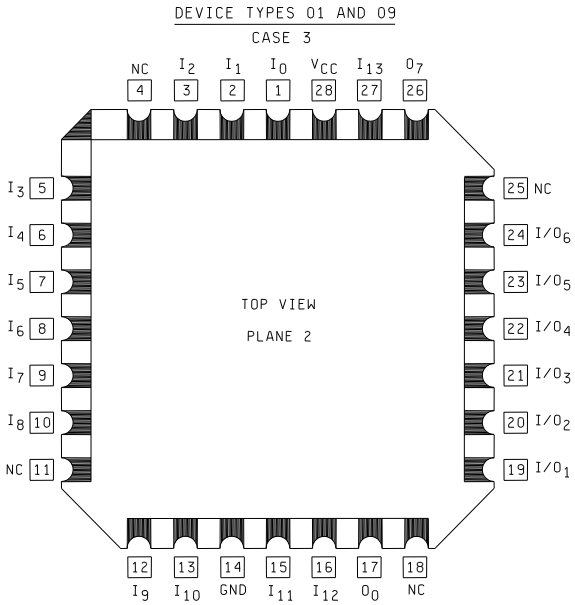
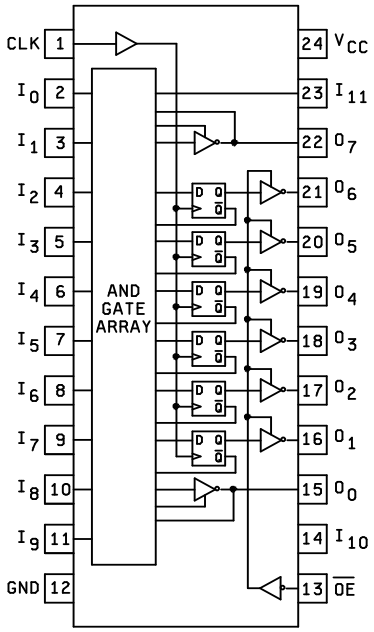


FIGURE 1. Terminal connections.

DEVICE TYPES 02 AND 10
CASES J,K AND L



DEVICE TYPES 02 AND 10
CASE 3

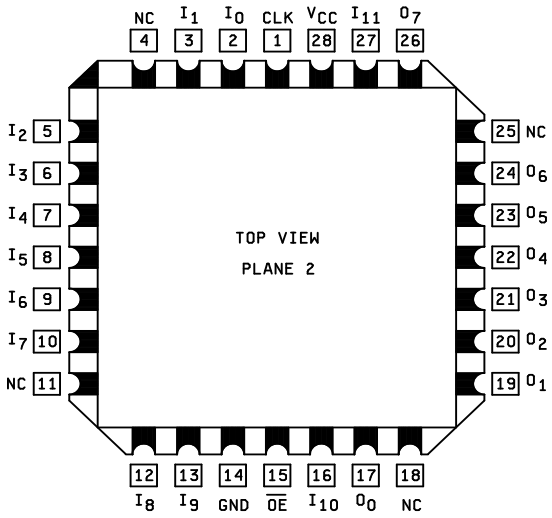
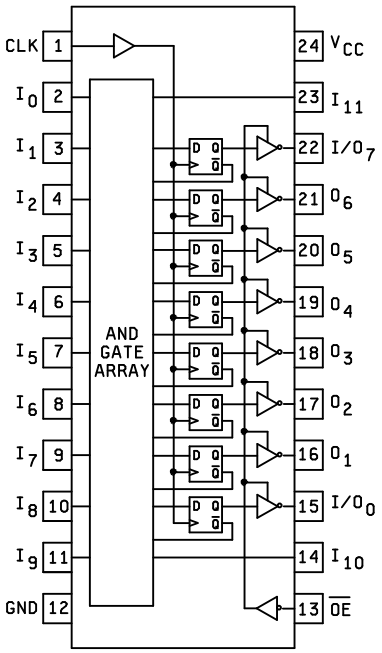


FIGURE 1. Terminal connections – Continued.

DEVICE TYPE 03 AND 11
CASES J,K AND L



DEVICE TYPES 03 AND 11
CASE 3

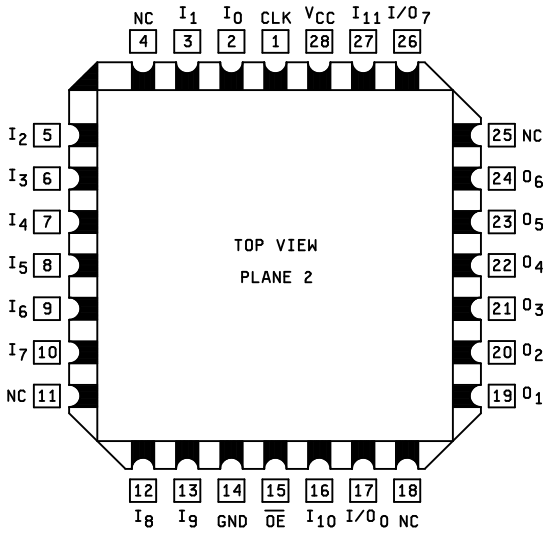
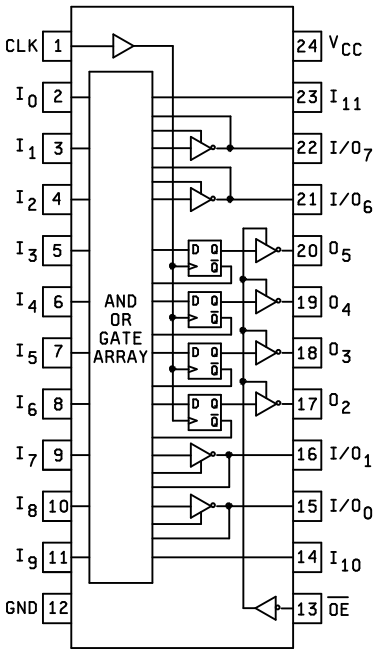


FIGURE 1. Terminal connections – Continued.

DEVICE TYPES 04 AND 12
CASES J,K AND L



DEVICE TYPES 04 AND 12
CASE 3

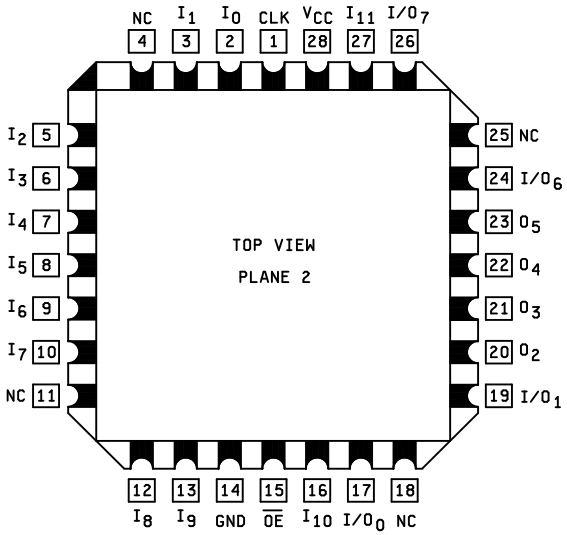


FIGURE 1. Terminal connections – Continued.

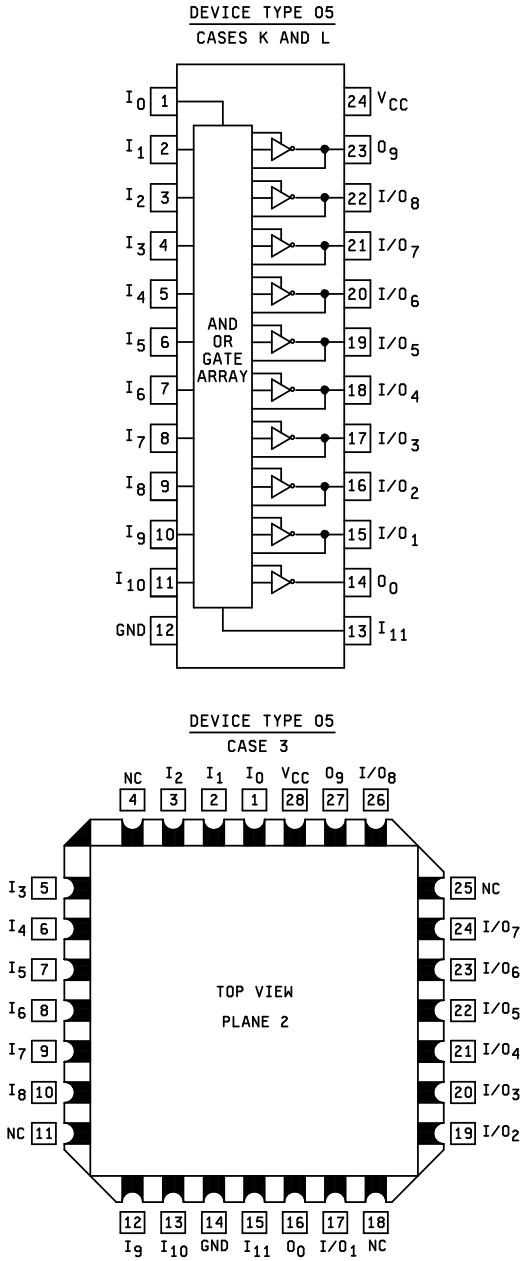
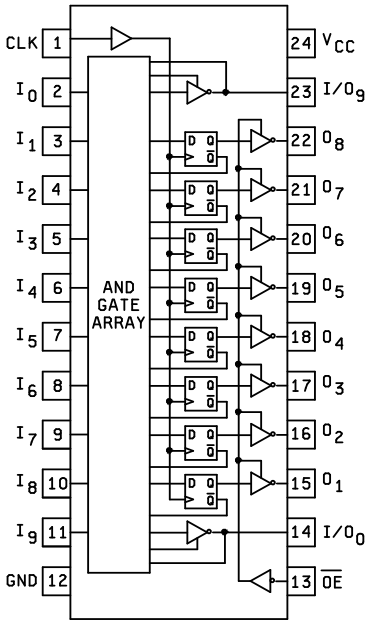


FIGURE 1. Terminal connections – Continued.

DEVICE TYPE 06
CASES K AND L



DEVICE TYPE 06
CASE 3

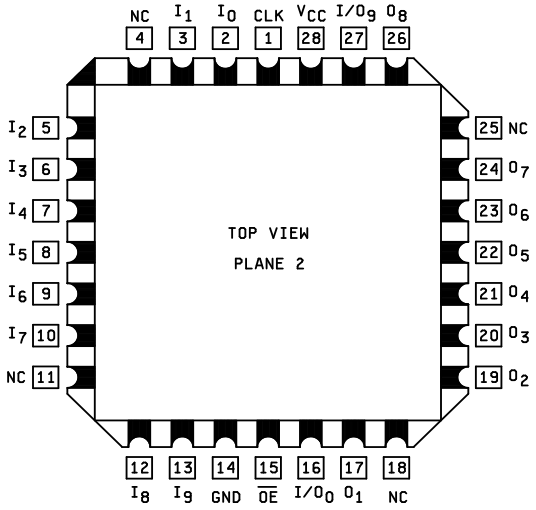
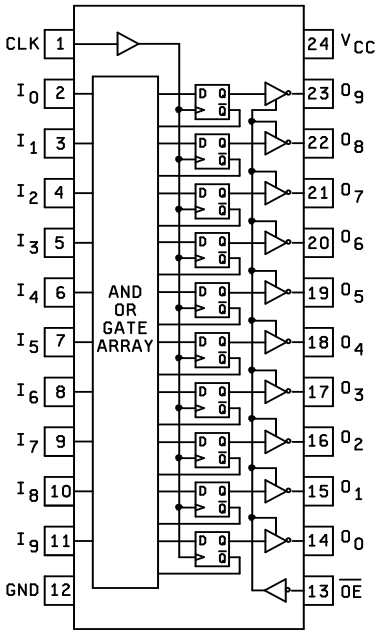


FIGURE 1. Terminal connections – Continued.

DEVICE TYPE 07
CASES K AND L



DEVICE TYPE 07
CASE 3

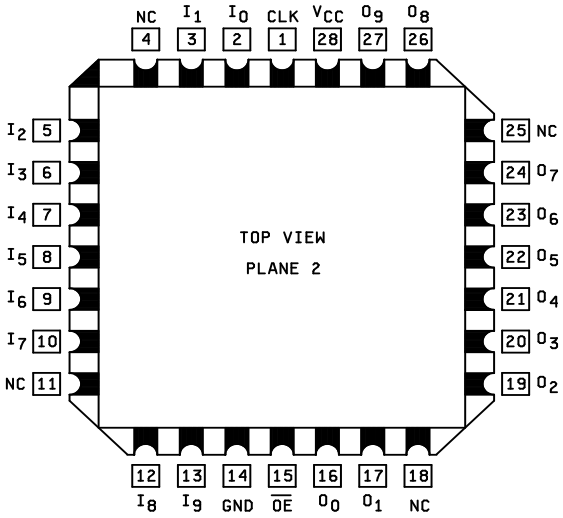


FIGURE 1. Terminal connections – Continued.

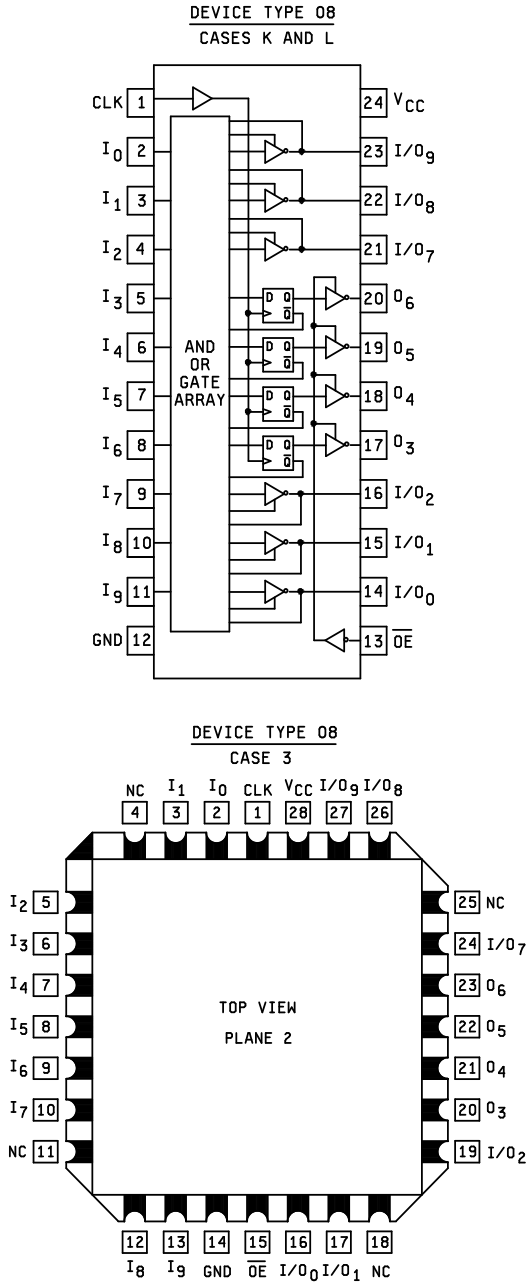


FIGURE 1. Terminal connections – Continued.

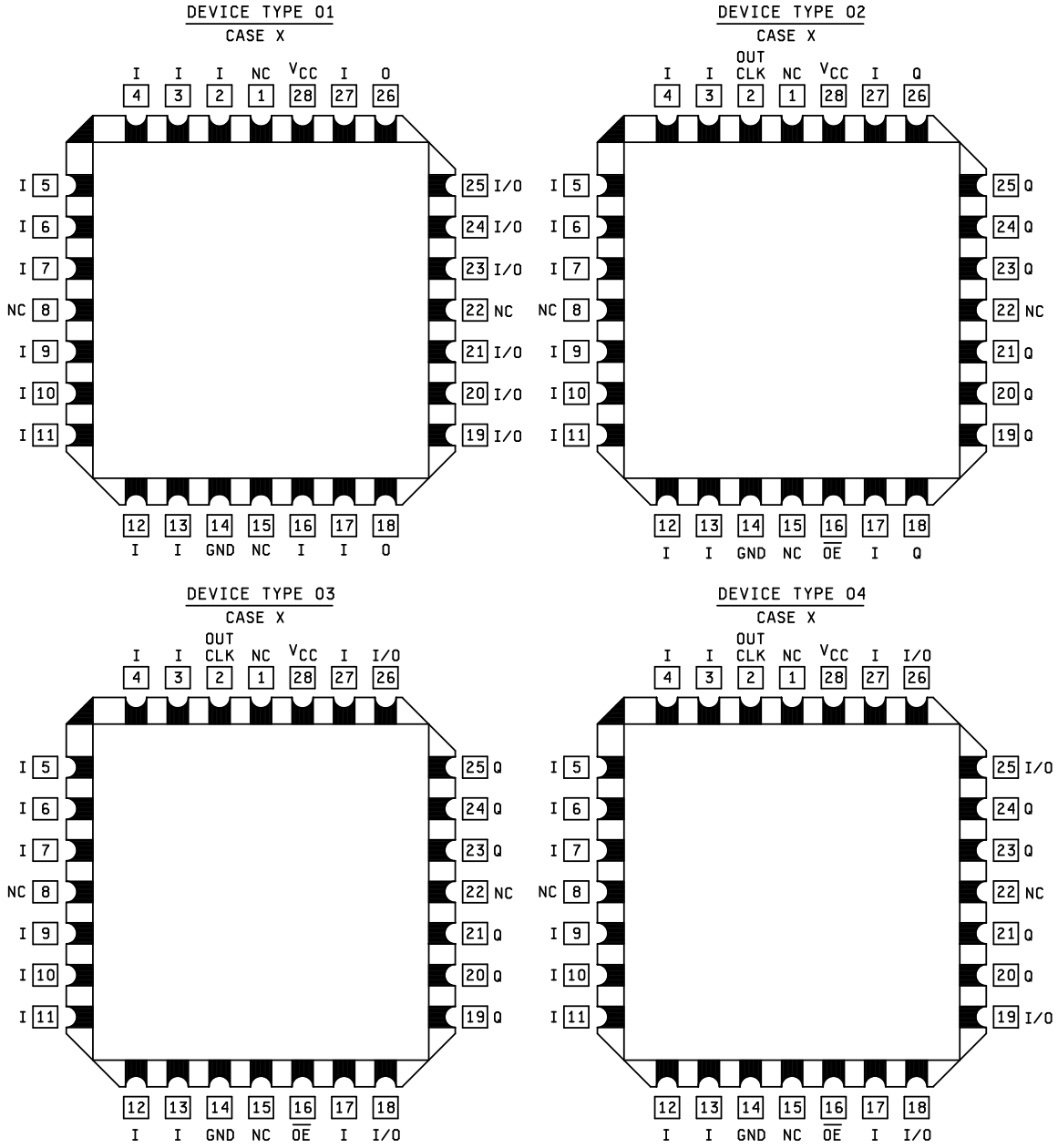


FIGURE 1. Terminal connections – Continued.

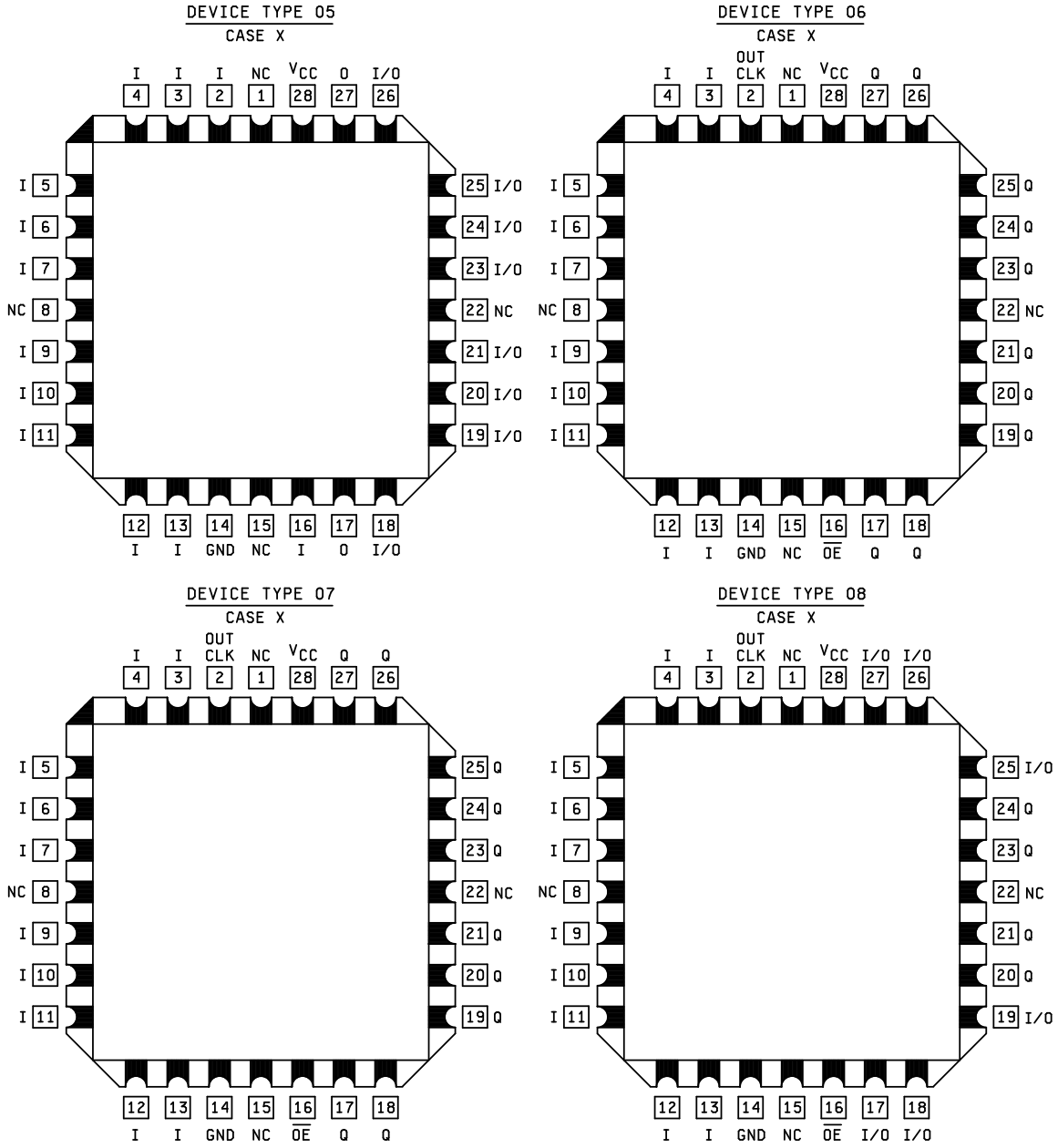


FIGURE 1. Terminal connections – Continued.

Device types 01 and 09

INPUTS														OUTPUTS							
I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	O_0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z

Device types 02 and 10

INPUTS														OUTPUTS							
$\overline{OE}$	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	CLK	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	H	H	H	H	H	H	H	H

Device types 03 and 11

INPUTS														OUTPUTS							
$\overline{OE}$	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	CLK	I/O_7	O_6	O_5	O_4	O_3	O_2	O_1	I/O_0
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	H	H	H	H	H	H	Z

Device types 04 and 12

INPUTS														OUTPUTS							
$\overline{OE}$	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	CLK	I/O_7	I/O_6	O_5	O_4	O_3	O_2	I/O_1	I/O_0
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	H	H	H	H	Z	Z

FIGURE 2. Truth tables (unprogrammed).

Device types 05

INPUTS												OUTPUTS									
I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	O_0
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Device types 06

INPUTS												OUTPUTS									
$\overline{OE}$	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	CLK	I/O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	I/O_0
H	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	CLK	Z	H	H	H	H	H	H	H	H	Z

Device types 07

INPUTS												OUTPUTS									
$\overline{OE}$	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	CLK	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
H	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	CLK	H	H	H	H	H	H	H	H	H	H

Device types 08

INPUTS												OUTPUTS									
$\overline{OE}$	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	CLK	I/O_9	I/O_8	I/O_7	O_6	O_5	O_4	O_3	I/O_2	I/O_1	I/O_0
H	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	H	H	H	H	Z	Z	Z

FIGURE 2. Truth tables (unprogrammed) – Continued.

DEVICE TYPES 01 AND 09

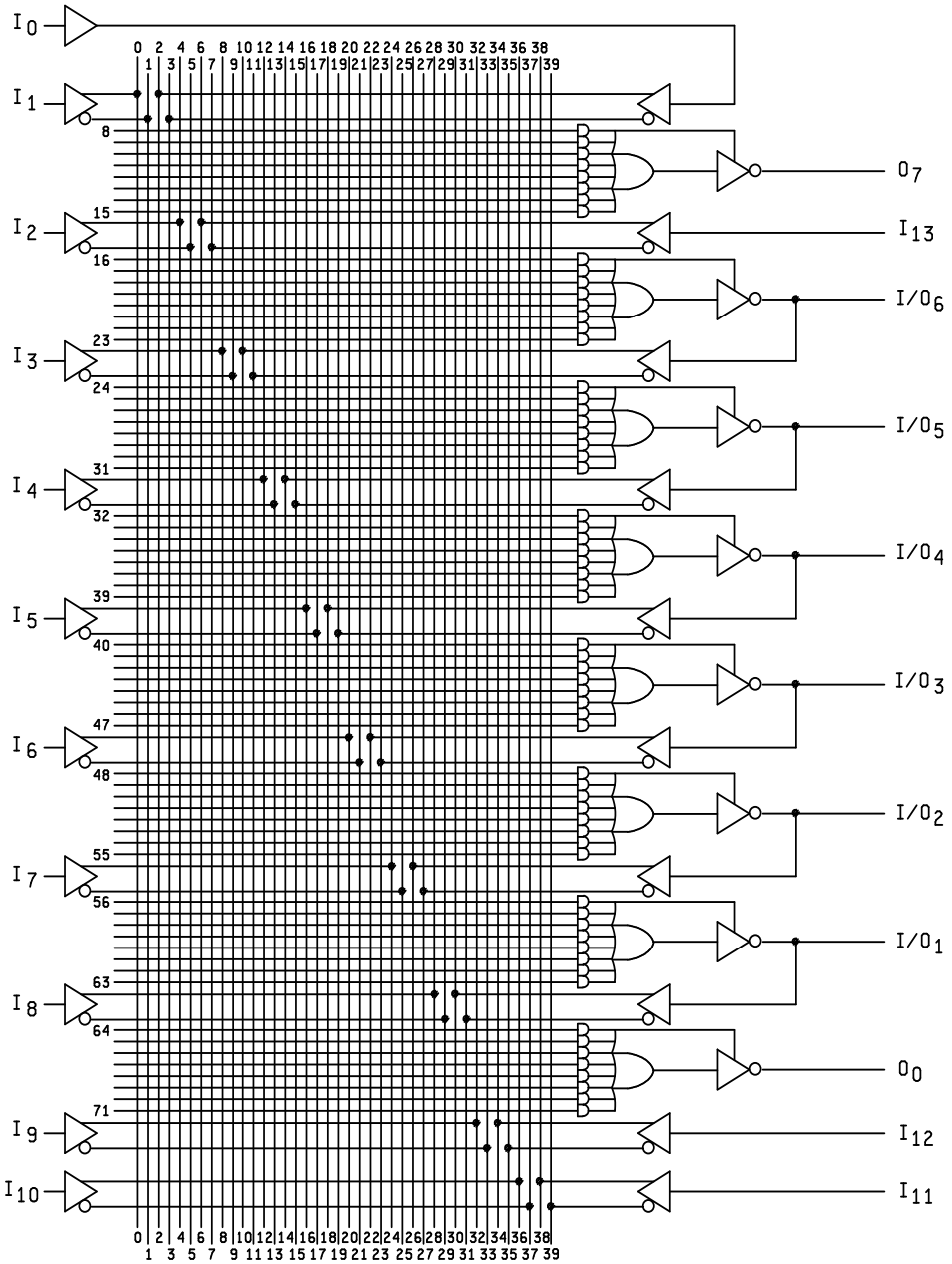


FIGURE 3. (Unprogrammed) Logic diagrams.

DEVICE TYPES 02 AND 10

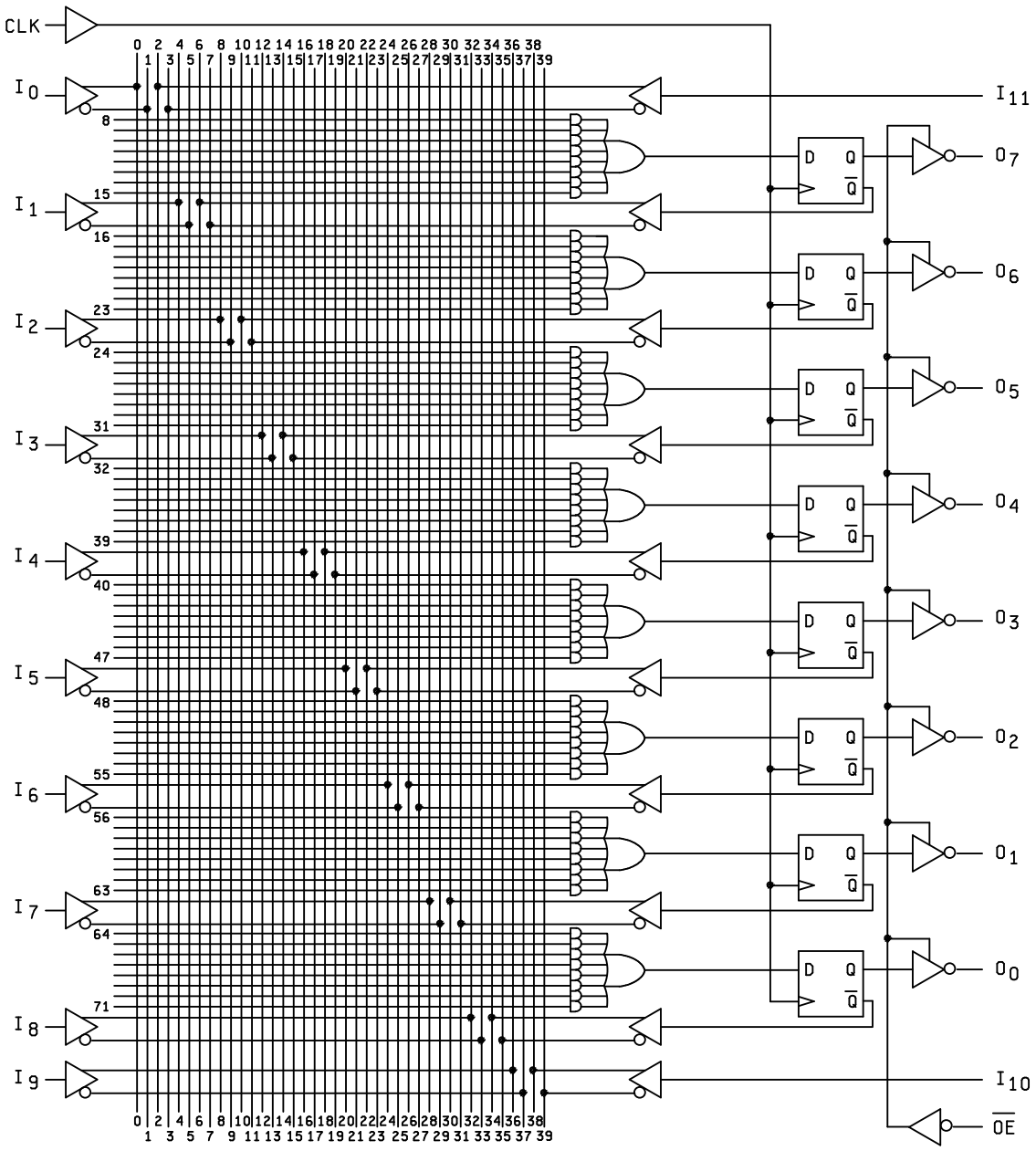


FIGURE 3. (Unprogrammed) Logic diagrams – Continued.

DEVICE TYPES 03 AND 11

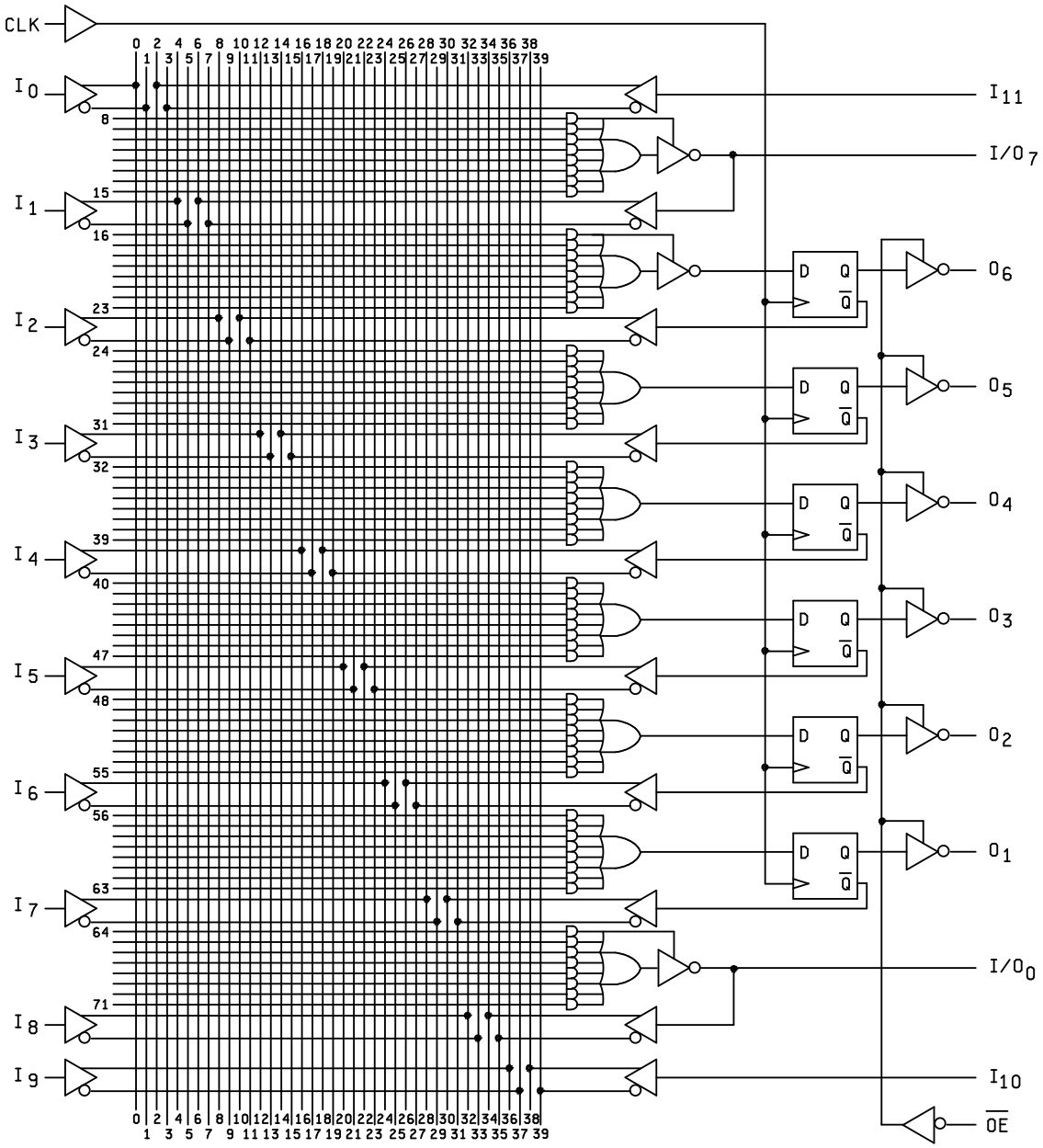


FIGURE 3. (Unprogrammed) Logic diagrams – Continued.

DEVICE TYPES 04 AND 12

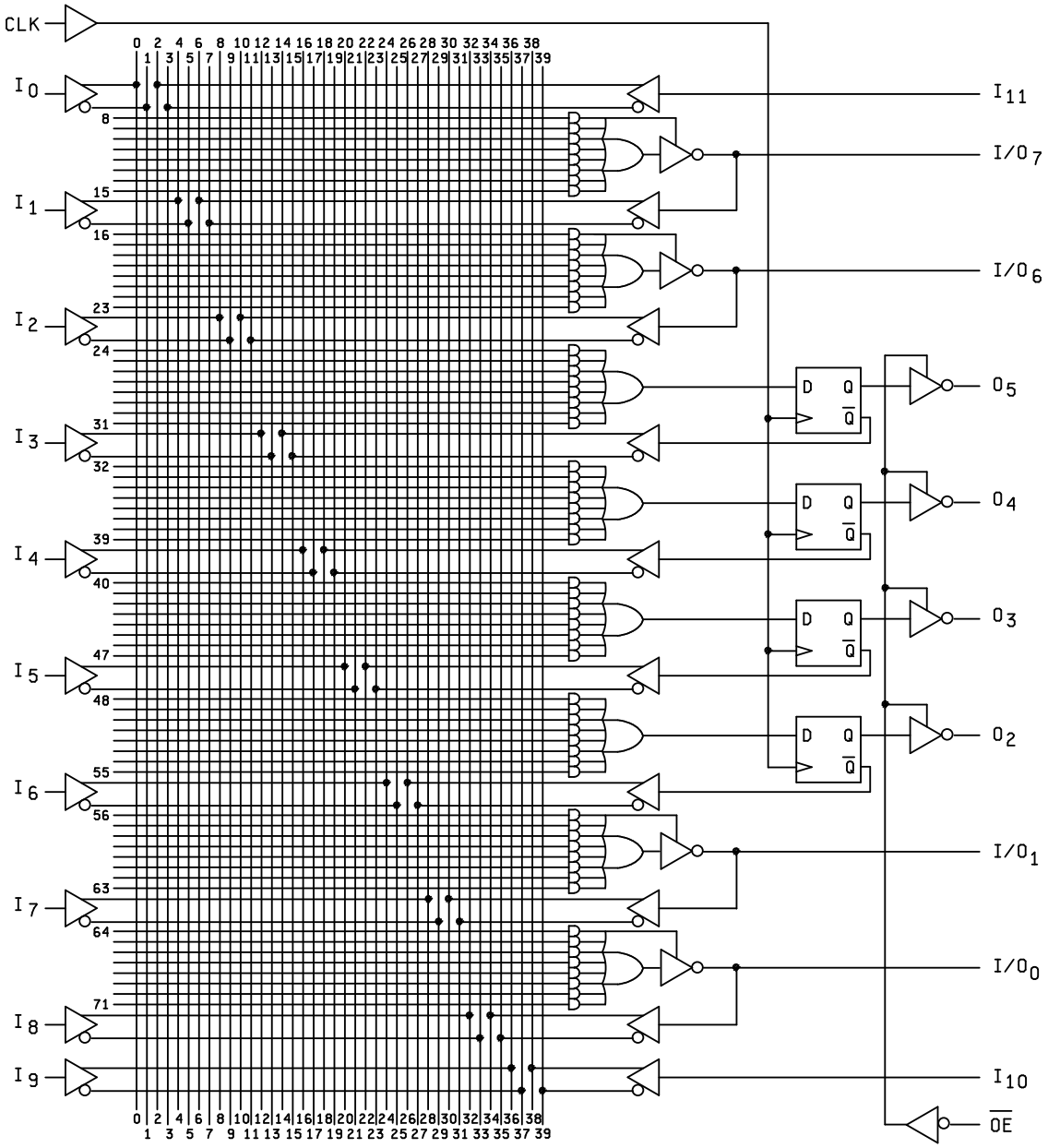


FIGURE 3. (Unprogrammed) Logic diagrams – Continued.

DEVICE TYPE 05

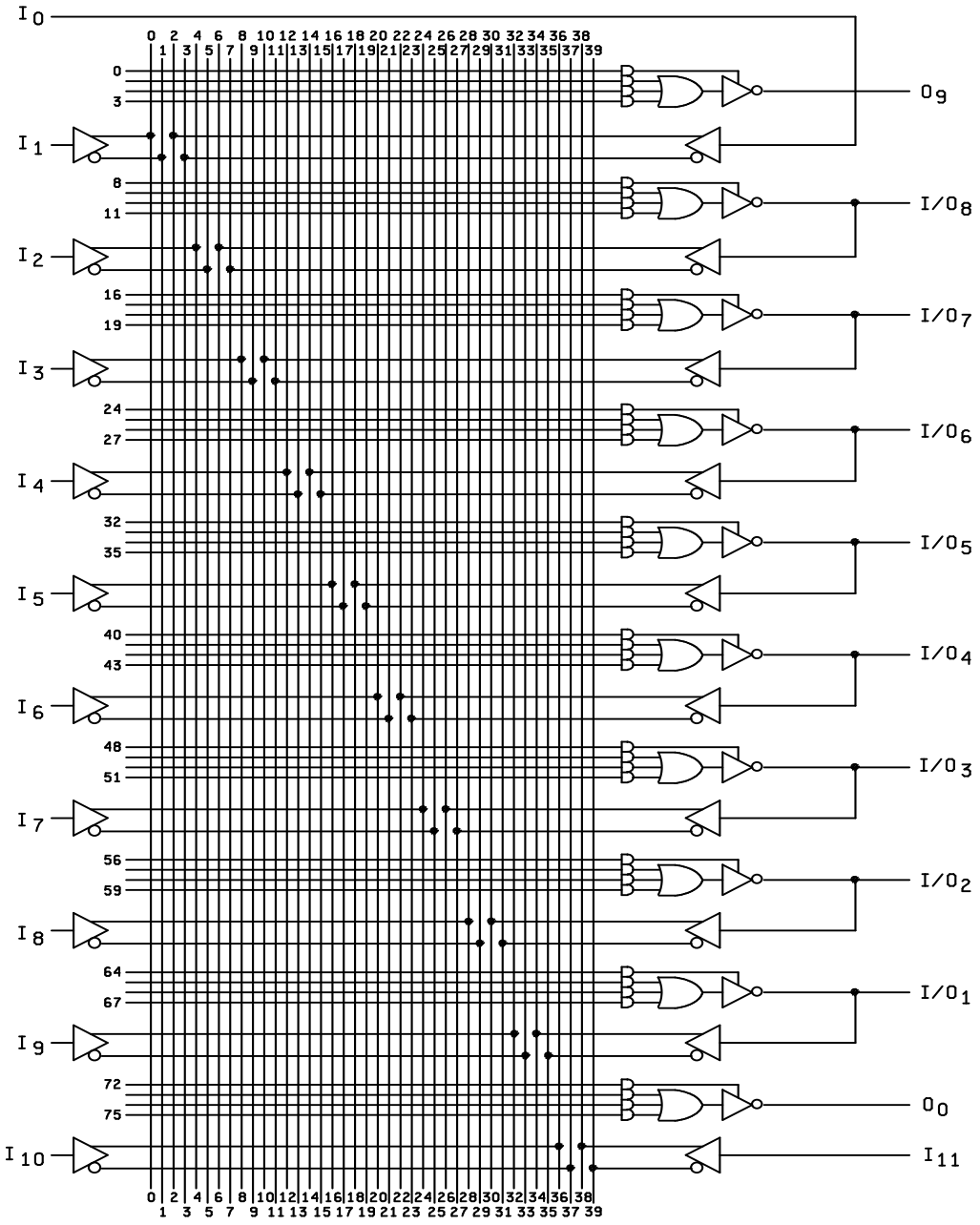


FIGURE 3. (Unprogrammed) Logic diagrams – Continued.

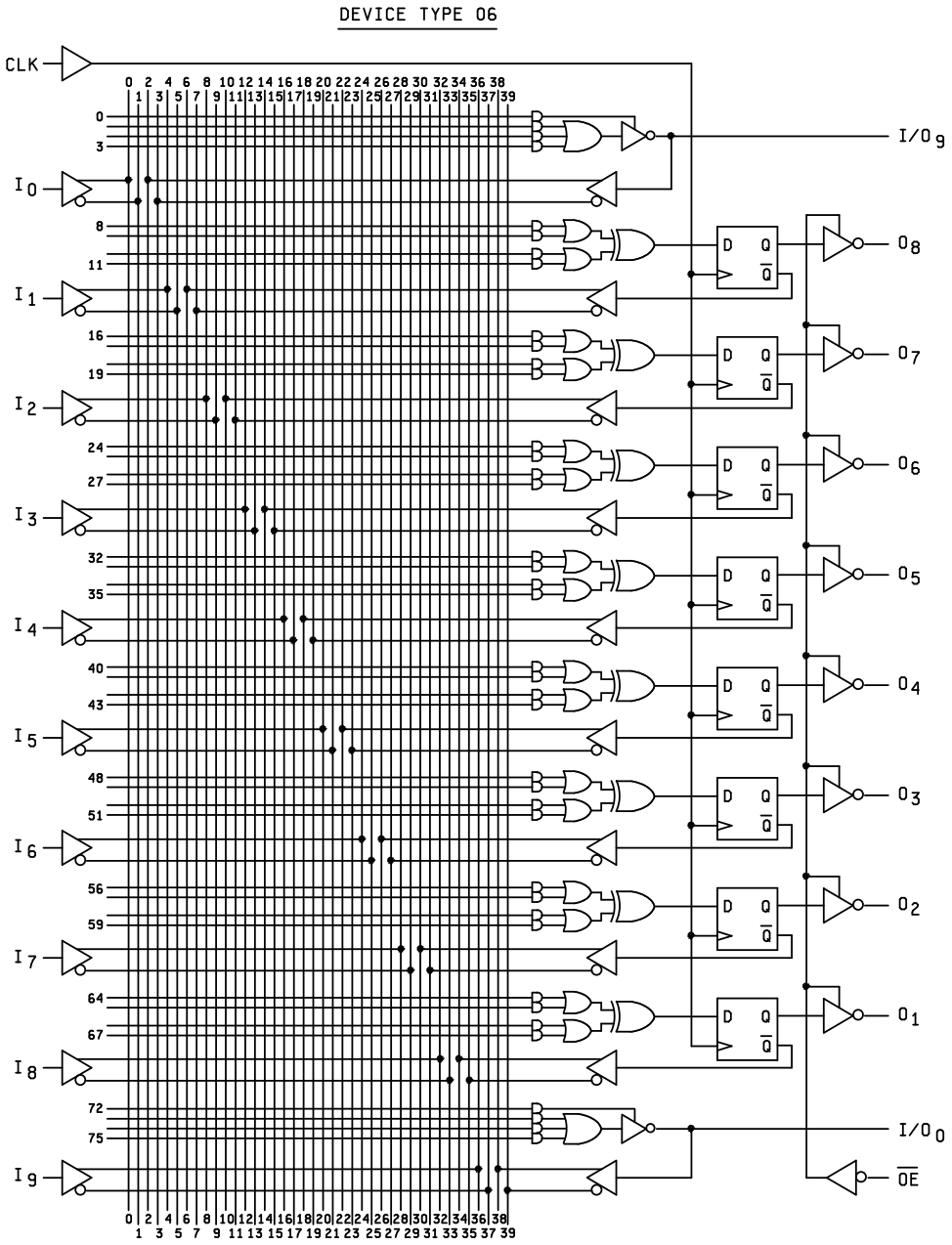


FIGURE 3. (Unprogrammed) Logic diagrams – Continued.

DEVICE TYPE 07

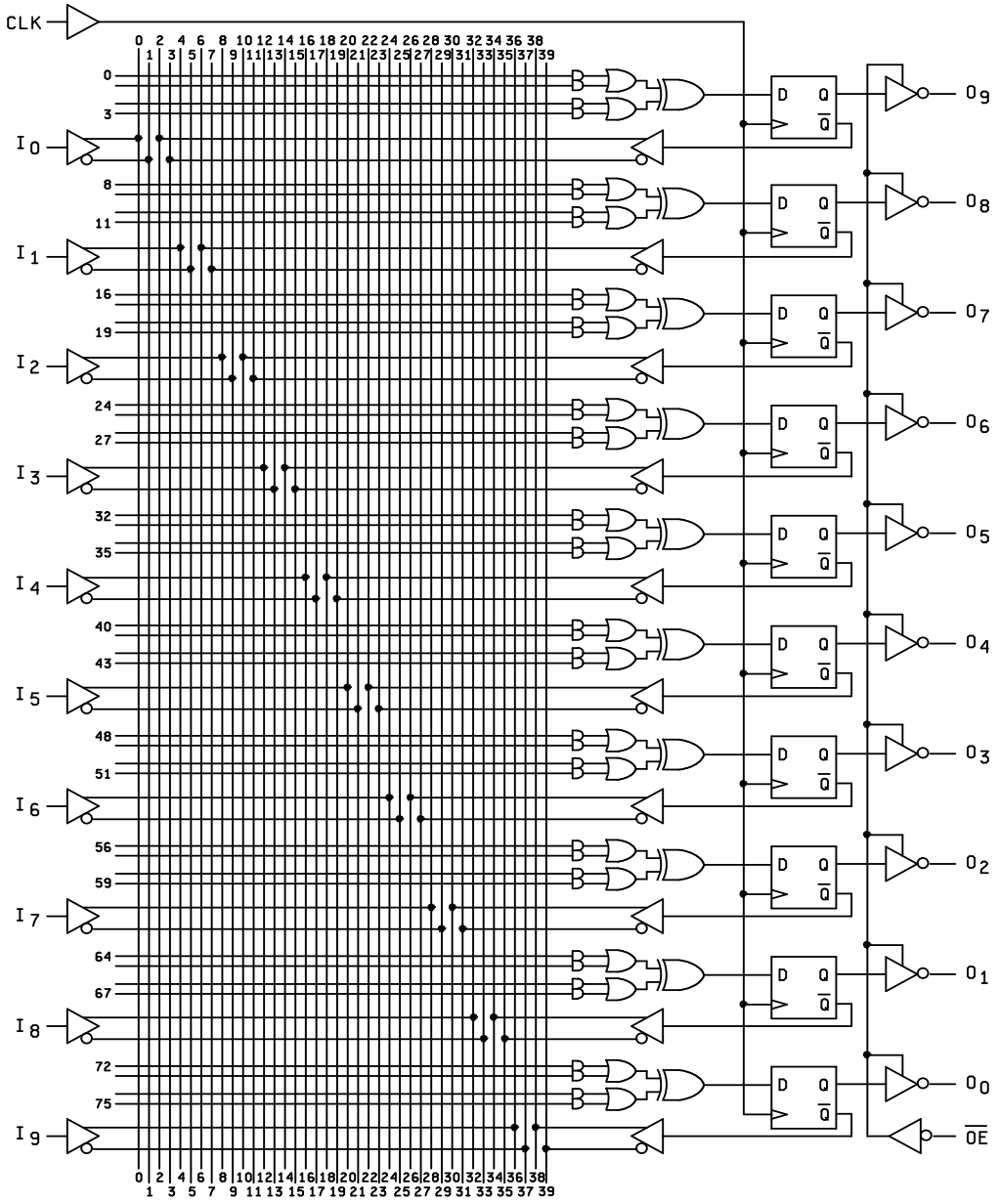


FIGURE 3. (Unprogrammed) Logic diagrams – Continued.

DEVICE TYPE 08

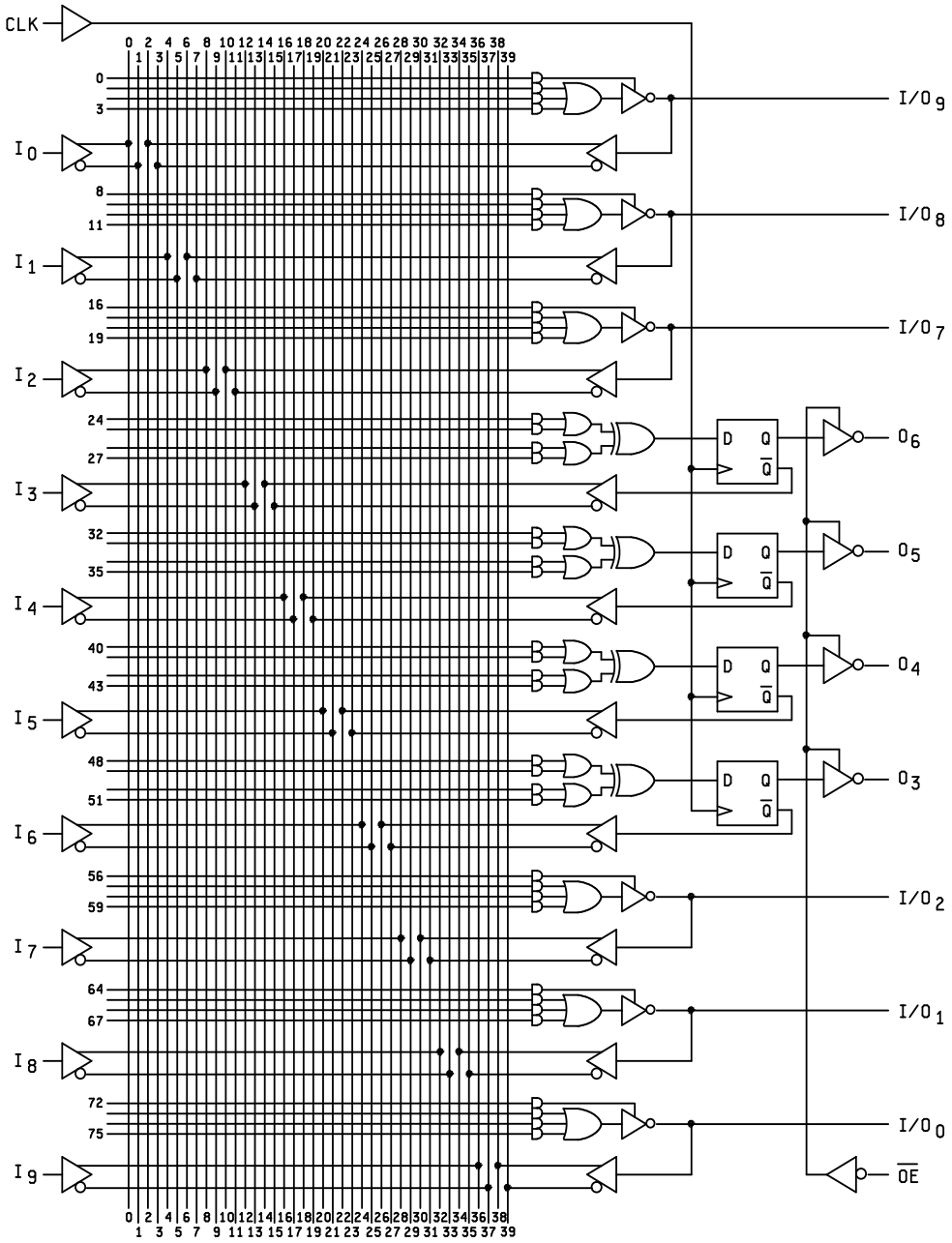


FIGURE 3. (Unprogrammed) Logic diagrams – Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8A, 8B,9
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*,8A, 8B
Group A test requirements (method 5005)	1,2,3,7,8A,8B,9 10, 11 4/
Groups C and D end-point electrical parameters (method 5005)	1,2,3

1/ * PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall also verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ Subgroups 10 and 11, if not tested, shall be guaranteed to specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroup 9. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.

d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroup 9. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-09-27

Approved sources of supply for SMD 84129 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr.

Standard Microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar part 2/ number	Reference military specification part number
84129013A	3/	PAL20L8AML/883B	M38510/50501B3A
8412901JA	3/	PAL20L8AMJTB	
8412901KA	3/	PAL20L8AMW/883B	
	3/	TIBPAL20L8-20MWB	
8412901LA	01295	TIBPAL20L8-20MJTB	M38510/50501BLA
	3/	PAL20L8AMJS/883B	
8412901XA	01295	TIBPAL20L8-20	
84129023A	3/	PAL20R8AML/883B	M38510/50502B3A
8412902JA	3/	PAL20R8AMJTB	
8412902KA	3/	PAL20R8AMW/883B	
	3/	TIBPAL20R8-20MWB	
8412902LA	01295	TIBPAL20R8-20MJTB	M38510/50502BLA
	3/	PAL20R8AMJS/883B	
8412902XA	3/	TIBPAL20R8-20	
84129033A	3/	PAL20R6AML/883B	M38510/50503B3A
8412903JA	3/	PAL20R6AMTJB	
8412903KA	3/	PAL20R6AMW/883B	
	3/	TIBPAL20R6-20MWB	
8412903LA	01295	TIBPAL20R6-20MJTB	M38510/50503BLA
	3/	PAL20R6AMJS/883B	
8412903XA	3/	TIBPAL20R6-20	
84129043A	3/	PAL20R4AML/883B	M38510/50504B3A
8412904JA	3/	PAL20R4AMJTB	
8412904KA	3/	PAL20R4AMW/883B	
	3/	TIBPAL20R4-20MWB	
8412904LA	01295	TIBPAL20R4-20MJTB	M38510/50504BLA
	3/	PAL20R4AMJS/883B	
8412904XA	3/	TIBPAL20R4-20	
84129053A	3/	PAL20L10AML/883B	
8412905KA	3/	PAL20L10AMW/883B	
	3/	TIBPAL20L10-25MWB	
8412905LA	3/	TIBPAL20L10-25MJTB	
	3/	PAL20L10AMJS/883B	
8412905XA	3/	TIBPAL20L10-25MFKB	
84129063A	3/	PAL20X8AML/883B	
8412906KA	3/	PAL20X8AMW/883B	
	3/	TIBPAL20X8-25MWB	
8412906LA	3/	TIBPAL20X8-25MJTB	
	3/	PAL20X8AMJS/883B	
8412906XA	3/	TIBPAL20X8-25MFKB	
84129073A	3/	PAL20X10AML/883B	
8412907KA	3/	PAL20X10AMW/883B	
	3/	TIBPAL20X10-25MWB	
8412907LA	3/	TIBPAL20X10-25MJTB	
	3/	PAL20X10AMJS/883B	
8412907XA	3/	TIBPAL20X10-25MFKB	

See footnotes at end of table.

Standard Microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar part 2/ number	Reference military specification part number
84129083A	3/	PAL20X4AML/883B	
8412908KA	3/	PAL20X4AMW/883B	
	3/	TIBPAL20X4-25MWB	
8412908LA	3/	TIBPAL20X4-25MJTB	
	3/	PAL20X4AMJS/883B	
8412908XA	3/	TIBPAL20X4-25MFKB	
84129093A	3/	PAL20L8A-2ML/883B	
8412909KA	3/	PAL20L8A-2MW/883B	
8412909LA	3/	PAL20L8A-2MJS/883B	
84129103A	3/	PAL20R8A-2ML/883B	
8412910KA	3/	PAL20R8A-2MW/883B	
8412910LA	3/	PAL20R8A-2MJS/883B	
84129113A	3/	PAL20L6A-2ML/883B	
8412911KA	3/	PAL20R6A-2MW/883B	
8412911LA	3/	PAL20R6A-2MJS/883B	
84129123A	3/	PAL20R4A-2ML/883B	
8412912KA	3/	PAL20R4A-2MW/883B	
8412912LA	3/	PAL20R4A-2MJS/883B	

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address	Fusible link
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P O Box 660199 Dallas, TX 75243	Titanium-Tungsten

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.