Data Sheet

AD4855

Buffered, 8-Channel Simultaneous Sampling, 16-Bit 250 kSPS DAS

FEATURES

- Complete 16-bit data acquisition system
  - Simultaneous sampling of 8 internally buffered channels
  - 250 kSPS per channel throughput
  - Differential, wide common-mode range inputs
  - ±75 pA typical input leakage at 25°C
  - Full-scale input step settling time < 300 ns
  - Integrated reference and reference buffer (4.096 V)
  - Integrated supply decoupling capacitors
  - 27 mW per channel at 250 kSPS, scales with throughput
- Minimal external signal conditioning
- Seamless high dynamic range
  - Per sample, per channel automatic gain ranging
  - Maintains ppm-level INL
- Per channel SoftSpan input ranges, bipolar or unipolar
  - ±40 V, ±25 V, ±20 V, ±12.5 V, ±10 V, ±6.25 V, ±5 V, ±2.5 V
  - 0 V to 40 V, 25 V, 20 V, 12.5 V, 10 V, 6.25 V, 5 V, 2.5 V
- Rail-to-rail input overdrive tolerance
- High performance
  - INL: ±160 µV typical (±40 V range)
  - SNR: 94.6 dB single-conversion typical (±40 V range)
  - DR: 98.1 dB single-conversion typical (±40 V range)
  - THD: −117 dB typical (±40 V range)
  - CMRR: 120 dB typical
- Digital flexibility
  - SPI CMOS (0.9 V to 5.25 V) and LVDS serial input and output
  - Optional oversampling with 16-bit digital averaging
  - Optional offset, gain, and phase correction
- 7.00 mm × 7.00 mm, 64-ball BGA full solution footprint

APPLICATIONS

- Automatic test equipment
- Avionics and aerospace
- Instrumentation and control systems
- Semiconductor manufacturing
- Test and measurement

FUNCTIONAL BLOCK DIAGRAM

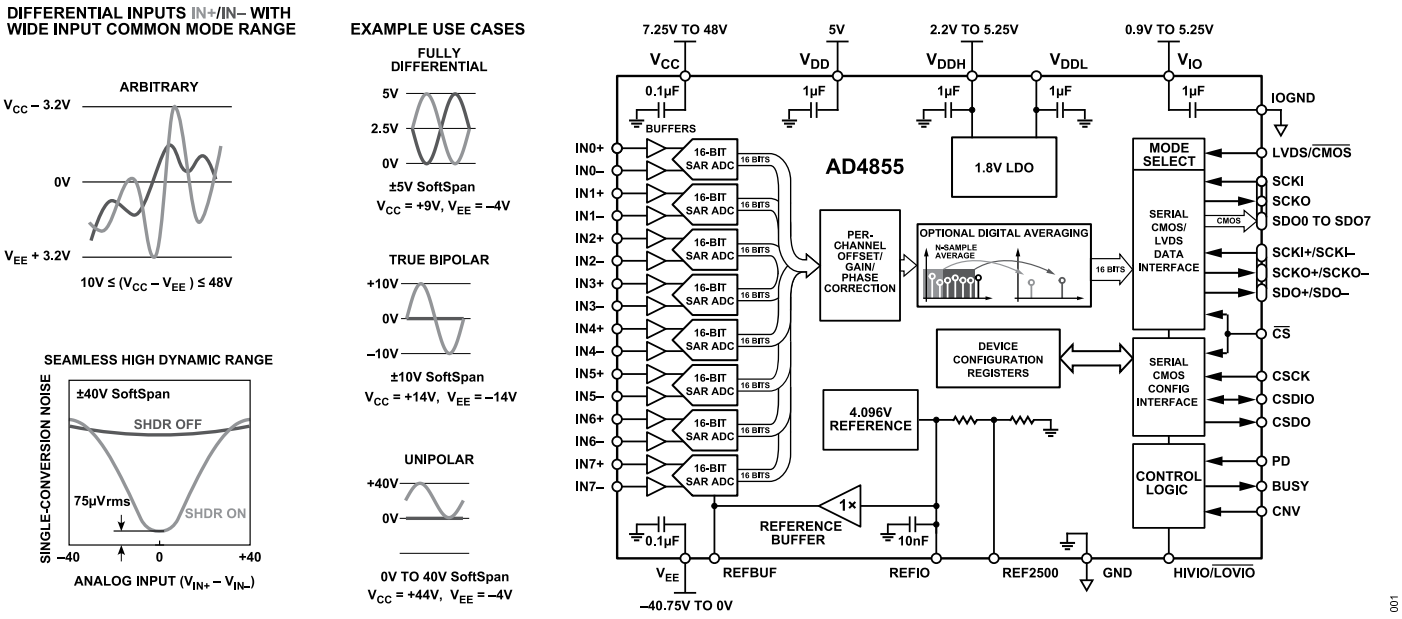

Figure 1. Functional Block Diagram (Example Analog-Input Signal Use Cases Shown)

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

8/2024—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD4855 is a fully buffered, 8-channel simultaneous sampling, 16-bit, 250 kSPS data acquisition system (DAS) with differential, wide common-mode range inputs. Its functional architecture is shown in Figure 1. Operating from a 5 V low voltage supply, flexible input buffer supplies, and using the precision low drift internal reference and reference buffer, the AD4855 allows the SoftSpan range of each channel to be independently configured to match the native application signal swing, minimizing additional external signal conditioning. To further maximize single-conversion dynamic range, the AD4855 incorporates seamless high dynamic range (SHDR) technology. When enabled, the input signal path gain of the channel is automatically optimized on a sample-by-sample basis, minimizing converter noise on each sample without impacting linearity.

The 11 MHz bandwidth, picoamp input analog buffers, wide input common-mode range, and 120 dB common-mode rejection ratio (CMRR) of the AD4855 allow the DAS to directly digitize input signals with arbitrary swings on INx+ and INx−. Its input signal flexibility, combined with ±160 µV integral nonlinearity (INL), no missing codes at 16 bits, 94.6 dB signal to noise ratio (SNR), and 98.1 dB dynamic range, make the AD4855 an ideal choice for applications requiring high accuracy, throughput, and precision in a compact solution footprint. Enabling 16-bit oversampling offers further SNR and dynamic range improvements. Optional per channel offset, gain, and phase adjustment provide the ability to calibrate and remove system-level errors upstream to the DAS.

The AD4855 features a serial peripheral interface (SPI) register configuration bus (0.9 V to 5.25 V) and supports both low voltage differential signaling buses (LVDS) and complementary metal-oxide semiconductor (CMOS) conversion data output buses, selectable using the LVDS/$\overline{\text{CMOS}}$ pin. Between one and eight lines of data output can be employed in CMOS mode, allowing the user to optimize bus width and throughput.

The 7.00 mm × 7.00 mm, 64-ball, ball grid array (BGA) of the AD4855 includes all critical power supply and reference bypass capacitors, minimizing full solution footprint and component count and reducing sensitivity to application printed circuit board (PCB) layout. The device operates over an extended industrial temperature range of −40°C to +125°C.

Note that throughout this data sheet, multifunction pins such as LVDS/$\overline{\text{CMOS}}$ are referred to either by the entire pin name or by a single function of the pin. For example, LVDS when only that function is relevant.

COMPANION PRODUCTS

- **Voltage references:** LTC6655-4.096 or ADR4540
- **Power solutions:** LT1761, LT8330, and/or LT3042

SPECIFICATIONS

V_{EE} = −40.75 V to 0 V, V_{CC} = 7.25 V to 48 V, (V_{CC} − V_{EE}) = 10 V to 48 V, V_{DD} = 5 V, V_{DDH} = 2.5 V, 1.8 V low drop out (LDO) regulator enabled, and V_{IO} = 0.9 V to 5.25 V. All channels convert at a sampling frequency (f_S) = 250 kSPS, internal reference and reference buffer enabled, all SoftSpan ranges, fully-differential input signal drive in SoftSpan 15 and SoftSpan 13, true bipolar or unipolar signal drive in other bipolar or unipolar SoftSpan ranges, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUTS					
Absolute Input Voltage	V_{INx+}[1], V_{INx-}[2] to V_{CC} and V_{EE}	V_{EE} + 3.2		V_{CC} − 3.2	V
Differential Input Range	(V_{INx+} − V_{INx-}), V_{REF}[3] = V_{REFBUF}[4]/1.024				
	SoftSpan 15: ±10 × V_{REF} range	−10 × V_{REF}		+10 × V_{REF}	V
	SoftSpan 14: 0 V to 10 × V_{REF} range	0		10 × V_{REF}	V
	SoftSpan 13: ±6.25 × V_{REF} range	−6.25 × V_{REF}		+6.25 × V_{REF}	V
	SoftSpan 12: 0 V to 6.25 × V_{REF} range	0		6.25 × V_{REF}	V
	SoftSpan 11: ±5 × V_{REF} range	−5 × V_{REF}		+5 × V_{REF}	V
	SoftSpan 10: 0 V to 5 × V_{REF} range	0		5 × V_{REF}	V
	SoftSpan 9: ±3.125 × V_{REF} range	−3.125 × V_{REF}		+3.125 × V_{REF}	V
	SoftSpan 8: 0 V to 3.125 × V_{REF} range	0		3.125 × V_{REF}	V
	SoftSpan 7: ±2.5 × V_{REF} range	−2.5 × V_{REF}		+2.5 × V_{REF}	V
	SoftSpan 6: 0 V to 2.5 × V_{REF} range	0		2.5 × V_{REF}	V
	SoftSpan 5: ±1.5625 × V_{REF} range	−1.5625 × V_{REF}		+1.5625 × V_{REF}	V
	SoftSpan 4: 0 V to 1.5625 × V_{REF} range	0		1.5625 × V_{REF}	V
	SoftSpan 3: ±1.25 × V_{REF} range	−1.25 × V_{REF}		+1.25 × V_{REF}	V
	SoftSpan 2: 0 V to 1.25 × V_{REF} range	0		1.25 × V_{REF}	V
	SoftSpan 1: ±0.625 × V_{REF} range	−0.625 × V_{REF}		+0.625 × V_{REF}	V
	SoftSpan 0: 0 V to 0.625 × V_{REF} range	0		0.625 × V_{REF}	V
Common-Mode Input Range	V_{CM}[5] = (V_{INx+} + V_{INx-})/2	V_{EE} + 3.2		V_{CC} − 3.2	V
CMRR	V_{CM} = 36 V p-p, 200 Hz sine, SHDR on	100	120		dB
Differential Input Overdrive Tolerance[6]	(V_{INx+} − V_{INx-})	−(V_{CC} − V_{EE})		(V_{CC} − V_{EE})	V
Input Overdrive Current Tolerance[6]	V_{INx+}, V_{INx-} > V_{CC}			10	mA
	V_{INx+}, V_{INx-} < V_{EE}	0			mA
Input Leakage Current	V_{INx+}, V_{INx-} = V_{CC} to V_{EE}	−40	±0.075	+40	nA
Input Resistance	R_{INx+}[7], R_{INx-}[8] for each pin		1000		GΩ
Input Capacitance	C_{INx+}[9], C_{INx-}[10] for each pin		4		pF
DC ACCURACY					
No Missing Codes		16			Bits
INL Error	SHDR on				
	SoftSpan 15 and SoftSpan 14: ±40 V and 0 V to 40 V ranges	−1220	±160	+1220	µV
	SoftSpan 13 and SoftSpan 12: ±25 V and 0 V to 25 V ranges	−763	±100	+763	µV
	SoftSpan 11 and SoftSpan 10: ±20 V and 0 V to 20 V ranges	−610	±100	+610	µV
	SoftSpan 9 and SoftSpan 8: ±12.5 V and 0 V to 12.5 V ranges	−381	±50	+381	µV
	SoftSpan 7 and SoftSpan 6: ±10 V and 0 V to 10 V ranges	−305	±50	+305	µV
	SoftSpan 5 and SoftSpan 4: ±6.25 V and 0 V to 6.25 V ranges	−190	±25	+190	µV

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	SoftSpan 3 and SoftSpan 2: ±5 V and 0 V to 5 V ranges	−152	±25	+152	µV
	SoftSpan 1 and SoftSpan 0: ±2.5 V and 0 V to 2.5 V ranges	−76	±15	+76	µV
Differential Nonlinearity (DNL) Error		−0.9	±0.2		LSB
Transition Noise[11]	SHDR on, near zero-scale		73		µV RMS
	SHDR off, near zero-scale				
	SoftSpan 15 and SoftSpan 14: ±40 V and 0 V to 40 V ranges		461		µV RMS
	SoftSpan 13 and SoftSpan 12: ±25 V and 0 V to 25 V ranges		287		µV RMS
	SoftSpan 11 and SoftSpan 10: ±20 V and 0 V to 20 V ranges		241		µV RMS
	SoftSpan 9 and SoftSpan 8: ±12.5 V and 0 V to 12.5 V ranges		155		µV RMS
	SoftSpan 7 and SoftSpan 6: ±10 V and 0 V to 10 V ranges		133		µV RMS
	SoftSpan 5 and SoftSpan 4: ±6.25 V and 0 V to 6.25 V ranges		94		µV RMS
	SoftSpan 3 and SoftSpan 2: ±5 V and 0 V to 5 V ranges		81		µV RMS
	SoftSpan 1 and SoftSpan 0: ±2.5 V and 0 V to 2.5 V ranges		73		µV RMS
Zero-Scale Error		−1300	−0.5 × LSB[12]	+1300	µV
Zero-Scale Error Drift			±1.5		µV/°C
Full-Scale Error[13]	V_{REFIO} = 4.096 V, REFIO overdriven[14]	−0.035	±0.01	+0.035	%FS
Full-Scale Error Drift[13]	V_{REFIO} = 4.096 V, REFIO overdriven[14]		±1.5		ppm/°C
AC ACCURACY[15]					
Dynamic Range	SHDR on/off				
	SoftSpan 15: ±40 V range		98.1/93.7		dB
	SoftSpan 14: 0 V to 40 V range		97.6/89.1		dB
	SoftSpan 13: ±25 V range		97.9/93.8		dB
	SoftSpan 12: 0 V to 25 V range		96.7/89.1		dB
	SoftSpan 11: ±20 V range		97.6/93.5		dB
	SoftSpan 10: 0 V to 20 V range		96.0/88.7		dB
	SoftSpan 9: ±12.5 V range		96.7/93.3		dB
	SoftSpan 8: 0 V to 12.5 V range		93.7/88.5		dB
	SoftSpan 7: ±10 V range		95.9/92.9		dB
	SoftSpan 6: 0 V to 10 V range		92.4/88.0		dB
	SoftSpan 5: ±6.25 V range		93.7/92.2		dB
	SoftSpan 4: 0 V to 6.25 V range		89.1/87.1		dB
	SoftSpan 3: ±5 V range		92.3/91.6		dB
	SoftSpan 2: 0 V to 5 V range		87.3/86.4		dB
	SoftSpan 1: ±2.5 V range		87.3/87.3		dB
	SoftSpan 0: 0 V to 2.5 V range		81.6/81.6		dB
Oversampled Dynamic Range[16]	OSR = 2, SoftSpan 0		Dynamic Range + 3		dB
	OSR = 2, SoftSpan 15		98.1		dB
	OSR = 1024, all SoftSpans		98.1		dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Signal-to-Noise-and-Distortion (SINAD) Ratio	SHDR on, input frequency (f_{IN}) = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	90.1	94.6		dB
	SoftSpan 14: 0 V to 40 V range	85.1	90.9		dB
	SoftSpan 13: ±25 V range	91.5	94.7		dB
	SoftSpan 12: 0 V to 25 V range	86.1	90.9		dB
	SoftSpan 11: ±20 V range	92.3	94.9		dB
	SoftSpan 10: 0 V to 20 V range	86.9	90.9		dB
	SoftSpan 9: ±12.5 V range	92.8	94.5		dB
	SoftSpan 8: 0 V to 12.5 V range	87.8	90.5		dB
	SoftSpan 7: ±10 V range	92.6	94.2		dB
	SoftSpan 6: 0 V to 10 V range	87.7	90		dB
	SoftSpan 5: ±6.25 V range	91.4	92.8		dB
	SoftSpan 4: 0 V to 6.25 V range	86.5	88.1		dB
	SoftSpan 3: ±5 V range	90.4	91.7		dB
	SoftSpan 2: 0 V to 5 V range	85.2	86.8		dB
	SoftSpan 1: ±2.5 V range	85.2	86.8		dB
	SoftSpan 0: 0 V to 2.5 V range	79.7	81.4		dB
	SHDR off, f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	92	93.4		dB
	SoftSpan 14: 0 V to 40 V range	86.8	88.7		dB
	SoftSpan 13: ±25 V range	92	93.4		dB
	SoftSpan 12: 0 V to 25 V range	86.9	88.7		dB
	SoftSpan 11: ±20 V range	91.7	93.2		dB
	SoftSpan 10: 0 V to 20 V range	86.6	88.3		dB
	SoftSpan 9: ±12.5 V range	91.6	93		dB
	SoftSpan 8: 0 V to 12.5 V range	86.5	88.2		dB
	SoftSpan 7: ±10 V range	91.2	92.6		dB
	SoftSpan 6: 0 V to 10 V range	85.9	87.7		dB
	SoftSpan 5: ±6.25 V range	90.4	91.7		dB
	SoftSpan 4: 0 V to 6.25 V range	85.2	86.7		dB
	SoftSpan 3: ±5 V range	89.7	91.1		dB
	SoftSpan 2: 0 V to 5 V range	84.5	86.1		dB
	SoftSpan 1: ±2.5 V range	85.2	86.8		dB
	SoftSpan 0: 0 V to 2.5 V range	79.7	81.4		dB
Signal-to-Noise Ratio (SNR)	SHDR on, f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	90.1	94.6		dB
	SoftSpan 14: 0 V to 40 V range	85.1	90.9		dB
	SoftSpan 13: ±25 V range	91.5	94.7		dB
	SoftSpan 12: 0 V to 25 V range	86.1	90.9		dB
	SoftSpan 11: ±20 V range	92.3	94.9		dB
	SoftSpan 10: 0 V to 20 V range	86.9	90.9		dB
	SoftSpan 9: ±12.5 V range	92.8	94.5		dB
	SoftSpan 8: 0 V to 12.5 V range	87.8	90.5		dB
	SoftSpan 7: ±10 V range	92.6	94.2		dB
	SoftSpan 6: 0 V to 10 V range	87.7	90.0		dB
	SoftSpan 5: ±6.25 V range	91.4	92.8		dB
	SoftSpan 4: 0 V to 6.25 V range	86.5	88.1		dB
	SoftSpan 3: ±5 V range	90.4	91.7		dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	SoftSpan 2: 0 V to 5 V range	85.2	86.8		dB
	SoftSpan 1: ±2.5 V range	85.2	86.8		dB
	SoftSpan 0: 0 V to 2.5V range	79.7	81.4		dB
	SHDR off, f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	92.0	93.4		dB
	SoftSpan 14: 0 V to 40 V range	86.8	88.7		dB
	SoftSpan 13: ±25 V range	92.0	93.4		dB
	SoftSpan 12: 0 V to 25 V range	86.9	88.7		dB
	SoftSpan 11: ±20 V range	91.7	93.2		dB
	SoftSpan 10: 0 V to 20 V range	86.6	88.3		dB
	SoftSpan 9: ±12.5 V range	91.6	93.0		dB
	SoftSpan 8: 0 V to 12.5 V range	86.5	88.2		dB
	SoftSpan 7: ±10 V range	91.2	92.6		dB
	SoftSpan 6: 0 V to 10 V range	85.9	87.7		dB
	SoftSpan 5: ±6.25 V range	90.4	91.7		dB
	SoftSpan 4: 0 V to 6.25 V range	85.2	86.7		dB
	SoftSpan 3: ±5 V range	89.7	91.1		dB
	SoftSpan 2: 0 V to 5 V range	84.5	86.1		dB
	SoftSpan 1: ±2.5 V range	85.2	86.8		dB
	SoftSpan 0: 0 V to 2.5 V range	79.7	81.4		dB
Total Harmonic Distortion (THD)	f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range		−117	−99	dB
	SoftSpan 14: 0 V to 40 V range		−109	−95	dB
	SoftSpan 13: ±25 V range		−117	−100	dB
	SoftSpan 12: 0 V to 25 V range		−111	−98	dB
	SoftSpan 11: ±20 V range		−114	−99	dB
	SoftSpan 10: 0 V to 20 V range		−112	−99	dB
	SoftSpan 9: ±12.5 V range		−114	−100	dB
	SoftSpan 8: 0 V to 12.5 V range		−113	−100	dB
	SoftSpan 7: ±10 V range		−115	−100	dB
	SoftSpan 6: 0 V to 10 V range		−113	−100	dB
	SoftSpan 5: ±6.25 V range		−115	−99	dB
	SoftSpan 4: 0 V to 6.25 V range		−113	−99	dB
	SoftSpan 3: ±5 V range		−114	−97	dB
	SoftSpan 2: 0 V to 5 V range		−113	−97	dB
	SoftSpan 1: ±2.5 V range		−109	−92	dB
	SoftSpan 0: 0 V to 2.5 V range		−110	−92	dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	101	119		dB
	SoftSpan 14: 0 V to 40 V range	99	113		dB
	SoftSpan 13: ±25 V range	101	119		dB
	SoftSpan 12: 0 V to 25 V range	103	115		dB
	SoftSpan 11: ±20 V range	103	119		dB
	SoftSpan 10: 0 V to 20 V range	103	116		dB
	SoftSpan 9: ±12.5 V range	104	119		dB
	SoftSpan 8: 0 V to 12.5 V range	104	116		dB
	SoftSpan 7: ±10 V range	105	119		dB
	SoftSpan 6: 0 V to 10 V range	105	116		dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	SoftSpan 5: ±6.25 V range	103	118		dB
	SoftSpan 4: 0 V to 6.25 V range	103	117		dB
	SoftSpan 3: ±5 V range	101	117		dB
	SoftSpan 2: 0 V to 5 V range	101	117		dB
	SoftSpan 1: ±2.5 V range	96	111		dB
	SoftSpan 0: 0 V to 2.5 V range	96	113		dB
Channel-to-Channel Crosstalk	All channels converting[17]		−120		dB
−3 dB Small-Signal Input Bandwidth			11		MHz
Aperture Delay			1		ns
Aperture Delay Matching			300		ps
Aperture Jitter			1		ps RMS
Full-Scale Input Step Settling Time	Full-scale step, 50 ppm settling		300		ns
INTERNAL REFERENCE ENABLED					
Internal Reference Output Voltage (V_{REFIO})	T_A = 25°C	4.093	4.096	4.099	V
Internal Reference Temperature Coefficient[18]		−10	±2	+10	ppm/°C
Internal Reference Line Regulation	V_{DD} = 4.75 V to 5.25 V		50		µV/V
REFIO Output Resistance			58		Ω
REFIO Output Capacitance			10		nF
INTERNAL REFERENCE DISABLED	REFIO overdriven[14]				
REFIO Input Voltage (V_{REFIO})		4.071	4.096	4.121	V
REFIO Input Resistance			38		kΩ
REFIO Input Capacitance			10		nF
REFERENCE BUFFER ENABLED					
Reference Buffer Offset Voltage (V_{OS})	V_{OS} = (V_{REFBUF} − V_{REFIO}), T_A = 25°C	−100	±20	+100	µV
Reference Buffer Offset Voltage Drift			±0.5		µV/°C
REFERENCE BUFFER DISABLED	REFBUF overdriven[19]				
REFBUF Input Voltage (V_{REFBUF})		4.071	4.096	4.121	V
REFBUF Input Current (I_{REFBUF})[20]	V_{REFBUF} = 4.096 V, f_S = 250 kSPS		2.5	3.4	mA
	V_{REFBUF} = 4.096 V, not converting		2.2		mA
SCALED REFERENCE OUTPUT					
REF2500 Output Voltage ($V_{REF2500}$)	T_A = 25°C	2.497	2.5	2.503	V
REF2500 Temperature Coefficient[18]		−10	±2	+10	ppm/°C
REF2500 Output Resistance			26		kΩ
CMOS DIGITAL INPUTS					
Input Voltage High (V_{IH})					
CNV		0.8			V
HIVIO/$\overline{\text{LOVIO}}$		4			V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
All Other Pins		0.85 × V_{IO}			V
Input Voltage Low (V_{IL})					
CNV				0.4	V
HIVIO/$\overline{\text{LOVIO}}$				1	V
All Other Pins				0.15 × V_{IO}	V
Digital Input Current (I_{IN})					
CNV		−100		+100	µA
HIVIO/$\overline{\text{LOVIO}}$		−10		+10	µA
All Other Pins		−10		+10	µA
Digital Input Capacitance (C_{IN})			2		pF
CMOS DIGITAL OUTPUTS					
Output Voltage High (V_{OH})	Source current (I_{SOURCE}) = 500 µA	V_{IO} − 0.2			V
Output Voltage Low (V_{OL})	Sink current (I_{SINK}) = 500 µA			0.2	V
High-Z Output Leakage Current (I_{OZ})		−10		+10	µA
LVDS DIGITAL INPUTS					
Differential Input Voltage (V_{ID})		±200	±350	±600	mV
Differential Termination Resistance (R_{ID})	$\overline{\text{CS}}$ = 0 V, V_{ICM} = 1.2 V, termination enabled[21]	95	107	120	Ω
	$\overline{\text{CS}}$ = V_{IO} or termination disabled[21]		10		MΩ
Common-Mode Input Voltage (V_{ICM})	1.71 V ≤ V_{IO} < 2.5 V	0.3	1.2	V_{IO} − 0.3	V
	2.5 V ≤ V_{IO} ≤ 5.25V	0.3	1.2	2.2	V
Common-Mode Input Current (I_{ICM})		−10		+10	µA
LVDS DIGITAL OUTPUTS					
Differential Output Voltage (V_{OD})	100 Ω differential termination, full-bias mode[21]	±260	±330	±400	mV
	100 Ω differential termination, half-bias mode[21]	±135	±185	±235	mV
Common-Mode Output Voltage (V_{OCM})	100 Ω differential termination	1.1	1.25	1.4	V
High-Z Output Leakage Current (I_{OZ})		−10		+10	µA
POWER SUPPLY VOLTAGES					
V_{CC}		7.25		48	V
V_{EE}		−40.75		0	V
V_{CC} − V_{EE}		10		48	V
V_{DD}		4.75	5.0	5.25	V
V_{DDH}	Disables 1.8 V LDO regulator		0		V
	Enables 1.8 V LDO regulator	2.2		5.25	V
V_{DDL}	Supplied externally, 1.8 V LDO regulator disabled	1.71	1.8	1.89	V
	Supplied by 1.8 V LDO regulator, no external connection		1.8		V
V_{IO}					
CMOS Conversion Data Output	HIVIO/$\overline{\text{LOVIO}}$ = V_{DD}	1.71		5.25	V
	HIVIO/$\overline{\text{LOVIO}}$ = GND	0.9		1.89	V
LVDS Conversion Data Output	HIVIO/$\overline{\text{LOVIO}}$ = V_{DD}	1.71		5.25	V
	HIVIO/$\overline{\text{LOVIO}}$ = GND	1.71		1.89	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY CURRENTS					
CMOS Conversion Data Output	25 pF load on CMOS outputs				
Operating Mode[22]	f_S = 250 kSPS, all channels converting				
V_{CC} Current ($I_{V_{CC}}$)	V_{CC} = +24 V, V_{EE} = −24 V		10.7	14.1	mA
	V_{CC} = +15 V, V_{EE} = −15 V		10.3		mA
	V_{CC} = +8.2 V, V_{EE} = −3.2 V		9.8		mA
V_{EE} Current ($I_{V_{EE}}$)	V_{CC} = +24 V, V_{EE} = −24 V	−12	−8.7		mA
	V_{CC} = +15 V, V_{EE} = −15 V		−8.2		mA
	V_{CC} = +8.2 V, V_{EE} = −3.2 V		−7.6		mA
V_{DD} Current ($I_{V_{DD}}$)	Reference and reference buffer enabled		12.2	18.7	mA
	V_{REFIO} = 4.096 V, REFIO overdriven[14]		10.2		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[19]		1.9		mA
V_{DDH} Current ($I_{V_{DDH}}$)	V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled		15	20.5	mA
V_{DDL} Current ($I_{V_{DDL}}$)	V_{DDH} = GND, 1.8 V LDO regulator disabled, V_{DDL} = 1.8 V		14.5	20	mA
V_{IO} Current ($I_{V_{IO}}$)	V_{IO} = 2.5 V		1.4	1.9	mA
Acquisition Mode					
$I_{V_{CC}}$	V_{CC} = +24 V, V_{EE} = −24 V		9.4		mA
$I_{V_{EE}}$	V_{CC} = +24 V, V_{EE} = −24 V		−7.4		mA
$I_{V_{DD}}$	Reference and reference buffer enabled		10.8		mA
	V_{REFIO} = 4.096 V, REFIO overdriven[14]		8.8		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[19]		1.4		mA
$I_{V_{DDH}}$	V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled		72		µA
$I_{V_{DDL}}$	V_{DDH} = GND, 1.8 V LDO regulator disabled, V_{DDL} = 1.8 V		16		µA
$I_{V_{IO}}$	V_{IO} = 2.5 V		1		µA
Nap Mode					
$I_{V_{CC}}$	V_{CC} = +24 V, V_{EE} = −24 V		4.5		mA
$I_{V_{EE}}$	V_{CC} = +24 V, V_{EE} = −24 V		−3.3		mA
$I_{V_{DD}}$	Reference and reference buffer enabled		10.3		mA
	V_{REFIO} = 4.096 V, REFIO overdriven[14]		8.3		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[19]		1.0		mA
$I_{V_{DDH}}$	V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled		72		µA
$I_{V_{DDL}}$	V_{DDH} = GND, 1.8 V LDO regulator disabled, V_{DDL} = 1.8 V		16		µA
$I_{V_{IO}}$	V_{IO} = 2.5 V		1		µA
Power-Down Mode					
$I_{V_{CC}}$	V_{CC} = +24 V, V_{EE} = −24 V		18		µA
$I_{V_{EE}}$	V_{CC} = +24 V, V_{EE} = −24 V		−4		µA
$I_{V_{DD}}$			130		µA
$I_{V_{DDH}}$	V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled		30		µA
$I_{V_{DDL}}$	V_{DDH} = GND, 1.8 V LDO regulator disabled, V_{DDL} = 1.8 V		16		µA
$I_{V_{IO}}$	V_{IO} = 2.5 V		1		µA
LVDS Conversion Data Output	100 Ω differential load on LVDS outputs				
Operating Mode	f_S = 250 kSPS, all channels converting				
$I_{V_{CC}}$	V_{CC} = +24 V, V_{EE} = −24 V		10.7	14.1	mA
	V_{CC} = +15 V, V_{EE} = −15 V		10.3		mA
	V_{CC} = +8.2 V, V_{EE} = −3.2 V		9.8		mA
$I_{V_{EE}}$	V_{CC} = +24 V, V_{EE} = −24 V	−12	−8.7		mA
	V_{CC} = +15 V, V_{EE} = −15 V		−8.2		mA
	V_{CC} = +8.2 V, V_{EE} = −3.2 V		−7.6		mA
$I_{V_{DD}}$	Reference and reference buffer enabled		13.7	20.4	mA

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	V_{REFIO} = 4.096 V, REFIO overdriven[14]		11.7		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[19]		3.4		mA
$I_{V_{DDH}}$	V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled		23.5	31	mA
$I_{V_{DDL}}$	V_{DDH} = GND, 1.8 V LDO regulator disabled, V_{DDL} = 1.8 V		23	30.5	mA
$I_{V_{IO}}$	V_{IO} = 2.5 V		22	165	µA
Acquisition Mode					
$I_{V_{CC}}$	V_{CC} = +24 V, V_{EE} = −24 V		9.4		mA
$I_{V_{EE}}$	V_{CC} = +24 V, V_{EE} = −24 V		−7.4		mA
$I_{V_{DD}}$	Reference and reference buffer enabled		11.6		mA
	V_{REFIO} = 4.096 V, REFIO overdriven[14]		9.6		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[19]		2.2		mA
$I_{V_{DDH}}$	V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled		8.4		mA
$I_{V_{DDL}}$	V_{DDH} = GND, 1.8 V LDO regulator disabled, V_{DDL} = 1.8 V		8.3		mA
$I_{V_{IO}}$	V_{IO} = 2.5 V		1		µA
Nap Mode					
$I_{V_{CC}}$	V_{CC} = +24 V, V_{EE} = −24 V		4.5		mA
$I_{V_{EE}}$	V_{CC} = +24 V, V_{EE} = −24 V		−3.3		mA
$I_{V_{DD}}$	Reference and reference buffer enabled		11.1		mA
	V_{REFIO} = 4.096 V, REFIO overdriven[14]		9.1		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[19]		1.8		mA
$I_{V_{DDH}}$	V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled		8.4		mA
$I_{V_{DDL}}$	V_{DDH} = GND, 1.8 V LDO regulator disabled, V_{DDL} = 1.8 V		8.3		mA
$I_{V_{IO}}$	V_{IO} = 2.5 V		1		µA
Power-Down Mode					
$I_{V_{CC}}$	V_{CC} = +24 V, V_{EE} = −24 V		18		µA
$I_{V_{EE}}$	V_{CC} = +24 V, V_{EE} = −24 V		−4		µA
$I_{V_{DD}}$			130		µA
$I_{V_{DDH}}$	V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled		30		µA
$I_{V_{DDL}}$	V_{DDH} = GND, 1.8 V LDO regulator disabled, V_{DDL} = 1.8 V		16		µA
$I_{V_{IO}}$	V_{IO} = 2.5 V		1		µA
POWER DISSIPATION	Reference and reference buffer enabled, V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled, V_{IO} = 2.5 V				
CMOS Conversion Data Output	25 pF load on CMOS outputs				
Operation Mode	f_S = 250 kSPS, all channels converting				
	V_{CC} = +24 V, V_{EE} = −24 V		568	776	mW
	V_{CC} = +15 V, V_{EE} = −15 V		380		mW
	V_{CC} = +8.2 V, V_{EE} = −3.2 V		207		mW
Acquisition Mode	V_{CC} = +24 V, V_{EE} = −24 V		457		mW
Nap Mode	V_{CC} = +24 V, V_{EE} = −24 V		239		mW
Power-Down Mode	V_{CC} = +24 V, V_{EE} = −24 V		1.3		mW
LVDS Conversion Data Output	100 Ω differential load on LVDS outputs				
Operation Mode	f_S = 250 kSPS, all channels converting				
	V_{CC} = +24 V, V_{EE} = −24 V		593	806	mW
	V_{CC} = +15 V, V_{EE} = −15 V		405		mW
	V_{CC} = +8.2 V, V_{EE} = −3.2 V		232		mW
Acquisition Mode	V_{CC} = +24 V, V_{EE} = −24 V		482		mW
Nap Mode	V_{CC} = +24 V, V_{EE} = −24 V		264		mW
Power-Down Mode	V_{CC} = +24 V, V_{EE} = −24 V		1.3		mW

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING TEMPERATURE RANGE[23]					
T_{MIN}		−40			°C
T_{MAX}				+125	°C

[1] Positive analog-input pin voltage.

[2] Negative analog-input pin voltage.

[3] REFBUF pin voltage scaled by (1/1.024), nominally 4 V.

[4] REFBUF pin voltage, nominally 4.096 V.

[5] Common-mode voltage of the positive analog-input pin and the negative analog-input pin.

[6] Exceeding these limits on any channel may corrupt conversion results on other channels. Driving an analog input greater than V_{CC} on any channel up to 10 mA does not affect conversion results on other channels. Driving an analog input less than V_{EE} may corrupt conversion results on other channels. Refer to the Analog Input Overdrive Tolerance section for further details. Refer to the Absolute Maximum Ratings section for pin voltage and current limits related to device reliability.

[7] Positive analog-input pin resistance.

[8] Negative analog-input pin resistance.

[9] Positive analog-input pin capacitance.

[10] Negative analog-input pin capacitance.

[11] A plot of the input-referred transition noise vs. the differential input level with SHDR on and off is shown in Figure 18.

[12] LSB vs. SoftSpan shown in Table 12.

[13] These specifications are measured while externally supplying V_{REFIO} = 4.096 V with the internal band-gap reference powered down. The specifications do not include nominal value or the temperature drift terms associated with the internal band-gap.

[14] When REFIO is overdriven, the internal band-gap reference must be disabled using the Device Control Register.

[15] All specifications in dB are referred to a full-scale input in the relevant SoftSpan input range, except for crosstalk, which is referred to the crosstalk injection signal amplitude, and the THD, which is referred to the fundamental input signal amplitude.

[16] A plot of dynamic range vs. oversampling ratio (OSR) is shown in Figure 34.

[17] Sine wave at frequency on injection channel (f_{INJ}) = 100 kHz and second sine wave at frequency on receiver channels (f_{RCV}) = 1 kHz.

[18] Temperature coefficient is calculated by dividing the maximum change in the output voltage by the specified temperature range (T_{MAX} − T_{MIN}).

[19] When REFBUF is overdriven, the internal band-gap reference and reference buffer must be disabled using the Device Control Register.

[20] I_{REFBUF} varies proportionally with the sample rate and the number of active channels.

[21] Enable or disable the LVDS termination resistance and half-bias mode using the Device Control Register.

[22] A plot of the CMOS operating mode currents vs. sample rate is shown in Figure 33.

[23] Refer to the Absolute Maximum Ratings section and the Junction Temperature section for the junction temperature limits related to device reliability.

SPECIFICATIONS

TIMING SPECIFICATIONS

V_{EE} = −40.75 V to 0 V, V_{CC} = 7.25 V to 48 V, (V_{CC} − V_{EE}) = 10 V to 48 V, V_{DD} = 5 V, V_{DDH} = 2.5 V, 1.8 V LDO regulator enabled, and V_{IO} = 0.9 V to 5.25 V. All channels convert at sampling frequency (f_S) = 250 kSPS, internal reference and reference buffer enabled, all SoftSpan ranges, fully-differential input signal drive in SoftSpan 15 and SoftSpan 13, true bipolar or unipolar signal drive in other bipolar or unipolar SoftSpan ranges, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C. Interface timing tested using a 25 pF load capacitance on CMOS outputs, a 100 Ω differential termination resistance between LVDS output differential pairs, internal termination resistance enabled on LVDS input differential pairs, LVDS full-bias mode enabled, and V_{ICM} = 1.2 V and V_{ID} = ±350 mV on LVDS input differential pairs.

Table 2. Universal Timing

Parameter	Symbol	Min	Typ	Max	Unit
Sampling Frequency	f_S	0		250	kSPS
Time Between Conversions	t_{CYC}	4000			ns
Conversion Time	t_{CONV}	605	665	725	ns
Acquisition Phase[1]	t_{ACQ}	3465			ns
CNV High Time	t_{CNVH}	40			ns
CNV Low Time	t_{CNVL}	750			ns
CNV Rising Edge to BUSY Rising Edge Delay	$t_{DCNVBUSY}$			15	ns
Data Valid to BUSY Falling Edge Delay	$t_{DSDOBUSY}$	2			ns
Last SCKI Edge to CNV Rising Edge	$t_{SCKICNV}$	20			ns
PD High Time	t_{PDH}	40			ns
PD Low Time	t_{PDL}	40			ns
Device Wake Time to Ready to Convert	t_{WAKE}			1	ms
Device Power-On-Reset Time	t_{POR}			1	ms

[1] The acquisition phase is the time available for the ADCs to acquire a new input with the DAS running at a throughput rate of 250 kSPS.

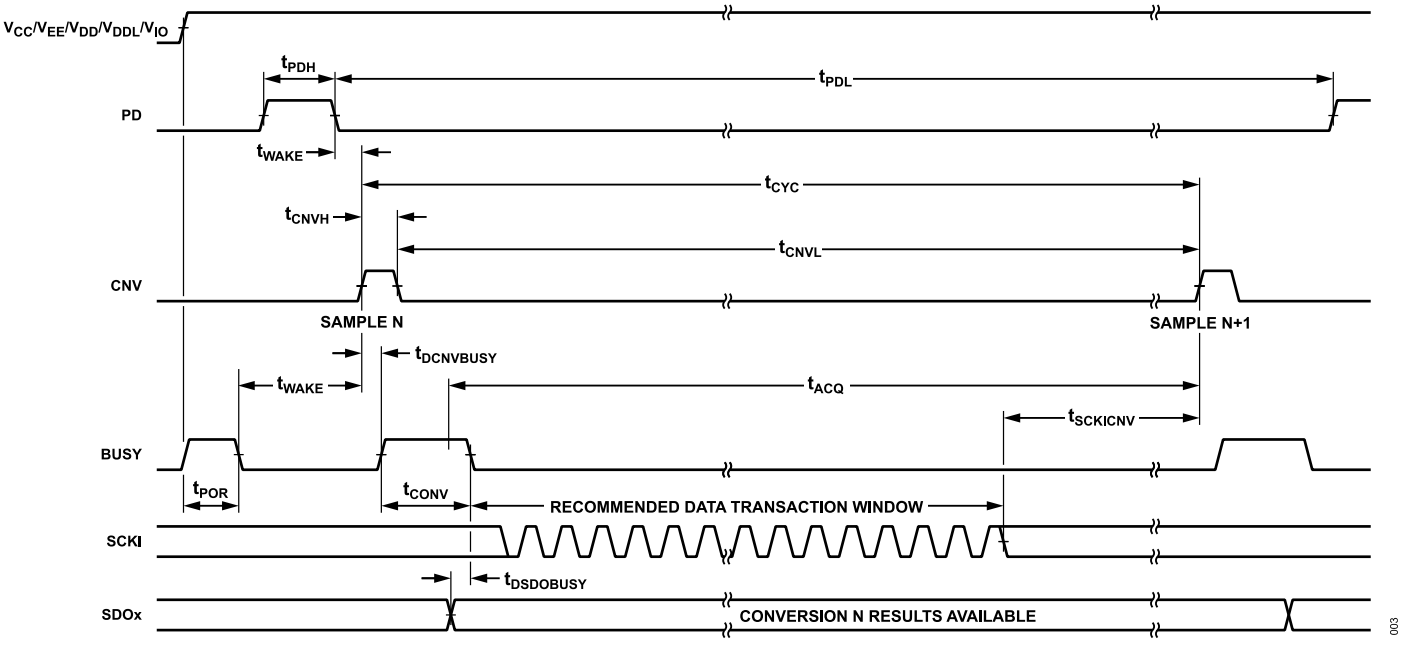

Figure 2. Universal Timing

SPECIFICATIONS

Table 3. SPI Register Configuration Bus Read/Write Timing

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ Low Time	t_{CSL}	15			ns
$\overline{CS}$ High Time	t_{CSH}	15			ns
$\overline{CS}$ Falling Edge to First CSCK Rising Edge	t_{CSCSCK}	15			ns
CSCK Period	t_{CSCK}	40			ns
CSCK Low Time	t_{CSCKL}	16			ns
CSCK High Time	t_{CSCKH}	16			ns
Last CSCK Edge to $\overline{CS}$ Rising Edge	t_{CSCKCS}	15			ns
CSDIO Valid Setup Time to CSCK Rising Edge	$t_{SCSDIOI}$	4			ns
CSDIO Valid Hold Time from CSCK Rising Edge	$t_{HCSDIOI}$	1			ns
CSCK 16th Rising Edge to CSDIO 3-Wire Output State Delay	t_{DIO}	2		10	ns
CSCK Falling Edge to CSDIO Data Valid Delay	$t_{DCSDIOO}$			11	ns
CSCK Falling Edge to CSDIO Data Remains Valid	$t_{HCSDIOO}$	1			ns
CSCK Falling Edge to CSDO Data Valid Delay	t_{DCSDO}			11	ns
CSCK Falling Edge to CSDO Data Remains Valid	t_{HCSDO}	1			ns
$\overline{CS}$ Falling Edge to 4-Wire Bus Low Impedance Delay	t_{DCSEN}			15	ns
$\overline{CS}$ Rising Edge to Bus High Impedance Delay	t_{DCSDIS}			15	ns

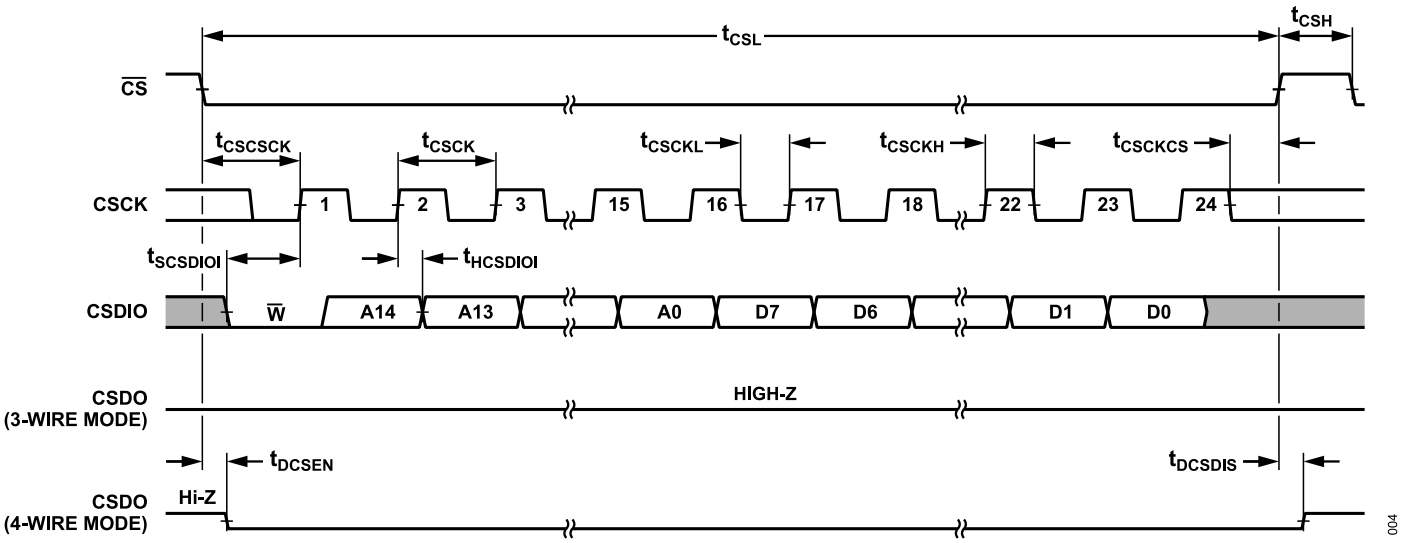

Figure 3. SPI Register Configuration Bus Write Timing

SPECIFICATIONS

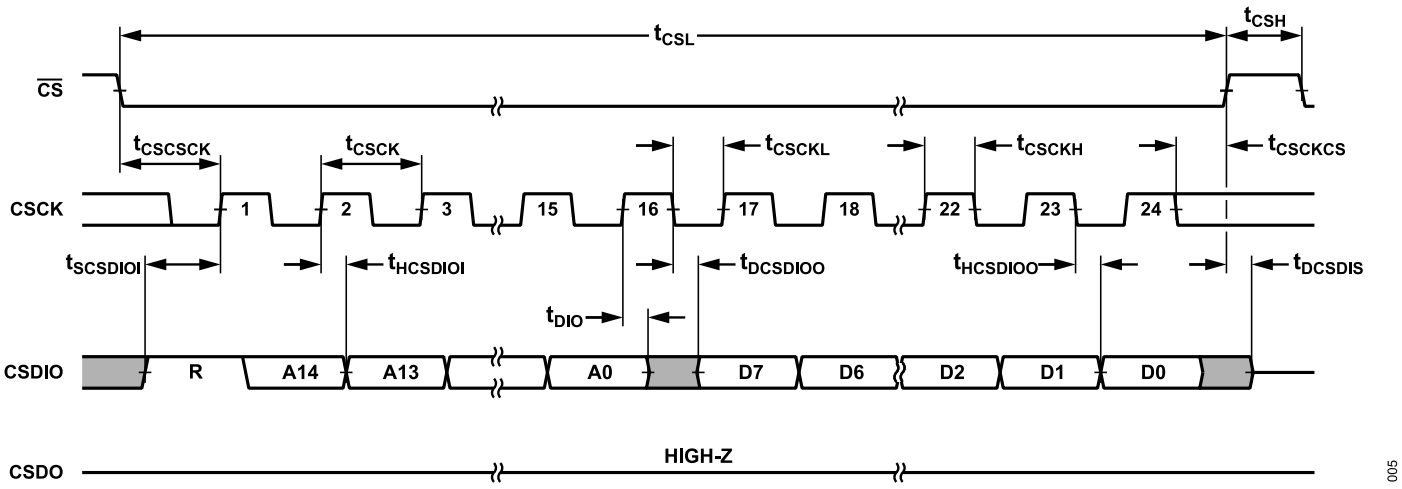

Figure 4. SPI Register Configuration Bus 3-Wire Read Timing

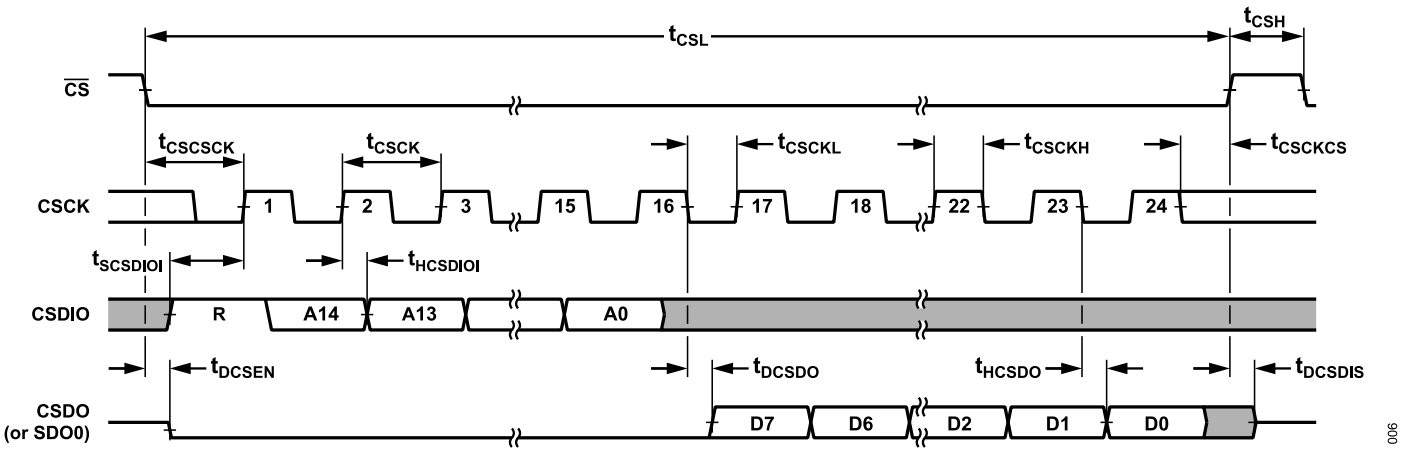

Figure 5. SPI Register Configuration Bus 4-Wire Read Timing

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Table 4. CMOS Conversion Data Output Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCKI Period	t_{SCKI}	10			ns
SCKI High Time	t_{SCKIH}	4			ns
SCKI Low Time	t_{SCKIL}	4			ns
SCKI Rising Edge to SDOx Data Valid Delay	t_{DSDO}			7.5	ns
SCKI Rising Edge to SDOx Remains Valid	t_{HSDO}	1.5			ns
Skew Between SDOx Data and SCKO	t_{SKEW}	−1	0	+1	ns
$\overline{CS}$ High Time	t_{CSH}	15			ns
$\overline{CS}$ Low Time	t_{CSL}	15			ns
$\overline{CS}$ Falling Edge to Bus Low Impedance Delay	t_{DCSEN}			15	ns
$\overline{CS}$ Rising Edge to Bus High Impedance Delay	t_{DCSDIS}			15	ns
$\overline{CS}$ Falling Edge to First SCKI Rising Edge	t_{CSSCKI}	15			ns
Last SCKI Edge to $\overline{CS}$ Rising Edge	t_{SCKICS}	15			ns
Last SCKI Edge to CNV Rising Edge	$t_{SCKICNV}$	20			ns

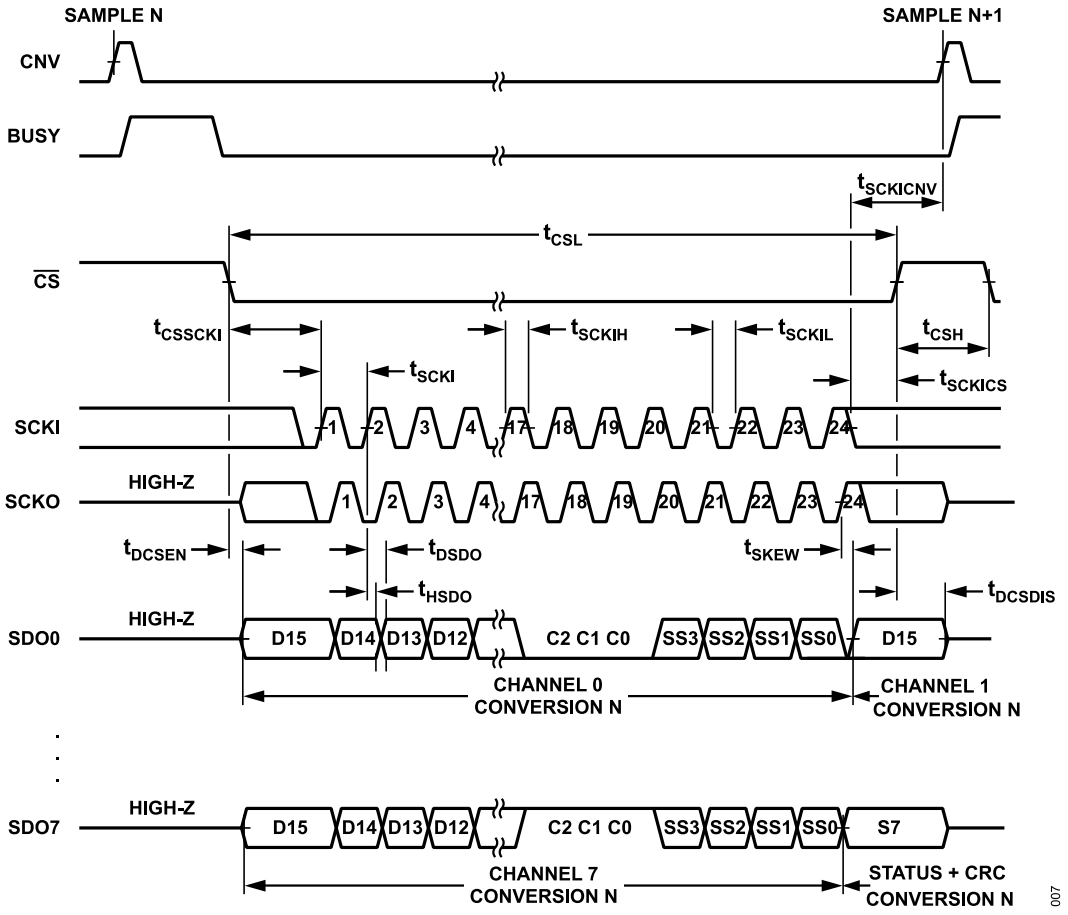


Figure 6. CMOS Conversion Data Bus Timing

SPECIFICATIONS

Table 5. LVDS Conversion Data Output Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCKI Period	t_{SCKI}	2.5			ns
SCKI High Time	t_{SCKIH}	0.75			ns
SCKI Low Time	t_{SCKIL}	0.75			ns
SCKI Edge to SDO Data Valid Delay	t_{DSDO}			7.5	ns
SCKI Edge to SDO Data Remains Valid	t_{HSDO}	1.5			
SDO to SCKO Skew	t_{SKEW}	−0.25	0	+0.25	ns
$\overline{CS}$ High Time	t_{CSH}	15			ns
$\overline{CS}$ Low Time	t_{CSL}	75			ns
$\overline{CS}$ Falling Edge to Bus Low Impedance Delay	t_{DCSEN}			75	ns
$\overline{CS}$ Rising Edge to Bus High Impedance Delay	t_{DCSDIS}			15	ns
$\overline{CS}$ Falling Edge to First SCKI Rising Edge	t_{CSSCKI}	75			
Last SCKI Falling Edge to $\overline{CS}$ Rising Edge	t_{SCKICS}	15			
Last SCKI Edge to CNV Rising Edge	$t_{SCKICNV}$	20			ns

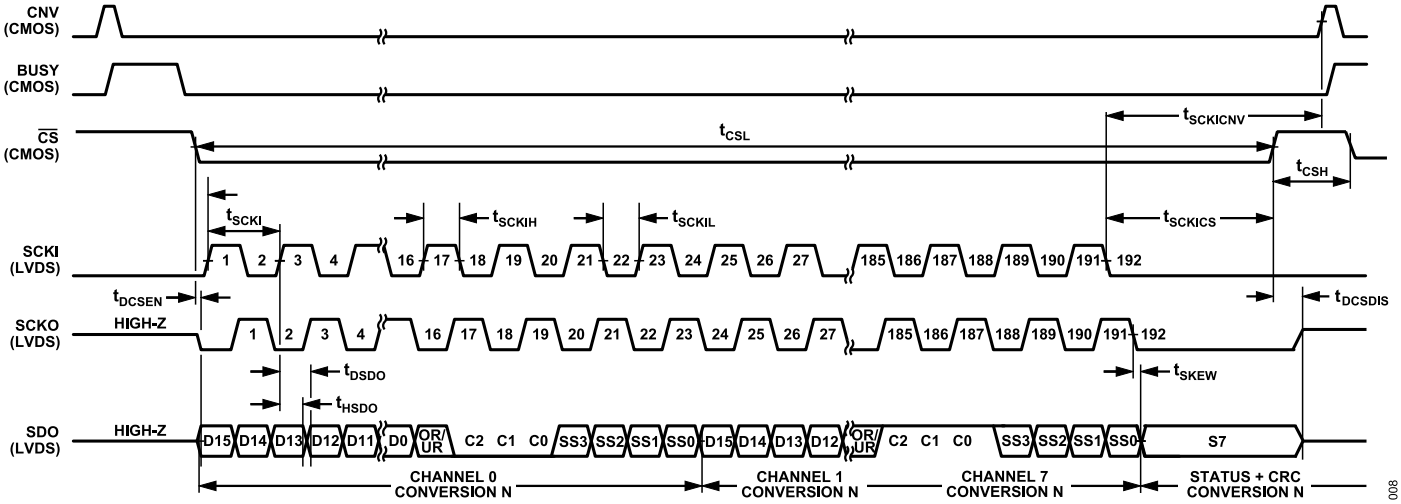


Figure 7. LVDS Conversion Data Bus Timing

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Rating
Analog Input and Output Voltages	
IN0+ to IN7+ and IN0− to IN7−	(V_{EE} − 0.3 V) to (V_{CC} + 0.3 V)
REFIO, REFBUF, and REF2500 to GND	−0.3 V to (V_{DD} + 0.3 V)
Supply Voltages	
V_{CC} to GND	−0.3 V to (V_{EE} + 50.4 V)
V_{EE} to GND	(V_{CC} − 50.4 V) to +0.3 V
V_{CC} to V_{EE}	50.4 V
V_{DD} and V_{DDH} to GND	−0.3 V to +6 V
V_{DDL} to GND	−0.3 V to +2.1 V
V_{IO} to GND[1]	
HIVIO/$\overline{\text{LOVIO}}$ = GND	−0.3 V to +2.1 V
HIVIO/$\overline{\text{LOVIO}}$ = V_{DD}	−0.3 V to +6 V
IOGND to GND	−0.3 V to +0.3 V
Digital Input Voltages	
CNV and HIVIO/$\overline{\text{LOVIO}}$ to GND	−0.3 V to (V_{DD} + 0.3 V)
All Other Inputs to GND	−0.3 V to (V_{IO} + 0.3 V)
Digital Output Voltages	−0.3 V to (V_{IO} + 0.3 V)
Transient Latchup Currents[2]	
IN0+ to IN7+ and IN0− to IN7−	
V_{CC} − V_{EE} ≤ 44 V	±100 mA
V_{CC} − V_{EE} > 44 V	±10 mA
All other inputs and outputs	±100 mA
Temperature	
Storage Range	−65°C to +150°C
Operating Junction Range[3]	−40°C to +105°C
Maximum Reflow (Package)	260°C

[1] The absolute maximum ratings of V_{IO} depend on the selected state of the HIVIO/$\overline{\text{LOVIO}}$ pin.

[2] Adding an external resistor in series with each of the INx+ and INx– pins is recommended in applications where V_{CC} − V_{EE} > 44 V to limit latchup current to these levels during fault conditions. See the Analog Input Overdrive Tolerance section for further information.

[3] The maximum junction temperature for continuous operation with nonderated device lifetime is 105°C. See the Junction Temperature section for more details.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

JUNCTION TEMPERATURE

The maximum junction temperature for continuous operation with nonderated device lifetime is 105°C. Operation at junction temperatures up to 125°C is also supported, with device specifications that are guaranteed from −40°C to +125°C. To avoid a reduction in operating lifetime due to operating at a temperature greater than 105°C, the device must operate at a temperature less than 105°C for a compensating time period (t_{COMP}) determined by the following equation:

$$t_{COMP} = (AF_{T>105} - 1)/(1 - AF_{T<105}) \quad (1)$$

where $AF_{T>105}$ and $AF_{T<105}$ are acceleration factors that are a function of the junction operating temperature.

For example, if the device operates at 115°C for 1 hour, the expected device lifetime is maintained if the device operates at 95°C for a compensating time period of 3.2 hours.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JCT} is the junction to case top thermal resistance. θ_{JCB} is the junction to case bottom thermal resistance.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JCT}	θ_{JCB}	Unit
05-08-7086	26.4	13.0	4.9	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4855

Table 8. AD4855, 64-Ball BGA

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±750	C4

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

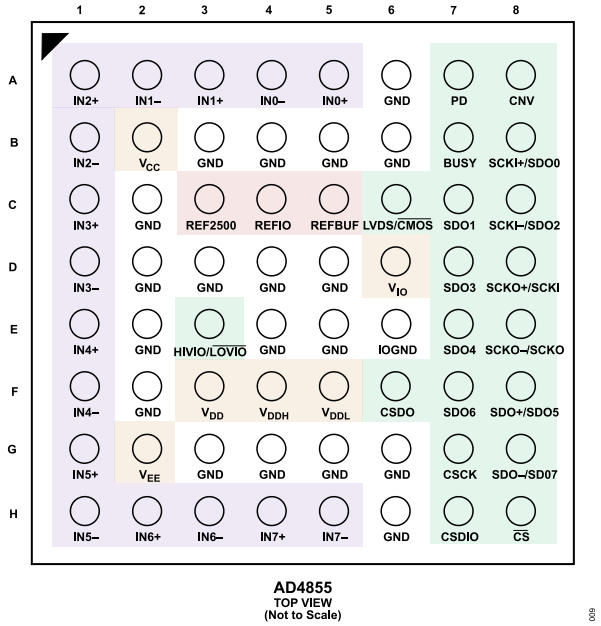


Figure 8. Pin Configuration

Table 9. Universal Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A5 and A4, A3 and A2, A1 and B1, C1 and D1, E1 and F1, G1 and H1, H2 and H3, H4 and H5	IN0+ and IN0− to IN7+ and IN7−	AI	Channel 0 to Channel 7 Positive and Negative Analog Inputs. The converter simultaneously samples and digitizes ($V_{INx+} - V_{INx-}$) for all channels. The wide input common-mode range and high common-mode rejection allow the inputs to accept arbitrary signal swings. The full-scale differential input range is determined by the SoftSpan configuration of each channel.
A6, B3 to B6, C2, D2 to D5, E2, E4, E5, F2, G3 to G6, H6	GND	P	Power Supply Ground. Solder all GND pins to a solid ground plane.
A7	PD	DI	Power Down Input. Bring the PD pin high to power down the device. If the PD pin is brought high while the BUSY pin is high, power down begins once the BUSY pin goes low. Bringing the PD pin high twice without an intervening conversion initiates a global device reset, equivalent to a POR event. Logic levels are determined by the V_{IO} supply.
A8	CNV	DI	Convert Input. A rising edge on the CNV pin initiates a new conversion. This signal must have low jitter to achieve specified device performance levels. The CNV high and low threshold voltages are 0.8 V and 0.4 V, respectively.
B2	V_{CC}	P	Analog Input Buffers Positive Power Supply. Connect the V_{CC} pin to an external supply between 7.25 V and 48 V with respect to the GND pins and between 10 V and 48 V with respect to the V_{EE} pin. The V_{CC} pin is internally bypassed to the GND pins with a 0.1 µF ceramic capacitor.
B7	BUSY	DO	Busy Output. The BUSY pin goes high at the start of each conversion (or oversampling window) and returns low once the conversion (or oversampling window) is complete. The BUSY pin also goes high during the start of power-on-reset and goes low once power-on-reset completes. Logic levels are determined by the V_{IO} supply.
C3	REF2500	AO	2.5 V Scaled Reference Output. The REF2500 pin outputs a precision scaled version of the REFIO pin voltage, nominally $V_{REFIO} \times (2.500/4.096)$. If connecting REF2500 externally, see the DAS Reference section for recommended use cases and precautions.
C4	REFIO	AI or AO	Band-gap Reference Output and Reference Buffer Input. An internal band-gap reference nominally outputs 4.096 V on the REFIO pin. The REFIO pin is internally bypassed to the GND pins with a 10 nF ceramic capacitor to filter the band-gap output noise. If the REFIO pin is overdriven with an external 4.096 V reference, disable the internal reference through the Device Control Register. If connecting the REFIO pin externally, see the DAS Reference section for recommended uses cases and precautions.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Universal Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
C5	REFBUF	AI or AO	Reference Buffer Output. An internal unity-gain reference buffer creates the converter main reference voltage, $V_{REFBUF} = V_{REFIO}$ on the REFBUF pin, nominally 4.096 V when using the internal band-gap reference. If the REFBUF pin is overdriven with an external 4.096 V reference, disable the internal reference buffer and band-gap reference through the Device Control Register and bypass the REFBUF pin to GND (pin B4) close to the REFBUF pin with an external 47 µF ceramic capacitor. If connecting the REFBUF pin externally, see the DAS Reference section for recommended uses cases and precautions.
C6	LVDS/$\overline{\text{CMOS}}$	DI	Conversion Data Bus Mode Select. Tie the LVDS/$\overline{\text{CMOS}}$ pin to the V_{IO} pin to select LVDS conversion data output mode or to the GND pins to select CMOS conversion data output mode. The state of the LVDS/$\overline{\text{CMOS}}$ pin does not affect the behavior of the SPI register configuration bus. Logic levels are determined by the V_{IO} supply.
D6[2]	V_{IO}	P	Digital Input and Output Power Supply. Connect the V_{IO} pin to an external supply between 0.9 V and 5.25 V with respect to the GND pins. The HIVIO/$\overline{\text{LOVIO}}$ pin must be tied appropriately based on application V_{IO} level. Tie the HIVIO/$\overline{\text{LOVIO}}$ pin to the V_{DD} pin for applications where 1.71 V ≤ V_{IO} ≤ 5.25 V or tie the HIVIO/$\overline{\text{LOVIO}}$ pin to the GND pins for applications where 0.9 V ≤ V_{IO} ≤ 1.89 V. Either tie option can be used when 1.71 V ≤ V_{IO} ≤ 1.89 V. The V_{IO} pin is internally bypassed to the IOGND pin with a 1 µF ceramic capacitor.
E3[2]	HIVIO/$\overline{\text{LOVIO}}$	DI	V_{IO} Voltage Mode Select. Tie the HIVIO/$\overline{\text{LOVIO}}$ pin to the V_{DD} pin for applications where 1.71 V ≤ V_{IO} ≤ 5.25 V or to the GND pins for applications where 0.9 V ≤ V_{IO} ≤ 1.89 V. Either tie option may be used when 1.71 V ≤ V_{IO} ≤ 1.89 V. Logic levels are determined by the V_{DD} supply.
E6	IOGND	P	Digital Input and Output Power Supply Ground. Solder the IOGND pin to the same ground plane as the GND pins.
F3	V_{DD}	P	5 V Power Supply. Connect the V_{DD} pin to an external 5 V supply. The V_{DD} pin is internally bypassed to the GND pins with a 1 µF ceramic capacitor.
F4	V_{DDH}	P	1.8 V LDO Regulator Power Supply. To supply the V_{DDL} pin using the internal 1.8 V LDO regulator, tie the V_{DDH} pin to the V_{DD} pin or to another external power supply between 2.2 V and 5.25 V. To disable the internal LDO regulator, tie the V_{DDH} pin to the GND pins as shown in Figure 61. The V_{DDH} pin is internally bypassed to the GND pins with a 1 µF ceramic capacitor.
F5	V_{DDL}	P	1.8 V Power Supply. To supply the V_{DDL} pin using the internal 1.8 V LDO regulator, tie the V_{DDH} pin to the V_{DD} pin or to another external power supply between 2.2 V and 5.25 V. Do not externally connect the V_{DDL} pin in this case. To externally supply the V_{DDL} pin, disable the internal LDO regulator by tying the V_{DDH} pin to the GND pins and connect the V_{DDL} pin to an external 1.8 V supply as shown in Figure 61. The V_{DDL} pin is internally bypassed to the GND pins with a 1 µF ceramic capacitor.
F6	CSDO	DO	SPI Register Configuration Bus Data Output. During 3-wire SPI register configuration bus operation, the CSDO pin remains high-Z. During 4-wire bus operation, the CSDO pin outputs serial data during read transactions. Logic levels are determined by the V_{IO} supply.
G2	V_{EE}	P	Analog Input Buffers Negative Power Supply. Connect the V_{EE} pin to an external supply between 0 V and −40.75 V with respect to the GND pins and between −10 V and −48 V with respect to the V_{CC} pin. The V_{EE} pin is internally bypassed to the GND pins with a 0.1 µF ceramic capacitor.
G7	CSCK	DI	SPI Register Configuration Bus Clock Input. Drive the CSCK pin with the SPI register configuration bus clock. The CSCK pin is allowed to idle either high or low. Logic levels are determined by the V_{IO} supply.
H7	CSDIO	DI and DO	SPI Register Configuration Bus Data Input and Output. During both 3- and 4-wire SPI register configuration bus operation, the CSDIO pin accepts serial input data. During 3-wire bus operation, the CSDIO pin also outputs serial data during read transactions. Logic levels are determined by the V_{IO} supply.
H8	$\overline{\text{CS}}$	DI	Chip Select Input. The SPI register configuration and conversion data buses are enabled when the $\overline{\text{CS}}$ pin is low and disabled and high-Z when the $\overline{\text{CS}}$ pin is high. Logic levels are determined by the V_{IO} supply.

[1] AI is analog input, AO is analog output, P is power, DI is digital input, and DO is digital output.

[2] The maximum operating and absolute maximum ratings of the V_{IO} supply, and associated digital inputs and outputs, are defined by the HIVIO/$\overline{\text{LOVIO}}$ pin state.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. CMOS Conversion Data Bus Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
B8, C7, C8, D7, E7, F7, F8, G8	SDO0 to SDO7	DO	Channel 0 to Channel 7 CMOS Conversion Data Outputs. Conversion results and optional channel status information are output on these pins synchronized to the SCKI pin. The SDO0 pin may also be configured through the SPI Configuration D Register to output SPI register configuration bus serial data during 4-wire read operations. Logic levels are determined by the V_{IO} supply.
D8	SCKI	DI	CMOS Conversion Data Clock Input. Drive the SCKI pin with the CMOS conversion data bus clock. The SCKI pin is allowed to idle either high or low. Logic levels are determined by the V_{IO} supply.
E8	SCKO	DO	CMOS Conversion Data Clock Output. The SCKO pin outputs a copy of the SCKI pin skew-matched to the serial output data on the SDO0 to SDO7 pins. If clock echoing is disabled through the Device Control Register, the SCKO pin is high-Z. Logic levels are determined by the V_{IO} supply.

[1] AI is analog input, AO is analog output, P is power, DI is digital input, and DO is digital output.

Table 11. LVDS Conversion Data Bus Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
B8 and C8	SCKI+ and SCKI−	DI	LVDS Conversion Data Clock Input. Differentially drive the SCKI+ and SCKI− pins with the LVDS conversion data bus clock. Idle the SCKI+ and SCKI− pins low (including when transitioning $\overline{CS}$). By default, the SCKI+ and SCKI− pins are internally terminated with a 100 Ω differential resistor when the $\overline{CS}$ pin is low. This termination can be disabled through the Device Control Register.
C7, D7, E7, F7	SDO1, SDO3, SDO4, SDO6	DO	CMOS Conversion Data Outputs. In LVDS conversion data output mode, the SDO1, SDO3, SDO4, and SDO6 pins are high-Z.
D8 and E8	SCKO+ and SCKO−	DO	LVDS Conversion Data Clock Output. The SCKO+ and SCKO− pins output a copy of the SCKI+ and SCKI− pins, skew-matched with the serial output data on the SDO+ and SDO− pins. The SCKO+ and SCKO− output pair must be differentially terminated with a 100 Ω resistor at the receiver field programmable gate array (FPGA). If clock echoing is disabled through the Device Control Register, these pins are high-Z.
F8 and G8	SDO+ and SDO−	DO	LVDS Conversion Data Output. Conversion results and optional channel status information are output on these pins synchronized to the SCKI+ and SCKI− pins. The SDO+ and SDO− output pair must be differentially terminated with a 100 Ω resistor at the receiver (FPGA).

[1] AI is analog input, AO is analog output, P is power, DI is digital input, and DO is digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{EE} = −24 V, V_{CC} = +24 V, V_{DD} = +5 V, V_{DDH} = +2.5 V, 1.8 V LDO regulator enabled, V_{IO} = +2.5 V, f_S = 250 kSPS, internal reference and reference buffer enabled, fully-differential input signal drive in SoftSpan 15 and SoftSpan 13, true bipolar or unipolar signal drive in other bipolar or unipolar SoftSpan ranges, and T_A = 25°C, unless otherwise noted.

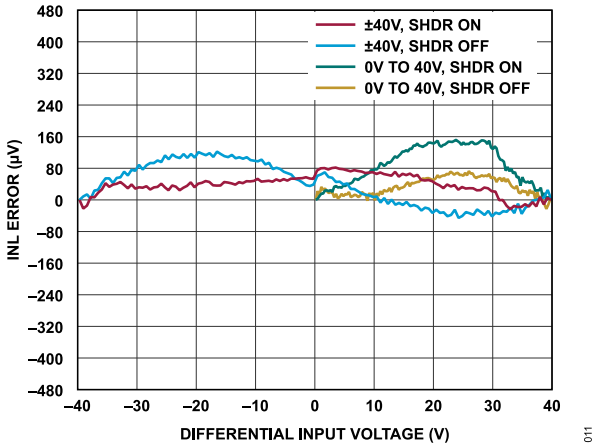


Figure 9. INL Error vs. Differential Input Voltage, SoftSpan 15 to SoftSpan 14

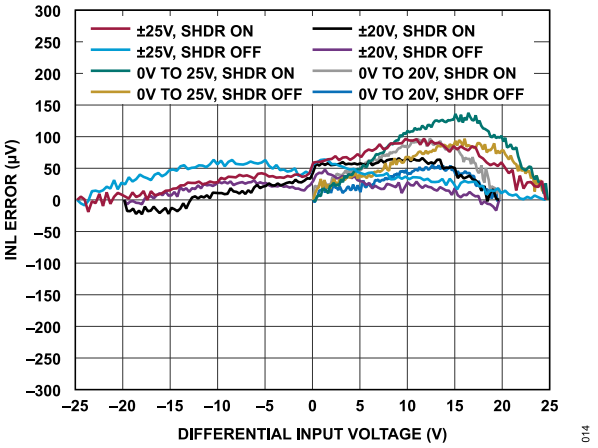


Figure 12. INL Error vs. Differential Input Voltage, SoftSpan 13 to SoftSpan 10

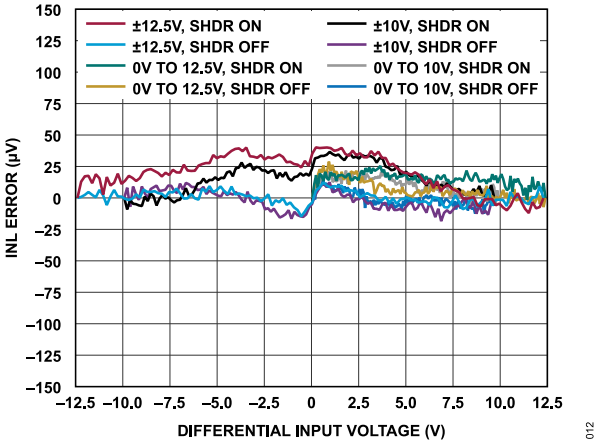


Figure 10. INL Error vs. Differential Input Voltage, SoftSpan 9 to SoftSpan 6

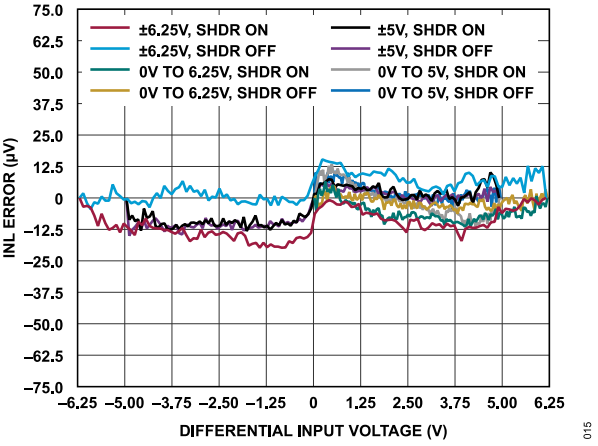


Figure 13. INL Error vs. Differential Input Voltage, SoftSpan 5 to SoftSpan 2

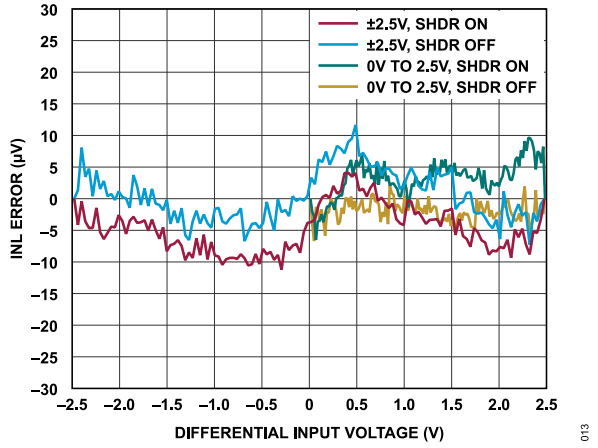


Figure 11. INL Error vs. Differential Input Voltage, SoftSpan 1 to SoftSpan 0

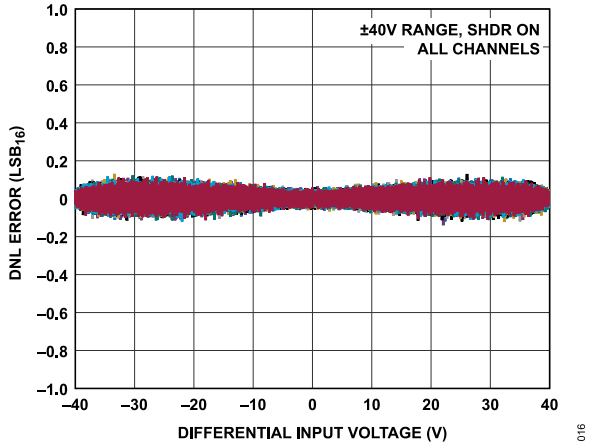


Figure 14. DNL Error vs. Differential Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

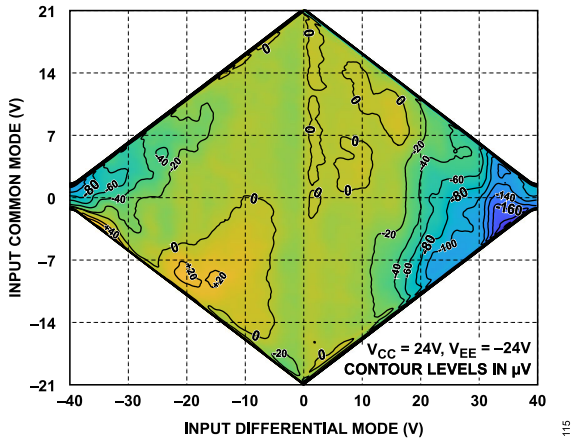


Figure 15. INL Error vs. Input Common Mode and Input Differential Voltage

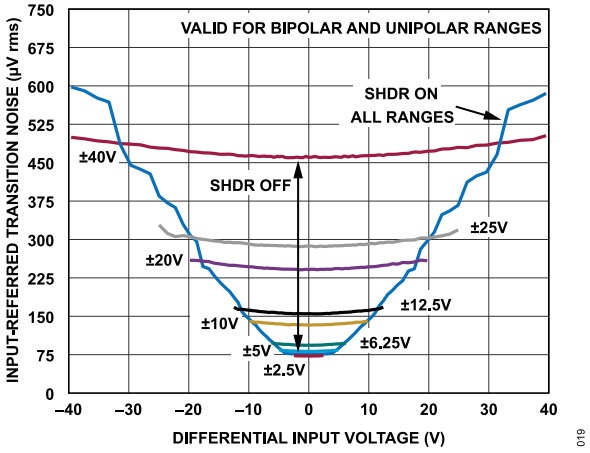


Figure 18. Input-Referred Transition Noise vs. Differential Input Voltage

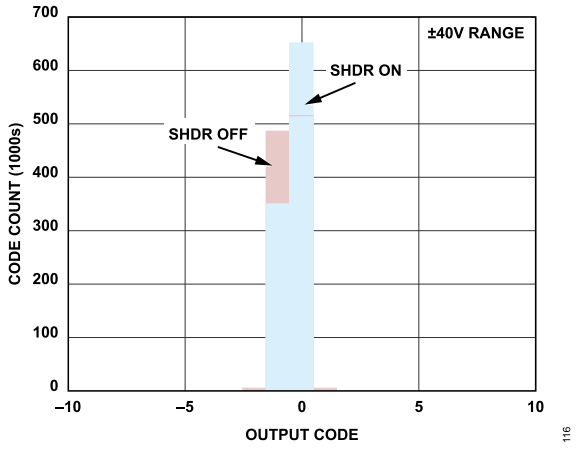


Figure 16. DC Code Histogram, Near Zero Scale

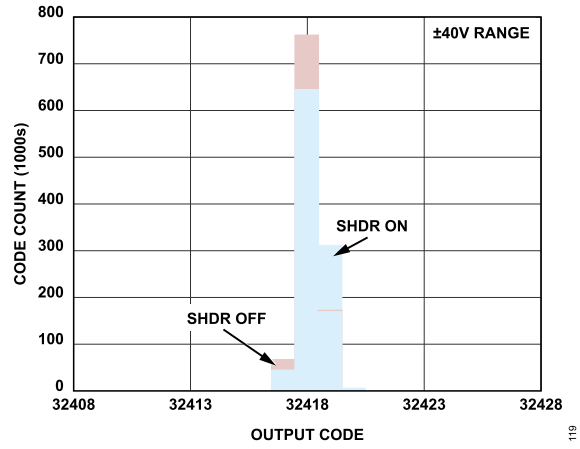


Figure 19. DC Code Histogram, Near Full Scale

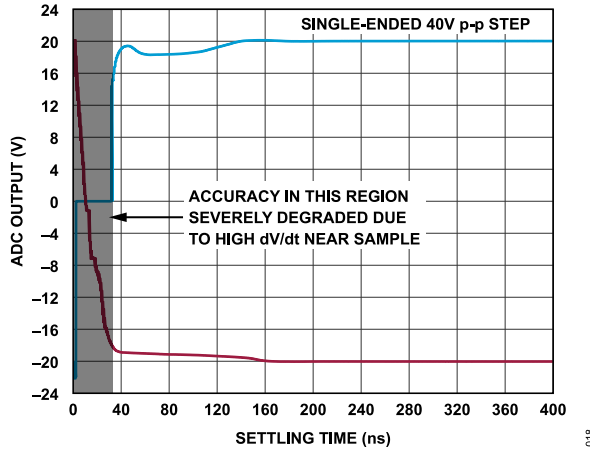


Figure 17. Input Step Response, Large Signal Settling

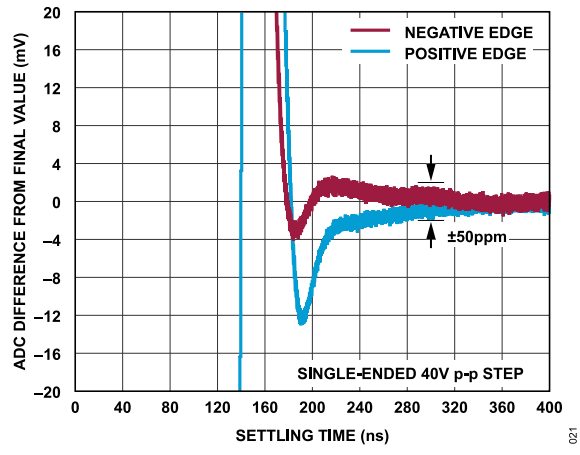


Figure 20. Input Step Response, Fine Settling

TYPICAL PERFORMANCE CHARACTERISTICS

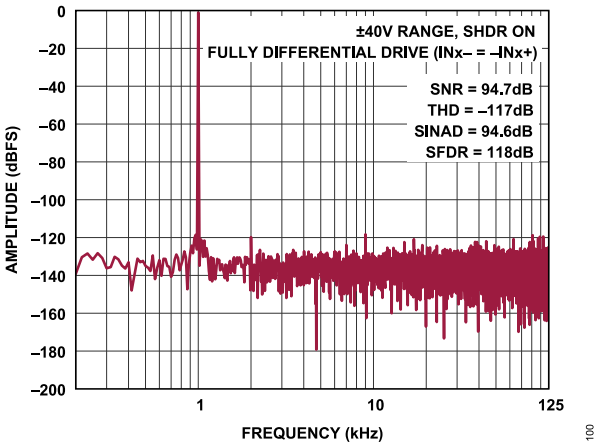


Figure 21. FFT, 250 kSPS, f_{IN} = 1 kHz, ±40 V Range

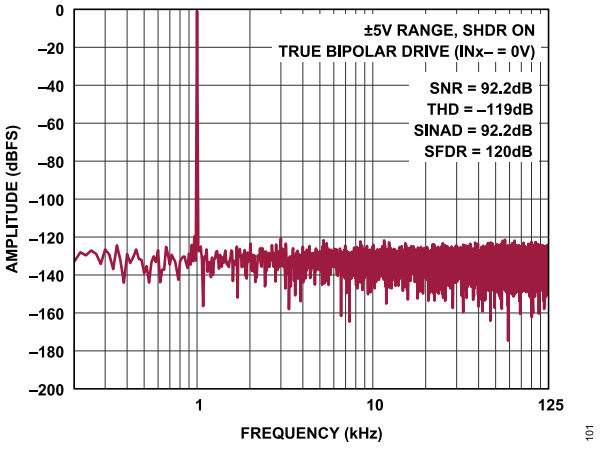


Figure 22. FFT, 250 kSPS, f_{IN} = 1 kHz, ±5 V Range

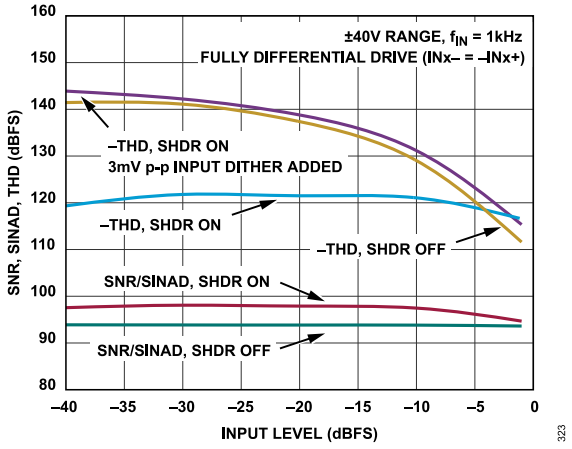


Figure 23. SNR, SINAD, and THD vs. Input Level

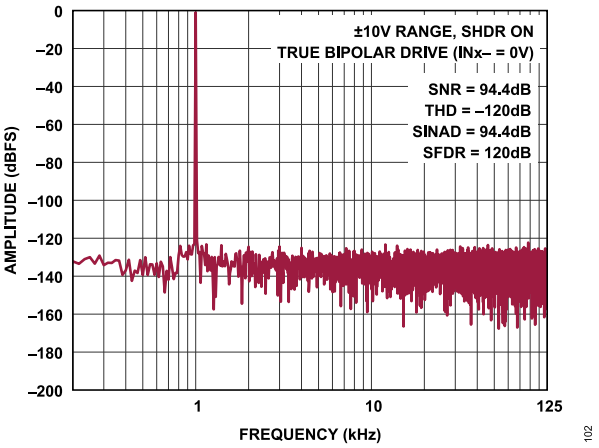


Figure 24. FFT, 250 kSPS, f_{IN} = 1 kHz, ±10 V Range

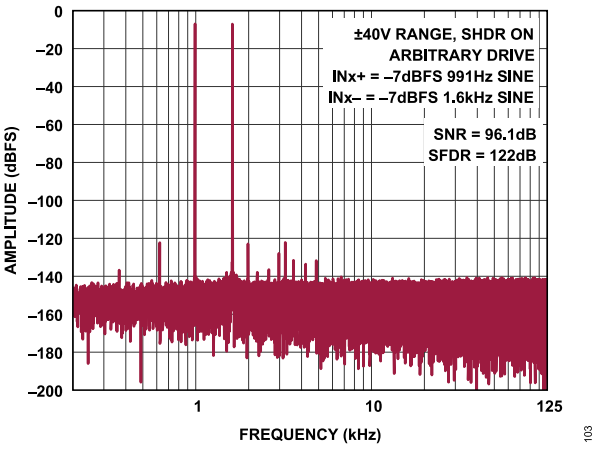


Figure 25. FFT, 250 kSPS, f_{INx+} = 991 Hz, f_{INx-} = 1.6 kHz, ±40 V Range

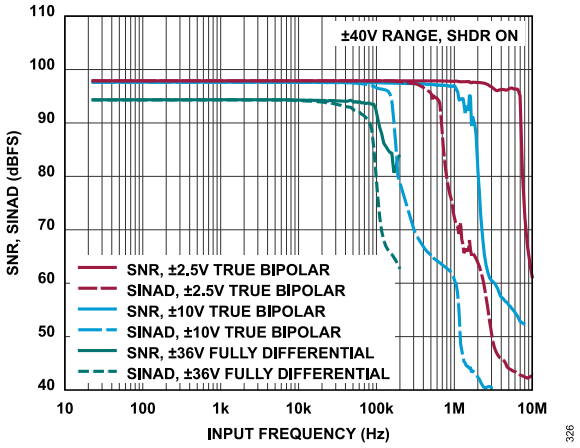


Figure 26. SNR and SINAD vs. Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

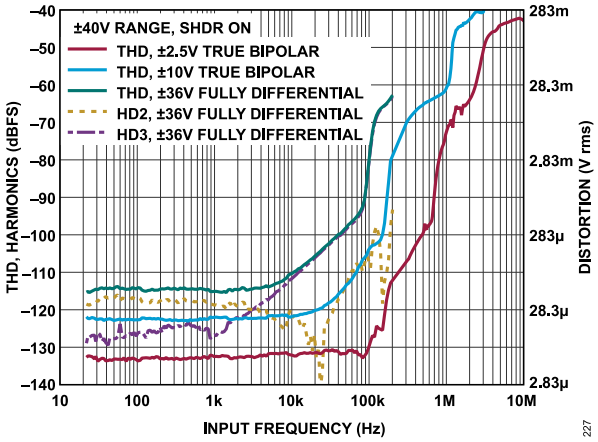


Figure 27. THD, Harmonics and Distortion vs. Input Frequency

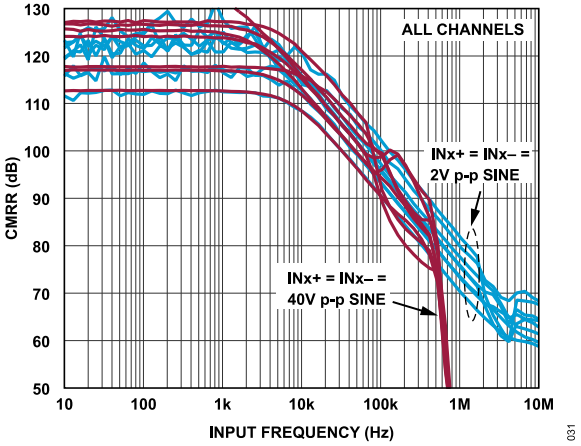


Figure 30. CMRR vs. Input Frequency

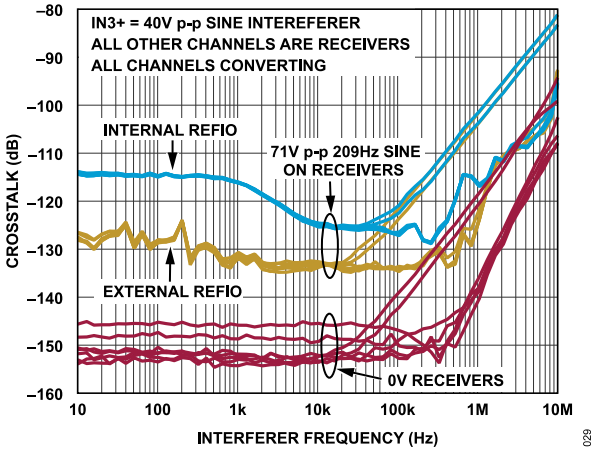


Figure 28. Crosstalk vs. Interferer Frequency

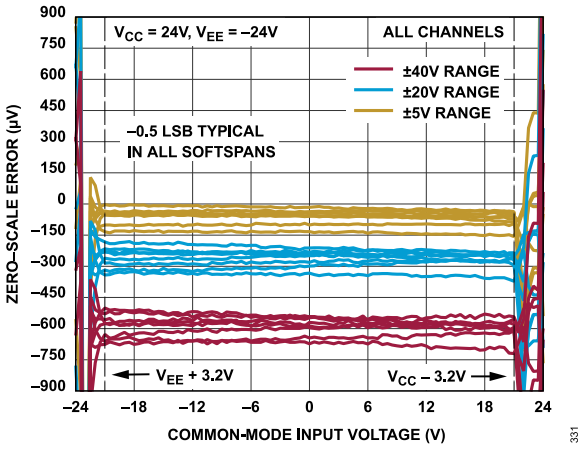


Figure 31. Zero-Scale Error vs. Common-Mode Input Voltage

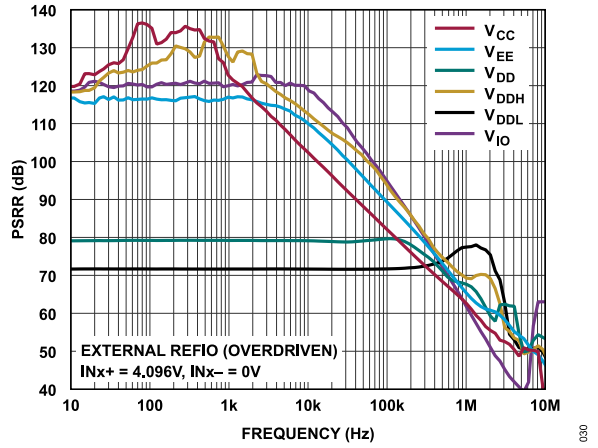


Figure 29. Power Supply Rejection Ratio (PSRR) vs. Frequency

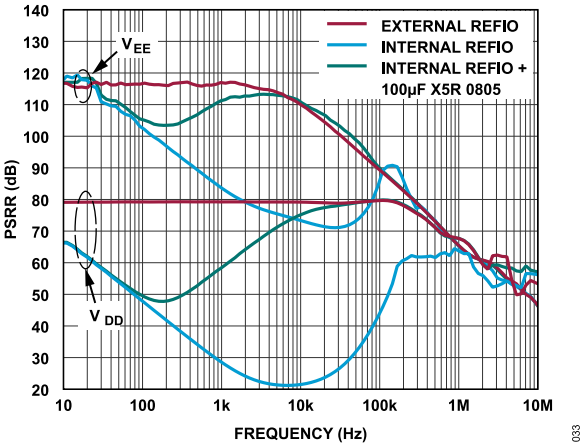


Figure 32. PSRR vs. Frequency, Internal and External Reference

TYPICAL PERFORMANCE CHARACTERISTICS

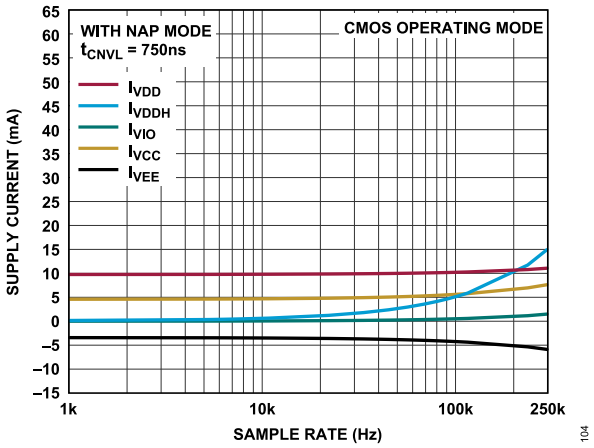


Figure 33. Supply Current vs. Sample Rate

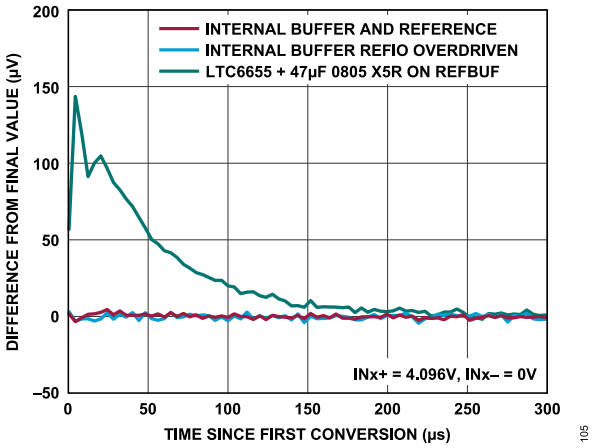


Figure 36. Burst Conversion Response, f_S = 250 kSPS

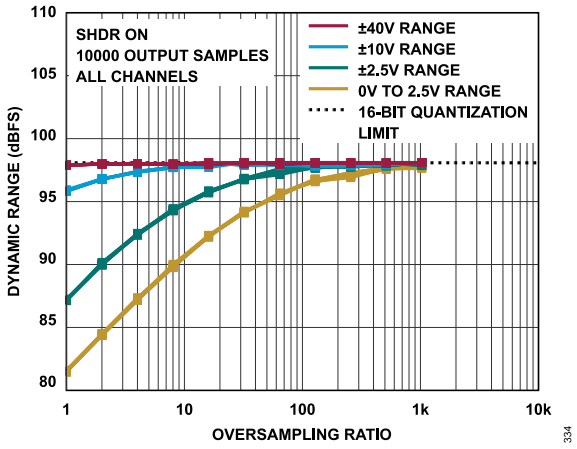


Figure 34. Dynamic Range vs. Oversampling Ratio

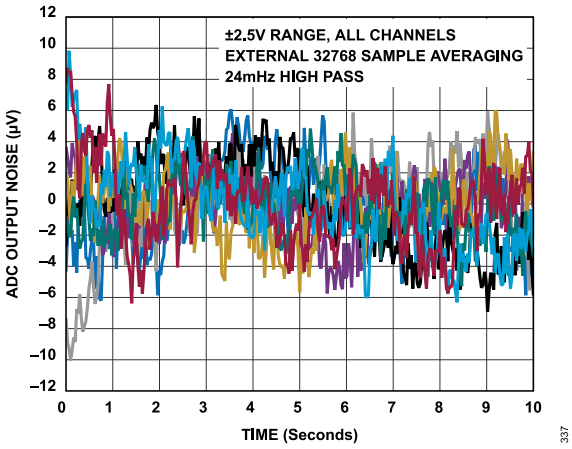


Figure 37. Low Frequency Noise over 10 Seconds

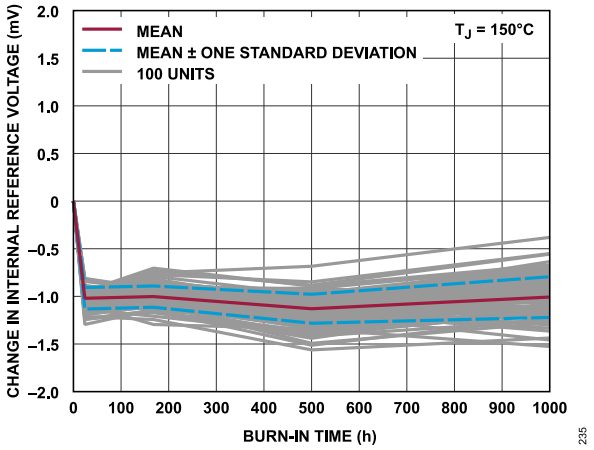


Figure 35. Change in Internal Reference Voltage vs. Burn-In Time

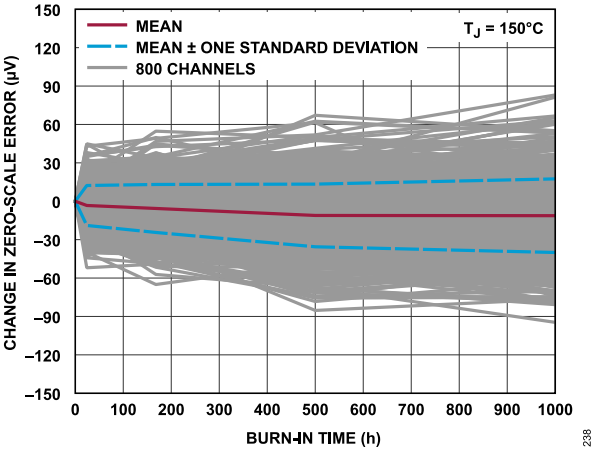


Figure 38. Change in Zero-Scale Error vs. Burn-In Time

TYPICAL PERFORMANCE CHARACTERISTICS

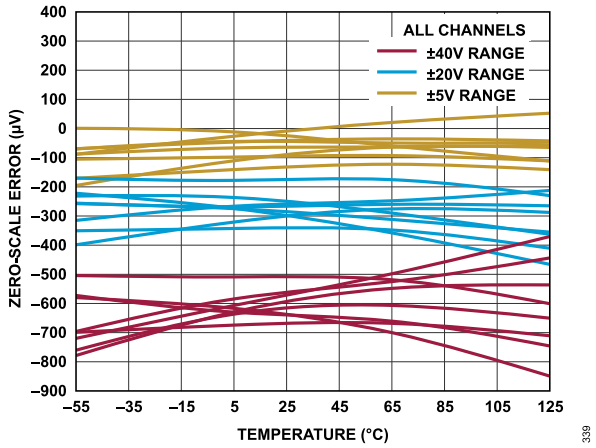


Figure 39. Zero-Scale Error vs. Temperature

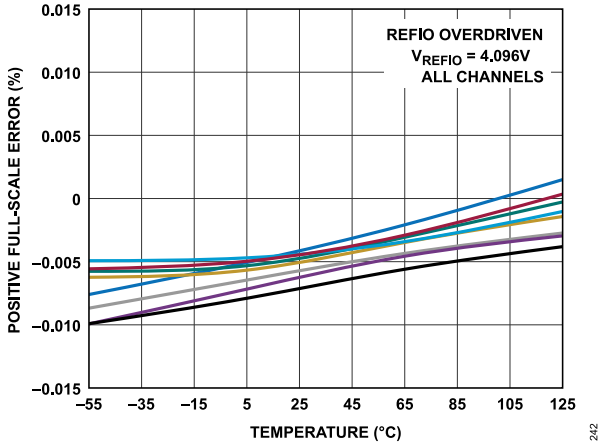


Figure 42. Positive Full-Scale Error vs. Temperature

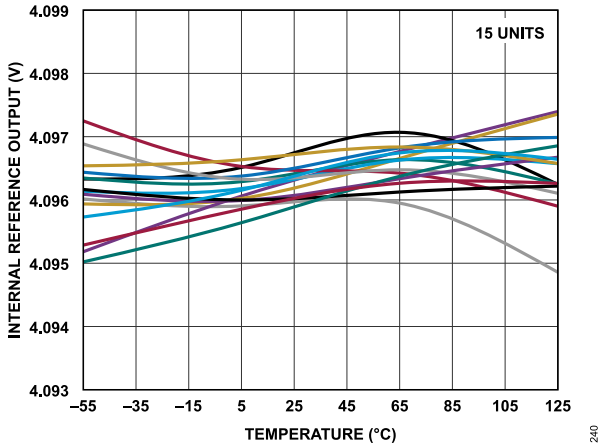


Figure 40. Internal Reference Output vs. Temperature

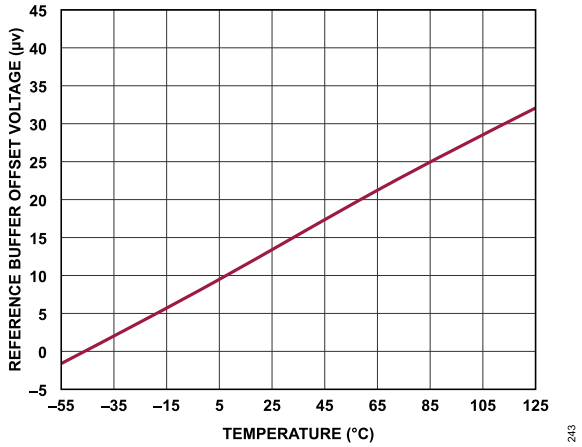


Figure 43. Reference Buffer Offset Voltage vs. Temperature

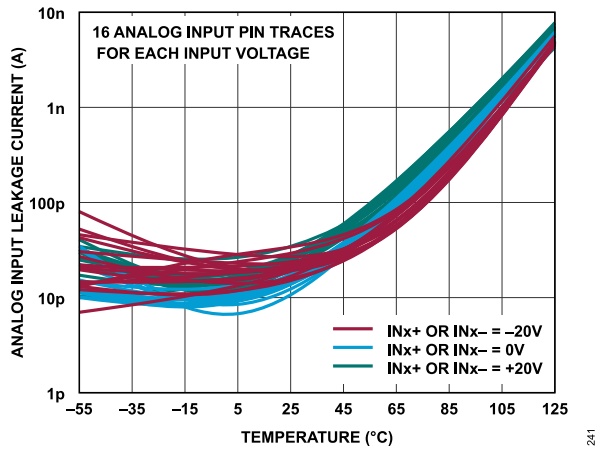


Figure 41. Analog Input Leakage Current vs. Temperature

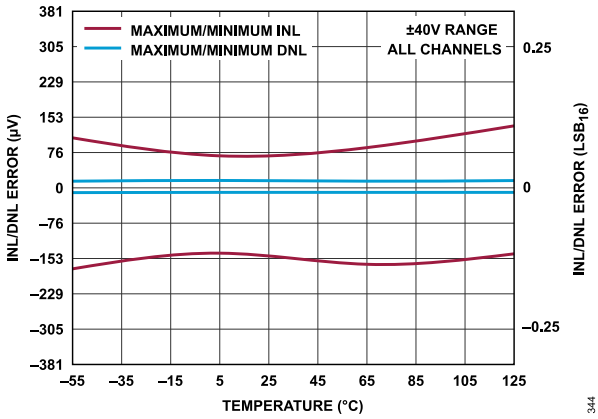


Figure 44. INL/DNL Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

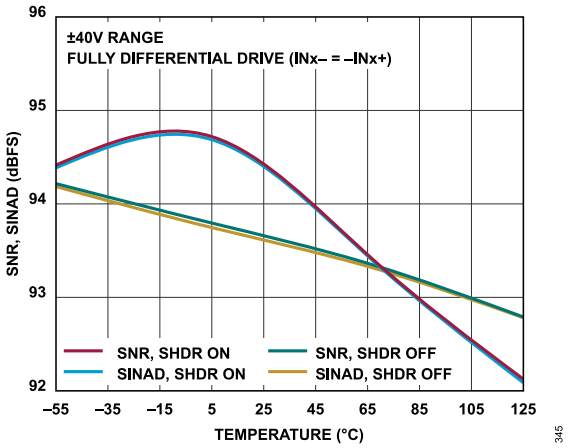


Figure 45. SNR and SINAD vs. Temperature

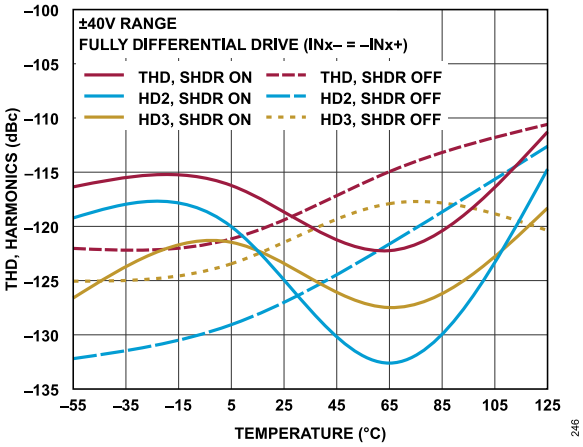


Figure 47. THD, Harmonics vs. Temperature

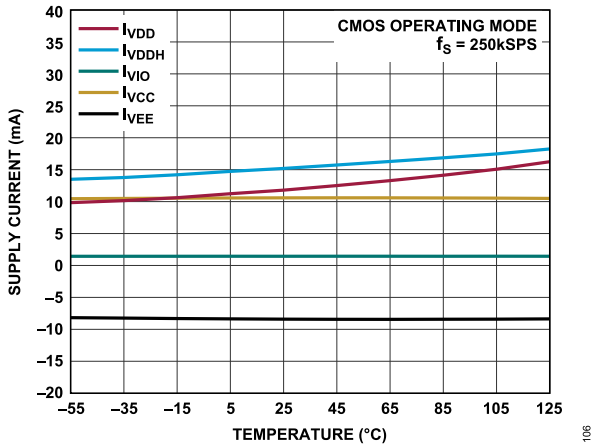


Figure 46. Supply Current vs. Temperature

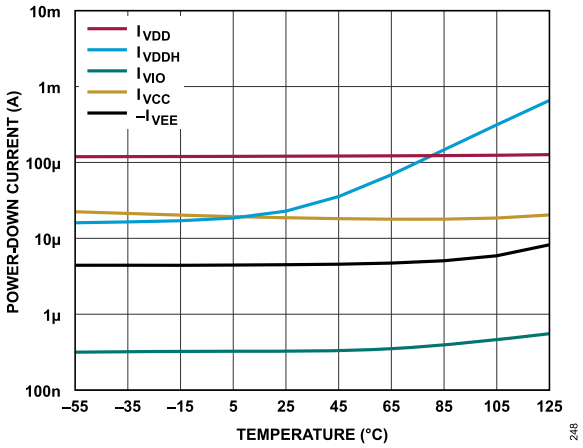


Figure 48. Power-Down Current vs. Temperature

TERMINOLOGY

Integral Nonlinearity (INL) Error

INL is the deviation of each individual code from a line drawn through the two endpoints of the ADC transfer function. The two endpoints of the transfer function are ½ LSB before the first code transition and 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Zero-Scale Error

For both bipolar and unipolar SoftSpan ranges, zero-scale error is the difference between the ideal zero-scale input voltage of 0 V and the actual input voltage which produces the zero-scale output code of 0 LSB.

Full-Scale Error

For bipolar SoftSpan ranges, full-scale error is the worst-case deviation of the first and last code transitions from ideal. It includes the effect of zero-scale error and any contributions from the reference buffer.

For unipolar SoftSpan ranges, full-scale error is the worst-case deviation of the last code transition from ideal. It includes the effect of zero-scale error and any contributions from the reference buffer.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

ENOB is expressed in bits.

Dynamic Range

Dynamic range is the ratio of the RMS amplitude of a full-scale sine wave to the total RMS noise and is expressed in decibels (dB). It is measured with a −60 dBFS input signal to include all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the RMS amplitude of a full-scale sine wave to the RMS sum of all other spectral components below the Nyquist frequency, excluding the first five harmonics and DC. The value for SNR is expressed in decibels (dB).

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the RMS amplitude of a full-scale sine wave to the RMS sum of all other spectral components below the Nyquist frequency, including harmonics but excluding DC. The value for SINAD is expressed in decibels (dB).

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first five harmonic components to the RMS amplitude of the fundamental input signal and is expressed in decibels (dB).

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference in decibels (dB) between the RMS amplitude of a full-scale input signal and the peak spurious signal.

Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is measured by applying a sine wave at frequency (f_{INJ}) on one interferer injection channel and a second sine wave at a different frequency (f_{RCV}) on all receiver channels. Crosstalk is the ratio of the RMS sum of the spectral tones at f_{INJ} and up to fifth-order intermodulation products on the receiver and injector channels. Channel-to-channel crosstalk is expressed in decibels (dB). All channels convert at f_S = 250 kSPS with the internal reference and reference buffer enabled during the measurement.

Aperture Delay

Aperture delay is a measure of acquisition performance. It is the time between the rising edge of the CNV input and when the input signals are held for a conversion.

Transient Response

Transient response is the time required for the ADC to acquire a full-scale input step to 50 ppm settling accuracy.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the RMS amplitude of a sine wave of frequency (f) applied to the analog input common-mode voltage to the RMS amplitude of the ADC output data at frequency (f). The value for CMRR is expressed in decibels (dB).

Power Supply Rejection Ratio (PSRR)

PSRR is the ratio of the RMS amplitude of a sine wave of frequency (f) applied to the power supply voltage to the RMS amplitude of the ADC output data at frequency (f). The value for PSRR is expressed in decibels (dB).

THEORY OF OPERATION

OVERVIEW

The AD4855 is a fully buffered, 8-channel simultaneous sampling, 16-bit 250 kSPS DAS with differential, wide common-mode range inputs. Its functional architecture is shown in Figure 1. Operating from a 5 V low voltage supply, flexible input buffer supplies, and using the precision low drift internal reference and reference buffer, the AD4855 allows the SoftSpan range of each channel to be independently configured to match the native application signal swing, minimizing additional external signal conditioning. To further maximize single-conversion dynamic range, the AD4855 incorporates SHDR technology. When enabled, the input signal path gain of a channel is automatically optimized on a sample-by-sample basis, minimizing converter noise on each sample without impacting linearity.

The 11 MHz bandwidth, picoamp-input analog buffers, wide input common-mode range, and 120 dB CMRR of the AD4855 allow the DAS to directly digitize input signals with arbitrary swings on INx+ and INx−. This input signal flexibility, combined with ±160 µV INL, no missing codes at 16 bits, 94.6 dB SNR, and 98.1 dB dynamic range makes the AD4855 an ideal choice for applications requiring high accuracy, throughput, and precision in a compact solution footprint.

The absolute input range of the AD4855 analog-input buffers spans (V_{EE} + 3.2 V) to (V_{CC} – 3.2 V). The buffer supplies, V_{CC} and V_{EE}, are flexible, allowing them to be chosen to match the native application signal swing requirements and eliminating the need for additional signal conditioning. The supplies can be biased asymmetrically around ground and include the ability for the V_{EE} pin to be tied directly to GND.

Digital features of the AD4855 include optional 16-bit oversampling, which offers further SNR and dynamic range improvements, and optional per channel offset, gain, and phase adjustment that allow for system-level errors upstream to the DAS to be corrected.

The AD4855 features a dedicated SPI register configuration bus (0.9 V to 5.25 V), and pin selectable serial LVDS and CMOS conversion data output buses. Between 1 line and 8 lines of data output can be employed in CMOS mode to optimize bus width and throughput.

The AD4855 typically dissipates 27 mW per channel when converting 8 channels simultaneously at 250 kSPS. Use the optional nap and power down modes to further reduce power consumption during inactive periods.

CONVERTER OPERATION

The AD4855 operates in two phases. During the acquisition phase, the sampling capacitors in the sample-and-hold circuit of each channel connect to their respective analog-input buffers (see Figure 53) and track the differential input voltage (V_{INx+} – V_{INx-}). A rising edge on the CNV pin transitions all of the sample-and-hold circuits from track mode to hold mode, simultaneously sampling the input signals on all channels and initiating a conversion. During the conversion phase, the sampling capacitors of each channel are connected to a 16-bit charge redistribution capacitor digital-to-analog converter (CDAC). The CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input voltage with binary-weighted fractions of the SoftSpan full-scale range of the channel (for example, $V_{FSR}/2$, $V_{FSR}/4$ ... $V_{FSR}/2^{16}$) using a differential comparator. At the end of this process, the CDAC outputs approximate the sampled analog inputs of each channel. Once all channels have been converted in this manner, the ADC control logic prepares the 16-bit digital output codes from each channel for serial transfer.

TRANSFER FUNCTION

The AD4855 digitizes the full-scale voltage range of each channel into 2^{16} discrete levels. In conjunction with the ADC main reference voltage, V_{REFBUF}, the SoftSpan configuration of each channel determines its differential input voltage range, LSB size, and the binary format of its conversion result, as shown in Table 12. Conversion results are output in twos complement binary format for all bipolar SoftSpan ranges and in straight binary format for all unipolar SoftSpan ranges. The ideal bipolar input transfer function is shown in Figure 49, and the ideal unipolar input transfer function is shown in Figure 50.

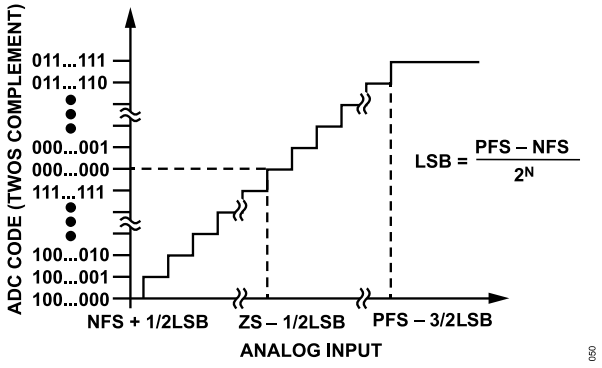


Figure 49. AD4855 Ideal Bipolar Input Transfer Function, N = 16 Bits

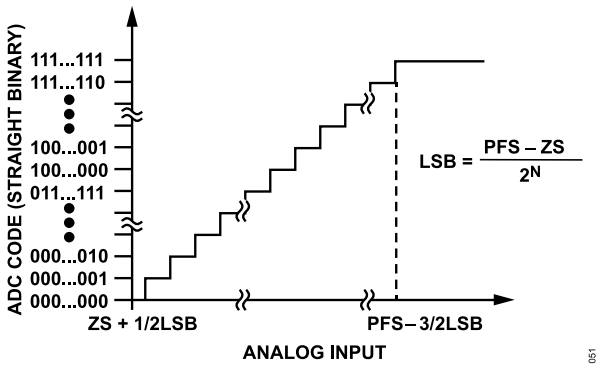


Figure 50. AD4855 Ideal Unipolar Input Transfer Function, N = 16 Bits

THEORY OF OPERATION

Table 12. SoftSpan Range Properties

SoftSpan	Differential Input Voltage Range ($V_{INx+} - V_{INx-}$)	Ideal Ranges (V_{REFBUF} = 4.096 V)			
		Negative Full Scale (V)	Zero Scale (V)	Positive Full Scale (V)	LSB (µV)
	Bipolar (Twos Complement Output Code)				
15	±10 × (V_{REFBUF}/1.024)	−40	0	+40	1220.703
13	±6.25 × (V_{REFBUF}/1.024)	−25	0	+25	762.939
11	±5 × (V_{REFBUF}/1.024)	−20	0	+20	610.352
9	±3.125 × (V_{REFBUF}/1.024)	−12.5	0	+12.5	381.470
7	±2.5 × (V_{REFBUF}/1.024)	−10	0	+10	305.176
5	±1.5625 × (V_{REFBUF}/1.024)	−6.25	0	+6.25	190.735
3	±1.25 × (V_{REFBUF}/1.024)	−5	0	+5	152.588
1	±0.625 × (V_{REFBUF}/1.024)	−2.5	0	+2.5	76.294
	Unipolar (Straight Binary Output Code)				
14	0 to 10 × (V_{REFBUF}/1.024)		0	40	610.352
12	0 to 6.25 × (V_{REFBUF}/1.024)		0	25	381.470
10	0 to 5 × (V_{REFBUF}/1.024)		0	20	305.176
8	0 to 3.125 × (V_{REFBUF}/1.024)		0	12.5	190.735
6	0 to 2.5 × (V_{REFBUF}/1.024)		0	10	152.588
4	0 to 1.5625 × (V_{REFBUF}/1.024)		0	6.25	95.367
2	0 to 1.25 × (V_{REFBUF}/1.024)		0	5	76.294
0	0 to 0.625 × (V_{REFBUF}/1.024)		0	2.5	38.147

SOFTSPAN

Each channel of the AD4855 can be independently configured in one of the 16 SoftSpan ranges, as shown in Table 12. Select the SoftSpan range of each channel based on the required differential analog input ($V_{INx+} - V_{INx-}$) range to be digitized. All channels default to SoftSpan 15, corresponding to a nominal ±40 V bipolar input span. To configure a channel for a different range, write the 4-bit SoftSpan code to the corresponding register address shown in Table 13.

Table 13. Per Channel SoftSpan Registers

Register Name	Register Address
CH0_SOFTSPAN	0x2A
CH1_SOFTSPAN	0x3C
CH2_SOFTSPAN	0x4E
CH3_SOFTSPAN	0x60
CH4_SOFTSPAN	0x72
CH5_SOFTSPAN	0x84
CH6_SOFTSPAN	0x96
CH7_SOFTSPAN	0xA8

Regardless of the chosen SoftSpan range, the wide common-mode input range and high CMRR of the INx+ and INx− analog inputs allow them to swing with an arbitrary relationship to each other, provided each pin remains between (V_{EE} + 3.2 V) and (V_{CC} − 3.2 V).

SEAMLESS HIGH DYNAMIC RANGE

SHDR is a proprietary technique that provides the lowest possible input-referred conversion noise on a sample-by-sample basis.

With SHDR disabled, the SoftSpan range of each channel automatically defines a fixed converter analog signal gain that is applied to every sample for that channel. The fixed gain must be low enough that the channel does not saturate at the maximum signal level of the chosen SoftSpan. The fixed gain results in a fixed input-referred noise level for all samples.

With SHDR enabled, the converter dynamically adjusts analog signal gain based on the differential voltage of each sample. For differential voltage magnitudes near the maximum of the chosen SoftSpan range, the gain employed is the same as the value used with SHDR disabled. However, for samples with lower magnitude, the converter automatically increases gain, resulting in lower input-referred conversion noise for these samples and improved dynamic range.

All conversion results are reported in the selected SoftSpan range format, requiring no additional output data manipulation to employ this mode. A comparison of converter input-referred transition noise with SHDR on and off is shown in Figure 18. As shown in Table 1, enabling SHDR offers up to 4.4 dB improvement in single-conversion dynamic range.

Seamless high dynamic range is enabled on all channels by default. To disable SHDR on a channel, clear the corresponding control bit in the SEAMLESS_HDR register.

THEORY OF OPERATION

DIGITAL PROCESSING FEATURES

The AD4855 supports several digital data postprocessing features that can be applied to conversion results, including oversampling, and offset, gain, and phase correction. These features are configured via the AD4855 control registers described in the Register Summary section.

Oversampling Mode

The AD4855 operates in nonoversampling mode by default. As shown in Figure 6 and Figure 7, in this mode, the BUSY line transitions low to high at the start of each conversion, and the SDO0 to SDO7 lines (CMOS) or SDO lines (LVDS) are updated with the latest conversion results from each channel at the end of every conversion, just prior to the falling edge of the BUSY line.

With oversampling mode enabled, the AD4855 computes the digital average of multiple conversion results for each channel. In this mode, all channels share a single common oversampling ratio, and only the averaged result for each channel is available to be read from the AD4855. Oversampling is useful in applications requiring lower noise and higher dynamic range per output data-word, which the AD4855 supports with 16-bit output resolution and reduced average output data rates. Oversampling mode also supports optional digital phase correction (see the Digital Phase Correction section).

To use oversampling mode, select the oversampling ratio from Table 43 corresponding to the number of conversion results to be digitally averaged for each channel. Program the chosen 4-bit OS_RATIO to the OVERSAMPLE register while clearing the OS_EN bit to 0. Then, reprogram the OVERSAMPLE register with the chosen OS_RATIO while setting the OS_EN bit to 1. This sequence ensures the next CNV rising edge is interpreted as the first sample of oversampling mode.

As shown in Figure 51, in oversampling mode, the BUSY line transitions low to high at the start of the first conversion of the oversampling window and remains high through the end of the final conversion of the window. Though the BUSY line remains high, separate CNV rising edges are still required to begin each conversion within the oversampling window. Averaged results for each analog input channel are updated on the SDO0 to SDO7 lines (CMOS) or SDO lines (LVDS) at the end of each oversampling window, just prior to the falling edge of the BUSY line.

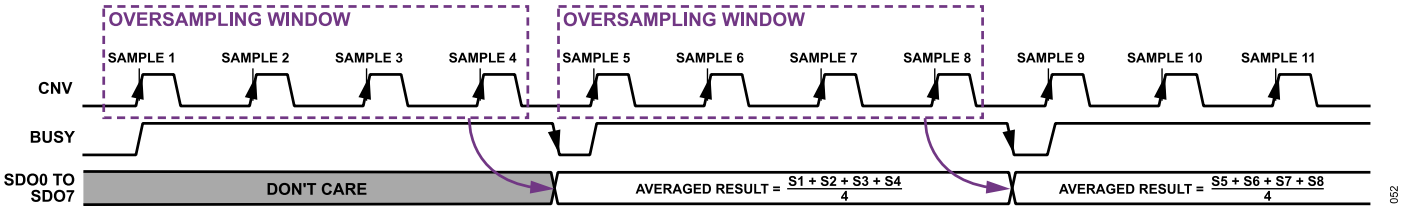


Figure 51. Oversampling Mode with 4× Oversampling Ratio (OS_RATIO = 0x1)

THEORY OF OPERATION

Digital Offset Correction

Each channel of the AD4855 can be independently programmed to add a 16-bit signed digital offset correction value to every conversion result. This feature can be used to correct for fixed offset errors upstream to the DAS analog inputs. The default offset correction for all channels is zero. To employ a nonzero value, compute the 16-bit signed offset correction CHx_OFFSET using the following equation:

$$Digital\ Offset\ Correction\ (\mu V) = CHx_OFFSET \times LSB\ Size\ (\mu V) \quad (2)$$

where *LSB Size* is a function of the channel SoftSpan range, as shown in Table 12. Program the 16-bit signed offset correction to the corresponding CHx_OFFSET register, shown in Table 14.

Offset correction is added to the conversion results of a channel prior to output code saturation. Code saturation occurs at zero scale and positive full scale for unipolar SoftSpan ranges, and it occurs at negative and positive full scale for bipolar SoftSpan ranges. Because offset correction precedes output code saturation, artifacts may be introduced near negative or positive full scale, depending on the magnitude and the polarity of the digital offset employed. The AD4855 offers approximately 5% additional analog input range beyond the SoftSpan range limits shown in Table 12. This additional analog input span is usually not observable due to the output code saturation but can be observed using a combination of digital offset and gain correction terms.

Table 14. Per Channel Offset Correction Registers

Register Name	Register Addresses
CH0_OFFSET	0x2B to 0x2D
CH1_OFFSET	0x3D to 0x3F
CH2_OFFSET	0x4F to 0x51
CH3_OFFSET	0x61 to 0x63
CH4_OFFSET	0x73 to 0x75
CH5_OFFSET	0x85 to 0x87
CH6_OFFSET	0x97 to 0x99
CH7_OFFSET	0xA9 to 0xAB

Digital Gain Correction

Each channel of the AD4855 can be independently programmed to apply a digital gain correction factor to every conversion result, which can be used to correct for fixed gain errors upstream to the DAS analog inputs. The default gain correction factor for all channels is 1.00000. To employ a nonunity factor, compute the 16-bit unsigned gain correction CHx_GAIN using the following equation:

$$Digital\ Gain\ Correction = \frac{CHx_GAIN}{0x8000} \quad (3)$$

Program the value from this equation into the corresponding CHx_GAIN register, shown in Table 15. The gain correction factor spans 0 to 1.99997 as CHx_GAIN traverses 0x0000 to 0xFFFF, with the default of 1.00000 corresponding to CHx_GAIN = 0x8000.

Gain correction is applied to the conversion results of a channel after the digital offset correction and prior to the output code saturation. Code saturation occurs at zero scale and positive full scale for unipolar SoftSpan ranges and at negative and positive full scale for bipolar SoftSpan ranges. Because gain correction precedes output code saturation, artifacts may be introduced near negative or positive full scale depending on the magnitude of digital gain employed. The AD4855 offers approximately 5% additional analog input range beyond the SoftSpan range limits shown in Table 12. This additional analog input span is usually not observable due to the output code saturation but can be observed using a combination of digital offset and gain correction terms.

Table 15. Per Channel Gain Correction Registers

Register Name	Register Addresses
CH0_GAIN	0x2E to 0x2F
CH1_GAIN	0x40 to 0x41
CH2_GAIN	0x52 to 0x53
CH3_GAIN	0x64 to 0x65
CH4_GAIN	0x76 to 0x77
CH5_GAIN	0x88 to 0x89
CH6_GAIN	0x9A to 0x9B
CH7_GAIN	0xAC to 0xAD

Digital Phase Correction

While operating in Oversampling Mode, each channel of the AD4855 can be independently programmed to apply a digital phase correction term to the oversampled digital averages. This feature can be used to compensate for phase errors upstream to the DAS analog inputs. The default phase correction for all channels is zero, which results in digital averages of all channels being computed using the same phase-aligned sample groups (for example, Sample 1 to Sample 4, Sample 5 to Sample 8, Sample 9 to Sample 12, and so forth) as shown in Figure 51.

To employ digital phase correction, program the desired 16-bit unsigned phase correction term (in integer number of conversion cycles) to the corresponding CHx_PHASE register, shown in Table 16. The maximum phase correction allowed is one less than the number of conversions in the oversampling ratio. Comparing Figure 52 with Figure 51, the oversampled digital average of a channel with nonzero phase is shifted by an integer number of conversion cycles relative to the start of oversampling. The oversampled average data for all channels are updated on the SDO0 to SDO7 lines (CMOS) or the SDO lines (LVDS) once the values for all channels are available, just prior to the falling edge of the BUSY line. The averaged results of all channels in Figure 52 are updated one conversion cycle later than in Figure 51 due to the CH7_PHASE = 0x0001 setting.

THEORY OF OPERATION

Table 16. Per Channel Phase Correction Registers

Register Name	Register Addresses
CH0_PHASE	0x30 to 0x31
CH1_PHASE	0x42 to 0x43
CH2_PHASE	0x54 to 0x55
CH3_PHASE	0x66 to 0x67
CH4_PHASE	0x78 to 0x79
CH5_PHASE	0x8A to 0x8B
CH6_PHASE	0x9C to 0x9D
CH7_PHASE	0xAE to 0xAF

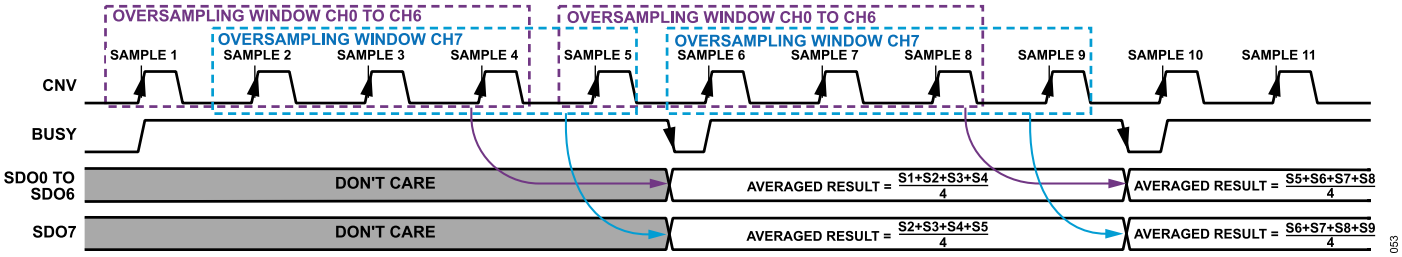


Figure 52. Oversampling Mode with 4× Oversampling Ratio (OS_RATIO = 0x1), Channel 7 Averages Phase-Shifted by One Sample (CH7_PHASE = 0x0001)

THEORY OF OPERATION

Channel Overrange and Underrange Limits

Every conversion result on each channel of the AD4855 is compared with the 16-bit signed overrange and underrange limits CHx_OR and CHx_UR, shown in Table 17 and Table 18. If any out-of-range conversion result is detected, the corresponding flag in the CH_OR_STATUS register or CH_UR_STATUS register is set. This limit checking is particularly useful during oversampling mode (see the Oversampling Mode section) because it allows the digital host to determine if any out-of-range conversion results contributed to an oversampled digital average. The default overrange and underrange limits are the positive and negative full scale of a bipolar input range, respectively. To employ other limits, program the desired 16-bit signed code limits to the corresponding CHx_OR and CHx_UR registers, shown in Table 17 and Table 18.

Table 17. Per Channel Overrange Limit Registers

Register Name	Register Addresses
CH0_OR	0x32 to 0x34
CH1_OR	0x44 to 0x46
CH2_OR	0x56 to 0x58
CH3_OR	0x68 to 0x6A
CH4_OR	0x7A to 0x7C
CH5_OR	0x8C to 0x8E
CH6_OR	0x9E to 0xA0
CH7_OR	0xB0 to 0xB2

Table 18. Per Channel Underrange Limit Registers

Register Name	Register Addresses
CH0_UR	0x35 to 0x37
CH1_UR	0x47 to 0x49
CH2_UR	0x59 to 0x5B
CH3_UR	0x6B to 0x6D
CH4_UR	0x7D to 0x7F
CH5_UR	0x8F to 0x91
CH6_UR	0xA1 to 0xA3
CH7_UR	0xB3 to 0xB5

APPLICATIONS INFORMATION

BUFFERED ANALOG INPUTS

Each channel of the AD4855 simultaneously samples the voltage difference ($V_{INx+} - V_{INx-}$) between its analog input pins over a wide common-mode input range while high CMRR attenuates unwanted signals common to both inputs. Wide common-mode input range coupled with high CMRR allows the INx+ and INx− analog inputs to swing with an arbitrary relationship to each other, provided each pin remains between (V_{EE} + 3.2 V) and (V_{CC} − 3.2 V). This feature of the AD4855 simplifies signal chain design by accepting a wide variety of signal swings, including traditional classes of analog input signals (such as pseudo-differential unipolar, pseudo-differential true bipolar, and fully differential).

The wide operating ranges of the buffer V_{CC} and V_{EE} supplies offer further input common-mode flexibility. As long as the voltage difference limits of 10 V ≤ (V_{CC} − V_{EE}) ≤ 48 V are observed, the V_{CC} and V_{EE} supplies can be independently biased anywhere within their own individually allowed operating ranges, including the ability for the V_{EE} pin to be tied directly to ground. This feature enables the absolute input range of the AD4855 to be tailored to specific application requirements.

In all SoftSpan ranges, the analog inputs of each channel can be modeled by the equivalent circuit shown in Figure 53. At the start of acquisition, the sampling capacitors (C_{SAMP}) connect to the integrated buffers, BUFFER+ and BUFFER−, through the sampling switches. The sampled voltage is reset during the conversion process and is, therefore, reacquired for each new conversion. As shown in Figure 17 and Figure 20, the wideband analog-input buffers are well-suited to acquiring inputs signals that undergo transient step settling between successive conversions. To ensure best performance, limit the analog-input signal slew rate to less than 100 V/µs at the sampling moment.

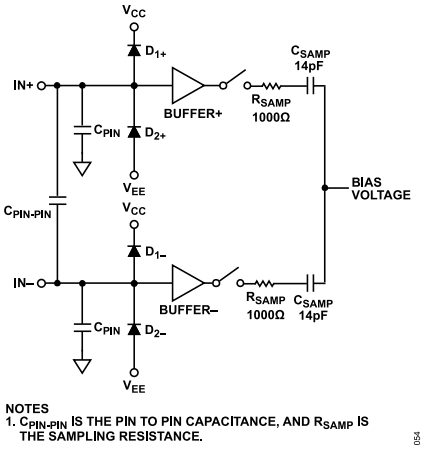


Figure 53. Equivalent Circuit for Differential Analog Inputs, Single Channel

The diodes (Dx+ and Dx−) between the inputs and the V_{CC} and V_{EE} supplies provide input ESD protection. While within the supply voltages, the analog inputs of the AD4855 draw only 75 pA typical DC leakage current, and the ESD protection diodes do not turn on. This protection offers a significant advantage over external op amp buffers, which often have diode protection that turns on during transients, injecting a current into the input signal path that corrupts the signal voltage.

ANALOG INPUT DRIVE CIRCUITS

The buffer input stage offers a high degree of transient isolation from the sampling process. Most sensors, signal conditioning amplifiers, and filter networks with less than 10 kΩ impedance can drive the passive 4 pF analog input capacitance (C_{PIN}) directly. For higher impedances and slow settling circuits, add a 680 pF capacitor between the analog input pins and the GND pins to maintain the full DC accuracy of the AD4855.

The high input impedance of the unity-gain buffers in the AD4855 reduces the input drive requirements, and this high impedance enables the inclusion of optional RC filters with kΩ impedance and arbitrarily slow time constants for anti-aliasing or other purposes. Micropower op amps with limited drive capability are also well-suited to driving the high impedance analog inputs directly.

The AD4855 features proprietary circuitry to achieve 120 dB typical internal crosstalk isolation between channels. Maintaining this level of isolation can require care with the PCB layout. Ensure input signal traces are short and well shielded to minimize external coupling. Capacitive coupling between the input pins of the different channels of the AD4855 is tens of femtofarads, orders of magnitude less than the coupling that can be present in a poor PCB design. Low source resistance and/or high source capacitance help reduce external capacitively coupled crosstalk. A single-ended input drive also enjoys additional external crosstalk isolation because every other input pin is grounded or at a low impedance source, and this grounding serves as a shield between channels.

ANALOG INPUT OVERDRIVE TOLERANCE

Driving an analog input greater than the V_{CC} supply on any channel up to 10 mA does not affect conversion results on other channels. Approximately 70% of this overdrive current flows out of the V_{CC} pin, and the remaining 30% flows out of the V_{EE} pin. The current flowing out of V_{EE} produces heat across the V_{CC} − V_{EE} voltage drop and must be taken into account for the absolute maximum operating junction temperature. Driving an analog input less than the V_{EE} supply may corrupt the conversion results on other channels.

Adding an external resistor (for example, 100 Ω to 1000 Ω) in series with each INx+ and INx− pin is recommended in applications where (V_{CC} − V_{EE}) > 44 V to limit latchup current to under ±10 mA during fault conditions, as shown in Figure 54. These resistors are transparent in normal operation of the AD4855. Refer to absolute maximum ratings in Table 6 for pin voltage and current limits related to device reliability.

Driving the inputs greater than V_{CC} or less than V_{EE} can reverse the normal current flow from the external power supplies driving these pins.

APPLICATIONS INFORMATION

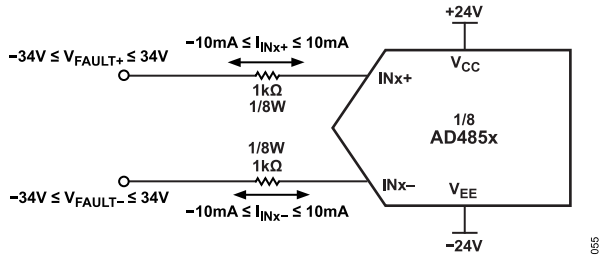


Figure 54. External Series Resistors Limit Latchup Current During Fault Conditions and Are Transparent in Normal Operation for the AD4855

ANALOG INPUT FILTERING

The true high impedance analog inputs can accommodate a wide range of passive or active signal conditioning filters. The buffered DAS inputs have an analog bandwidth of 11 MHz and impose no particular bandwidth requirement on external filters. Any external input filters can, therefore, be optimized independently of the DAS to reduce signal chain noise and interference. A common filter configuration is the simple antialiasing and noise reducing RC filter with its pole at half the sampling frequency, as shown in Figure 55.

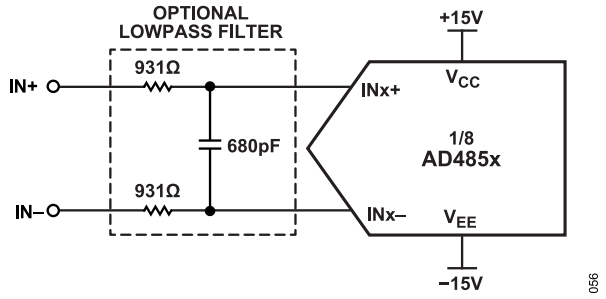


Figure 55. Example Differential Input Filter for the AD4855

Use high quality capacitors and resistors in the RC filters because these components may add distortion. Ceramic capacitors with NPO/COG type dielectric have excellent linearity. Carbon surface-mount resistors may generate distortion from self heating and from damage that may occur during soldering. Note that metal film surface mount resistors are much less susceptible to either problem.

DAS REFERENCE

The AD4855 supports three reference configurations as follows:

- Internal band-gap reference and reference buffer
- External reference and internal reference buffer
- External reference and external reference buffer

Most applications employ the internal band-gap reference and reference buffer, which is the default configuration of the AD4855. For applications requiring better initial accuracy and/or lower reference temperature drift, disable the internal band-gap reference and overdrive the REFIO pin with an external reference. This configuration (external reference and internal reference buffer) retains the internal reference buffer, isolating the external reference from ADC conversion transients, and is ideal for sharing a single precision external reference across multiple devices. The final configuration (external reference and external reference buffer) disables the internal band-gap reference and the internal reference buffer and overdrives the REFBUF pin with an external reference.

Internal Reference with Internal Buffer

The AD4855 includes a low noise, low drift (10 ppm/°C maximum), temperature compensated band-gap reference that is factory trimmed to 4.096 V. The reference output connects to the REFIO pin, which serves as the input to the on-chip reference buffer (see Figure 56). The REFIO pin is internally bypassed to the GND pins with a 10 nF ceramic capacitor to filter wideband noise of the band-gap reference. The precision unity-gain reference buffer creates the converter main reference voltage (V_{REFBUF} = V_{REFIO}) on the REFBUF pin, nominally 4.096 V when using the internal band-gap reference.

The internal band-gap reference PSRR vs. frequency is shown in Figure 32. For best performance, supply the V_{DD} pin using a high PSRR, low noise LDO regulator, such as the LT3042. Optionally, adding an external 100 µF, X5R, and 0805 capacitor between the REFIO pin and the B4 GND pin can significantly improve the PSRR of the internal reference at frequencies between 100 Hz and 1 MHz.

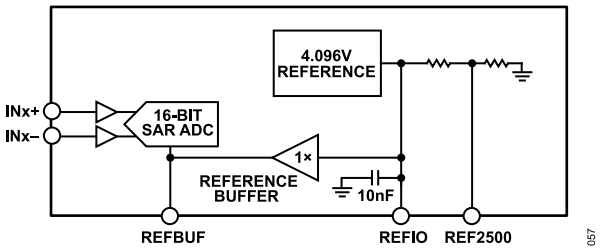


Figure 56. Internal Reference with Internal Buffer Configuration

External Reference with Internal Buffer

If better initial accuracy and/or lower reference temperature drift is required, the REFIO pin can be overdriven by an external reference, as shown in Figure 57. With its small size, low power, and high accuracy, the LTC6655-4.096 is well-suited for use with the AD4855 when overdriving the REFIO pin. Bypassing the LTC6655-4.096 to the B4 GND pin with a 10 µF, X5R, and 0805 ceramic capacitor close to the REFIO pin is recommended. Disable the internal band-gap reference through the DEVICE_CTRL register in this configuration.

This configuration retains the internal reference buffer, isolating the external reference from the ADC conversion transients. This configuration is ideal for sharing a single precision external reference across multiple devices. It also offers the best transient response performance when employing burst sampling, as explained in the Internal Reference Buffer Transient Response section.

APPLICATIONS INFORMATION

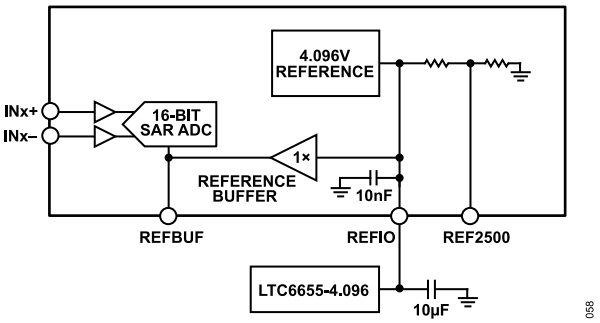


Figure 57. External Reference with Internal Buffer Configuration

External Reference with Disabled Internal Buffer

In applications employing an external reference, the external reference with internal buffer configuration is the recommended use case (see the External Reference with Internal Buffer section). In the rare case that it is necessary, the AD4855 supports overdriving the REFBUF pin directly with an external reference as shown in Figure 58. With its small size, low power, and high accuracy, the LTC6655-4.096 is well-suited for use with the AD4855 when overdriving the REFBUF pin. Bypass the LTC6655-4.096 to the B4 GND pin with a 47 µF, X5R, 0805 ceramic capacitor close to the REFBUF pin to absorb transient conversion currents and minimize noise. Disable the internal band-gap reference and the internal reference buffer through the DEVICE_CTRL register in this configuration and connect the REFIO pin to the GND pins.

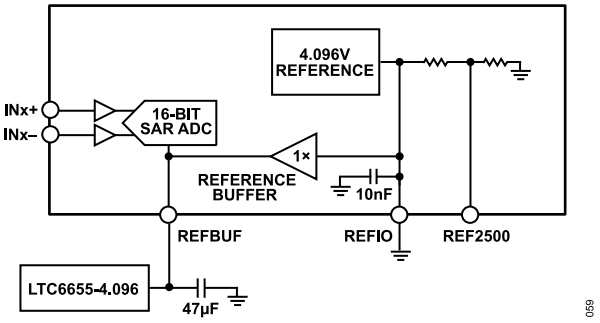


Figure 58. External Reference with Disabled Internal Buffer Configuration

The AD4855 converters draw a charge (Q_{CONV}) from the REFBUF pin during each conversion cycle. The internal reference buffer is designed to optimally provide this charge, minimizing V_{REFBUF} movement. If the internal buffer is disabled, the external reference circuitry on the REFBUF pin must supply this charge. On short time scales, the charge is provided by the external bypass capacitor; however, on longer time scales, all of the charge is supplied by the external reference. This charge draw corresponds to a DC current equivalent of $I_{REFBUF} = Q_{CONV} \times f_S$, which is proportional to the sample rate. In applications where a burst of samples is taken after idling for long periods of time (see Figure 59), the I_{REFBUF} quickly transitions from approximately 2.2 mA to 2.5 mA (V_{REFBUF} = 4.096 V, f_S = 250 kSPS). This current step triggers a transient response in the external reference that must be considered because any deviation in the V_{REFBUF} affects converter accuracy. If an external reference is used to overdrive the REFBUF pin, the fast settling LTC6655 family of references is recommended.

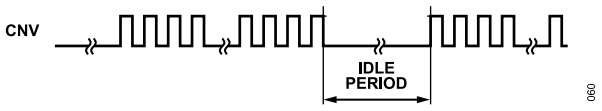


Figure 59. CNV Waveform Showing Burst Sampling

Internal Reference Buffer Transient Response

For optimum performance in applications employing burst sampling, use the internal reference buffer. The internal reference buffer incorporates a proprietary design that minimizes movements in the V_{REFBUF} when responding to a burst of conversions following an idle period. Figure 60 compares the burst conversion response of the AD4855 with a DC input level for the three supported reference configurations. The first configuration employs the internal reference and reference buffer as shown in Figure 56. The second employs the internal reference buffer with the REFIO pin externally overdriven by an LTC6655-4.096, as shown in Figure 57. The third configuration disables the internal reference buffer and overdrives the REFBUF pin with an external LTC6655-4.096, as shown in Figure 58.

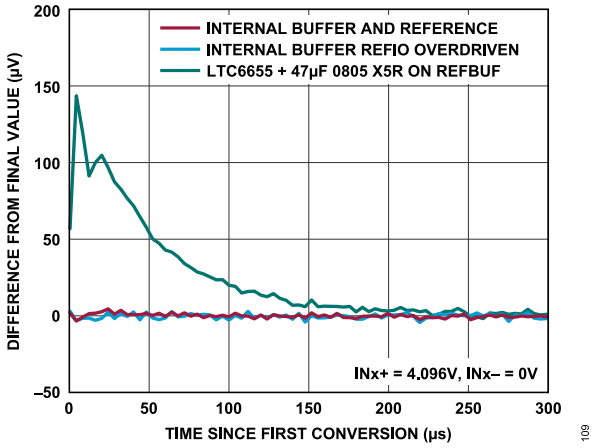


Figure 60. Burst Conversion Response of the AD4855, f_S = 250 kSPS

POWER CONSIDERATIONS

The AD4855 requires the following five power supplies:

- V_{CC} and V_{EE}, the positive and negative analog input buffer supplies
- V_{DD}, the 5 V core power supply
- V_{DDH} (or V_{DDL}), the 1.8 V LDO (or 1.8 V core) power supply
- V_{IO}, the digital input and output power supply

All five power supplies have internal bypass capacitance, and no additional external bypass is required or recommended.

APPLICATIONS INFORMATION

The V_{CC} and V_{EE} supplies can be independently biased anywhere within their individual allowable operating ranges, including the ability for the V_{EE} supply to be tied directly to the ground. This feature enables the absolute input range of the AD4855 to be tailored to the specific requirements of the application.

In the recommended use case, the V_{DDL} pin is supplied by the internal 1.8 V LDO, as shown in Figure 1. Tie the V_{DDH} pin to the V_{DD} pin or to another external supply between 2.2 V and 5.25 V, and do not externally connect the V_{DDL} pin in this case. To externally supply the V_{DDL} pin, disable the internal LDO by tying the V_{DDH} pin to the GND pins and connect the V_{DDL} pin to an external 1.8 V supply, as shown in Figure 61.

The flexible V_{IO} supply allows the AD4855 to communicate with the CMOS logic operating between 0.9 V and 5.25 V (controlled by the HIVIO/$\overline{\text{LOVIO}}$ pin logic state), including 2.5 V and 3.3 V systems. When using LVDS data output mode, the range of the V_{IO} supply is 1.71 V to 5.25 V (controlled by the HIVIO/$\overline{\text{LOVIO}}$ pin logic state). See Table 1 and Table 9 for more details.

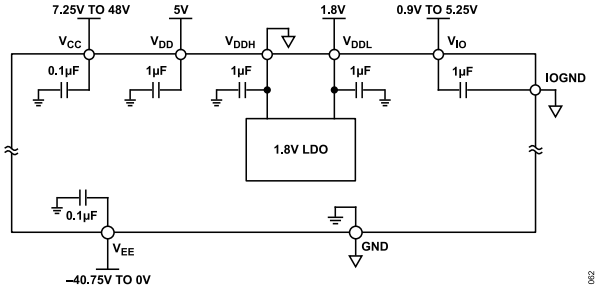


Figure 61. Power Supply Pins of the AD4855 when V_{DDL} Is Supplied Externally

Power Supply Sequencing

The AD4855 does not have any specific power supply sequencing requirements. Take care to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The AD4855 has an internal POR circuit that resets the converter on initial power up and whenever the V_{DD} supply drops to less than 3.4 V or the V_{DDL} supply drops to less than 1.2 V. Once the supply voltage re-enters the nominal supply voltage range, the POR circuit reinitializes the DAS. Do not initiate any conversions until at least the maximum t_{WAKE} ($t_{WAKE,MAX}$) = 1 ms after the falling edge of the BUSY line, which indicates the end of the POR event. Any conversion initiated before this time produces invalid results.

TIMING AND CONTROL

The AD4855 sampling and conversion is controlled by the CNV pin. A rising edge on the CNV pin transitions the sample-and-hold circuits of all channels from track mode to hold mode, simultaneously sampling the input signals on all channels and initiating a conversion. Once a conversion is started, it cannot be terminated early except by resetting the DAS (see the Reset Timing section). For optimum performance, drive the CNV pin with a clean, low jitter signal and avoid transitions on data input and output lines leading up to the rising edge of the CNV pin. Additionally, avoid high slew rates on the analog inputs for 100 ns before and after the rising edge of the CNV pin. Converter status is indicated by the BUSY output, which transitions low to high at the start of each conversion and stays high until the conversion is complete. After the CNV pin is brought high to begin a conversion, it must be returned low between 40 ns and 60 ns later or after the falling edge of the BUSY line to minimize external disturbances during the internal conversion process. The CNV timing required to take advantage of reduced power at slower sampling rates is described in the Nap Mode section.

The AD4855 has an internal clock that is trimmed to guarantee a maximum conversion time of 725 ns and a minimum acquisition time of 3465 ns when converting at 250 kSPS. The architecture of the AD4855 allows the converter to begin acquiring the next sample before the conversion of the previous sample is completed, as shown in Figure 2. The minimum acquisition time varies with the sampling frequency.

Nap Mode

The AD4855 can be placed into nap mode after a conversion is completed to reduce power consumption between conversions. In this mode, a portion of the device circuitry is turned off, including circuits associated with sampling the analog input signals. Nap mode is enabled by keeping the CNV pin high between conversions, as shown in Figure 62. To initiate a new conversion after entering nap mode, bring the CNV pin low and hold for at least 750 ns before bringing it high again. The converter acquisition time is set by the CNV pin low time when using nap mode.

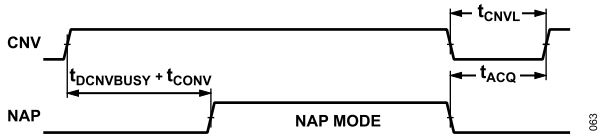


Figure 62. Nap Mode Timing for the AD4855

Power-Down Mode

When the PD pin is brought high, or the PWR_MODE bits (Bits[1:0]) in the Device Configuration Register are set to 0x3, the AD4855 is powered down, and subsequent conversion requests are ignored. If either toggling the PD pin or changing the PWR_MODE bits occurs during a conversion, the device powers down once the conversion completes. In this mode, the AD4855 draws only a small standby current resulting in a typical power dissipation of 1.3 mW. To exit power-down mode, bring the PD pin low and wait at least $t_{WAKE,MAX}$ = 1 ms before initiating a conversion. Any conversion initiated before this time produces invalid results.

APPLICATIONS INFORMATION

Channel Sleep

Each channel in the AD4855 can be independently put into sleep mode to reduce power consumption. With sleep mode enabled, the input buffers and ADC of a channel are placed in a low power, standby state, and conversion requests are ignored. Sleep mode is disabled on all channels by default. To enable sleep mode on a channel, set the corresponding control bit in the CH_SLEEP register.

Reset Timing

A global reset of the AD4855, equivalent to a POR event, can be executed without needing to cycle the supplies. This feature is useful when recovering from system-level events that require the entire system to be reset to a known synchronized state. To initiate a global reset, bring the PD pin high twice without an intervening conversion, as shown in the Figure 63 section. Alternatively, an equivalent global reset can be triggered by entering, exiting, and then re-entering power-down mode using the PWR_MODE bits (Bits[1:0]) in the Device Configuration Register without an intervening conversion.

The reset event is triggered on the second rising edge of the PD pin and asynchronously ends based on an internal timer. Reset clears all serial data output registers and restores all device states to their POR default conditions. If reset is triggered during a conversion, the conversion is immediately halted. The normal power-down behavior associated with the PD pin going high is not affected by the reset. Once the PD pin is brought low, wait at least $t_{WAKE,MAX}$ = 1 ms before initiating a conversion. Any conversion initiated before this time produces invalid results.

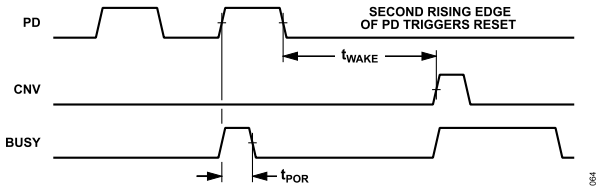


Figure 63. Reset Timing for the AD4855

DIGITAL INTERFACE

The AD4855 supports both CMOS (see Figure 64) and LVDS (see Figure 69) serial conversion data output interfaces, selectable using the LVDS/$\overline{\text{CMOS}}$ pin. The flexible V_{IO} supply allows the AD4855 to communicate with any CMOS logic operating between 0.9 V and 5.25 V (controlled by the HIVIO/$\overline{\text{LOVIO}}$ pin logic state), while the LVDS interface supports low noise digital systems. In CMOS conversion data output mode, applications can employ between one and eight lanes of serial data output, allowing for optimized bus width and conversion data throughput.

CMOS CONVERSION DATA OUTPUT MODE

As shown in Figure 64 and Figure 65, the serial CMOS conversion data output bus consists of the following lines:

- One serial clock input (SCKI)
- One serial clock output (SCKO)
- Eight serial data output lanes (SDO0 to SDO7)

Communication with the AD4855 across this bus occurs during predefined data transaction windows. Within a window, the device outputs user-configurable packets containing either conversion or oversampling results, optional channel configuration, and device status information from the SDO0 lane to the SDO7 lane. Following the eighth channel packet, a ninth packet containing device status and 16-bit cyclic redundancy check (CRC) can be read out for diagnostic and error checking purposes. The AD4855 supports two user-selectable packet sizes from 16-bits to 24-bits in length (see the Packet Format section).

Complete the data transaction with a minimum last SCKI signal edge to CNV signal rising edge time ($t_{SCKICNV,MIN}$) = 20 ns prior to the start of the next conversion (see Figure 64). It is still possible to read packets after starting the next conversion; however, this degrades conversion accuracy and, therefore, is not recommended.

Just prior to the falling edge of the BUSY pin, the SDO0 lane to the SDO7 lane are updated with the latest conversion or oversampling results from analog input Channels 0 to Channel 7, respectively. Rising edges on the SCKI signal serially clock data out on the SDO0 lane to the SDO7 lane. The SCKO signal echoes the SCKI signal but is skew matched with data on the SDO0 lane to the SDO7 lane. The SCKI signal is allowed to idle either high or low in CMOS mode. The CMOS conversion data output bus is enabled when the $\overline{\text{CS}}$ signal is low, and it is disabled and high-Z when $\overline{\text{CS}}$ is high, allowing the bus to be shared across multiple devices.

When interfacing the AD4855 with a standard SPI host, capture output data at the receiver on rising edges of the SCKI signal. In other applications, such as interfacing the AD4855 with an FPGA, the SCKO signal can be used to capture serial output data from the SDO0 lane to the SDO7 lane at the receiver. Capturing data using the SCKO signal adds robustness to delay variations over temperature and supply.

As shown in Figure 64 and Figure 66, each SDO lane outputs packets for all analog input channels in a sequential circular manner. For example, the first packet output on the SDO0 lane corresponds to the analog input for Channel 0, followed by the packets for Channel 1 through Channel 7. Finally, the packet containing the device status and 16-bit CRC can be read out. The data output on the SDO0 lane then wraps back to Channel 0, and this pattern repeats indefinitely. Other SDO lanes follow a similar circular pattern—except the first packet presented on each lane corresponds to its associated analog input channel. To achieve full 250 kSPS per channel throughput, data packets can be captured from all eight SDO data output lanes in parallel. In applications that do not require full throughput, increasing the number of SCKI pulses applied during the data transaction window allows all data packets to be read using fewer physical SDO lanes.

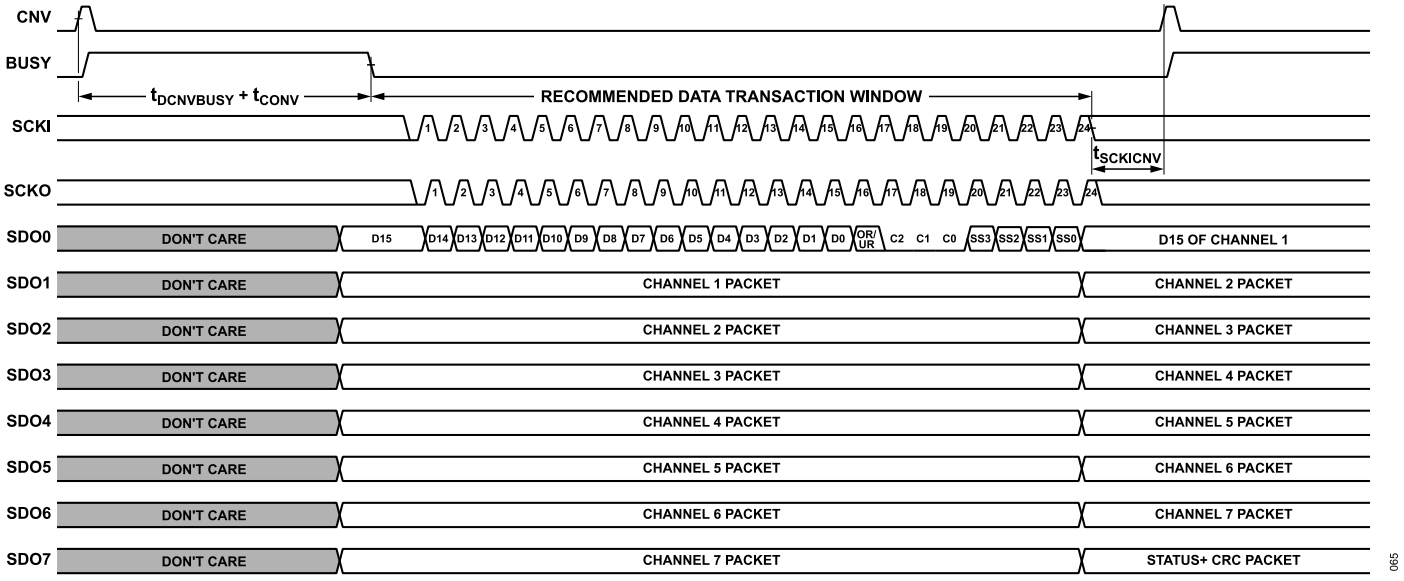


Figure 64. CMOS Conversion Data Bus Timing, PACKET_SIZE = 0x1, OS_EN = 0, TEST_PAT = 0

DIGITAL INTERFACE

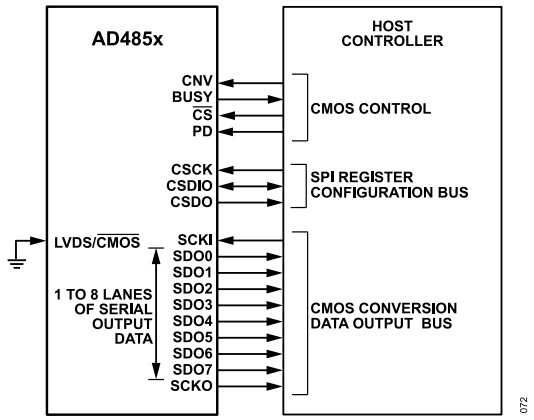


Figure 65. CMOS Conversion Data Output Mode for the AD4855

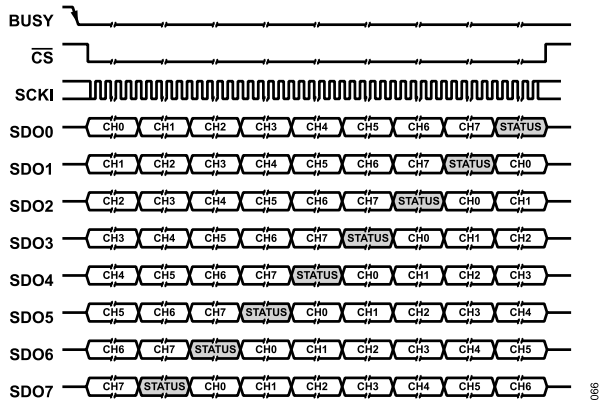


Figure 66. All Packets May Be Read Using Fewer SDO Lanes By Increasing the Number of SCKI Pulses Applied

LVDS CONVERSION DATA OUTPUT MODE

In LVDS conversion data output mode, information is transmitted using positive and negative signal pairs with bits differentially encoded as (LVDS+ − LVDS−). These signals are typically routed using differential transmission lines with 100 Ω characteristic impedance. Logical 1s and Logical 0s are nominally represented by differential +350 mV and −350 mV, respectively.

As shown in Figure 69, the serial LVDS conversion data output bus consists of the following lines:

- SCKI+ and SCKI−, the differential serial clock input pair
- SCKO+ and SCKO−, the differential serial clock output pair
- SDO+ and SDO−, the differential serial data output pair

Communication with the AD4855 across this bus occurs during predefined data transaction windows. Within a window, the device outputs user-configurable packets containing the conversion or oversampling results, optional channel configuration, and device status information on the SDO line. Following the eighth channel packet, a ninth packet containing device status and 16-bit CRC can be read out for diagnostic and error checking purposes. The AD4855 supports two user-selectable packet sizes from 16-bits to 24-bits in length (see the Packet Format section).

Complete the data transaction with a minimum $t_{SCKICNV,MIN}$ = 20 ns prior to the start of the next conversion, as shown in Figure 69. It is still possible to read packets after starting the next conversion, but this degrades conversion accuracy and is not recommended.

Just prior to the falling edge of the BUSY signal, the SDO line is updated with the latest conversion or oversampling results from the analog input for Channel 0. Both rising and falling edges on the SCKI signal serially clock data out on the SDO line. The SCKI signal is also echoed on the SCKO signal, skew matched to the data on the SDO line.

Whenever possible, it is recommended that rising and falling edges of the SCKO line be used to capture double data rate (DDR) serial output data on the SDO line because this yields the best robustness to delay variations over supply and temperature. The LVDS bus is enabled when the $\overline{CS}$ signal is low. It is disabled and high-Z when the $\overline{CS}$ signal is high, allowing the bus to be shared across multiple devices. Due to the high speeds involved in LVDS signaling, LVDS bus sharing must be carefully considered. Transmission line limitations imposed by the shared bus may limit the maximum achievable bus clock speed. The LVDS inputs are internally terminated with a 100 Ω differential resistor when the $\overline{CS}$ signal is low, while outputs must be differentially terminated with a 100 Ω resistor at the receiver (FPGA). The SCKI line must idle in the low state in LVDS output mode, including when transitioning the $\overline{CS}$ signal.

As shown in Figure 68 and Figure 69, the SDO line outputs data packets for all analog input channels in a sequential circular manner. For example, the first packet output on the SDO line corresponds to the analog input for Channel 0, followed by the packet for Channel 1 all the way to Channel 7. Finally, a packet containing device status and 16-bit CRC can be read out. The data output on the SDO line then wraps back to Channel 0, and this pattern repeats indefinitely.

DIGITAL INTERFACE

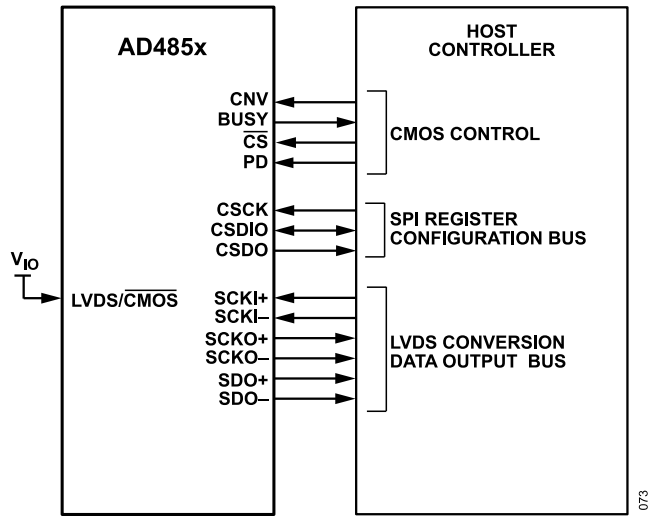


Figure 67. LVDS Conversion Data Output Mode for the AD4855

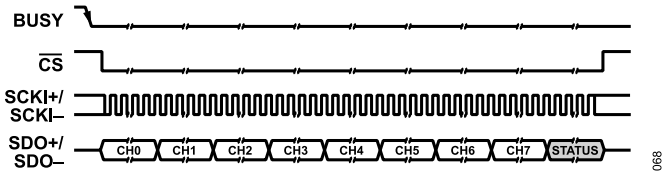


Figure 68. All Packets Are Sequentially Output on SDO+ and SDO−

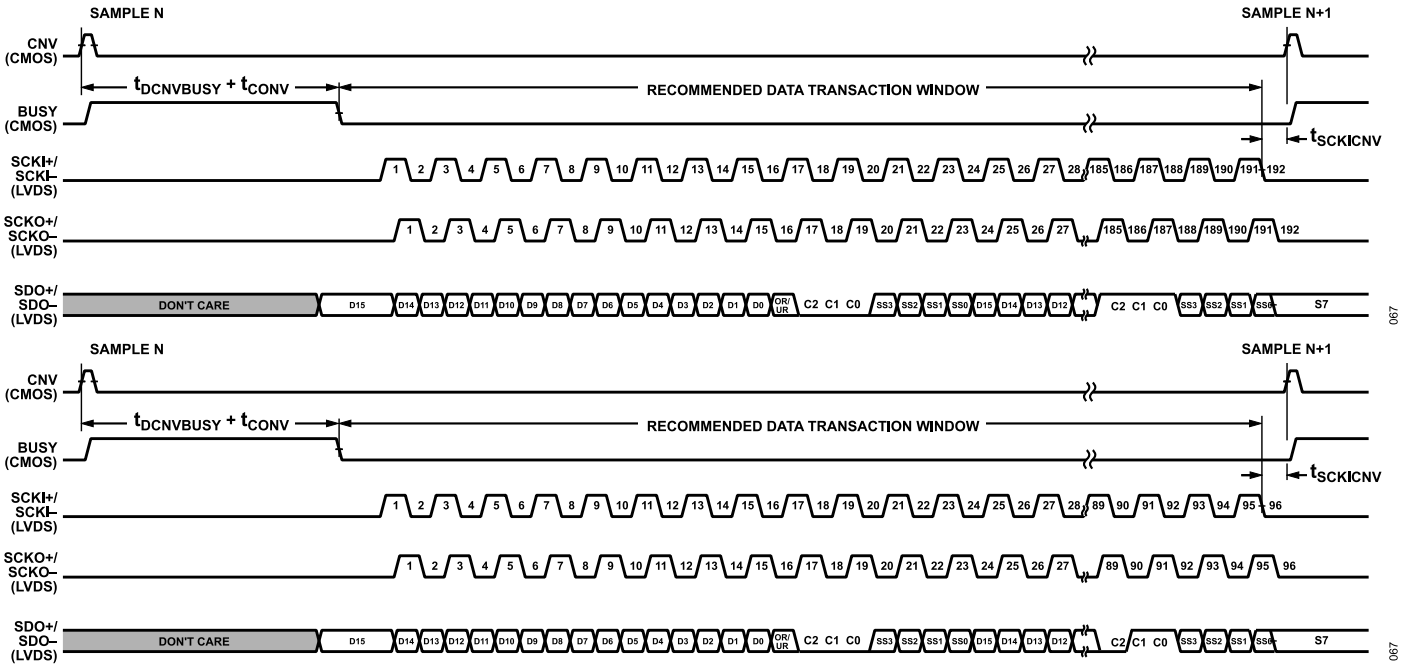


Figure 69. LVDS Serial Conversion Data Bus Timing, PACKET_SIZE = 0x1, OS_EN = 0, TEST_PAT = 0

DIGITAL INTERFACE

PACKET FORMAT

Data provided on the CMOS and LVDS conversion data output buses are packaged into eight channel packets and a ninth status packet, as shown in Figure 66 and Figure 68. Packet data formats are a function of packet size, oversampling mode, and test pattern configuration. The AD4855 offers two user-selectable packet sizes: 16-bit, and 24-bit. The default packet size is 24-bit.

Nonoversampling Packet Formats

With the AD4855 configured in nonoversampling mode, the channel and status packet data formats shown in Figure 70 are available. Select from these packet options using the PACKET_SIZE bits in the PACKET register. The channel packets include 16-bit conversion results plus options to report overrange or underrange of the conversion result, channel number identification, and channel SoftSpan identification. The status packet includes DEVICE_STATUS register state information and a 16-bit CRC computed for all data in the eight channel packets plus the ninth status packet.

The following CRC polynomial is used to calculate the checksums:

$$x^{16} + x^{14} + x^{13} + x^{12} + x^{10} + x^8 + x^6 + x^4 + x^3 + x + 1 \quad (4)$$

where the initial value for the CRC calculation is 0x0000 in all transactions.

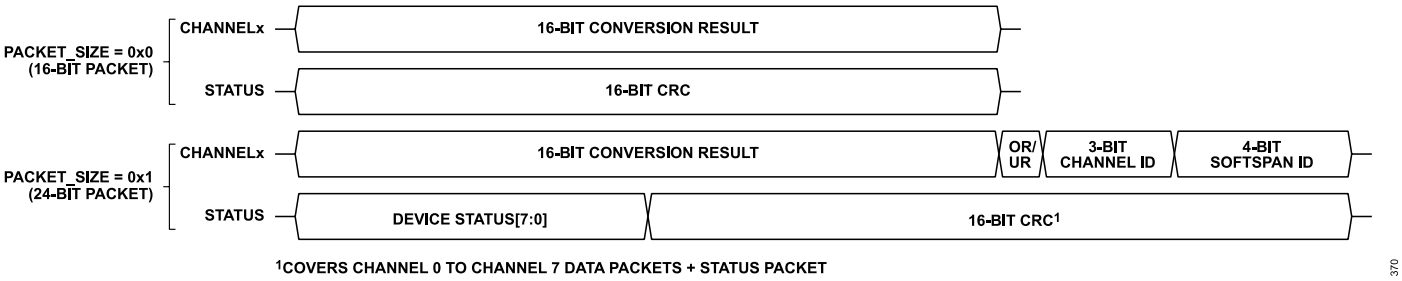


Figure 70. Channel and Status Packet Data Formats in Nonversampling Mode (OS_EN = 0), Test Pattern Output Disabled (TEST_PAT = 0)

DIGITAL INTERFACE

Oversampling Packet Formats

With the AD4855 configured in oversampling mode, the channel and status packet data formats shown in Figure 71 are available. Select from these packet options using the PACKET_SIZE bits (Bits[1:0]) in the Packet Format Register register. The channel packets include 16-bit averaged conversion results plus options to report the overrange or the underrange of any conversion included in the averaged result, channel number identification, and channel SoftSpan identification. The status packet includes Device Status Register register state information and a 16-bit CRC computed for all data in the eight channel packets and the ninth status packet.

The following CRC polynomial is used to calculate the checksums:

$$x^{16} + x^{14} + x^{13} + x^{12} + x^{10} + x^{8} + x^{6} + x^{4} + x^{3} + x + 1 \quad (5)$$

where the initial value for the CRC calculation is 0x0000 in all transactions.

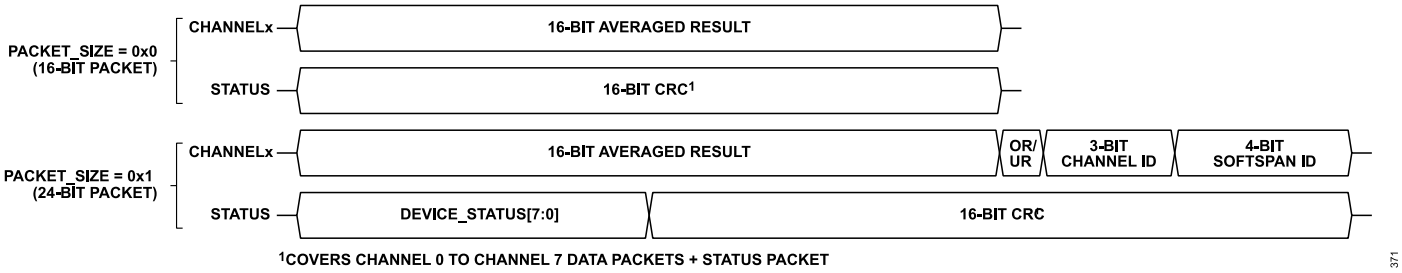


Figure 71. Channel and Status Packet Data Formats in Oversampling Mode (OS_EN = 1), Test Pattern Output Disabled (TEST_PAT = 0)

DIGITAL INTERFACE

Test Pattern Packet Format

The AD4855 offers a test pattern data output option that can be used to validate the CMOS or LVDS conversion data output bus operation. To enable this mode, set the TEST_PAT bit (Bit 2) to 1 in the Packet Format Register register. When the test pattern data output is enabled, the channel and status packet data formats shown in Figure 72 are available. Select from these packet options using the PACKET_SIZE bits (Bits[1:0]) in the Packet Format Register register. The channel packet data in this mode are defined by the data in the CHx_TESTPAT registers, shown in Table 19. In their default state, the CHx_TESTPAT registers contain a channel number identification in the most-significant nibble followed by a fixed pattern of 0xACE3C2A. Update these registers to match the test patterns required by the application. The status packet contains a 16-bit CRC computed for all data in the eight channel packets and the ninth status packet.

Table 19. Per Channel Test Pattern Registers

Register Name	Register Addresses	Default Pattern
CH0_TESTPAT	0x38 to 0x3B	0x0ACE3C2A
CH1_TESTPAT	0x4A to 0x4D	0x1ACE3C2A
CH2_TESTPAT	0x5C to 0x5F	0x2ACE3C2A
CH3_TESTPAT	0x6E to 0x71	0x3ACE3C2A
CH4_TESTPAT	0x80 to 0x83	0x4ACE3C2A
CH5_TESTPAT	0x92 to 0x95	0x5ACE3C2A
CH6_TESTPAT	0xA4 to 0xA7	0x6ACE3C2A
CH7_TESTPAT	0xB6 to 0xB9	0x7ACE3C2A

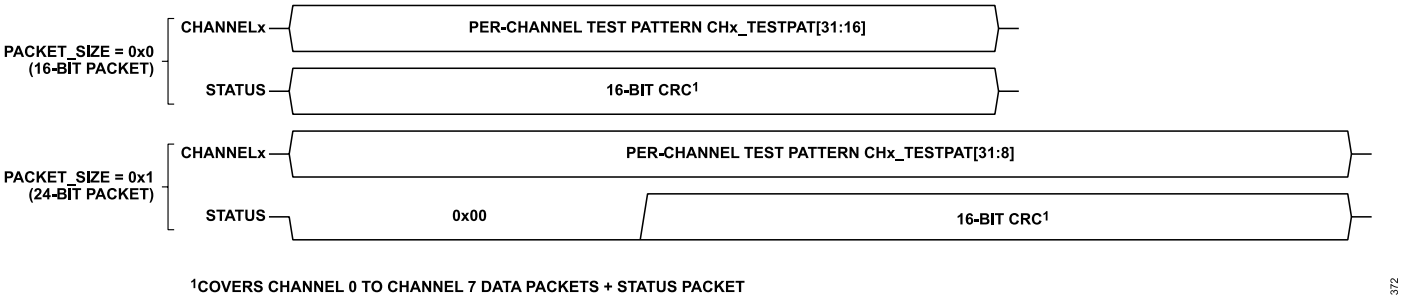


Figure 72. Channel and Status Packet Data Formats with Test Pattern Output Enabled (TEST_PAT = 1)

DIGITAL INTERFACE

SPI REGISTER CONFIGURATION BUS

The SPI register configuration bus allows the digital host to read from and write to the AD4855 memory map registers. This bus is independent of the CMOS or LVDS conversion data output buses.

On device power up or global reset, the SPI register configuration bus defaults to 3-wire operation, consisting of the CSCK pin, the CSDIO pin, and the $\overline{CS}$ pin. The 4-wire mode can be enabled by setting the CSDO_EN bit (Bit 4) to 1 in the SPI Configuration A Register register. The 4-wire mode SPI serial data is output on the CSDO line by default, but it can be output on the SDO0 lane by setting the CSDO_ON_SDO0 bit (Bit 0) to 1 in the SPI Configuration D Register register.

A basic SPI frame begins with a $\overline{CS}$ falling edge, followed by a 16-bit instruction phase and variable-length data phase, and terminates with a $\overline{CS}$ rising edge. Input data on the CSDIO lane is latched on the CSCK line rising edges while data is shifted out on the CSDIO lane (3-wire mode) or the CSDO line (4-wire mode) on the CSCK falling edges. Data is aligned at the MSB first for all SPI transactions.

Instruction Phase

Every SPI frame begins with a $\overline{CS}$ falling edge immediately followed by an instruction phase. The instruction phase consists of a read or write (R/$\overline{W}$) bit followed by a 15-bit register address word. Set the R/$\overline{W}$ bit high to initiate a read instruction or low to initiate a write instruction, as shown in Figure 73 and Figure 74. The register address word specifies the address of the register to be accessed.

Two instruction modes are supported by the AD4855. In streaming instruction mode, multiple contiguous addresses can be accessed during a variable-length data phase, which ends with a $\overline{CS}$ rising edge (see Streaming Instruction Mode section). In nonstreaming instruction mode, each instruction is followed by a single-byte (plus optional CRC byte) data phase, providing access to a single address per instruction (see the Nonstreaming Instruction Mode section). In this mode, multiple instruction and data phase pairs can be provided in a single SPI frame.

Data Phase

During the data phase, register data is shifted out on the CSDIO line (3-wire mode) or the CSDO line (4-wire mode) on the CSCK line falling edge for register reads. Register data is latched in on the CSDIO line on the CSCK line rising edge for register writes. Register contents are updated as each complete byte is received during register writes. If SPI bus CRC checking is enabled, the registers are only updated if a valid CRC checksum byte is received following each data byte (see the SPI Bus CRC Checking section).

3-Wire SPI Operation

On device power up or after a global reset, the SPI register configuration bus defaults to 3-wire operation, consisting of the CSCK pin, the CSDIO pin, and the $\overline{CS}$ pin. The timing diagrams shown in Figure 73 illustrate single-byte SPI read and write transactions in this operation mode.

During write transactions, the CSDIO pin functions as a serial data input during both the instruction and data phases. During read transactions, the CSDIO pin functions as a serial data input during the instruction phase and a serial data output during the data phase. The transition from input to output occurs after the last CSCK rising edge of the instruction phase. By using 3-wire mode, only three digital lines are required to be routed between the AD4855 and the digital host.

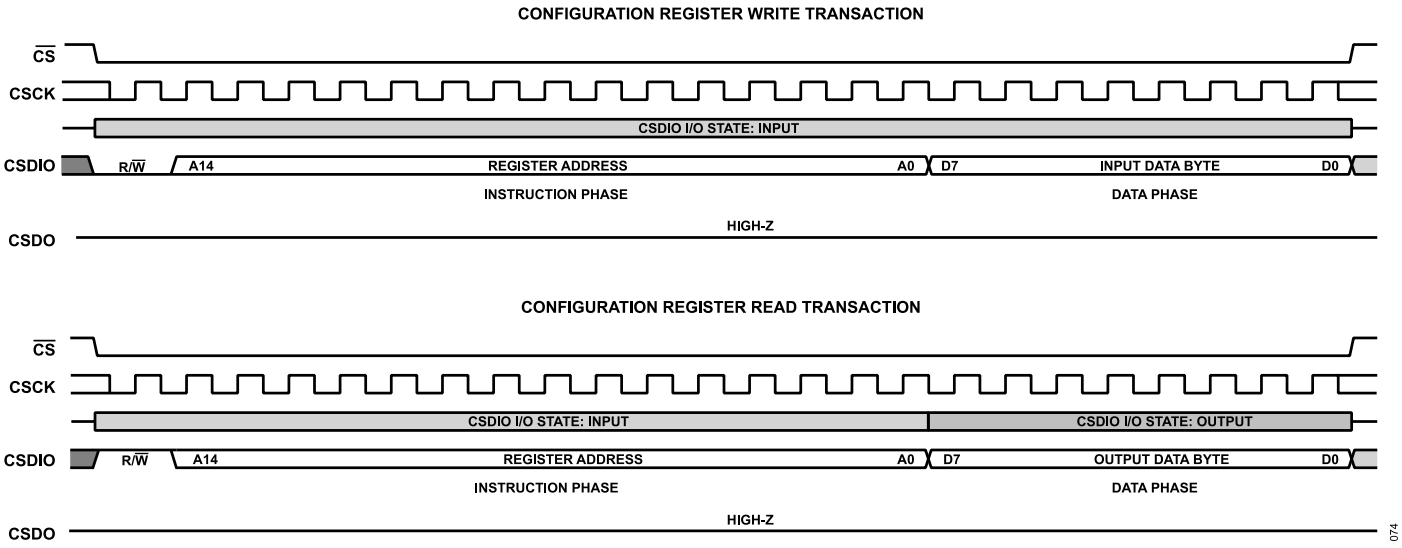


Figure 73. 3-Wire SPI Register Configuration Bus Frame

DIGITAL INTERFACE

4-Wire SPI Operation

To enable 4-wire operation of the SPI register configuration bus, set the CSDO_EN bit (Bit 4) to 1 in the SPI Configuration A Register register. In 4-wire mode, SPI serial data is output on the CSDO pin by default (see Figure 74); however, it can be optionally output on the SDO0 pin by setting the CSDO_ON_SDO0 bit (Bit 0) to 1 in the SPI Configuration D Register register. The latter option reduces the number of data lines required between the AD4855 and the host controller. In 4-wire bus operation, the CSDIO pin always functions as a serial data input, and either the CSDO pin or the SDO0 pin functions as the serial data output.

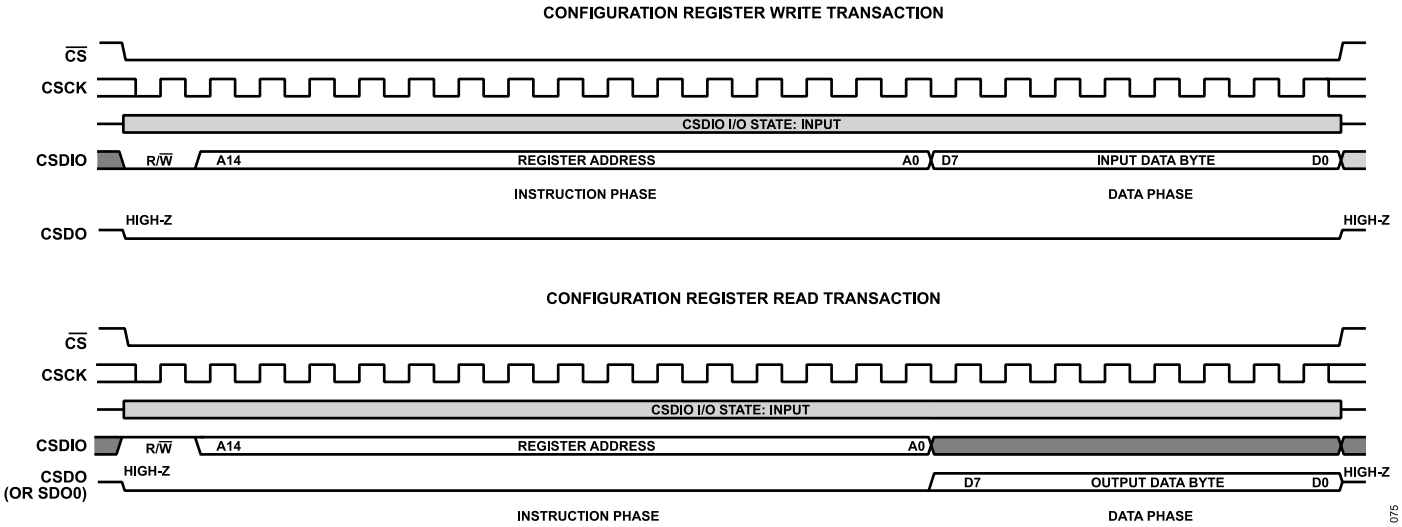


Figure 74. 4-Wire SPI Register Configuration Bus Frame

DIGITAL INTERFACE

Streaming Instruction Mode

When the INST_MODE bit (Bit 7) in the SPI Configuration B Register is set to 0, streaming mode is enabled. In streaming mode, only one instruction phase (see the Instruction Phase section) is accepted per SPI frame and is followed by multiple data phases (see the Data Phase section), one per register being accessed.

The register address being read from or written to is automatically incremented (ADDR_DIR bit high, Bit 5 of the SPI Configuration A Register) or decremented (ADDR_DIR bit low, Bit 5 of the SPI Configuration A Register) after each data phase. Streaming mode enables efficient access to large, contiguous register addresses of the AD4855 memory map and is enabled by default.

If the ascending address option is selected, the address automatically increments the number of times defined by the LOOP_SIZE bits (Bits[7:0] in the Loop Configuration A Register). If the address reaches 0xB9, it then continues from Address 0x00 on the subsequent byte access.

If the descending address option is selected, the address automatically decrements the number of times defined by LOOP_SIZE bits (Bits[7:0] in the Loop Configuration A Register). If the address reaches 0x00, it then continues from Address 0xB9 on the subsequent byte access.

By default, the LOOP_SIZE bits (Bits[7:0] in the Loop Configuration A Register) reset to 0 at every rising edge of the $\overline{CS}$ pin; therefore, a user-set value only persists for one SPI frame. If persistent looping is required, set KEEP_LOOP_SIZE bit (Bit 2 in the Loop Configuration B Register) to 1.

There is only one instruction phase per frame in streaming mode; therefore, all SPI transactions in a given SPI frame are either all reads or all writes.

Nonstreaming Instruction Mode

When the INST_MODE bit (Bit 7 in the SPI Configuration B Register register) is set to 1, nonstreaming instruction mode is selected. In nonstreaming instruction mode, one or more SPI transactions can be provided in a single SPI frame. Each transaction includes an instruction phase to specify whether a read or write is being performed, and which address is being accessed. Nonstreaming instruction mode allows the digital host to quickly read from and write to registers with nonadjacent register addresses in a single SPI frame, as opposed to streaming mode, which allows exclusively reading from or writing to registers with adjacent addresses in an SPI frame.

SPI Bus CRC Checking

The AD4855 register bus data includes optional error checking based on an 8-bit CRC. When the CRC is enabled, an 8-bit checksum code is appended to the data phase of the read or write transaction for each register. The value of the checksum is calculated from the data read or written, allowing the AD4855 and the digital host to detect if data corruption has occurred. If the checksum does not match the corresponding register data, the register read or write is considered invalid.

Use the following CRC polynomial to calculate the checksums:

$$x^8 + x^2 + x + 1 \quad (6)$$

The initial value for the CRC calculation is 0xA5 in all transactions.

REGISTER SUMMARY

The AD4855 has programmable user registers that are used to configure the device and monitor its state. These registers can be accessed using the SPI register configuration bus (see the SPI Register Configuration Bus section). Table 20 gives an overview of the full AD4855 register map and the bit fields contained in each single-byte register. Any register address that is not specified in this table is reserved. The Register Details section describes each register in more detail. The register details for Channel 0 are described, but the descriptions apply to all subsequent channel registers, Channel 1 through Channel 7. The reset state shows the default state of registers and bit fields after device reset. The access mode specifies whether bits are read-only (R), read or write (R/W), or read or write one to clear (R/W1C).

Table 20. Register Summary

Addr	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	SPI_CONFIG_A	[7:0]	SW_RST_MSB	RESERVED	ADDR_DIR	CSDO_EN	RESERVED			SW_RST_LSB	0x00	R/W
0x01	SPI_CONFIG_B	[7:0]	INST_MODE	RESERVED							0x00	R/W
0x02	DEVICE_CONFIG	[7:0]	RESERVED						PWR_MODE		0xF0	R/W
0x03	DEVICE_TYPE	[7:0]	RESERVED				DEVICE_TYPE				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x63	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	DEVICE_GRADE	[7:0]	DEVICE_GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	SPI_TYPE		VERSION						0x83	R
0x0C	VENDOR_ID_L	[7:0]	VENDOR_ID[7:0]								0x56	R
0x0D	VENDOR_ID_H	[7:0]	VENDOR_ID[15:8]								0x04	R
0x0E	LOOP_CONFIG_A	[7:0]	LOOP_SIZE								0x00	R/W
0x0F	LOOP_CONFIG_B	[7:0]	RESERVED					KEEP_LOOP_SIZE	RESERVED		0x00	R/W
0x10	SPI_CONFIG_C	[7:0]	CRC_ENABLE		RESERVED				CRC_ENABLE_N		0x03	R/W
0x11	SPI_STATUS	[7:0]	NOT_RDY_ERR	RESERVED		CLK_COUNT_ERR	CRC_ERR	WRITE_INVALID	RESERVED	ADDR_INVALID	0x00	R/W
0x14	SPI_CONFIG_D	[7:0]	RESERVED							CSDO_ON_SDO0	0x00	R/W
0x20	DEVICE_STATUS	[7:0]	DEVICE_READY_FLAG	RESET_FLAG	FUSE_CRC_FLAG	REGMAP_CRC_FLAG	SPI_FLAG	CH_ORUR_FLAG	PD_FLAG	SLEEP_FLAG	0x40	R/W
0x21	CH_OR_STATUS	[7:0]	CH7_OR_FLAG	CH6_OR_FLAG	CH5_OR_FLAG	CH4_OR_FLAG	CH3_OR_FLAG	CH2_OR_FLAG	CH1_OR_FLAG	CH0_OR_FLAG	0x00	R/W
0x22	CH_UR_STATUS	[7:0]	CH7_UR_FLAG	CH6_UR_FLAG	CH5_UR_FLAG	CH4_UR_FLAG	CH3_UR_FLAG	CH2_UR_FLAG	CH1_UR_FLAG	CH0_UR_FLAG	0x00	R/W
0x23	REGMAP_CRC	[7:0]	REGMAP_CRC[7:0]								0x00	R/W
0x24		[15:8]	REGMAP_CRC[15:8]								0x00	R/W
0x25	DEVICE_CTRL	[7:0]	TEST_CRCS	RESERVED		LVDS_TERM	LVDS_HALF_BIAS	REFBUF_PD	REF_SEL	SCKO_ECHO	0x11	R/W
0x26	PACKET	[7:0]	RESERVED					TEST_PAT	PACKET_SIZE		0x01	R/W
0x27	OVERSAMPLE	[7:0]	OS_EN	RESERVED			OS_RATIO				0x00	R/W
0x28	SEAMLESS_HDR	[7:0]	CH7_SHDR_EN	CH6_SHDR_EN	CH5_SHDR_EN	CH4_SHDR_EN	CH3_SHDR_EN	CH2_SHDR_EN	CH1_SHDR_EN	CH0_SHDR_EN	0xFF	R/W
0x29	CH_SLEEP	[7:0]	CH7_SLEEP	CH6_SLEEP	CH5_SLEEP	CH4_SLEEP	CH3_SLEEP	CH2_SLEEP	CH1_SLEEP	CH0_SLEEP	0x00	R/W
0x2A	CH0_SOFTSPAN	[7:0]	RESERVED				CH0_SOFTSPAN				0x0F	R/W
0x2B	CH0_OFFSET	[7:0]	RESERVED				RESERVED				0x00	R/W
0x2C		[15:8]	CH0_OFFSET[7:0]								0x00	R/W
0x2D		[23:16]	CH0_OFFSET[15:8]								0x00	R/W

REGISTER SUMMARY

Table 20. Register Summary (Continued)

Addr	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x2E	CH0_GAIN	[7:0]	CH0_GAIN[7:0]								0x00	R/W
0x2F		[15:8]	CH0_GAIN[15:8]								0x80	R/W
0x30	CH0_PHASE	[7:0]	CH0_PHASE[7:0]								0x00	R/W
0x31		[15:8]	CH0_PHASE[15:8]								0x00	R/W
0x32	CH0_OR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x33		[15:8]	CH0_OR[7:0]								0xFF	R/W
0x34		[23:16]	CH0_OR[15:8]								0x7F	R/W
0x35	CH0_UR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x36		[15:8]	CH0_UR[7:0]								0x00	R/W
0x37		[23:16]	CH0_UR[15:8]								0x80	R/W
0x38	CH0_TESTPAT	[7:0]	CH0_TESTPAT[7:0]								0x2A	R/W
0x39		[15:8]	CH0_TESTPAT[15:8]								0x3C	R/W
0x3A		[23:16]	CH0_TESTPAT[23:16]								0xCE	R/W
0x3B		[31:24]	CH0_TESTPAT[31:24]								0x0A	R/W
0x3C	CH1_SOFTSPAN	[7:0]	RESERVED				CH1_SOFTSPAN				0x0F	R/W
0x3D	CH1_OFFSET	[7:0]	RESERVED				RESERVED				0x00	R/W
0x3E		[15:8]	CH1_OFFSET[7:0]								0x00	R/W
0x3F		[23:16]	CH1_OFFSET[15:8]								0x00	R/W
0x40	CH1_GAIN	[7:0]	CH1_GAIN[7:0]								0x00	R/W
0x41		[15:8]	CH1_GAIN[15:8]								0x80	R/W
0x42	CH1_PHASE	[7:0]	CH1_PHASE[7:0]								0x00	R/W
0x43		[15:8]	CH1_PHASE[15:8]								0x00	R/W
0x44	CH1_OR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x45		[15:8]	CH1_OR[7:0]								0xFF	R/W
0x46		[23:16]	CH1_OR[15:8]								0x7F	R/W
0x47	CH1_UR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x48		[15:8]	CH1_UR[7:0]								0x00	R/W
0x49		[23:16]	CH1_UR[15:8]								0x80	R/W
0x4A	CH1_TESTPAT	[7:0]	CH1_TESTPAT[7:0]								0x2A	R/W
0x4B		[15:8]	CH1_TESTPAT[15:8]								0x3C	R/W
0x4C		[23:16]	CH1_TESTPAT[23:16]								0xCE	R/W
0x4D		[31:24]	CH1_TESTPAT[31:24]								0x1A	R/W
0x4E	CH2_SOFTSPAN	[7:0]	RESERVED				CH2_SOFTSPAN				0x0F	R/W
0x4F	CH2_OFFSET	[7:0]	RESERVED				RESERVED				0x00	R/W
0x50		[15:8]	CH2_OFFSET[7:0]								0x00	R/W
0x51		[23:16]	CH2_OFFSET[15:8]								0x00	R/W
0x52	CH2_GAIN	[7:0]	CH2_GAIN[7:0]								0x00	R/W
0x53		[15:8]	CH2_GAIN[15:8]								0x80	R/W
0x54	CH2_PHASE	[7:0]	CH2_PHASE[7:0]								0x00	R/W
0x55		[15:8]	CH2_PHASE[15:8]								0x00	R/W
0x56	CH2_OR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x57		[15:8]	CH2_OR[7:0]								0xFF	R/W
0x58		[23:16]	CH2_OR[15:8]								0x7F	R/W
0x59	CH2_UR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x5A		[15:8]	CH2_UR[7:0]								0x00	R/W
0x5B		[23:16]	CH2_UR[15:8]								0x80	R/W

REGISTER SUMMARY

Table 20. Register Summary (Continued)

Addr	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x5C	CH2_TESTPAT	[7:0]	CH2_TESTPAT[7:0]								0x2A	R/W
0x5D		[15:8]	CH2_TESTPAT[15:8]								0x3C	R/W
0x5E		[23:16]	CH2_TESTPAT[23:16]								0xCE	R/W
0x5F		[31:24]	CH2_TESTPAT[31:24]								0x2A	R/W
0x60	CH3_SOFTSPAN	[7:0]	RESERVED				CH3_SOFTSPAN				0x0F	R/W
0x61	CH3_OFFSET	[7:0]	RESERVED				RESERVED				0x00	R/W
0x62		[15:8]	CH3_OFFSET[7:0]								0x00	R/W
0x63		[23:16]	CH3_OFFSET[15:8]								0x00	R/W
0x64	CH3_GAIN	[7:0]	CH3_GAIN[7:0]								0x00	R/W
0x65		[15:8]	CH3_GAIN[15:8]								0x80	R/W
0x66	CH3_PHASE	[7:0]	CH3_PHASE[7:0]								0x00	R/W
0x67		[15:8]	CH3_PHASE[15:8]								0x00	R/W
0x68	CH3_OR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x69		[15:8]	CH3_OR[7:0]								0xFF	R/W
0x6A		[23:16]	CH3_OR[15:8]								0x7F	R/W
0x6B	CH3_UR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x6C		[15:8]	CH3_UR[7:0]								0x00	R/W
0x6D		[23:16]	CH3_UR[15:8]								0x80	R/W
0x6E	CH3_TESTPAT	[7:0]	CH3_TESTPAT[7:0]								0x2A	R/W
0x6F		[15:8]	CH3_TESTPAT[15:8]								0x3C	R/W
0x70		[23:16]	CH3_TESTPAT[23:16]								0xCE	R/W
0x71		[31:24]	CH3_TESTPAT[31:24]								0x3A	R/W
0x72	CH4_SOFTSPAN	[7:0]	RESERVED				CH4_SOFTSPAN				0x0F	R/W
0x73	CH4_OFFSET	[7:0]	RESERVED				RESERVED				0x00	R/W
0x74		[15:8]	CH4_OFFSET[7:0]								0x00	R/W
0x75		[23:16]	CH4_OFFSET[15:8]								0x00	R/W
0x76	CH4_GAIN	[7:0]	CH4_GAIN[7:0]								0x00	R/W
0x77		[15:8]	CH4_GAIN[15:8]								0x80	R/W
0x78	CH4_PHASE	[7:0]	CH4_PHASE[7:0]								0x00	R/W
0x79		[15:8]	CH4_PHASE[15:8]								0x00	R/W
0x7A	CH4_OR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x7B		[15:8]	CH4_OR[7:0]								0xFF	R/W
0x7C		[23:16]	CH4_OR[15:8]								0x7F	R/W
0x7D	CH4_UR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x7E		[15:8]	CH4_UR[7:0]								0x00	R/W
0x7F		[23:16]	CH4_UR[15:8]								0x80	R/W
0x80	CH4_TESTPAT	[7:0]	CH4_TESTPAT[7:0]								0x2A	R/W
0x81		[15:8]	CH4_TESTPAT[15:8]								0x3C	R/W
0x82		[23:16]	CH4_TESTPAT[23:16]								0xCE	R/W
0x83		[31:24]	CH4_TESTPAT[31:24]								0x4A	R/W
0x84	CH5_SOFTSPAN	[7:0]	RESERVED				CH5_SOFTSPAN				0x0F	R/W
0x85	CH5_OFFSET	[7:0]	RESERVED				RESERVED				0x00	R/W
0x86		[15:8]	CH5_OFFSET[7:0]								0x00	R/W
0x87		[23:16]	CH5_OFFSET[15:8]								0x00	R/W
0x88	CH5_GAIN	[7:0]	CH5_GAIN[7:0]								0x00	R/W
0x89		[15:8]	CH5_GAIN[15:8]								0x80	R/W
0x8A	CH5_PHASE	[7:0]	CH5_PHASE[7:0]								0x00	R/W

REGISTER SUMMARY

Table 20. Register Summary (Continued)

Addr	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x8B		[15:8]	CH5_PHASE[15:8]								0x00	R/W
0x8C	CH5_OR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x8D		[15:8]	CH5_OR[7:0]								0xFF	R/W
0x8E		[23:16]	CH5_OR[15:8]								0x7F	R/W
0x8F	CH5_UR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x90		[15:8]	CH5_UR[7:0]								0x00	R/W
0x91		[23:16]	CH5_UR[15:8]								0x80	R/W
0x92	CH5_TESTPAT	[7:0]	CH5_TESTPAT[7:0]								0x2A	R/W
0x93		[15:8]	CH5_TESTPAT[15:8]								0x3C	R/W
0x94		[23:16]	CH5_TESTPAT[23:16]								0xCE	R/W
0x95		[31:24]	CH5_TESTPAT[31:24]								0x5A	R/W
0x96	CH6_SOFTSPAN	[7:0]	RESERVED				CH6_SOFTSPAN				0x0F	R/W
0x97	CH6_OFFSET	[7:0]	RESERVED				RESERVED				0x00	R/W
0x98		[15:8]	CH6_OFFSET[7:0]								0x00	R/W
0x99		[23:16]	CH6_OFFSET[15:8]								0x00	R/W
0x9A	CH6_GAIN	[7:0]	CH6_GAIN[7:0]								0x00	R/W
0x9B		[15:8]	CH6_GAIN[15:8]								0x80	R/W
0x9C	CH6_PHASE	[7:0]	CH6_PHASE[7:0]								0x00	R/W
0x9D		[15:8]	CH6_PHASE[15:8]								0x00	R/W
0x9E	CH6_OR	[7:0]	RESERVED				RESERVED				0x00	R/W
0x9F		[15:8]	CH6_OR[7:0]								0xFF	R/W
0xA0		[23:16]	CH6_OR[15:8]								0x7F	R/W
0xA1	CH6_UR	[7:0]	RESERVED				RESERVED				0x00	R/W
0xA2		[15:8]	CH6_UR[7:0]								0x00	R/W
0xA3		[23:16]	CH6_UR[15:8]								0x80	R/W
0xA4	CH6_TESTPAT	[7:0]	CH6_TESTPAT[7:0]								0x2A	R/W
0xA5		[15:8]	CH6_TESTPAT[15:8]								0x3C	R/W
0xA6		[23:16]	CH6_TESTPAT[23:16]								0xCE	R/W
0xA7		[31:24]	CH6_TESTPAT[31:24]								0x6A	R/W
0xA8	CH7_SOFTSPAN	[7:0]	RESERVED				CH7_SOFTSPAN				0x0F	R/W
0xA9	CH7_OFFSET	[7:0]	RESERVED				RESERVED				0x00	R/W
0xAA		[15:8]	CH7_OFFSET[7:0]								0x00	R/W
0xAB		[23:16]	CH7_OFFSET[15:8]								0x00	R/W
0xAC	CH7_GAIN	[7:0]	CH7_GAIN[7:0]								0x00	R/W
0xAD		[15:8]	CH7_GAIN[15:8]								0x80	R/W
0xAE	CH7_PHASE	[7:0]	CH7_PHASE[7:0]								0x00	R/W
0xAF		[15:8]	CH7_PHASE[15:8]								0x00	R/W
0xB0	CH7_OR	[7:0]	RESERVED				RESERVED				0x00	R/W
0xB1		[15:8]	CH7_OR[7:0]								0xFF	R/W
0xB2		[23:16]	CH7_OR[15:8]								0x7F	R/W
0xB3	CH7_UR	[7:0]	RESERVED				RESERVED				0x00	R/W
0xB4		[15:8]	CH7_UR[7:0]								0x00	R/W
0xB5		[23:16]	CH7_UR[15:8]								0x80	R/W
0xB6	CH7_TESTPAT	[7:0]	CH7_TESTPAT[7:0]								0x2A	R/W
0xB7		[15:8]	CH7_TESTPAT[15:8]								0x3C	R/W
0xB8		[23:16]	CH7_TESTPAT[23:16]								0xCE	R/W
0xB9		[31:24]	CH7_TESTPAT[31:24]								0x7A	R/W

REGISTER DETAILS

SPI CONFIGURATION A REGISTER

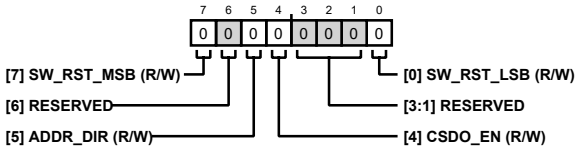


Figure 75. Address: 0x00, Reset: 0x00, Name: SPI_CONFIG_A

Table 21. Bit Descriptions for SPI_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RST_MSB	Software Reset (MSB). Setting both SW_RST_MSB and SW_RST_LSB to 1 using a single register write initiates a software reset of the AD4855. This software reset resets all registers to their default states, except for the ADDR_DIR and CSDO_EN bits in the SPI_CONFIG_A register.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	ADDR_DIR	Address Direction. Selects between descending or ascending register addressing during multibyte read or write transactions on the SPI register configuration bus (see the Streaming Instruction Mode section). 0: Descending Addressing. Register address decremented by one for each data byte. 1: Ascending Addressing. Register address incremented by one for each data byte.	0x0	R/W
4	CSDO_EN	CSDO Pin Enable. Selects between 3-wire or 4-wire operation of the SPI register configuration bus (see the the 3-Wire SPI Operation section and the 4-Wire SPI Operation section). 0: CSDO Disabled. SPI bus operates in 3-wire mode with data input and output on CSDIO. CSDO is not used and remains high-Z. 1: CSDO Enabled. SPI bus operates in 4-wire mode with data input on CSDIO and data output on CSDO (or SDO0 if CSDO_ON_SDO0 in SPI_CONFIG_D register is set to 1).	0x0	R/W
[3:1]	RESERVED	Reserved.	0x0	R
0	SW_RST_LSB	Software Reset (LSB). Setting both SW_RST_MSB and SW_RST_LSB to 1 using a single register write initiates a software reset of the AD4855. This software reset resets all registers to their default states, except for the ADDR_DIR and CSDO_EN bits in the SPI_CONFIG_A register.	0x0	R/W

REGISTER DETAILS

SPI CONFIGURATION B REGISTER

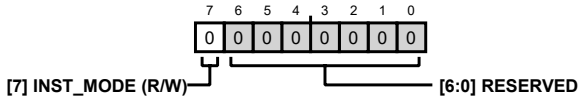


Figure 76. Address: 0x01, Reset: 0x00, Name: SPI_CONFIG_B

Table 22. Bit Descriptions for SPI_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	INST_MODE	Instruction Mode. Selects between streaming and nonstreaming instruction modes of the SPI register configuration bus (see the Streaming Instruction Mode section and the Nonstreaming Instruction Mode section). 0: Streaming Instruction Mode. The SPI bus accepts multibyte read or write transactions. The register address is automatically updated for each successive data byte based on the ADDR_DIR bit (Bit 5) in SPI Configuration A Register register. 1: Nonstreaming Instruction Mode. The SPI bus accepts single-byte read or write transactions.	0x0	R/W
[6:0]	RESERVED	Reserved.	0x0	R

DEVICE CONFIGURATION REGISTER

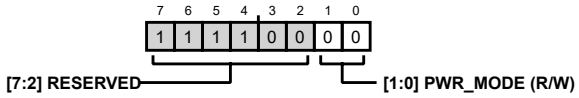


Figure 77. Address: 0x02, Reset: 0xF0, Name: DEVICE_CONFIG

Table 23. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x3C	R
[1:0]	PWR_MODE	Power Mode. Software-controllable alternative to PD pin functionality. 00: Normal Operating Mode. 11: Power-Down Mode. Same effect as driving the PD pin to a high state.	0x0	R/W

DEVICE TYPE REGISTER

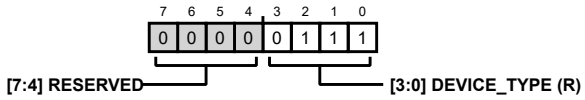


Figure 78. Address: 0x03, Reset: 0x07, Name: DEVICE_TYPE

Table 24. Bit Descriptions for DEVICE_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	DEVICE_TYPE	Device Type. Identifies the AD4855 as a precision ADC product.	0x7	R

REGISTER DETAILS

PRODUCT ID LOW REGISTER

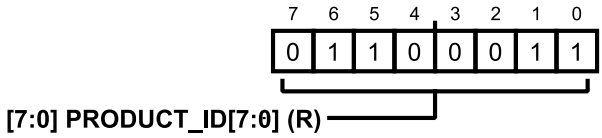


Figure 79. Address: 0x04, Reset: 0x63, Name: PRODUCT_ID_L

Table 25. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product Identification. One byte of the AD4855 PRODUCT_ID.	0x63	R

PRODUCT ID HIGH REGISTER

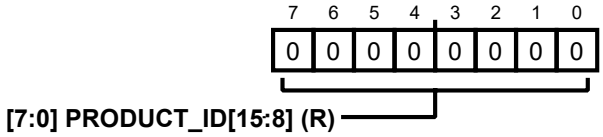


Figure 80. Address: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

Table 26. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product Identification. One byte of the AD4855 PRODUCT_ID.	0x0	R

DEVICE GRADE REGISTER

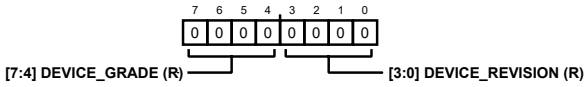


Figure 81. Address: 0x06, Reset: 0x00, Name: DEVICE_GRADE

Table 27. Bit Descriptions for DEVICE_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	DEVICE_GRADE	Device Performance Grade. Identifies the AD4855 performance grade.	0x0	R
[3:0]	DEVICE_REVISION	Device Hardware Revision. Identifies the AD4855 hardware revision.	0x0	R

SCRATCH PAD REGISTER

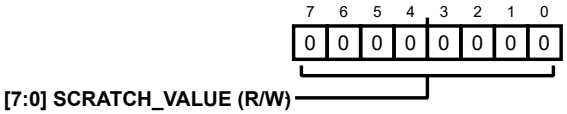


Figure 82. Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

Table 28. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Software can write to and read from this location without any device side effects. Use this register to test SPI register configuration bus communication.	0x0	R/W

REGISTER DETAILS

SPI REVISION REGISTER

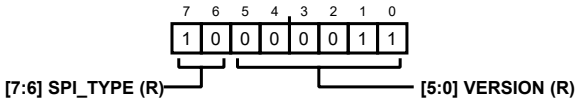


Figure 83. Address: 0x0B, Reset: 0x83, Name: SPI_REVISION

Table 29. Bit Descriptions for SPI_REVISION

Bits	Bit Name	Description	Reset	Access
[7:6]	SPI_TYPE	SPI Type. Identifies the ADI SPI type supported by the AD4855.	0x2	R
[5:0]	VERSION	SPI Version. Identifies the ADI SPI version supported by the AD4855.	0x3	R

VENDOR ID LOW REGISTER

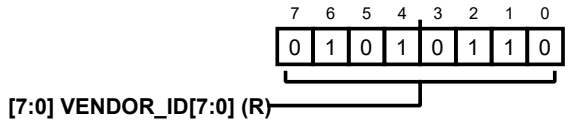


Figure 84. Address: 0x0C, Reset: 0x56, Name: VENDOR_ID_L

Table 30. Bit Descriptions for VENDOR_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]	Vendor Identification. One byte of the ADI VENDOR_ID. This value is the same for all ADI precision ADCs.	0x56	R

VENDOR ID HIGH REGISTER

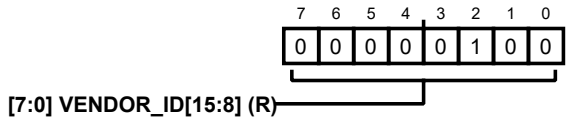


Figure 85. Address: 0x0D, Reset: 0x04, Name: VENDOR_ID_H

Table 31. Bit Descriptions for VENDOR_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]	Vendor Identification. One byte of the ADI VENDOR_ID. This value is the same for all ADI precision ADCs.	0x4	R

LOOP CONFIGURATION A REGISTER

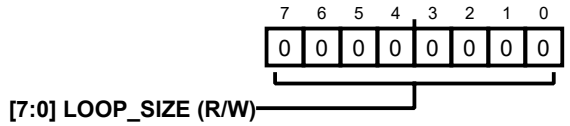


Figure 86. Address: 0x0E, Reset: 0x00, Name: LOOP_CONFIG_A

Table 32. Bit Descriptions for LOOP_CONFIG_A

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_SIZE	Loop Size. When streaming instruction mode is enabled (see the Streaming Instruction Mode section), the value of LOOP_SIZE defines the number of data bytes to be sequentially read or written before	0x0	R/W

REGISTER DETAILS

Table 32. Bit Descriptions for LOOP_CONFIG_A (Continued)

Bits	Bit Name	Description	Reset	Access
		looping back to the starting address. A maximum of 255 bytes can be repeatedly looped using this approach. The default value of 0x00 disables looping, in which case, addressing wraps around the upper or lower limits of the register map.		

LOOP CONFIGURATION B REGISTER

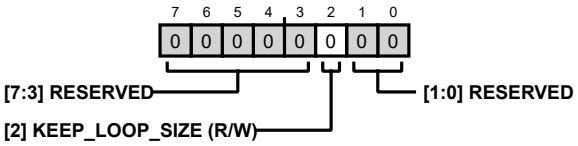


Figure 87. Address: 0x0F, Reset: 0x00, Name: LOOP_CONFIG_B

Table 33. Bit Descriptions for LOOP_CONFIG_B

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	KEEP_LOOP_SIZE	Keep Loop Size. Selects between resetting or retaining the LOOP_SIZE bits (Bits[7:0]) in the Loop Configuration A Register register at the completion of the current streaming SPI register configuration bus transaction. 0: Resets LOOP_SIZE to 0x00 with the rising edge of $\overline{CS}$. 1: Do not reset LOOP_SIZE.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

SPI CONFIGURATION C REGISTER

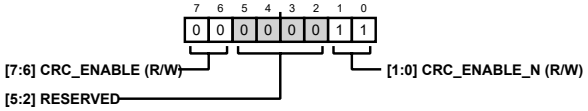


Figure 88. Address: 0x10, Reset: 0x03, Name: SPI_CONFIG_C

Table 34. Bit Descriptions for SPI_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:6]	CRC_ENABLE	CRC Enable. Optional CRC checking is enabled on the SPI register configuration bus transactions when CRC_ENABLE = 0x1 and CRC_ENABLE_N = 0x2. Any other combination of values in these bits disables SPI CRC checking.	0x0	R/W
[5:2]	RESERVED	Reserved.	0x0	R
[1:0]	CRC_ENABLE_N	Inverted CRC Enable. Optional CRC checking is enabled on the SPI register configuration bus transactions when CRC_ENABLE = 0x1 and CRC_ENABLE_N = 0x2. Any other combination of values in these bits disables SPI CRC checking.	0x3	R/W

REGISTER DETAILS

SPI STATUS REGISTER

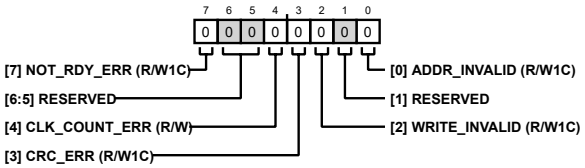


Figure 89. Address: 0x11, Reset: 0x00, Name: SPI_STATUS

Table 35. Bit Descriptions for SPI_STATUS

Bits	Bit Name	Description	Reset	Access
7	NOT_RDY_ERR	Not Ready for Transaction Error. This flag is set to 1 if an SPI register configuration bus transaction is initiated before the AD4855 is ready to respond, for example, before the AD4855 power-on reset initialization sequence successfully completes.	0x0	R/W1C
[6:5]	RESERVED	Reserved.	0x0	R
4	CLK_COUNT_ERR	Clock Count Error. This flag is set to 1 if an SPI register configuration bus transaction presents an incorrect number of CSCK edges, for example, if the SPI frame ends in the middle of a data byte.	0x0	R/W
3	CRC_ERR	CRC Error. This flag is set to 1 if CRC checking is enabled and the AD4855 receives a checksum that does not match its computed value.	0x0	R/W1C
2	WRITE_INVALID	Invalid Write Error. This flag is set to 1 if the digital host attempts to write to a register that exclusively contains read-only bits.	0x0	R/W1C
1	RESERVED	Reserved.	0x0	R
0	ADDR_INVALID	Invalid Register Address Error. This flag is set to 1 if the digital host attempts to read from or write to an undefined register address.	0x0	R/W1C

SPI CONFIGURATION D REGISTER

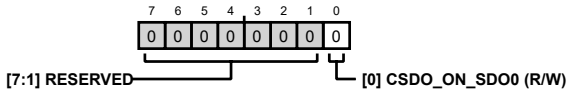


Figure 90. Address: 0x14, Reset: 0x00, Name: SPI_CONFIG_D

Table 36. Bit Descriptions for SPI_CONFIG_D

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	CSDO_ON_SDO0	Output CSDO Data on SDO0. Selects between providing 4-wire SPI register configuration bus output data on CSDO or SDO0 (see the 4-Wire SPI Operation section). 0: Output 4-wire SPI bus data on CSDO. 1: Output 4-wire SPI bus data on SDO0.	0x0	R/W

REGISTER DETAILS

DEVICE STATUS REGISTER

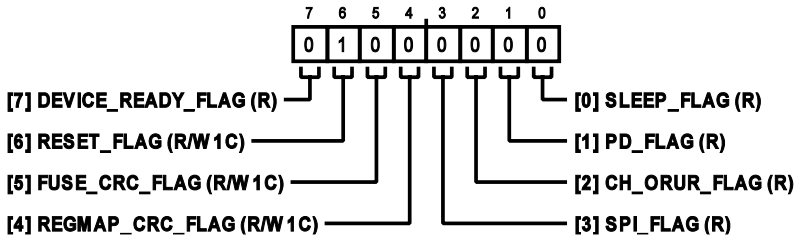


Figure 91. Address: 0x20, Reset: 0x40, Name: DEVICE_STATUS

Table 37. Bit Descriptions for DEVICE_STATUS

Bits	Bit Name	Description	Reset	Access
7	DEVICE_READY_FLAG	Device Ready Flag. The AD4855 internal state is continually monitored for potential corruption due to alpha particles, system supply glitches, etc. This flag is set to 1 upon successful completion of the power-on reset initialization sequence at the falling edge of BUSY. A value of 0 at any time past this point indicates an error in the internal device state that requires a user-initiated global reset (see the Reset Timing section).	0x0	R
6	RESET_FLAG	Reset Flag. This flag is set to 1 at the beginning of any reset event.	0x1	R/W1C
5	FUSE_CRC_FLAG	Fuse CRC Flag. The AD4855 internal state is continually monitored for potential corruption due to alpha particles, system supply glitches, etc. A value of 1 at any time in this flag indicates an error has been detected that requires a user-initiated global reset (see the Reset Timing section).	0x0	R/W1C
4	REGMAP_CRC_FLAG	Register Map CRC Flag. The state of the AD4855 register map is continually monitored for potential corruption due to alpha particles, system supply glitches, etc. A value of 1 at any time in this flag indicates a CRC error has been detected and the digital host must check the register map for errors. Ignore this flag if the Register Map CRC register has not been programmed with the proper CRC code.	0x0	R/W1C
3	SPI_FLAG	SPI Flag. This flag is the logical OR of all bits in the SPI Status Register register.	0x0	R
2	CH_ORUR_FLAG	Channel Overrange/Underrange Flag. This flag is the logical OR of all bits in the Channel Overrange Status Register register and Channel Underrange Status Register register.	0x0	R
1	PD_FLAG	Power Down Flag. This flag is set to 1 when the AD4855 is currently in power-down mode.	0x0	R
0	SLEEP_FLAG	Channel Sleep Flag. This flag is the logical OR of all bits in the Channel Sleep Register register.	0x0	R

REGISTER DETAILS

CHANNEL OVERRANGE STATUS REGISTER

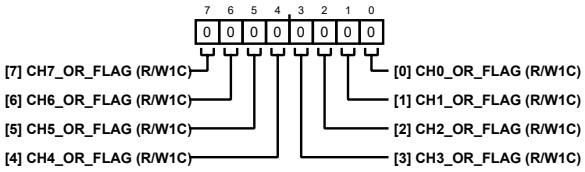


Figure 92. Address: 0x21, Reset: 0x00, Name: CH_OR_STATUS

Table 38. Bit Descriptions for CH_OR_STATUS

Bits	Bit Name	Description	Reset	Access
7	CH7_OR_FLAG	Channel 7 Overrange Flag. This flag is set to 1 when a conversion result on Channel 7 exceeds the overrange limit set in the CH7_OR register.	0x0	R/W1C
6	CH6_OR_FLAG	Channel 6 Overrange Flag. This flag is set to 1 when a conversion result on Channel 6 exceeds the overrange limit set in the CH6_OR register.	0x0	R/W1C
5	CH5_OR_FLAG	Channel 5 Overrange Flag. This flag is set to 1 when a conversion result on Channel 5 exceeds the overrange limit set in the CH5_OR register.	0x0	R/W1C
4	CH4_OR_FLAG	Channel 4 Overrange Flag. This flag is set to 1 when a conversion result on Channel 4 exceeds the overrange limit set in the CH4_OR register.	0x0	R/W1C
3	CH3_OR_FLAG	Channel 3 Overrange Flag. This flag is set to 1 when a conversion result on Channel 3 exceeds the overrange limit set in the CH3_OR register.	0x0	R/W1C
2	CH2_OR_FLAG	Channel 2 Overrange Flag. This flag is set to 1 when a conversion result on Channel 2 exceeds the overrange limit set in the CH2_OR register.	0x0	R/W1C
1	CH1_OR_FLAG	Channel 1 Overrange Flag. This flag is set to 1 when a conversion result on Channel 1 exceeds the overrange limit set in the CH1_OR register.	0x0	R/W1C
0	CH0_OR_FLAG	Channel 0 Overrange Flag. This flag is set to 1 when a conversion result on Channel 0 exceeds the overrange limit set in the CH0_OR register.	0x0	R/W1C

CHANNEL UNDERRANGE STATUS REGISTER

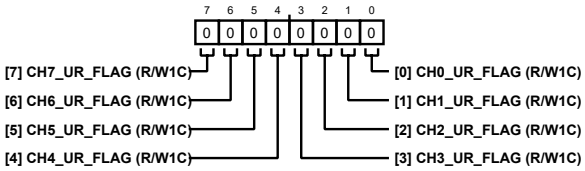


Figure 93. Address: 0x22, Reset: 0x00, Name: CH_UR_STATUS

Table 39. Bit Descriptions for CH_UR_STATUS

Bits	Bit Name	Description	Reset	Access
7	CH7_UR_FLAG	Channel 7 Underrange Flag. This flag is set to 1 when a conversion result on Channel 7 exceeds the underrange limit set in the CH7_UR register.	0x0	R/W1C
6	CH6_UR_FLAG	Channel 6 Underrange Flag. This flag is set to 1 when a conversion result on Channel 6 exceeds the underrange limit set in the CH6_UR register.	0x0	R/W1C
5	CH5_UR_FLAG	Channel 5 Underrange Flag. This flag is set to 1 when a conversion result on Channel 5 exceeds the underrange limit set in the CH5_UR register.	0x0	R/W1C
4	CH4_UR_FLAG	Channel 4 Underrange Flag. This flag is set to 1 when a conversion result on Channel 4 exceeds the underrange limit set in the CH4_UR register.	0x0	R/W1C

REGISTER DETAILS

Table 39. Bit Descriptions for CH_UR_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
3	CH3_UR_FLAG	Channel 3 Underrange Flag. This flag is set to 1 when a conversion result on Channel 3 exceeds the underrange limit set in the CH3_UR register.	0x0	R/W1C
2	CH2_UR_FLAG	Channel 2 Underrange Flag. This flag is set to 1 when a conversion result on Channel 2 exceeds the underrange limit set in the CH2_UR register.	0x0	R/W1C
1	CH1_UR_FLAG	Channel 1 Underrange Flag. This flag is set to 1 when a conversion result on Channel 1 exceeds the underrange limit set in the CH1_UR register.	0x0	R/W1C
0	CH0_UR_FLAG	Channel 0 Underrange Flag. This flag is set to 1 when a conversion result on Channel 0 exceeds the underrange limit set in the CH0_UR register.	0x0	R/W1C

REGISTER MAP CRC

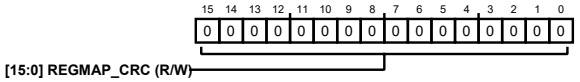


Figure 94. Address: 0x23 to Address: 0x24, Reset: 0x0000, Name: REGMAP_CRC

Table 40. Bit Descriptions for REGMAP_CRC

Bits	Bit Name	Description	Reset	Access
[15:0]	REGMAP_CRC	Register Map CRC. User-calculated CRC checksum covering Address 0xB9 down to 0x25. May be used to continually monitor the state of the AD4855 register map for potential corruption due to alpha particles, system supply glitches, etc. The following CRC polynomial is used to calculate the checksums: $x^{16} + x^{14} + x^{13} + x^{12} + x^{10} + x^8 + x^6 + x^4 + x^3 + x + 1$ where the initial value for the CRC calculation is 0xFFFF.	0x0	R/W

DEVICE CONTROL REGISTER

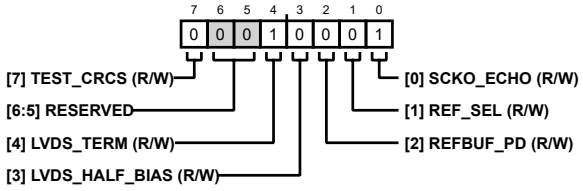


Figure 95. Address: 0x25, Reset: 0x11, Name: DEVICE_CTRL

Table 41. Bit Descriptions for DEVICE_CTRL

Bits	Bit Name	Description	Reset	Access
7	TEST_CRCS	Test CRC Engines. Set to 1 while running conversions to introduce a simulated bit error into the FUSE CRC and REGMAP CRC engines. To validate CRC engine functionality, verify that both the FUSE_CRC_FLAG bit (Bit 5) and the REGMAP_CRC_FLAG bit (Bit 4) in the Device Status Register register are set to 1.	0x0	R/W
[6:5]	RESERVED	Reserved.	0x0	R
4	LVDS_TERM	LVDS Termination Enable. Set to 1 to enable the internal termination resistor on LVDS input pairs.	0x1	R/W

REGISTER DETAILS

Table 41. Bit Descriptions for DEVICE_CTRL (Continued)

Bits	Bit Name	Description	Reset	Access
3	LVDS_HALF_BIAS	LVDS Half-Bias Enable. Set to 1 to enable half-bias output drive mode on LVDS output pairs.	0x0	R/W
2	REFBUF_PD	Reference Buffer Power Down. Set to 1 to power down the internal reference buffer. When powered down, an external reference can be connected to the REFBUF pin as shown in Figure 58.	0x0	R/W
1	REF_SEL	Reference Selection. Select whether to use an external or internal reference 0: Internal Reference. Enables the internal reference. 1: External Reference. Powers down the internal reference. Connect an external reference on the REFIO pin, as shown in the Figure 57.	0x0	R/W
0	SCKO_ECHO	SCKO Echo Enable. Set to 1 to enable SCKO echoing of SCKI signal.	0x1	R/W

PACKET FORMAT REGISTER

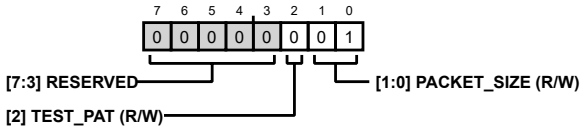


Figure 96. Address: 0x26, Reset: 0x01, Name: PACKET

Table 42. Bit Descriptions for PACKET

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	TEST_PAT	Test Pattern Enable. Set to 1 to enable test pattern output data. When enabled, normal conversion data output packets are replaced with fixed data defined by the upper bits of each channels CHx_TESTPAT register (see the Test Pattern Packet Format section). Use this functionality to validate CMOS or LVDS conversion data output bus communication.	0x0	R/W
[1:0]	PACKET_SIZE	Packet Size. Selects between 16-bit, or 24-bit packet sizes on the CMOS or LVDS conversion data output bus. Packet data formatting for each packet size depends on whether the AD4855 is operating in non-oversampling or oversampling mode, and whether test pattern data output is enabled (see the Packet Format section and the Test Pattern Packet Format section). 00: 16-bit packet size. 01: 24-bit packet size. 10: Reserved, do not use. 11: Reserved, do not use.	0x1	R/W

OVERSAMPLE CONTROL REGISTER

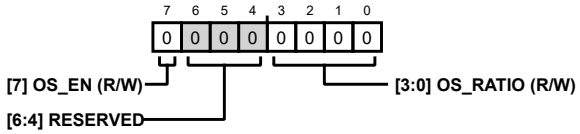


Figure 97. Address: 0x27, Reset: 0x00, Name: OVERSAMPLE

Table 43. Bit Descriptions for OVERSAMPLE

Bits	Bit Name	Description	Reset	Access
7	OS_EN	Oversample Enable. Selects between oversampling and non-oversampling mode (see the Oversampling Mode section).	0x0	R/W

REGISTER DETAILS

Table 43. Bit Descriptions for OVERSAMPLE (Continued)

Bits	Bit Name	Description	Reset	Access
		0: Oversampling disabled. Disable oversampling before changing oversampling ratio. 1: Oversampling enabled.		
[6:4]	RESERVED	Reserved.	0x0	R
[3:0]	OS_RATIO	Oversampling Ratio. When oversampling is enabled, selects the number of conversion results to be digitally averaged for each channel (see the Oversampling Mode section). 0000: Average 2 conversions results. 0001: Average 4 conversions results. 0010: Average 8 conversions results. 0011: Average 16 conversions results. 0100: Average 32 conversions results. 0101: Average 64 conversions results. 0110: Average 128 conversions results. 0111: Average 256 conversions results. 1000: Average 512 conversions results. 1001: Average 1024 conversions results. 1010: Average 2048 conversions results. 1011: Average 4096 conversions results. 1100: Average 8192 conversions results. 1101: Average 16,384 conversions results. 1110: Average 32,768 conversions results. 1111: Average 65,536 conversions results.	0x0	R/W

SEAMLESS HIGH DYNAMIC RANGE REGISTER

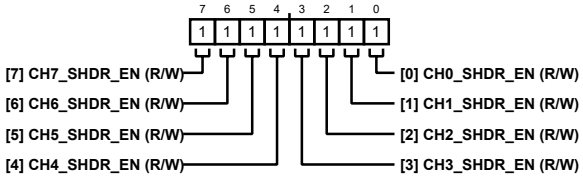


Figure 98. Address: 0x28, Reset: 0xFF, Name: SEAMLESS_HDR

Table 44. Bit Descriptions for SEAMLESS_HDR

Bits	Bit Name	Description	Reset	Access
7	CH7_SHDR_EN	Channel 7 SHDR Enable. Set to 1 to enable SHDR on this channel.	0x1	R/W
6	CH6_SHDR_EN	Channel 6 SHDR Enable. Set to 1 to enable SHDR on this channel.	0x1	R/W
5	CH5_SHDR_EN	Channel 5 SHDR Enable. Set to 1 to enable SHDR on this channel.	0x1	R/W
4	CH4_SHDR_EN	Channel 4 SHDR Enable. Set to 1 to enable SHDR on this channel.	0x1	R/W
3	CH3_SHDR_EN	Channel 3 SHDR Enable. Set to 1 to enable SHDR on this channel.	0x1	R/W
2	CH2_SHDR_EN	Channel 2 SHDR Enable. Set to 1 to enable SHDR on this channel.	0x1	R/W
1	CH1_SHDR_EN	Channel 1 SHDR Enable. Set to 1 to enable SHDR on this channel.	0x1	R/W
0	CH0_SHDR_EN	Channel 0 SHDR Enable. Set to 1 to enable SHDR on this channel.	0x1	R/W

REGISTER DETAILS

CHANNEL SLEEP REGISTER

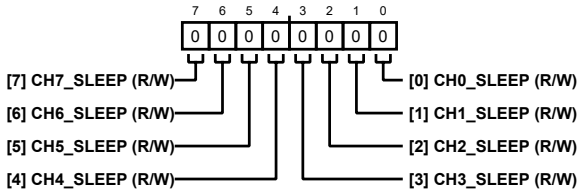


Figure 99. Address: 0x29, Reset: 0x00, Name: CH_SLEEP

Table 45. Bit Descriptions for CH_SLEEP

Bits	Bit Name	Description	Reset	Access
7	CH7_SLEEP	Channel 7 Sleep. Set to 1 to sleep channel, saving power. Channel ignores conversion requests.	0x0	R/W
6	CH6_SLEEP	Channel 6 Sleep. Set to 1 to sleep channel, saving power. Channel ignores conversion requests.	0x0	R/W
5	CH5_SLEEP	Channel 5 Sleep. Set to 1 to sleep channel, saving power. Channel ignores conversion requests.	0x0	R/W
4	CH4_SLEEP	Channel 4 Sleep. Set to 1 to sleep channel, saving power. Channel ignores conversion requests.	0x0	R/W
3	CH3_SLEEP	Channel 3 Sleep. Set to 1 to sleep channel, saving power. Channel ignores conversion requests.	0x0	R/W
2	CH2_SLEEP	Channel 2 Sleep. Set to 1 to sleep channel, saving power. Channel ignores conversion requests.	0x0	R/W
1	CH1_SLEEP	Channel 1 Sleep. Set to 1 to sleep channel, saving power. Channel ignores conversion requests.	0x0	R/W
0	CH0_SLEEP	Channel 0 Sleep. Set to 1 to sleep channel, saving power. Channel ignores conversion requests.	0x0	R/W

CHANNEL 0 SOFTSPAN REGISTER

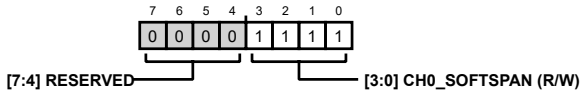


Figure 100. Address: 0x2A, Reset: 0x0F, Name: CH0_SOFTSPAN

Table 46. Bit Descriptions for CH0_SOFTSPAN

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CH0_SOFTSPAN	Channel 0 SoftSpan. Selects the SoftSpan range for this channel (see the SoftSpan section). 0000: 0 V to 2.5V range. 0001: ±2.5 V range. 0010: 0 V to 5V range. 0011: ±5 V range. 0100: 0 V to 6.25 V range. 0101: ±6.25 V range. 0110: 0 V to 10 V range. 0111: ±10 V range. 1000: 0 V to 12.5 V range. 1001: ±12.5 V range. 1010: 0 V to 20 V range.	0xF	R/W

REGISTER DETAILS

Table 46. Bit Descriptions for CH0_SOFTSPAN (Continued)

Bits	Bit Name	Description	Reset	Access
		1011: ±20 V range. 1100: 0 V to 25 V range. 1101: ±25V range. 1110: 0 V to 40 V range. 1111: ±40 V range.		

CHANNEL 0 OFFSET REGISTER

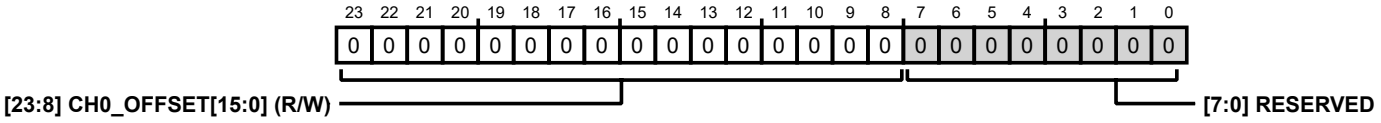


Figure 101. Address: 0x2B to Address: 0x2D, Reset: 0x000000, Name: CH0_OFFSET

Table 47. Bit Descriptions for CH0_OFFSET

Bits	Bit Name	Description	Reset	Access
[23:8]	CH0_OFFSET[15:0]	Channel 0 Offset. The 16-bit signed digital offset correction value to be added to every conversion result on this channel (see the Digital Offset Correction section). Offset default state corresponds to zero offset correction.	0x0	R/W
[7:0]	RESERVED	Reserved.	0x0	R

CHANNEL 0 GAIN REGISTER

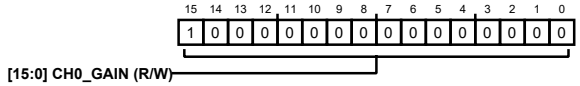


Figure 102. Address: 0x2E to Address: 0x2F, Reset: 0x8000, Name: CH0_GAIN

Table 48. Bit Descriptions for CH0_GAIN

Bits	Bit Name	Description	Reset	Access
[15:0]	CH0_GAIN	Channel 0 Gain. The 16-bit unsigned digital gain correction factor to be applied to every conversion result on this channel (see the Digital Gain Correction section). Default state corresponds to factor of 1.00000.	0x8000	R/W

CHANNEL 0 PHASE REGISTER

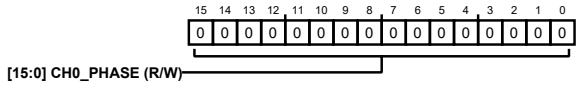


Figure 103. Address: 0x30 to Address: 0x31, Reset: 0x0000, Name: CH0_PHASE

Table 49. Bit Descriptions for CH0_PHASE

Bits	Bit Name	Description	Reset	Access
[15:0]	CH0_PHASE	Channel 0 Phase. The 16-bit unsigned phase correction term to be applied to this channel. This register is only relevant when operating in oversampling mode (see the Oversampling Mode section and the Digital Phase Correction section).	0x0	R/W

REGISTER DETAILS

CHANNEL 0 OVERRANGE LIMIT REGISTER

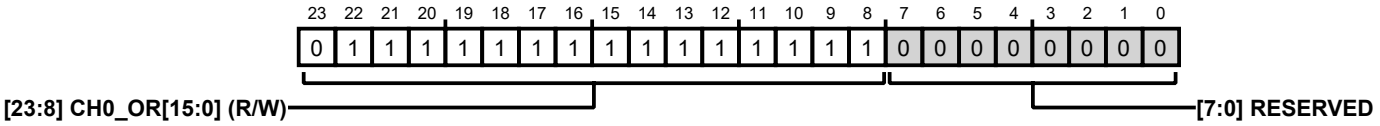


Figure 104. Address: 0x32 to Address 0x34, Reset: 0x7FFF00, Name: CH0_OR

Table 50. Bit Descriptions for CH0_OR

Bits	Bit Name	Description	Reset	Access
[23:8]	CH0_OR[15:0]	Channel 0 Overrange Limit. If any conversion result on Channel 0 is larger than this 16-bit signed digital overrange threshold value, the CH0_OR_FLAG bit (Bit 0) in the Channel Overrange Status Register is set to 1.	0x7FFF	R/W
[7:0]	RESERVED	Reserved.	0x0	R

CHANNEL 0 UNDERRANGE LIMIT REGISTER

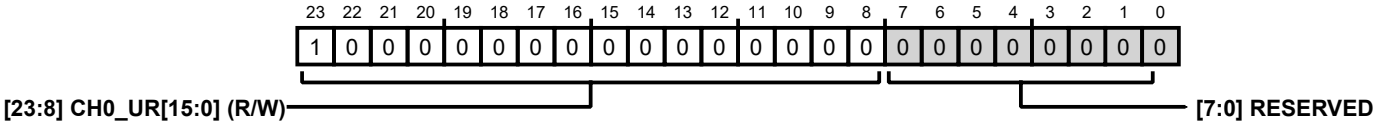


Figure 105. Address: 0x35 to Address 0x37, Reset: 0x800000, Name: CH0_UR

Table 51. Bit Descriptions for CH0_UR

Bits	Bit Name	Description	Reset	Access
[23:8]	CH0_UR[15:0]	Channel 0 Underrange Limit. If any conversion result on Channel 0 is less than this 16-bit signed digital underrange threshold value, the CH0_UR_FLAG bit (Bit 0) in the Channel Underrange Status Register is set to 1.	0x8000	R/W
[7:0]	RESERVED	Reserved.	0x0	R

CHANNEL 0 TEST PATTERN REGISTER

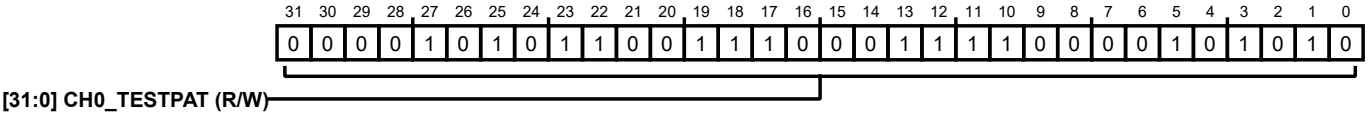
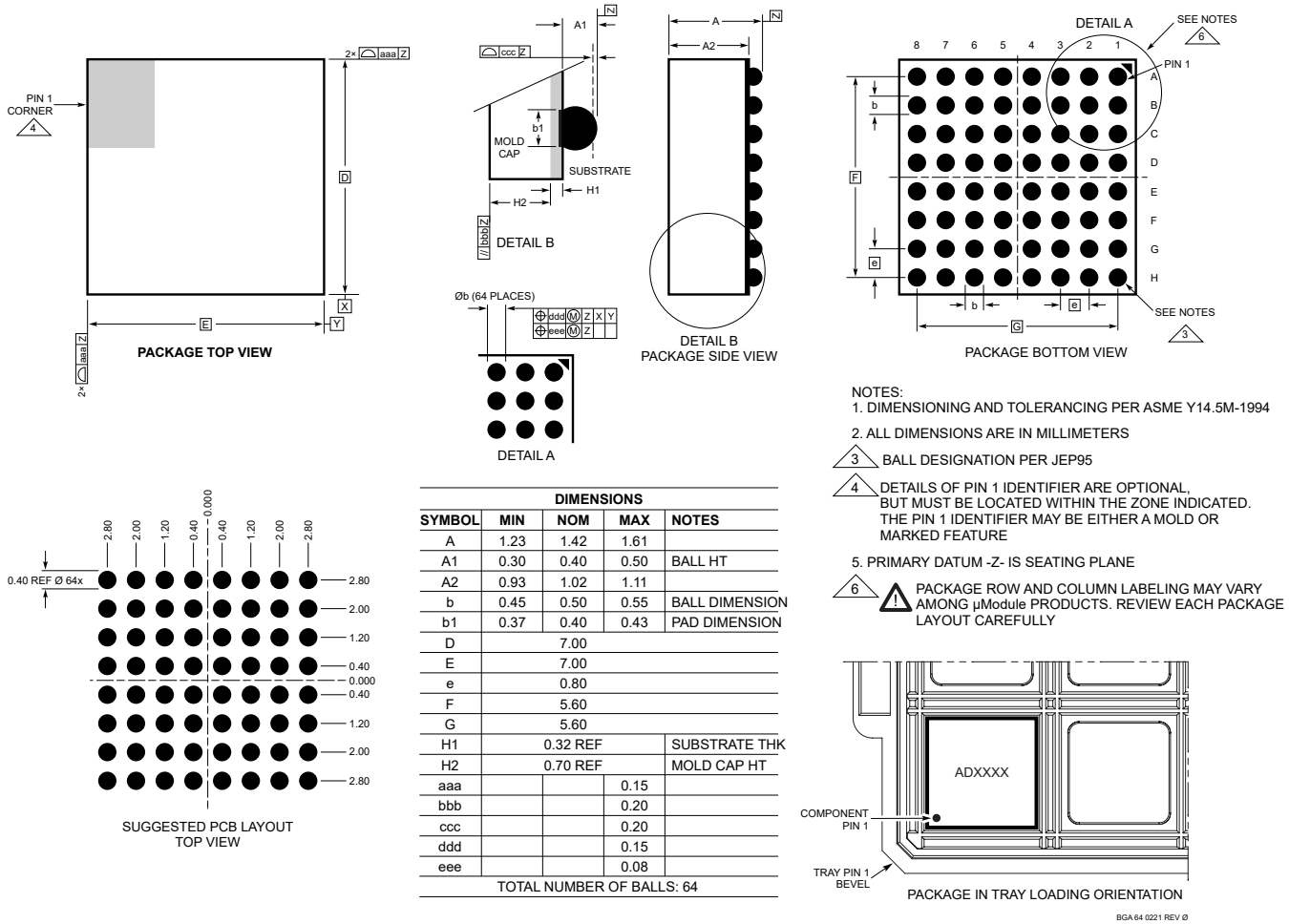


Figure 106. Address: 0x38 to Address:0x3B, Reset: 0x0ACE3C2A, Name: CH0_TESTPAT

Table 52. Bit Descriptions for CH0_TESTPAT

Bits	Bit Name	Description	Reset	Access
[31:0]	CH0_TESTPAT	Channel 0 Test Pattern. When the test pattern output is enabled (see the Test Pattern Packet Format section), the normal conversion data output packets for Channel 0 are replaced with fixed data defined by CH0_TESTPAT. The reset state of the most-significant nibble of the CHx_TESTPAT registers corresponds to the numerical value of the channel (that is, 0x0 for Channel 0, 0x1 for Channel 1, and so on).	0xACE3C2A	R/W

OUTLINE DIMENSIONS



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.23	1.42	1.61	
A1	0.30	0.40	0.50	BALL HT
A2	0.93	1.02	1.11	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		7.00		
E		7.00		
e		0.80		
F		5.60		
G		5.60		
H1		0.32 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.15	
bbb			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 64				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

Figure 107. 64-Ball BGA Package
7 mm × 7 mm × 1.42 mm
(05-08-7086)
Dimensions shown in millimeters

Updated: November 17, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4855BBCZ	−40°C to +125°C	64-Lead BGA (7 mm × 7 mm × 1.42 mm)	Tray, 416	05-08-7086
AD4855BBCZ-RL-13	−40°C to +125°C	64-Lead BGA (7 mm × 7 mm × 1.42 mm)	Reel, 2000	05-08-7086

[1] Z = RoHS Compliant Part.

EVALUATION BOARD

Model[1, 2]	Description
EVAL-AD4857FMCZ	AD4857 Evaluation Board

[1] Z = RoHS Compliant Part.

[2] The EVAL-AD4857FMCZ evaluation board can be used to evaluate the AD4855.

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