Dual Mode HDMI/MHL Receiver

Data Sheet

ADV7480

FEATURES

- Mobile High-Definition Link (MHL) capable receiver
  - High-bandwidth Digital Content Protection (HDCP) authentication and decryption support
  - 75 MHz maximum pixel clock frequency, allowing HDTV formats up to 720p/1080i at 60 Hz
  - 24 bits per pixel mode supported
  - HDCP repeater support, up to 25 KSVs supported
  - Adaptive TMDS equalizer
- High-Definition Multimedia Interface (HDMI) capable receiver
  - HDCP authentication and decryption support
  - 162 MHz maximum pixel clock frequency, allowing HDTV formats up to 1080p and display resolutions up to UXGA (1600 × 1200 at 60 Hz)
  - HDCP repeater support, up to 25 KSVs supported
  - Integrated CEC controller, CEC 1.4 compatible
  - Adaptive TMDS equalizer
  - 5 V detect and Hot Plug assert
- Component video processor
  - Any-to-any 3 × 3 color space conversion (CSC) matrix
  - Contrast/brightness/hue/saturation video adjustment
  - Timing adjustments controls for horizontal sync (HS)/vertical sync (VS)/data enable (DE) timing
  - Video mute function
- Serial digital audio output interface
  - HDMI/MHL audio extraction support
  - Advanced audio muting feature
  - I²S-compatible, left justified and right justified audio output modes
  - 8-channel TDM output mode available
- Mobile Industry Processor Interface (MIPI) Camera Serial Interface 2 (CSI-2) transmitter
  - 4-lane transmitter with 4 lanes, 2 lanes, and 1 lane muxing options for HDMI/MHL/digital input port sources
- 8-bit digital input/output port
- General
  - 2-wire serial microprocessor unit (MPU) interface (I²C compatible)
  - −40°C to +85°C temperature grade
  - 100-ball, 9 mm × 9 mm, RoHS-compliant CSP_BGA package
  - Qualified for automotive applications

APPLICATIONS

- Portable devices
- Automotive infotainment (head unit and rear seat entertainment systems)
- HDMI repeaters and video switches

FUNCTIONAL BLOCK DIAGRAM

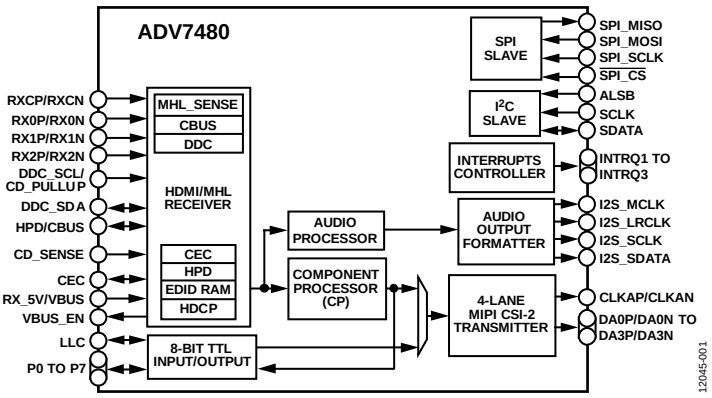

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

6/14—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADV7480 is a combined HDMI®/MHL® receiver targeted at connectivity enabled head units requiring a wired, uncompressed digital audio/video link from smartphones and other consumer electronics devices to support streaming and integration of cloud-based multimedia content and applications into an automotive infotainment system.

The ADV7480 MHL 2.1 capable receiver supports a maximum pixel clock frequency of 75 MHz, allowing resolutions up to 720p/1080i at 60 Hz in 24-bit mode. The ADV7480 features a link control bus (CBUS) that handles the link layer, translation layer, CBUS electrical discovery, and display data channel (DDC) commands. The implementation of the MHL sideband channel (MSC) commands by the system processor can be handled either by the I²C bus, or via a dedicated serial peripheral interface (SPI) bus. A dedicated interrupt pin (INTRQ3) is available to indicate that events related to CBUS have occurred.

The ADV7480 also features an enable pin (VBUS_EN) to dynamically enable or disable the output of a voltage regulator, which provides a 5 V voltage bus (VBUS) signal to the MHL source.

The ADV7480 HDMI capable receiver supports a maximum pixel clock frequency of 162 MHz, allowing HDTV formats up to 1080p, and display resolutions up to UXGA (1600 × 1200 at 60 Hz). The device integrates a consumer electronics control (CEC) controller that supports the capability discovery and control (CDC) feature. The HDMI input port has dedicated 5 V detect and Hot Plug™ assert pins.

The HDMI/MHL receiver includes an adaptive transition minimized differential signaling (TMDS) equalizer that ensures robust operation of the interface with long cables.

The ADV7480 single receiver port is capable of accepting both HDMI and MHL electrical signals. Automatic detection between HDMI and MHL is achieved by using cable impedance detection through the CD_SENSE pin.

The ADV7480 contains a component processor (CP) that processes the video signals from the HDMI/MHL receiver. It provides features such as contrast, brightness, and saturation adjustments, as well as free run and timing adjustment controls for HS/VS/DE timing.

The ADV7480 features an 8-bit digital input/output port, supporting input and output video resolutions up to 720p/1080i in both the 8-bit interleaved 4:2:2 SDR and DDR modes.

To enable glueless interfacing of these video input sources to the latest generation of infotainment system on chips (SoCs), the ADV7480 features a MIPI® CSI-2 transmitter. The four-lane transmitter provides four data lanes, two data lanes, and one data lane muxing options, and can be used to output video from the HDMI receiver, the MHL receiver, and the digital input port.

The ADV7480 offers a flexible audio output port for audio data extracted from the MHL or HDMI streams. The HDMI/MHL receiver has advanced audio functionality, such as a mute controller that prevents audible extraneous noise in the audio output. Additionally, the ADV7480 can be set to output time division multiplexing (TDM) serial audio, which allows the transmission of eight multiplexed serial audio channels on a single audio output interface port.

The ADV7480 is programmed via a 2-wire, serial, bidirectional port (I²C compatible).

Fabricated in an advanced CMOS process, the ADV7480 is available in a 9 mm × 9 mm, RoHS-compliant, 100-ball CSP_BGA package and is specified over the −40°C to +85°C temperature range.

The ADV7480 is offered in automotive and industrial versions.

DETAILED FUNCTIONAL BLOCK DIAGRAM

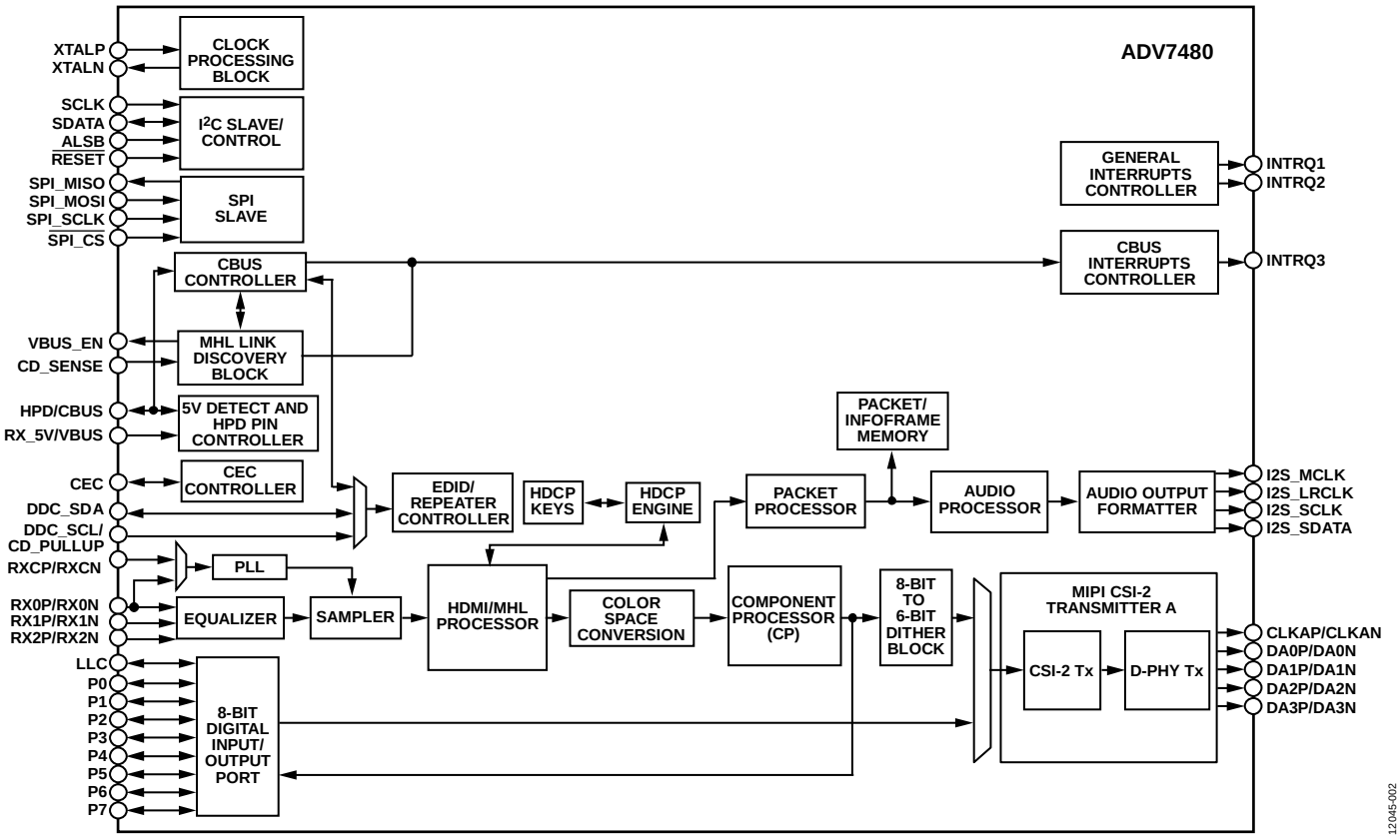

Figure 2.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

AVDD = 1.71 V to 1.89 V, DVDD = 1.71 V to 1.89 V, PVDD = 1.71 V to 1.89 V, MVDD = 1.71 V to 1.89 V, CVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, and TVDD = 3.14 V to 3.46 V, specified at operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS[1]		SCLK, SDATA, $\overline{\text{RESET}}$, ALSB, $\overline{\text{SPI_CS}}$, SPI_SCLK, SPI_MOSI, LLC, and P0 to P7				
Input High Voltage	V_{IH}	DVDDIO = 3.14 V to 3.46 V	2			V
Input Low Voltage	V_{IL}	DVDDIO = 3.14 V to 3.46 V			0.8	V
Input Leakage Current	I_{IN}		−10		+10	µA
Input Capacitance[2]	C_{IN}				10	pF
CRYSTAL INPUT						
Input High Voltage	V_{IH}	XTALP	1.2			V
Input Low Voltage	V_{IL}	XTALP			0.4	V
DIGITAL OUTPUTS[1]		LLC, P0 to P7, I2S_MCLK, I2S_SCLK, I2S_LRCLK, I2S_SDATA, SPI_MISO, SDATA, INTRQ1 to INTRQ3 (when configured to drive when active), and VBUS_EN				
Output High Voltage	V_{OH}	DVDDIO = 3.14 V to 3.46 V and I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage	V_{OL}	DVDDIO = 3.14 V to 3.46 V and I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}			10		µA
Output Capacitance[2]	C_{OUT}				20	pF
POWER REQUIREMENTS						
Digital Power Supply	D_{VDD}		1.71	1.8	1.89	V
HDMI/MHL Terminator Supply	T_{VDD}		3.14	3.3	3.46	V
HDMI/MHL Comparator Supply	C_{VDD}		1.71	1.8	1.89	V
PLL Power Supply	P_{VDD}		1.71	1.8	1.89	V
MIPI Transmitter Power Supply	M_{VDD}		1.71	1.8	1.89	V
Digital Input/Output Power Supply[1]	D_{VDDIO}	3.3 V operation	3.14	3.3	3.46	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
CURRENT CONSUMPTION[1, 2, 3, 4]						
Digital Supply Current	I_{DVDD}				204	mA
HDMI Input				68.1		mA
MHL Input				93.5		mA
8-Bit Digital Input				32.5		mA
HDMI/MHL Terminator Supply Current	I_{TVDD}				40	mA
HDMI Input				35		mA
MHL Input				24.4		mA
8-Bit Digital Input				0.7		mA
HDMI/MHL Comparator Supply Current	I_{CVDD}				92	mA
HDMI Input				63.9		mA
MHL Input				55.9		mA
8-Bit Digital Input				0.1		mA
PLL Supply Current	I_{PVDD}				39	mA
HDMI Input				29.2		mA
MHL Input				29.3		mA
8-Bit Digital Input				27.9		mA
MIPI Transmitters Supply Current	I_{MVDD}				62	mA
HDMI Input				45.7		mA
MHL Input				38.5		mA
8-Bit Digital Input				38.1		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Digital Input/Output Supply Current	I_{DVDDIO}				78	mA
HDMI Input				3.6		mA
MHL Input				0.6		mA
8-Bit Digital Input				0.2		mA
Analog Supply Current	I_{AVDD}				1	mA
HDMI Input				0.1		mA
MHL Input				0.1		mA
8-Bit Digital Input				0.1		mA
POWER-DOWN CURRENTS[2, 5]						
Digital Supply	I_{DVDD_PD}			0.2		mA
HDMI/MHL Terminator Supply	I_{TVDD_PD}			0.4		mA
HDMI/MHL Comparator Supply	I_{CVDD_PD}			0.1		mA
PLL Supply	I_{PVDD_PD}			0.1		mA
MIPI Transmitter Supply	I_{MVDD_PD}			0.1		mA
Digital Input/Output Supply	I_{DVDDIO_PD}			0.2		mA
Analog Supply	I_{AVDD_PD}			0.1		mA
Total Power Dissipation in Power-Down Mode				4		mW

[1] The 8-bit digital input/output port is only available when the DVDDIO supply is between 3.14 V and 3.46 V
[2] Guaranteed by lab characterization.
[3] Typical current consumption values are recorded with nominal voltage supply levels (including DVDDIO = 3.3 V), Philips test pattern, and at room temperature.
[4] Maximum current consumption values are recorded with maximum rated voltage supply levels (including DVDDIO = 3.46 V), pseudorandom test pattern for digital inputs, and at worst-case temperature.
[5] Typical power-down current consumption values are recorded with nominal voltage supply levels (including DVDDIO = 3.3 V) at room temperature.

MIPI VIDEO OUTPUT SPECIFICATIONS

AVDD = 1.71 V to 1.89 V, DVDD = 1.71 V to 1.89 V, PVDD = 1.71 V to 1.89 V, MVDD = 1.71 V to 1.89 V, CVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, and TVDD = 3.14 V to 3.46 V, specified at operating temperature range, unless otherwise noted.

The ADV7480 MIPI CSI-2 transmitter conforms to the MIPI D-PHY Version 1.00.00 specification by characterization. The clock lane of the ADV7480 remains in high speed (HS) mode even when the data lane enters low power (LP) mode. For this reason, some measurements on the clock lane that pertain to low power mode are not applicable. Unless otherwise stated, all high speed measurements were performed with the ADV7480 operating with a nominal 1 Gbps output data rate.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
UNIT INTERVAL[1]	UI	1		12.5	ns
DATA LANE LP Tx DC SPECIFICATIONS[2]					
Thevenin Output					
High Level	V_{OH}	1.1	1.2	1.3	V
Low Level	V_{OL}	−50	0	+50	mV
CLOCK LANE LP Tx DC SPECIFICATIONS[2]					
Thevenin Output					
High Level	V_{OH}	1.1	1.2	1.3	V
Low Level	V_{OL}	−50	0	+50	mV
DATA LANE HS Tx SIGNALING REQUIREMENTS					
High Speed Differential Voltage Swing	$\|V_1\|$	140	200	270	mV p-p
Differential Voltage Mismatch				10	mV
Single-Ended Output High Voltages				360	mV
Static Common-Mode Voltage Level		150	200	250	mV
CLOCK LANE HS Tx SIGNALING REQUIREMENTS					
High Speed Differential Voltage Swing	$\|V_2\|$	140	200	270	mV p-p
Differential Voltage Mismatch				10	mV
Single-Ended Output High Voltages				360	mV
Static Common-Mode Voltage Level		150	200	250	mV
HS Tx CLOCK TO DATA LANE TIMING REQUIREMENTS					
Data to Clock Skew		0.35 × UI		0.65 × UI	ns

[1] Guaranteed by design.
[2] These measurements were performed with C_{LOAD} = 50 pF.

TIMING SPECIFICATIONS

AVDD = 1.71 V to 1.89 V, DVDD = 1.71 V to 1.89 V, PVDD = 1.71 V to 1.89 V, MVDD = 1.71 V to 1.89 V, CVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, and TVDD = 3.14 V to 3.46 V, specified at operating temperature range, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK AND CRYSTAL						
Nominal Frequency[1]				28.63636		MHz
Frequency Stability[1]					±50	ppm
Input LLC Clock Frequency Range[2,3]		DVDDIO = 3.14 V to 3.46 V	13.5		148.5	MHz
Output LLC Clock Frequency Range[2,3]		DVDDIO = 3.14 V to 3.46 V	13.5		148.5	MHz
SPI_SCLK Frequency[3]					10	MHz
I2S_SCLK Frequency[3]					12.288	MHz
I2S_MCLK Frequency[3]					24.576	MHz
I²C PORT						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width High	t_1		0.6			µs
SCLK Minimum Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDATA Setup Time	t_5		100			ns
SCLK and SDATA Rise Times	t_6				300	ns
SCLK and SDATA Fall Times	t_7				300	ns
Setup Time (Stop Condition)	t_8			0.6		µs
SPI PORT						
Slave Mode						
$\overline{\text{SPI_CS}}$ Falling Edge to SPI_SCLK Active Edge	t_9	SPI_SCLK active edge (rising or falling edge) depends on the values of CPHA and CPOL	35			ns
SPI_SCLK Active Edge to $\overline{\text{SPI_CS}}$ Rising Edge	t_{10}	SPI_SCLK active edge (rising or falling edge) depends on the values of CPHA and CPOL	35			ns
$\overline{\text{SPI_CS}}$ Pulse Width	t_{11}		50			ns
SPI_SCLK High Time[3]	t_{12}		45		55	% duty cycle
SPI_SCLK Low Time[3]	t_{12}		45		55	% duty cycle
SPI_MOSI Setup Time	t_{13}	SPI Mode 0, SPI Mode 3	0			ns
SPI_MOSI Hold Time	t_{14}	SPI Mode 0, SPI Mode 3	35			ns
SPI_SCLK Falling Edge to SPI_MISO Start of Data Invalid[3]	t_{15}	SPI Mode 0, SPI Mode 3			50	ns
SPI_SCLK Falling Edge to SPI_MISO End of Data Invalid[3]	t_{16}	SPI Mode 0, SPI Mode 3			50	ns
SPI_MOSI Setup Time	t_{17}	SPI Mode 1, SPI Mode 2	0			ns
SPI_MOSI Hold Time	t_{18}	SPI Mode 1, SPI Mode 2	35			ns
SPI_SCLK Rising Edge to SPI_MISO Start of Data Invalid	t_{19}	SPI Mode 1, SPI Mode 2			35	ns
SPI_SCLK Rising Edge to SPI_MISO End of Data Invalid	t_{20}	SPI Mode 1, SPI Mode 2			35	ns
$\overline{\text{RESET}}$ FEATURE						
$\overline{\text{RESET}}$ Pulse Width[1]			5			ms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
8-BIT DIGITAL INPUT PORT[2]		DVDDIO = 3.14 V to 3.46 V				
LLC High Time[3]	t_{21}		45		55	% duty cycle
LLC Low Time[3]			45		55	% duty cycle
SDR and DDR Modes Setup Time	t_{22}	Data latched on rising edge	1			ns
SDR and DDR Modes Hold Time	t_{23}	Data latched on rising edge	1			ns
DDR Mode Setup Time	t_{24}	Data latched on falling edge	1			ns
DDR Mode Hold Time	t_{25}	Data latched on falling edge	1			ns
8-BIT DIGITAL OUTPUT PORT[2]		DVDDIO = 3.14 V to 3.46 V				
LLC High Time	t_{26}		40		60	% duty cycle
LLC Low Time			40		60	% duty cycle
SDR Modes Setup Time[4, 5]	t_{36}	At P0 to P7 output pin, data latched on rising edge	1.98			ns
SDR Modes Hold Time[4, 5]	t_{37}	At P0 to P7 output pin, data latched on rising edge	2.50			ns
DDR Modes Setup Time[4, 5]	t_{27}	At P0 to P7 output pin, data latched on rising edge	1.66			ns
DDR Modes Hold Time[4, 5]	t_{28}	At P0 to P7 output pin, data latched on rising edge	3.52			ns
DDR Mode Setup Time[4, 5]	t_{29}	At P0 to P7 output pin, data latched on falling edge	1.71			ns
DDR Modes Hold Time[4, 5]	t_{30}	At P0 to P7 output pin, data latched on falling edge	3.17			ns
I²S PORT, MASTER MODE						
I2S_SCLK High Time	t_{31}		45		55	% duty cycle
I2S_SCLK Low Time			45		55	% duty cycle
I2S_LRCLK Data Transition Time	t_{32}	End of valid data to I2S_SCLK falling edge			10	ns
	t_{33}	I2S_SCLK falling edge to start of valid data			10	ns
I2S_SDATA Data Transition Time	t_{34}	End of valid data to I2S_SCLK falling edge			5	ns
	t_{35}	I2S_SCLK falling edge to start of valid data			5	ns

[1] Required by design.
[2] The 8-bit digital input/output port is only available when the DVDDIO supply is between 3.14 V and 3.46 V.
[3] Guaranteed by design.
[4] These specifications only apply when the LLC_DLL_PHASE[4:0] (IO Map, Register 0x0C[4:0]) is set to 00000
[5] Guaranteed by lab characterization.

Timing Diagrams

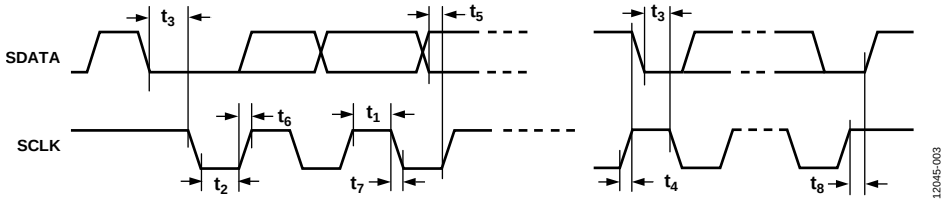

Figure 3. I²C Timing

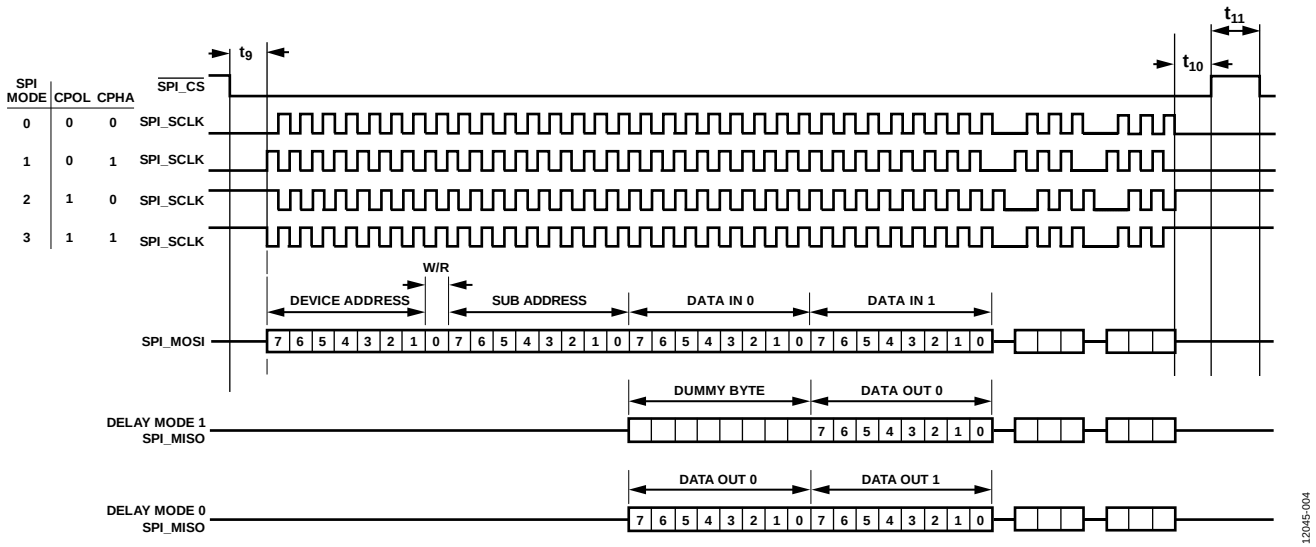

Figure 4. Detailed SPI Slave Timing Diagram

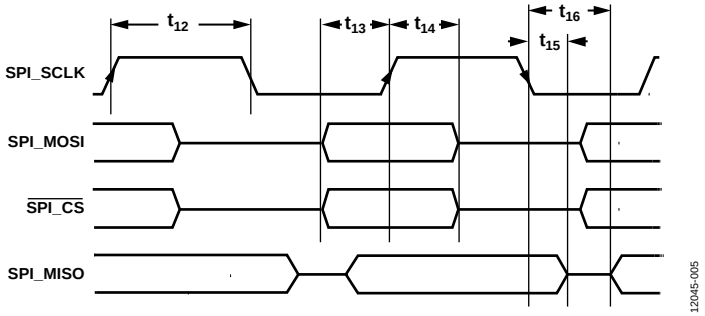

Figure 5. SPI Slave Mode Timing (SPI Mode 0 and SPI Mode 3)

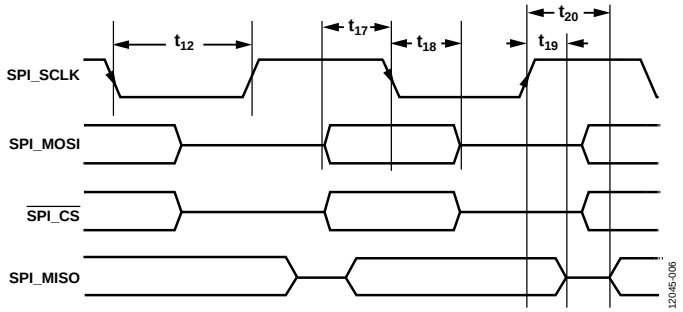

Figure 6. SPI Slave Mode Timing (SPI Mode 1 and SPI Mode 2)

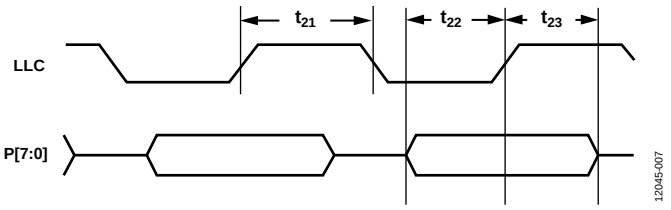

Figure 7. 8-Bit Digital Pixel Video Input, SDR Video Data Timing

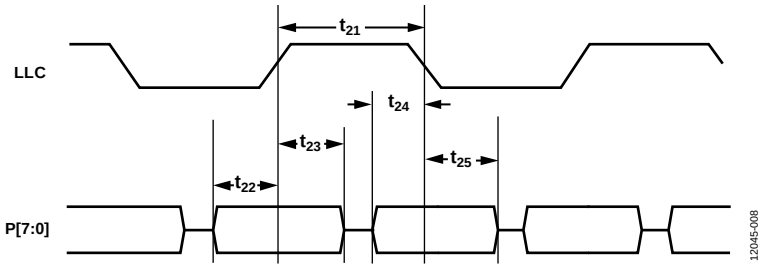

Figure 8. 8-Bit Digital Pixel Video Input, DDR Video Data Timing

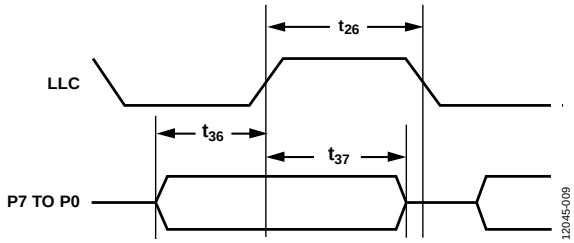

Figure 9. 8-Bit Digital Pixel Video Output, SDR Video Data Timing

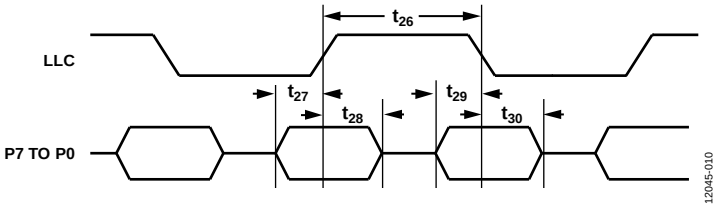

Figure 10. 8-Bit Digital Pixel Video Output, DDR Video Data Timing

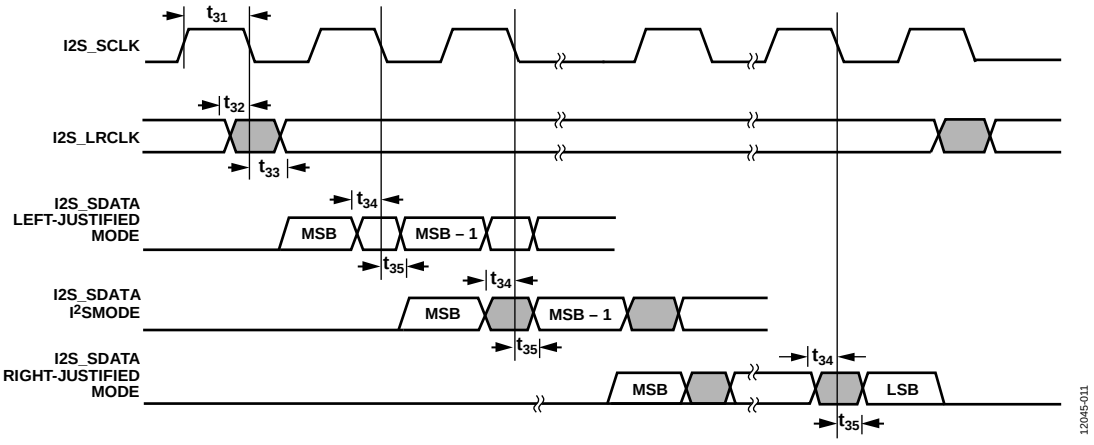

Figure 11. I2S Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
TVDD, DVDDIO to GND	4 V
AVDD, PVDD, MVDD, DVDD, CVDD to GND	2.2 V
CVDD to DVDD	−0.3 V to +0.3 V
MVDD to DVDD	−0.3 V to +0.3 V
PVDD to DVDD	−0.3 V to +0.3 V
AVDD to DVDD	−0.3 V to +0.3 V
Digital Inputs Voltage to GND	GND − 0.3 V to DVDDIO + 0.3 V
Digital Outputs Voltage to GND	GND − 0.3 V to DVDDIO + 0.3 V
Analog Inputs to GND	−0.3 V to AVDD + 0.3 V
XTALN and XTALP to GND	−0.3 V to PVDD + 0.3 V
HDMI/MHL Digital Inputs Voltage to GND	−0.3 V to CVDD + 0.3 V
5 V Tolerant Inputs Voltage to GND[1]	−0.3 V to +5.5 V
Maximum Junction Temperature (T_J max)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] The following inputs are 3.3 V inputs but are 5 V tolerant: DDC_SCL/CD_PULLUP, DDC_SDA, HPD/CBUS, RX_5V/VBUS, CD_SENSE, and CEC.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

To reduce power consumption when using the ADV7480, turn off unused sections of the device.

Due to printed circuit board (PCB) metal variation, and, therefore, variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is achieved using the package surface temperature to estimate the die temperature. This eliminates the variance associated with the θ_{JA} value.

Do not exceed the maximum junction temperature (T_J max) of 125°C. The following equation calculates the junction temperature (T_J) using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:
T_S is the package surface temperature (°C).
Ψ_{JT} = 0.81°C/W for the 100-ball CSP_BGA (based on 2s2p test board defined by JEDEC standards.

$$W_{TOTAL} = (PVDD \times I_{PVDD}) + (TVDD \times I_{TVDD}) - P_{UpStream} + (CVDD \times I_{CVDD}) + (AVDD \times I_{AVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}) + (MVDD \times I_{MVDD})$$

where $P_{UpStream}$ is the quantity of TVDD power consumed on the upstream HDMI or MHL transmitter. $P_{UpStream}$ can be estimated to be around 110 mW for a nominal HDMI transmitter. $P_{UpStream}$ can be estimated to be around 42.82 mW for a nominal MHL transmitter.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

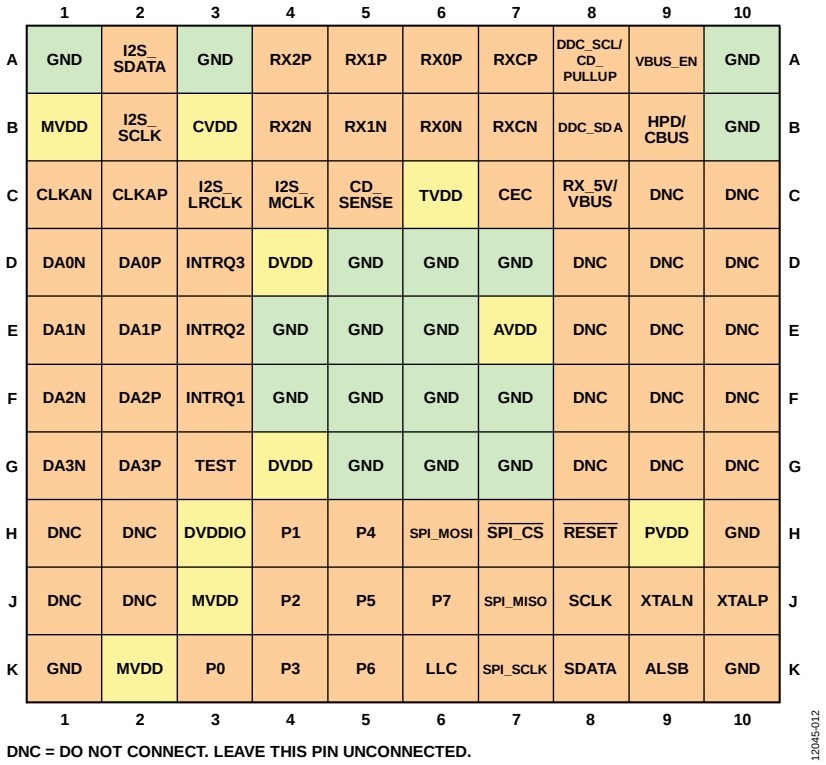

Figure 12. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	GND	Ground	Ground.
A2	I2S_SDATA	Output	I^2S Audio Output.
A3	GND	Ground	Ground.
A4	RX2P	HDMI	HDMI Digital Input Channel 2.
A5	RX1P	HDMI	HDMI Digital Input Channel 1.
A6	RX0P	HDMI/MHL	HDMI Digital Input Channel 0 or MHL TMDS+.
A7	RXCP	HDMI	HDMI Input Clock.
A8	DDC_SCL/CD_PULLUP	HDMI/MHL	HDCP Slave Serial Clock or MHL Cable Detect Pull-Up.
A9	VBUS_EN	MHL	Enable Control Signal for Voltage Regulator Providing a 5 V VBUS Supply.
A10	GND	Ground	Ground.
B1	MVDD	Power	MIPI Supply Voltage (1.8 V).
B2	I2S_SCLK	Output	Audio Serial Clock.
B3	CVDD	Power	HDMI/MHL Comparator Supply Voltage (1.8 V). This is the supply for the HDMI/MHL sensitive analog circuitry. Blocks on this supply include the TMDS PLL and the equalizers.
B4	RX2N	HDMI	HDMI Digital Input Channel 2 Complement.
B5	RX1N	HDMI	HDMI Digital Input Channel 1 Complement.
B6	RX0N	HDMI/MHL	HDMI Digital Input Channel 0 Complement or MHL TMDS–.
B7	RXCN	HDMI	HDMI Input Clock Complement.
B8	DDC_SDA	HDMI	HDCP Slave Serial Data.
B9	HPD/CBUS	HDMI/MHL	HDMI Hot Plug Assert or MHL CBUS.
B10	GND	Ground	Ground.

Pin No.	Mnemonic	Type	Description
C1	CLKAN	Output	MIPI Transmitter A Negative Output Clock.
C2	CLKAP	Output	MIPI Transmitter A Positive Output Clock.
C3	I2S_LRCLK	Output	Audio Left/Right Clock.
C4	I2S_MCLK	Output	Audio Master Clock Output.
C5	CD_SENSE	MHL	MHL Cable Detection Sense Input.
C6	TVDD	Power	HDMI/MHL Terminator Supply Voltage (3.3 V).
C7	CEC	HDMI	CEC Channel.
C8	RX_5V/VBUS	HDMI/MHL	HDMI 5 V Detect or MHL VBUS. A large pull-down resistor (100 kΩ, typical) to ground must be connected to this pin.
C9	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
C10	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
D1	DA0N	Output	MIPI Transmitter A Negative Data Output.
D2	DA0P	Output	MIPI Transmitter A Positive Data Output.
D3	INTRQ3	Output	Interrupt Request Output.
D4	DVDD	Power	Digital Supply Voltage (1.8 V).
D5	GND	Ground	Ground.
D6	GND	Ground	Ground.
D7	GND	Ground	Ground.
D8	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
D9	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
D10	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
E1	DA1N	Output	MIPI Transmitter A Negative Data Output.
E2	DA1P	Output	MIPI Transmitter A Positive Data Output.
E3	INTRQ2	Output	Interrupt Request Output.
E4	GND	Ground	Ground.
E5	GND	Ground	Ground.
E6	GND	Ground	Ground.
E7	AVDD	Power	Analog Supply Voltage (1.8 V).
E8	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
E9	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
E10	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
F1	DA2N	Output	MIPI Transmitter A Negative Data Output.
F2	DA2P	Output	MIPI Transmitter A Positive Data Output.
F3	INTRQ1	Output	Interrupt Request Output.
F4	GND	Ground	Ground.
F5	GND	Ground	Ground.
F6	GND	Ground	Ground.
F7	GND	Ground	Ground.
F8	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
F9	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
F10	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
G1	DA3N	Output	MIPI Transmitter A Negative Data Output.
G2	DA3P	Output	MIPI Transmitter A Positive Data Output.
G3	TEST	Miscellaneous	Do Not Connect. Leave this pin unconnected.
G4	DVDD	Power	Digital Supply Voltage (1.8 V).
G5	GND	Ground	Ground.
G6	GND	Ground	Ground.
G7	GND	Ground	Ground.
G8	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
G9	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
G10	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.

Pin No.	Mnemonic	Type	Description
H1	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
H2	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
H3	DVDDIO	Power	Digital Input/Output Supply Voltage (3.3 V).
H4	P1	Input/Output	Video Pixel Input/Output Port.
H5	P4	Input/Output	Video Pixel Input/Output Port.
H6	SPI_MOSI	Input	SPI Slave Data Input.
H7	$\overline{\text{SPI_CS}}$	Input	SPI Slave Chip Select Input.
H8	$\overline{\text{RESET}}$	Input	System Reset Input, Active Low. A minimum low reset pulse of 5 ms is required to reset the chip.
H9	PVDD	Power	PLL Supply Voltage (1.8 V).
H10	GND	Ground	Ground.
J1	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
J2	DNC	Miscellaneous	Do Not Connect. Leave this pin unconnected.
J3	MVDD	Power	MIPI Supply Voltage (1.8 V).
J4	P2	Input/Output	Video Pixel Input/Output Port.
J5	P5	Input/Output	Video Pixel Input/Output Port.
J6	P7	Input/Output	Video Pixel Input/Output Port.
J7	SPI_MISO	Output	SPI Slave Data Output.
J8	SCLK	Input	I^2C Port Serial Clock Input.
J9	XTALN	Output	Crystal Output. This pin must be connected to the 28.63636 MHz crystal or not connected if an external 1.8 V, 28.63636 MHz clock oscillator is used. In crystal mode, the crystal must be a fundamental crystal.
J10	XTALP	Input	Crystal Input or External Clock Input. This pin must be connected to the 28.63636 MHz crystal or connected to an external 1.8 V, 28.63636 MHz clock oscillator if a clock oscillator is used. In crystal mode, the crystal must be a fundamental crystal.
K1	GND	Ground	Ground.
K2	MVDD	Power	MIPI Supply Voltage (1.8 V).
K3	P0	Input/Output	Video Pixel Input/Output Port.
K4	P3	Input/Output	Video Pixel Input/Output Port.
K5	P6	Input/Output	Video Pixel Input/Output Port.
K6	LLC	Input/Output	Line Locked Clock. Input/output clock for the pixel data.
K7	SPI_SCLK	Input	SPI Slave Clock Input.
K8	SDATA	Input/Output	I^2C Port Serial Data Input/Output.
K9	ALSB	Input	Main I^2C Address Selection Pin. This pin selects the main I^2C address (IO Map I^2C address) for the device. When ALSB is set to Logic 0, the IO Map I^2C write address is 0xE0; when ALSB is set to Logic 1, the IO Map I^2C write address is 0xE2.
K10	GND	Ground	Ground.

POWER SUPPLY RECOMMENDATION

POWER-UP SEQUENCE

Adhere to the absolute maximum ratings at all times during power-up (see Table 4). The power-up sequence for the ADV7480 is as follows:

1. Assert $\overline{\text{RESET}}$ (pull the pin low).
2. Power up the 3.3 V supplies (D_{VDDIO} and T_{VDD}). These supplies must be powered up simultaneously.
3. Power up the 1.8 V supplies (D_{VDD}, C_{VDD}, P_{VDD}, M_{VDD}, and A_{VDD}). These supplies must be powered up simultaneously.
4. $\overline{\text{RESET}}$ can be deasserted (pulled high) 5 ms after all supplies are fully powered up.
5. After all power supplies and the $\overline{\text{RESET}}$ pin are powered up and stable, wait an additional 5 ms before initiating I^2C communication with the ADV7480.

POWER-DOWN SEQUENCE

The ADV7480 power supplies can be deasserted simultaneously as long as a higher rated supply (for example, D_{VDDIO}) does not fall to a voltage level less than a lower rated supply (for example, D_{VDD}), and the absolute maximum ratings specifications are followed.

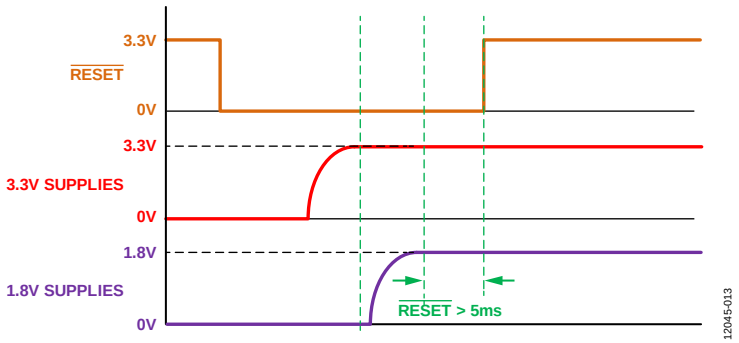

Figure 13. Supply Power-Up Sequence

THEORY OF OPERATION

COMBINED HDMI/MHL RECEIVER

The ADV7480 features a combined HDMI/MHL receiver. This single receiver port is capable of accepting both HDMI and MHL electrical signals. Automatic detection between HDMI and MHL is achieved by using cable impedance detection through the CD_SENSE pin.

Both MHL and HDMI interfaces of the ADV7480 allow authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission, as specified by the HDCP 1.4 protocol.

Dual extended display identification data (EDID) support is provided via an on-chip 512-byte EDID RAM. The EDID RAM must be programmed at power-up. It can be configured as two 256-byte EDIDs for dual mode operation (one 256-byte EDID for the HDMI receiver, and one 256-byte EDID for the MHL receiver), or as a single 512-byte EDID for single mode operation.

The ADV7480 has a synchronization regeneration block used to regenerate the data enable (DE) signal based on the measurement of the video format being displayed and to filter the horizontal and vertical synchronization signals to prevent glitches.

The combined HDMI/MHL receiver also supports TMDS error reduction coding, 4-bit (TERC4) error detection, used for the detection of corrupted HDMI or MHL packets.

MHL RECEIVER

The MHL receiver supports video formats ranging from 480i to 720p/1080i, and display resolutions from VGA (640 × 480 at 60 Hz) to XGA (1024 × 768 at 60 Hz).

The MHL receiver allows programmable equalization of the MHL data signals. This equalization compensates for the high frequency losses inherent in MHL cabling, especially at longer lengths and higher frequencies. The receiver is capable of equalizing for cable lengths of up to 2 meters to achieve robust receiver performance.

The MHL receiver includes the following pins:

- RX0N and RX0P. In MHL mode, this differential pair receives the data transmitted as a differential signal, and the clock transmitted on the common mode.
- HPD/CBUS. In MHL mode, this pin is used for CBUS communication.
- VBUS_EN. This pin provides an enable signal for an external source providing 5 V of power to the MHL source on VBUS.
- RX_5V/VBUS. In MHL mode, this pin is an input monitoring the VBUS signal provided by an external source enabled by VBUS_EN.
- CD_SENSE. This pin detects whether the signals provided to the HDMI/MHL receiver are HDMI signals or MHL signals. A high level indicates MHL, and a low level indicates HDMI.

The implementation of the MSC commands by the system processor can be handled either through the I^2C bus, or via a dedicated SPI bus. A dedicated interrupt pin (INTRQ3) is available to indicate that events related to the CBUS have occurred.

The main MHL receiver features include

- Support for a pixel clock up to 75 MHz in 24-bit mode, allowing support for video formats up to 720p/1080i and display resolutions up to XGA in either RGB, YCbCr 4:4:4, or YCbCr 4:2:2 formats.
- Integrated fully adaptive equalizer for cable lengths up to 2 meters.
- HDCP 1.4 support.
- Internal HDCP keys.
- HDCP repeater support, up to 25 key selection vectors (KSVs) supported.
- Pulse code modulation (PCM) audio packet support.
- Support for 8-channel TDM output data up to 48 kHz.
- Repeater support.
- Internal EDID RAM (512-byte for single mode, and 256-byte for dual mode operation).
- Scratchpad register support with a size of 64 bytes.

HDMI RECEIVER

The HDMI receiver supports video formats ranging from 480i to 1080p, and display resolutions from VGA (640 × 480 at 60 Hz) to UXGA (1600 × 1200 at 60 Hz).

The HDMI receiver allows programmable equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. The receiver is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance.

The main HDMI receiver features include

- 162.0 MHz (UXGA at 24 BPP) maximum TMDS clock frequency.
- Integrated fully adaptive equalizer for cable lengths up to 30 meters.
- HDCP 1.4 support.
- Internal HDCP keys.
- HDCP repeater support, up to 25 key selection vectors (KSVs) supported.
- PCM audio packet support.
- Support for 8-channel TDM output data up to 48 kHz.
- Repeater support.
- Internal EDID RAM (512-byte for single mode, and 256-byte for dual mode operation).
- Hot Plug assert output pin (HPD/CBUS).
- CEC controller.

COMPONENT PROCESSOR

The ADV7480 has one any-to-any 3 × 3 CSC matrix. The CSC block is located in the processing path before the CP section. CSC enables YCbCr-to-RGB and RGB-to-YCbCr conversions. Many other standards of color space can be implemented using the color space converter.

CP features include

- Support for all video modes supported by the HDMI/MHL receiver. These include 525i, 625i, 525p, 625p, 1080i, 1080p, and display resolutions from VGA (640 × 480 at 60 Hz) to UXGA (1600 × 1200 at 60 Hz).
- Manual adjustments including gain (contrast), offset (brightness), hue, and saturation.
- Free run output mode that provides stable timing when no video input is present.
- Timing adjustments controls for HS/VS/DE timing.

8-BIT DIGITAL INPUT/OUTPUT PORT

The ADV7480 features an 8-bit digital bidirectional port. The following formats are supported both as input and output ports:

- 8-bit interleaved 4:2:2 SDR input/output with embedded timing codes
- 8-bit interleaved 4:2:2 DDR input/output with embedded timing codes

The maximum input and output video resolution supported is 720p/1080i in both SDR and DDR modes.

Video received on the 8-bit digital input port can be routed to the four-lane MIPI CSI-2 transmitter. Video sent on the 8-bit digital output port can be routed from the CP core.

AUDIO PROCESSING

The ADV7480 features an audio processor that handles the audio extracted from the MHL or HDMI stream by the HDMI/MHL receiver. It contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. On detection of these conditions, a 2-channel linear PCM audio signal can be ramped down to a mute state to prevent audio clicks or pops.

The audio is output on a single flexible serial digital audio output port supporting I2S-compatible, left justified and right justified audio output modes in master mode only. TDM is also supported, allowing up to eight audio channels with a sample rate up to 48 kHz to be transmitted over the single serial digital audio interface.

MIPI CSI-2 TRANSMITTER

The ADV7480 features one MIPI CSI-2 transmitter (Transmitter A).

The four-lane transmitter consists of four differential data lanes (DA0N, DA0P, DA1N, DA1P, DA2N, DA2P, DA3N and DA3P), and a differential clock lane (CLKAN and CLKAP). It supports four data lanes, two data lanes and one data lane muxing options, and can be used to transmit video received on either the HDMI/MHL receiver (processed through the CP) or the 8-bit digital input port.

The main features of the 4-lane MIPI transmitter (Transmitter A) include

- Support for 8-bit and 10-bit YCbCr 4:2:2 video modes.
- Support for 24-bit RGB 4:4:4 (RGB888), 18-bit RGB 4:4:4 (RGB666), and 16-bit RGB 4:4:4 (RGB565) video modes.
- Support for video formats ranging from 480i to 1080p, and display resolutions from VGA to UXGA (certain restrictions apply to the muxing option, video mode, and video format that can be selected).
- Data lanes and clock lane remapping to ease PCB layout.

INTERRUPTS

The ADV7480 features three interrupt request pins. INTRQ1 and INTRQ2 can be programmed to trigger interrupts based on various selectable events related to the HDMI/MHL receiver (video and audio related) and the CP. INTRQ3 is dedicated to events related to the MHL CBUS.

OUTLINE DIMENSIONS

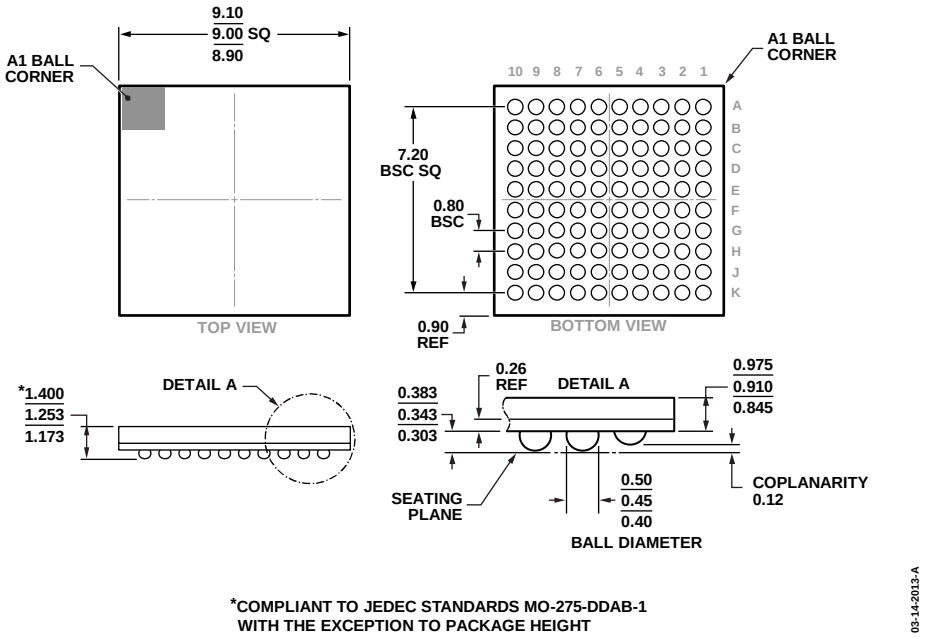

Figure 14. 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-100-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
ADV7480WBBCZ	−40°C to +85°C	100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-100-4
ADV7480WBBCZ-RL	−40°C to +85°C	100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-100-4

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] This device is programmed with internal HDCP keys. Customer must have HDCP adopter status (consult Digital Protection, LLC, for licensing requirements) to purchase any components with internal HDCP keys.

AUTOMOTIVE PRODUCTS

The ADV7480W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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