78Q2123/78Q2133 MicroPHY™ 10/100BASE-TX Transceiver

Simplifying System Integration™

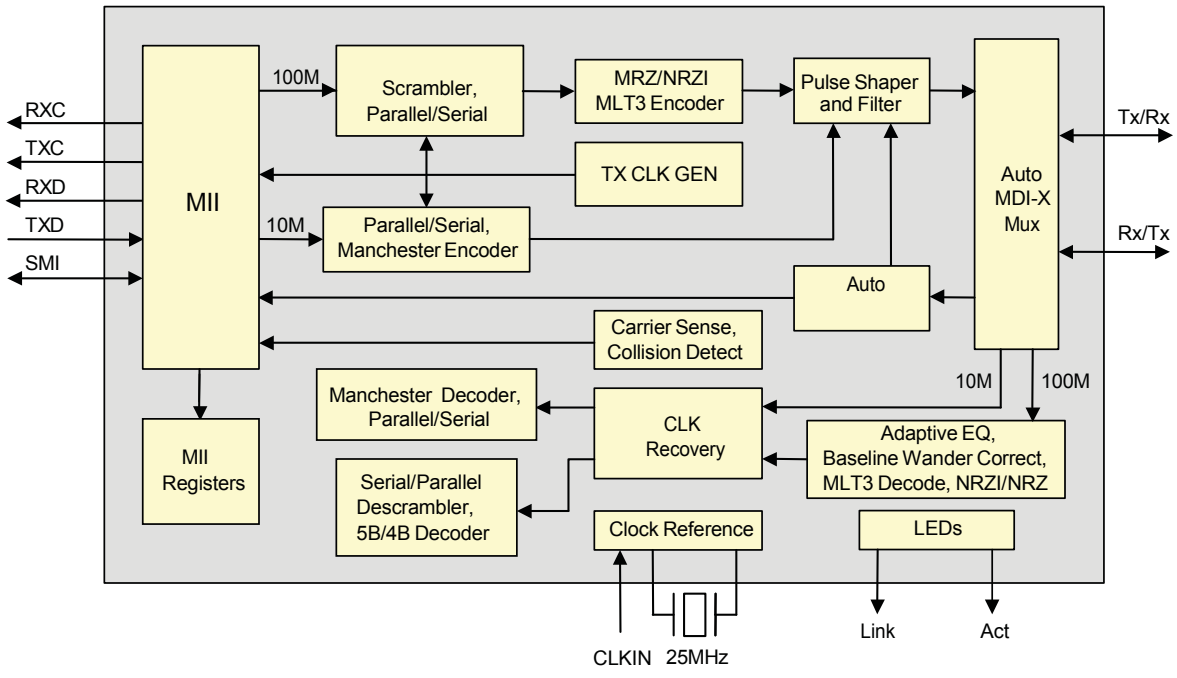
DATA SHEET

DESCRIPTION

The 78Q2123 and 78Q2133, MicroPHY™, are the smallest 10BASE-T/100BASE-TX Fast Ethernet transceivers in the market. They include integrated MII, ENDECs, scrambler/descrambler, dual-speed clock recovery, and full-featured auto-negotiation functions. The transmitter includes an on-chip pulse-shaper and a low-power line driver. The receiver has an adaptive equalizer and a baseline restoration circuit required for accurate clock and data recovery. The transceiver interfaces to Category-5 unshielded twisted pair (Cat-5 UTP) cabling for 100BASE-TX applications, and Category-3 unshielded twisted pair (Cat-3 UTP) for 10BASE-T applications. The MDI is connected to the line media via dual 1:1 isolation transformers. No external filter is required. Interface to the MAC is accomplished through an IEEE-802.3 compliant Media Independent Interface (MII). The 78Q2123/78Q2133 are intended to serve the embedded Ethernet market, tailored specifically to the needs of game consoles, broadband modems, printers, set top boxes and audio/visual equipment. It is designed for low-power consumption and operates from a single 3.3V supply. The 78Q2123 is rated for commercial temperature range and the 78Q2133 is rated for industrial temperature range.

FEATURES

- Smallest 10/100 PHY available
- 10BASE-T/100BASE-TX IEEE-802.3 compliant TX and RX functions requiring a dual 1:1 isolation transformer interface to the line
- Integrated MII, 10BASE-T/100BASE-TX ENDEC, 100BASE-TX scrambler/descrambler, and full-featured auto-negotiation function
- Full duplex operation capable
- Automatic MDI/MDI-X cross over correction
- Register-programmable transmit amplitude
- Automatic polarity correction during auto-negotiation and 10BASE-T signal reception
- Power-saving and power-down modes including transmitter disable
- 2 Programmable LED indicators (Link and Activity by default)
- User programmable Interrupt pin
- Packages: 32-QFN (5x5 mm) and 32-TQFN (5x5mm)
- Low Power (~290mW)
- Single 3.3 V ± 0.3V Supply
- 78Q2123 rated for 0°C to 70°C operation
- 78Q2133 rated for -40°C to 85°C operation



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1 Functional Description

1.1 General

1.1.1 Power Management

The 78Q2123 and 78Q2133 have three power saving modes:

- Chip Power-Down
- Receive Power Management
- Transmit High Impedance Mode

Chip power-down is activated by setting the PWRDN bit in MII register MR0.11. When the chip is in power-down mode, all on-chip circuitry is shut off, and the device consumes minimum power. While in the power-down state, the 78Q2123/78Q2133 still respond to management transactions.

Receive power management (RXCC mode) is activated by setting the RXCC bit in MII register MR16.0. In this mode of operation, the adaptive equalizer, the clock recovery phase lock loop (PLL), and all other receive circuitry will be powered down when no valid MLT-3 signal is present at the UTP receive line interface. As soon as a valid signal is detected, all circuits will automatically be powered up to resume normal operation. During this mode of operation, RX_CLK will be inactive when there is no data being received. Note that the RXCC mode is not supported during 10BASE-T operation.

Transmit high impedance mode is activated by setting the TXHIM bit in MII register MR16.12. In this mode of operation, the transmit UTP drivers are in a high impedance state and TX_CLK is tri-stated. A weak internal pull-up is enabled on TX_CLK. The receive circuitry remains fully operational. The default state of MR16.12 is a logic low for disabling the transmit high impedance mode. Only a reset condition will automatically clear MR16.12. The transmitter is fully functional when MR16.12 is cleared. This feature is useful when configuring a system for Wake-On LAN (when the 78Q2123/78Q2133 are coupled with a Wake-On LAN capable MAC).

1.1.2 Analog Biasing and Supply Regulation

The 78Q2123/78Q2133 require no external component to generate on-chip bias voltages and currents. High accuracy is maintained through a closed-loop trimmed biasing network.

On-chip digital logic runs off an internal voltage regulator. Hence only a single 3.3V ($\pm$ 0.3V) supply is required to power-up the device. The on-chip regulator is not affected by the power-down mode.

1.1.3 Clock Selection

The 78Q2123/78Q2133 have an on-chip crystal oscillator which can also be driven by an external oscillator. In this mode of operation, a 25 MHz crystal should be connected between the XTLP and XTLN pins. Alternatively, an external 25 MHz clock input can be connected to the XTLP pin. In this mode of operation, a crystal is not required and the XTLN pin must be tied to ground.

1.1.4 Transmit Clock Generation

The transmitter uses an on-chip frequency synthesizer to generate the transmit clock. In 100BASE-TX operation, the synthesizer multiplies the reference clock by 5 to obtain the internal 125 MHz serial transmit clock. In 10BASE-T mode, it generates an internal 20MHz transmit clock by multiplying the reference 25 MHz clock by 4/5. The synthesizer references either the local 25 MHz crystal oscillator, or the externally applied clock, depending on the selected mode of operation.

1.1.5 Receive Signal Qualification

The integrated signal qualifier has separate squelch and unsquelch thresholds. It also includes a built-in timer to ensure fast and accurate signal detection and line noise rejection. Upon detection of two or more valid 10BASE-T or 100BASE-TX pulses on the line receive port, signal detect is indicated. The signal detect threshold is then lowered by about 40%. All adaptive circuits are released from their initial states and allowed to lock onto the incoming data. In 100BASE-TX operation, signal detect is de-asserted when no signal is presented for a period of about 1.2 µs. In 10BASE-T operation, signal detect is de-asserted whenever no Manchester data is received. In either case, the signal detect threshold will return to the squelched level whenever the signal detect indication is de-asserted. Signal detect is also used to control the operation of the clock/data recovery circuit to assure fast acquisition.

1.1.6 Receive Clock Recovery

In 100BASE-TX mode, the 125 MHz receive clock is extracted using a digital DLL-based loop. When no receive signal is present, the CDR is directed to lock onto the 125 MHz transmit serial clock. When signal detect is asserted, the CDR will use the received MLT-3 signal as the clock reference. The recovered clock is used to re-time the data signal and for conversion of the data to NRZ format.

In 10BASE-T mode, the 20 MHz receive clock is recovered digitally from the Manchester data using a DLL locked to the reference clock. When Manchester-coded preambles are detected, the CDR immediately re-aligns the phase of the clock to synchronize with the incoming data. Hence clock acquisition is fast and immediate.

1.2 100BASE-TX OPERATION

1.2.1 100BASE-TX Transmit

The 78Q2123/78Q2133 contain all of the necessary circuitry to convert the transmit MII signaling from a MAC to an IEEE-802.3 compliant data-stream driving Cat-5 UTP cabling. The internal PCS interface maps 4 bit nibbles from the MII to 5 bit code groups as defined in Table 24-1 of IEEE-802.3. These 5 bit code groups are then scrambled and converted to a serial stream before being sent to the MLT-3 pulse shaping circuitry and line driver. The pulse-shaper uses current modulation to produce the desired output waveform. Controlled rise/fall time in the MLT-3 signal is achieved using an accurately controlled voltage ramp generator. The line driver requires an external 1:1 isolation transformer to interface with the line media. The center-tap of the primary side of the transformer must be connected to the Vcc supply (3.3V $\pm$ 0.3V).

1.2.2 100BASE-TX Receive

The 78Q2123/78Q2133 receive a 125MBaud MLT-3 signal through a 1:1 transformer. The signal then goes through a combination of adaptive offset adjustment (baseline wander correction) and adaptive equalization. The effect of these circuits is to sense the amount of dispersion and attenuation caused by the cable and transformer, and restore the received pulses to logic levels. The amount of gain and equalization applied to the pulses varies with the detected attenuation and dispersion and, therefore, with the length of the cable. The 78Q2123/78Q2133 can compensate for cable loss of up to 10dB at 16 MHz. This loss is represented as test_chan_5 in Annex A of the ANSI X3.263:199X. The equalized MLT-3 data signal is bi-directionally sliced and the resulting NRZI bit-stream is presented to the CDR where it is re-timed and decoded to NRZ format. The re-timed serial data passes through a serial-to-parallel converter, then descrambled and aligned into 5 bit code groups. The receive PCS interface maps these code groups to 4 bit data for the MII as outlined in Table 24-1 in Clause 24 of IEEE-802.3.

1.2.3 PCS Bypass Mode (Auto-negotiate must be off)

The PCS Bypass mode is entered by setting register bit MR 16.1. In this mode the 78Q2123/78Q2133 accept scrambled 5 bit code words at the TX_ER and TXD[3:0] pins, TX_ER being the MSB of the data input. The 5 bit code groups are converted to MLT-3 signal for transmission.

The received MLT-3 signal is converted to 5 bit NRZ code groups and output from the RX_ER and RXD[3:0] pins, RX_ER being the MSB of the data output. The RX_DV and TX_EN pins are unused in PCS Bypass mode.

1.3 10BASE-T OPERATION

1.3.1 10BASE-T Transmit

The 78Q2123/78Q2133 take 4-bit parallel NRZ data via the MII interface and passes it through a parallel to serial converter. The data is then passed through a Manchester encoder, pre-emphasis pulse-shaper, media filter, and finally to the twisted-pair line driver. The pulse-shaper and filter ensure the output waveforms meet the voltage template and spectral content requirements detailed in Clause 14 of IEEE-802.3. Interface to the twisted-pair media is through a center-tapped 1:1 transformer. No external filtering is required. During auto-negotiation and 10BASE-T idle periods, link pulses are transmitted. The 78Q2123/78Q2133 employ an onboard timer to prevent the MAC from capturing a network through excessively long transmissions. When this timer expires, the chip enters the jabber state and transmission is halted. The jabber state is exited after the MII goes idle for 500±250 ms.

1.3.2 10BASE-T Receive

The 78Q2123/78Q2133 receive Manchester-encoded 10BASE-T data through the twisted pair inputs and re-establishes logic levels through a slicer with a smart squelch function. The slicer automatically adjusts its level after detection of valid data with the appropriate levels. Data is passed on to the CDR where the clock is recovered, and the data is re-timed and decoded. From there, data enters the serial-to-parallel converter for transmission to the MAC via the Media Independent Interface. Interface to the twisted-pair media is through an external 1:1 transformer. Polarity information is detected and corrected within internal circuitry.

1.3.3 Polarity Correction

The 78Q2123/78Q2133 are capable of either automatic or manual polarity reversal for 10BASE-T and auto-negotiation functions. Register bits MR16.5 and MR16.4 control this feature. The default is automatic mode where MR16.5 is low and MR16.4 indicates if the detection circuitry has inverted the input signal. To enter manual mode, MR16.5 should be set high and MR16.4 will then control the signal polarity.

1.3.4 SQE TEST

The 78Q2123/78Q2133 support the Signal Quality Error (SQE) function detailed in IEEE-802.3. At an interval of 1μs after each negative transition of the TX_EN pin in 10BASE-T mode, the COL pin will go high for a period of 1 μs. SQE is not signaled during transmission after collision is detected. SQE is automatically disabled when repeater mode is enabled. This function can be disabled through register bit MR16.11.

1.3.5 Natural Loopback

When enabled, whenever the 78Q2123/78Q2133 are transmitting and not receiving on the twisted pair media (10BASE-T Half Duplex mode), data on the TXD3-0 pins are looped back onto the RXD3-0 pins. During a collision, data from the RXI pins is routed to the RXD3-0 pins. The natural loopback function is enabled through register bit MR16.10. This feature is off by default.

1.3.6 Repeater Mode

When register bit MR16.15 is set, the 78Q2123/78Q2133 are placed in repeater mode. In this mode, full duplex operation is prohibited, CRS responds only to receive activity and, in 10BASE-T mode, the SQE test function is disabled.

1.4 Auto-Negotiation

The 78Q2123/78Q2133 support the auto-negotiation functions of Clause 28 of IEEE-802.3 for 10/100 Mbps operation over copper wiring. This function can be enabled via register settings. The auto-negotiation function defaults to ON and bit MR0.12 (ANEGEN) is high after reset. Software can disable the auto-negotiation function by writing to bit MR0.12.

The contents of register MR4 are sent to the 78Q2123/78Q2133's link partner during auto-negotiation via fast link pulse coding.

The default values of the auto-negotiation registers are set as follows:

Register.Bits	Function	Default Value
0.13	Speed Select	1 (100 BASE TX)
0.12	AN Enable	1 (enabled)
0.8	Duplex	1 (full duplex)
4.8/1.14	100BASE-TX Full Duplex	1
4.7/1.13	100 BASE-TX	1
4.6/1.12	10 BASE-T Full Duplex	1
4.5/1.11	10 BASE-T	1

These default values can be changed by writing different values to the registers, then restarting auto-negotiation.

With auto-negotiation enabled, the 78Q2123/78Q2133 will start sending fast link pulses at power on, loss of link or upon a command to restart. At the same time, it will look for either 10BASE-T idle, 100BASE-TX idle, or fast link pulses from its link partner. If either idle pattern is detected, the 78Q2123/78Q2133 configure themselves in half-duplex mode at the appropriate speed. If it detects fast link pulses, it decodes and analyzes the link code transmitted by the link partner. When three identical link code words are received (ignoring the acknowledge bit) the link code word is stored in register MR5. Upon receiving three more identical link code words, with the acknowledge bit set, the 78Q2123/78Q2133 configure themselves to the highest priority technology common to the two link partners. The technology priorities are, in descending order:

100BASE-TX, Full Duplex
100BASE-TX, Half Duplex
10BASE-T, Full Duplex
10BASE-T, Half Duplex

Once auto-negotiation is complete, register bits MR18.11:10 will reflect the actual speed and duplex that was chosen.

If auto-negotiation fails to establish a link for any reason, register bit MR18.12 will reflect this and auto negotiation will restart from the beginning. Writing a '1' to bit MR0.9 (RANEG) will also cause auto-negotiation to restart.

1.5 Media Independent Interface

1.5.1 MII Transmit and Receive Operation

The MII interface on the 78Q2123/78Q2133 provide independent transmit and receive paths for both 10Mb/s and 100Mb/s data rates as described in Clause 22 of the IEEE-802.3 standard.

The transmit clock, TX_CLK, provides the timing reference for the transfer of TX_EN, TXD3-0, and TX_ER signals from the MAC to the 78Q2123/78Q2133. TXD3-0 is captured on the rising edge of TX_CLK when TX_EN is asserted. TX_ER is also captured on the rising edge of TX_CLK and is asserted by the MAC to request that an error code group is to be transmitted. The assertion of TX_ER is ignored when the 78Q2123/78Q2133 are operating in 10BASE-T mode.

The receive clock, RX_CLK, provides the timing reference to transfer RX_DV, RXD3-0, and RX_ER signals from the 78Q2123/78Q2133 to the MAC. RX_DV transitions synchronously with respect to RX_CLK and is asserted when the 78Q2123/78Q2133 are presenting valid data on RXD3-0. RX_ER is asserted and is synchronous to RX_CLK when a code group violation has been detected in the current receive packet.

1.5.2 Station Management Interface

The station management interface consists of circuitry which implements the serial protocol as described in Clause 22.2.4.4 of IEEE-802.3. A 16-bit shift register receives serial data applied to the MDIO pin at the rising-edge of the MDC clock signal. Once the preamble is received, the station management control logic looks for the start-of-frame sequence and a read or write op-code, followed by the PHYAD and REGAD fields. The default address for the 78Q2123/78Q2133 is 1. For a read operation, the MDIO port becomes enabled as an output and the register data is loaded into a shift register for transmission. The 78Q2123/78Q2133 can work with a one-bit preamble rather than the 32 bits prescribed by IEEE-802.3. This allows for faster programming of the registers. If a register does not exist at an address indicated by the REGAD field or if the PHYAD field does not match the 78Q2123/78Q2133 PHYAD, a read of the MDIO port will return all ones. For a write operation, the data is shifted in and loaded into the appropriate register after the sixteenth data bit has been received. Writes to registers not supported by the 78Q2123/78Q2133 are ignored.

When the PHYAD field is all zeros, the Station Management Entity (STA) is requesting a broadcast data transaction. All PHYs sharing the same Management Interface must respond to this broadcast request. The 78Q2123/78Q2133 will respond to the broadcast data transaction.

1.6 Additional Features

1.6.1 LED Indicators

There are two LED pins that can be used to indicate various states of operation of the 78Q2123/78Q2133. The function of these pins is programmable via the MR23 register as shown in the table below:

LED State	Indication
0	1 = Link OK (Default LED0)
1	1 = RX or TX Activity (Default LED1)
2	1 = TX Activity
3	1 = RX Activity
4	1 = Collision
5	1 = 100 BASE-TX mode
6	1 = 10 BASE-T mode
7	1 = Full Duplex
8	1= Link OK & Blink = RX or TX Activity

The default status of these LEDs are “Link OK” for LED0 and “RX or TX Activity” for LED1.

1.6.2 Interrupt Pin

The 78Q2123 and 78Q2133 have an Interrupt pin (INTR) that is asserted whenever any of the eight interrupt bits of MR17.7:0 are set. These interrupt bits can be disabled via the MR17.15:8 Interrupt Enable bits. The Interrupt Polarity bit, MR16.14, controls the active level of the INTR pin. When the INTR pin is not asserted, the pin is held in a high impedance state. An external pull-up or pull-down resistor may be required for use with the INTR pin.

1.6.3 Automatic MDI/ MDI-X Configuration

The 78Q2123 and 78Q2133 implement the automatic MDI/MDI-X configuration detailed in IEEE-802.3 2002. This function eliminates the need for cross over cables when connecting to another device. When auto-switching is enabled, the 78Q2123/78Q2133 will attempt to detect activity on its given configuration. If no activity is seen for 60 ms, the device will switch to the other configuration depending on a random number sequence. The initial seed of the random number generator can be set via MR24.3:0. In addition, the part includes an asynchronous MDIX reset that varies from 1.29 seconds to 1.57 seconds to ensure lock step will not occur between two devices.

The 78Q2123 and 78Q2133 will also allow for auto-switching while the part is not in auto-negotiation mode. The IEEE 802.3 specification will not work in this case if the other device is in auto-negotiation mode. The 78Q2123 and 78Q2133 default to auto MDIX enabled with parallel detection. Register bits MR24.6 and MR24.7 are both defaulted to 1. The 78Q2123 and 78Q2133 will resolve the proper configuration within 5 seconds.

2 Pin Description

2.1 Legend

Type	Description	Type	Description
A	Analog Pin	CI	TTL-level Input
CIU	TTL-level Input with Pull-up	CIO	TTL-compatible Bi-directional Pin
CIS	TTL-level Input with Schmitt Trigger	COZ	Tristate-able CMOS Output
CO	CMOS Output		
S	Supply	G	Ground

2.2 MII (Media Independent Interface)

Signal	Pin	Type	Description
TX_CLK	15	COZ	TRANSMIT CLOCK: TX_CLK is a continuous clock, which provides a timing reference for the TX_EN, TX_ER and TXD[3:0] signals from the MAC. The clock frequency is 25 MHz in 100BASE-TX mode and 2.5 MHz in 10BASE-T mode. This pin is tri-stated in isolate mode and the TXHIM mode.
TX_EN	16	CI	TRANSMIT ENABLE: TX_EN is asserted by the MAC to indicate that valid data for transmission is present on the TXD[3:0] pins.
TXD[3:0]	[20:17]	CI	TRANSMIT DATA: TXD[3:0] receives data from the MAC for transmission on a nibble basis. This data is captured on the rising edge of TX_CLK when TX_EN is high.
TX_ER	14	CI	TRANSMIT ERROR: TX_ER is asserted high by the MAC to request that an error code-group be transmitted when TX_EN is high. In PCS bypass mode, this pin becomes the MSB of the transmit 5-bit code group.
CRS	22	COZ	CARRIER SENSE: When the 78Q2123/78Q2133 are not in repeater mode, CRS is high whenever a non-idle condition exists on either the transmitter or the receiver. In repeater mode, CRS is only active when a non-idle condition exists on the receiver. This pin is tri-stated in isolate mode.
COL	21	COZ	COLLISION: COL is asserted high when a collision has been detected on the media. In 10BASE-T mode COL is also used for the SQE test function. This pin is tri-stated in isolate mode. During half duplex operation, the rising edge of COL will occasionally occur upon the rising edge of TX_CLK.
RX_CLK	12	COZ	RECEIVE CLOCK: RX_CLK is a continuous clock, which provides a timing reference to the MAC for the RX_DV, RX_ER and RXD[3:0] signals. The clock frequency is 25 MHz in 100BASE-TX mode and 2.5 MHz in 10BASE-T mode. To reduce power consumption in 100BASE-TX mode, the 78Q2123/78Q2133 provide an optional mode, enabled through MR16.0, in which RX_CLK is held inactive (low) when no receive data is detected. This pin is tri-stated in isolate mode.
RX_DV	11	COZ	RECEIVE DATA VALID: RX_DV is asserted high to indicate that valid data is present on the RXD[3:0] pins. In 100BASE-TX mode, it transitions high with the first nibble of the preamble and is pulled low when the last data nibble has been received. In 10BASE-T mode it transitions high when the start-of-frame delimiter (SFD) is detected. This pin is tri-stated in isolate mode.

RXD[3:0]	[5:8]	COZ	RECEIVE DATA: Received data is provided to the MAC via RXD[3:0]. These pins are tri-stated in isolate mode.
RX_ER	13	COZ	RECEIVE ERROR: RX_ER is asserted high when an error is detected during frame reception. In PCS bypass mode, this pin becomes the MSB of the receive 5-bit code group. This pin is tri-stated in isolate mode.
MDC	2	CIS	MANAGEMENT DATA CLOCK: MDC is the clock used for transferring data via the MDIO pin.
MDIO	1	CIO	MANAGEMENT DATA INPUT/OUTPUT: MDIO is a bi-directional port used to access management registers within the 78Q2123/78Q2133. This pin requires an external pull-up resistor as specified in IEEE-802.3.

2.3 Control and Status

Signal	Pin	Type	Description
RST	23	CIS	ACTIVE LOW RESET: When pulled low the pin resets the chip. The reset pulse must be long enough to guarantee stabilization of the supply voltage and startup of the oscillator. Refer to the Electrical Specifications for the reset pulse requirements. There are two other ways to reset the chip: 1. Through the internal power-on-reset (activated when the chip is being powered up). 2. Through the MII register bit (MR 0.15).
INTR	32	COZ	INTERRUPT PIN: This pin is used to signal an interrupt to the media access controller. The pin is held in the high impedance state when an interrupt is not indicated. The pin will be forced high or low to signal an interrupt depending upon the value of the INPOL bit (MR16.14). The events which trigger an interrupt can be programmed via the Interrupt Control Register located at address MR17.

2.4 MDI (Media Dependent Interface)

Signal	Pin	Type	Description
TXOP, TXON	30,31	A	TRANSMIT OUTPUT POSITIVE/NEGATIVE: Transmitter differential outputs for both 10base-T and 100base-TX.
RXIP, RXIN	28,27	A	RECEIVE INPUT POSITIVE/NEGATIVE: Receiver differential inputs for both 10BASE-T and 100BASE-TX.

2.5 Oscillator/Clock

Signal	Pin	Type	Description
XTLP	24	A	CRYSTAL INPUT: Should be connected to a 25 MHz crystal. If an externally generated TTL compatibility clock signal is used, that signal is applied here.
XTLN	25	A	CRYSTAL OUTPUT: Should be connected to a 25 MHz crystal. When an external clock source is being used, this pin must be grounded.

2.6 Power Supply and Ground

Signal	Pin	Type	Description
PWR	9, 26	S	+3.3VDC SUPPLY
GND	10, 29	G	GROUND

2.7 LED Signals (Programmability Is Secondary Requirement)

Signal	Pin	Type	Description
LED0	4	CO	PROGRAMMABLE LED. Active low. Default status: LINK OK. Active to indicate link with far end PHY.
LED1	3	CO	PROGRAMMABLE LED. Active low. Default status: RX or TX ACTIVITY. Active to indicate TX or RX activity on the MDI.
			Other LED options selectable via MR23: TRANSMIT: ON when there is a transmission (normally OFF). RECEIVE: ON when there is a reception (normally OFF). COLLISION: In half duplex mode, this is a collision indicator and turns-ON when a collision occurs. In full duplex mode, this LED is held OFF. BASE-TX: ON for 100BASE-TX connection and OFF for other connections. LEDBTX is OFF during auto-negotiation. BASE-T: ON for 10BASE-T connection and OFF for other connections. LEDBT is OFF during auto-negotiation. FULL DUPLEX: ON when in full duplex mode and OFF when in half duplex mode. LINK/ACT: ON for link, blink for activity.

3 Register Description

The 78Q2123/78Q2133 implement 13 16-bit registers, which are accessible via the MDIO and MDC pins. The supported registers are shown below in the following table. Attempts to read unsupported registers will be ignored and the MDIO pin will not be enabled as an output, as per the IEEE 802.3 specification. All of the registers except those that are unique to the 78Q2123/78Q2133 will respond to the broadcast PHYAD value of '00000'. The registers specific to the 78Q2123/78Q2133 occupy address space MR16-24.

Address	Symbol	Name	Default (Hex)
0	MR0	Control	(3100)
1	MR1	Status	(7849)
2	MR2	PHY Identifier 1	000E
3	MR3	PHY Identifier 2	7237
4	MR4	Auto-Negotiation Advertisement	(01E1)
5	MR5	Auto-Negotiation Link Partner Ability	0000
6	MR6	Auto-Negotiation Expansion	0000
7	MR7	Not Implemented	0000
8-14	MR8-14	Reserved	0000
15	MR15	Not Implemented	0000
16	MR16	Vendor Specific	(0140)
17	MR17	Interrupt Control/Status Register	0000
18	MR18	Diagnostic Register	0000
19	MR19	Transceiver Control	4XXX
20-22	MR20-22	Reserved	0000
23	MR23	LED Configuration Register	0010
24	MR24	MDI/MDIX Control Register	(00C0)

Legend

Type	Description	Type	Description
R	Readable by management.	W	Writeable by management.
WC	Writeable by management. Self Clearing.	RC	Readable by management. Cleared upon a read operation.
0/1	Default value upon power up or reset.		

3.1 MR0: Control Register

Bit	Symbol	Type	Default	Description
0.15	RESET	R/WC	0	Reset: Setting this bit to '1' resets the device and sets all registers to their default states. This bit is self-clearing.
0.14	LOOPBK	R/W	0	Loopback: When this bit is set to '1', input data at TXD[3:0] is output at RXD[3:0]. No transmission of data on the network medium occurs and receive data on the network medium is ignored. By default, the loopback signal path encompasses most of the digital functional blocks. This bit allows for diagnostic testing.
0.13	SPEEDSL	R/W	1	Speed Selection: This bit determines the speed of operation of the 78Q2123/78Q2133. Setting this bit to '1' indicates 100Base-TX operation and a '0' indicates 10Base-T mode. This bit will default to a '1' upon reset. When auto-negotiation is enabled, this bit will not be writable and will have no effect on the 78Q2123/78Q2133. If auto-negotiation is not enabled, this bit may be written to force manual configuration.
0.12	ANEGEN	R/W	1	Auto-Negotiation Enable: The auto-negotiation process is enabled by setting this bit to '1'. This bit will default to '1'. If this bit is cleared to '0', manual speed and duplex mode selection is accomplished through bits 0.13 (*SPEEDSL*) and 0.8 (*DUPLEX*) of the Control Register.
0.11	PWRDN	R/W	0	Power-Down: The device may be placed in a low power consumption state by setting this bit to '1'. While in the power-down state, the device will still respond to management transactions.
0.10	ISO	R/W	0	Isolate: When set to '1', the device will present a high-impedance on its MII output pins. This allows for multiple PHY's to be attached to the same MII interface. When the device is isolated, it still responds to management transactions.
0.9	RANEG	R/WC	0	Restart Auto-Negotiation: Normally, the Auto-Negotiation process is started at power up. The process can be restarted by setting this bit to '1'. This bit is self-clearing.
0.8	DUPLEX	R/W	1	Duplex Mode: This bit determines whether the device supports full- duplex or half-duplex. A '1' indicates full-duplex operation and a '0' indicates half-duplex. This bit will default to '1' upon reset. When auto-negotiation is enabled, this bit will not be writable and will have no effect on the 78Q2123/78Q2133. If auto-negotiation is not enabled, this bit may be written to force manual configuration.
0.7	COLT	R/W	0	Collision Test: When this bit is set to '1', the device will assert the COL signal in response to the assertion of the TX_EN signal. Collision test is disabled if the PCSBP bit, MR16.1, is high. Collision test can be activated regardless of the duplex mode of operation.
0.6:0	RSVD	R	0	Reserved

3.2 MR1: Status Register

Bits 1.15 through 1.11 reflect the ability of the 78Q2123/78Q2133. They do not reflect any ability changes made via the MII Management Interface to bits 0.13 (*SPEEDSL*) , 0.12 (*ANEGEN*) and 0.8 (*DUPLEX*) in the Control Register.

Bit	Symbol	Type	Default	Description
1.15	100T4	R	0	100BASE-T4 Ability: Reads '0' to indicate the 78Q2123/78Q2133 do not support 100Base-T4 mode.
1.14	100X_F	R	1	100BASE-TX Full Duplex Ability: 0 : Not able 1 : Able
1.13	100X_H	R	1	100BASE-TX Half Duplex Ability: 0 : Not able 1 : Able
1.12	10T_F	R	1	10BASE-T Full Duplex Ability: 0 : Not able 1 : Able
1.11	10T_H	R	1	10BASE-T Half Duplex Ability: 0 : Not able 1 : Able
1.10	100T2_F	R	0	100BASE-T2 Full Duplex Ability: Reads '0' to indicate the 78Q2123/78Q2133 do not support 100Base-T2 full duplex mode.
1.9	100T2_H	R	0	100BASE-T2 Half Duplex Ability: Reads '0' to indicate the 78Q2123/78Q2133 do not support 100Base-T2 full duplex mode.
1.8	EXTS	R	0	Extended Status Information Availability: Reads '0' to indicate the 78Q2123/78Q2133 do not support Extended Status information on MR15.
1.7	RSVD	R	0	Reserved
1.6	MFPS	R	0	Management Frame Preamble Suppression Support: A "0" indicates that the 78Q2123/78Q2133 can read management frames with a preamble.
1.5	ANEGC	R	0	Auto-Negotiation Complete: A logic one indicates that the Auto-Negotiation process has been completed, and that the contents of registers MR4,5,6 are valid.
1.4	RFAULT	RC	0	Remote Fault: A logic one indicates that a remote fault condition has been detected and it remains set until it is cleared. This bit can only be cleared by reading this register (MR1) via the management interface.
1.3	ANEGA	R	(1)	Auto-Negotiation Ability: When set, this bit indicates the device's ability to perform Auto-Negotiation. The value of this bit is determined by the *ANEGEN* bit (MR0.12).
1.2	LINK	R	0	Link Status: A logic one indicates that a valid link has been established. If the link status should transition from an OK status to a NOT-OK status, this bit will become cleared and remains cleared until it is read.
1.1	JAB	RC	0	Jabber Detect: In 10Base-T mode, this bit is set during a jabber event. After a jabber event, the bit remains set until

				cleared by a read operation.
1.0	EXTD	R	1	Extended Capability: Reads '1' to indicate the 78Q2123/78Q2133 provide an extended register set (MR2 and beyond).

3.3 MR2: PHY Identifier Register 1

Bit	Symbol	Type	Value	Description
2.15:0	OUI [23:6]	R	000Eh	Organizationally Unique Identifier: This value is 00-C0-39 for Teridian Semiconductor Corporation. This register contains the first 16-bits of the identifier.

3.4 MR3: PHY Identifier Register 2

Bit	Symbol	Type	Value	Description
3.15:10	OUI [5:0]	R	1Ch	Organizationally Unique Identifier: Remaining 6 bits of the OUI.
3.9:4	MN	R	23h	Model Number: The last 2 digits of the model number 78Q2123 are encoded into the 6 bits for both 78Q2123 and 78Q2133.
3.3:0	RN	R	07h	Revision Number: The value '0111' corresponds to the seventh revision of the silicon.

3.5 MR4: Auto-Negotiation Advertisement Register

Bit	Symbol	Type	Default	Description
4.15	NP	R	0	Next Page: Not supported. Reads logic zero.
4.14	RSVD	R	0	Reserved
4.13	RF	R/W	0	Remote Fault: Setting this bit to '1' allows the device to indicate to the link partner a Remote Fault Condition.
4.12	A7	R	0	Reserved.
4.11	A6	R/W	0	Asymmetric PAUSE Support Indication for Full Duplex Links. Default is 0 indicating not supported. If the MAC supports Asymmetric PAUSE, this bit can be written as 1. Writing to this register has no effect until auto-negotiation is re-initiated.
4.10	A5	R	0	PAUSE Support Indication for Full Duplex Links. Default is 0 indicating not supported. If the MAC supports PAUSE, this bit can be written as 1. Writing to this register has no effect until auto-negotiation is re-initiated
4.9	A4	R	0	100BASE-T4: The 78Q2123/78Q2133 do not support 100BASE-T4 operation.
4.8	A3	R/W	(1)	100BASE-TX Full Duplex: If the MR1.14 bit is '1', this bit will be set to '1' upon reset and will be writeable. Otherwise, this bit cannot be set to '1' by the management.
4.7	A2	R/W	(1)	100BASE-TX: If the MR1.13 bit is '1', this bit will be set to '1' upon reset and will be writeable. Otherwise, this bit cannot be set to '1' by the management.
4.6	A1	R/W	(1)	10BASE-T Full Duplex: If the MR1.12 bit is '1', this bit will be set to '1' upon reset and will be writeable. Otherwise, this bit cannot be set to '1' by the management.

4.5	A0	R/W	(1)	10BASE-T: If the MR1.11 bit is '1', this bit will be set to '1' upon reset and will be writeable. Otherwise, this bit cannot be set to '1' by the management.
4.4:0	S4:0	R	01h	Selector Field: Hard coded with the value of '00001' for IEEE 802.3.

Note: Technology Ability Field: MR4.12:5 are the Technology Ability Field bits (A7:0). The default value of this field is dependent upon the MR1.15:11 register bits. This field can be overwritten by management to auto-negotiate to an alternate common technology. Writing to this register has no effect until auto-negotiation is re-initiated.

3.6 MR5: Auto-Negotiation Link Partner Ability Register

Bit	Symbol	Type	Default	Description
5.15	NP	R	0	Next Page: When '1' is read, it indicates the link partner wishes to engage in Next Page exchange.
5.14	ACK	R	0	Acknowledge: When '1' is read, it indicates the link partner has successfully received at least 3 consecutive and consistent FLP bursts.
5.13	RF	R	0	Remote Fault: When '1' is read, it indicates the link partner has a fault.
5.12:5	A7:0	R	0	Technology Ability Field: This field contains the technology ability of the link partner. The bit definition is the same as MR4.12:5.
5.4:0	S4:0	R	00h	Selector Field: This field contains the type of message sent by the link partner. For an IEEE 802.3 compliant link partner, this field should be '00001'.

3.7 MR6: Auto-Negotiation Expansion Register

Bit	Symbol	Type	Default	Description
6.15:5	RSVD	R	0	Reserved
6.4	PDF	RC	0	Parallel Detection Fault: When '1' is read, it indicates that more than one technology has been detected during link up. This bit is cleared when read.
6.3	LPNPA	R	0	Link Partner Next Page Able: When '1' is read, it indicates the link partner supports the Next Page function.
6.2	NPA	R	0	Next Page Able: Reads '0' since the 78Q2123/78Q2133 do not support Next Page function.
6.1	PRX	RC	0	Page Received: Reads '1' when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon read.
6.0	LPANEGA	R	0	Link Partner Auto-Negotiation Able: When '1' is read, it indicates the link partner is able to participate in the Auto-Negotiation function.

3.8 MR16: Vendor Specific Register

Bit	Symbol	Type	Default	Description
16.15	RPTR	R/W	(0)	Repeater Mode: When set, the 78Q2123/78Q2133 are put into Repeater mode of operation. In this mode, full duplex is

				prohibited, CRS responds to receive activity only and, in 10Base-T mode, the SQE test function is disabled.
16.14	INPOL	R/W	0	When this bit is '0', the INTR pin is forced low to signal an interrupt. Setting this bit to '1' causes the INTR pin to be forced high to signal an interrupt.
16.13	RSVD	R	0	Reserved
16.12	TXHIM	R/W	0	Transmitter High-Impedance Mode: When set, the TXOP/TXON transmit pins and the TX_CLK pin are put into a high-impedance state. The receive circuitry remains fully functional.
16.11	SQEI	R/W	0	SQE Test Inhibit: Setting this bit to '1' disables 10Base-T SQE testing. By default, this bit is '0' and the SQE test is performed by generating a COL pulse following the completion of a packet transmission.
16.10	NL10	R/W	0	10Base-T Natural Loopback: Setting this bit to '1' causes transmit data received on the TXD0-3 pins to be automatically looped back to the RXD0-3 pins when 10Base-T mode is enabled.
16.9	RSVD	R	0	Reserved
16.8	RSVD	R	1	Reserved
16.7	RSVD	R	0	Reserved
16.6	RSVD	R	1	Reserved
16.5	APOL	R/W	0	Auto Polarity: During auto-negotiation and 10BASE-T mode, the 78Q2123/78Q2133 are able to automatically invert the received signal due to a wrong polarity connection. It does so by detecting the polarity of the link pulses. Setting this bit to '1' disables this feature.
16.4	RVSPOL	R/W	0	Reverse Polarity: The reverse polarity is detected either through 8 inverted 10Base-T link pulses (NLP) or through one burst of inverted clock pulses in the auto-negotiation link pulses (FLP). When the reverse polarity is detected and if the Auto Polarity feature is enabled, the 78Q2123/78Q2133 will invert the receive data input and set this bit to '1'. If Auto Polarity is disabled, then this bit is writeable. Writing a '1' to this bit forces the polarity of the receive signal to be reversed.
16.3:2	RSVD	R/W	0h	Reserved: Must set to '00'.
16.1	PCSBP	R/W	0	PCS Bypass Mode: When set, the 100Base-TX PCS and scrambling/ descrambling functions are bypassed. Scrambled 5-bit code groups for transmission are applied to the TX_ER, TXD3-0 pins and received on the RX_ER, RXD3-0 pins. The RX_DV and TX_EN signals are not valid in this mode. PCSBP mode is valid only when 100Base-TX mode is enabled and auto-negotiation is disabled.
16.0	RXCC	R/W	0	Receive Clock Control: This function is valid only in 100Base-TX mode. When set to '1', the RX_CLK signal will be held low when there is no data being received (to save power). The RX_CLK signal will restart 1 clock cycle before the assertion of RX_DV and will be shut off 64 clock cycles after RX_DV goes low. RXCC is disabled when loopback mode is enabled (MR0.14 is high). This bit should be kept at logic zero when PCS Bypass mode is used.

3.9 MR17: Interrupt Control/Status Register

The Interrupt Control/Status Register provides the means for controlling and observing the events, which trigger an interrupt on the INTR pin. This register can also be used in a polling mode via the MII Serial Interface as a means to observe key events within the PHY via one register address. Bits 0 through 7 are status bits, which are each set to logic one based upon an event. These bits are cleared after the register is read. Bits 8 through 15 of this register, when set to logic one, enable their corresponding bit in the lower byte to signal an interrupt on the INTR pin. The assertion level of this interrupt signal output on the INTR pin can be set via the MR16.14 (*INPOL*) bit.

Bit	Symbol	Type	Default	Description
17.15	JABBER_IE	R/W	0	Jabber Interrupt Enable
17.14	RXER_IE	R/W	0	Receive Error Interrupt Enable
17.13	PRX_IE	R/W	0	Page Received Interrupt Enable
17.12	PDF_IE	R/W	0	Parallel Detect Fault Interrupt Enable
17.11	LP-ACK_IE	R/W	0	Link Partner Acknowledge Interrupt Enable
17.10	LS-CHG_IE	R/W	0	Link Status Change Interrupt Enable
17.9	RFAULT_IE	R/W	0	Remote Fault Interrupt Enable
17.8	ANEG-COMP_IE	R/W	0	Auto-Negotiation Complete Interrupt Enable
17.7	JAB_INT	RC	0	Jabber Interrupt: This bit is set high when a Jabber event is detected by the 10Base-T circuitry.
17.6	RXER_INT	RC	0	Receive Error Interrupt: This bit is set high when the RX_ER signal transitions high.
17.5	PRX_INT	RC	0	Page Received Interrupt: This bit is set high when a new page has been received from the link partner during auto-negotiation.
17.4	PDF_INT	RC	0	Parallel Detect Fault Interrupt: This bit is set high by the auto-negotiation logic when a parallel detect fault condition is indicated.
17.3	LP-ACK_INT	RC	0	Link Partner Acknowledge Interrupt: This bit is set high by the auto-negotiation logic when FLP bursts are received with the acknowledge bit set.
17.2	LS-CHG_INT	RC	0	Link Status Change Interrupt: This bit is set when the link transitions from an OK status to a FAIL status.
17.1	RFAULT_INT	RC	0	Remote Fault Interrupt: This bit is set when a remote fault condition has been indicated by the link partner.
17.0	ANEG-COMP_INT	RC	0	Auto-Negotiation Complete Interrupt: This bit is set by the auto-negotiation logic upon successful completion of auto-negotiation.

3.10 MR18: Diagnostic Register

Bit	Symbol	Type	Default	Description
18.15:13	RSVD	R	0	Reserved
18.12	ANEGF	RC	0	Auto-Negotiation Fail Indication: This bit is set when auto-negotiation completes and no common technology was found. It remains set until read.
18.11	DPLX	R	0	Duplex Indication: This bit indicates the result of the auto-negotiation for duplex arbitration as follows: 0 = Half-duplex was the highest common denominator 1 = Full-duplex was the highest common denominator
18.10	RATE	R	0	Rate Indication: This bit indicates the result of the auto-negotiation for data rate arbitration as follows: 0 = 10Base-T was the highest common denominator 1 = 100Base-TX was the highest common denominator
18.9	RXSD	R	0	Receiver Signal Detect Indication: In 10Base-T mode, this bit indicates that Manchester data has been detected. In 100Base-TX mode, it indicates that the receive signal activity has been detected (but not necessarily locked on to).
18.8	RX_LOCK	R	0	Receive PLL Lock Indication: Indicates that the Receive PLL has locked onto the receive signal for the selected speed of operation (10Base-T or 100Base-TX).
18.7:0	RSVD	R	00h	Reserved: Must set to '00h'.

3.11 MR19: Transceiver Control

Bit	Symbol	Type	Default	Description
19.15:14	TXO[1:0]	R/W	01	Transmit Amplitude Selection: Sets the transmit output amplitude to account for transmit transformer insertion loss. 00 = Gain set for 0.0dB of insertion loss. 01 = Gain set for 0.4dB of insertion loss. 10 = Gain set for 0.8dB of insertion loss. 11 = Gain set for 1.2dB of insertion loss.
19.13:0	RSVD	R	XXXh	Reserved

3.12 MR20: Reserved

Bit	Symbol	Type	Default	Description
20.15:0	Reserved	NA	XXXXh	Reserved: must be 0000h.

3.13 MR21: Reserved

Bit	Symbol	Type	Default	Description
21.15:0	Reserved	NA	XXXXh	Reserved: must be 0000h.

3.14 MR22: Reserved

Bit	Symbol	Type	Default	Description
22.15:0	Reserved	NA	XXXXh	Reserved: must be 0000h.

3.15 MR23: LED Configuration Register

Bit	Symbol	Type	Default	Description
23.15:8	Reserved	NA	<0000>	Must set to zero on each write to MR23
23.7:4	LED1[3:0]	R/W	<1h>	0000 = Link OK 0001 = RX or TX Activity (Default LED1) 0010 = TX Activity 0011 = RX Activity 0100 = Collision 0101 = 100 BASE-TX mode 0110 = 10 BASE-T mode 0111 = Full Duplex 1000 = Link OK/Blink=RX or TX Activity
23.3:0	LED0[3:0]	R/W	<0h>	0000 = Link OK (Default LED0) 0001 = RX or TX Activity 0010 = TX Activity 0011 = RX Activity 0100 = Collision 0101 = 100 BASE-TX mode 0110 = 10 BASE-T mode 0111 = Full Duplex 1000 = Link OK/Blink=RX or TX Activity

3.16 MR24: MDI/MDIX Control Register

Bit	Symbol	Type	Default	Description
24.15:8	Reserved	R	0	Reserved
24.7	PD_MODE	R/W	1	Write a '1' to this bit to add Parallel Detect mode. This will allow auto-switching to work when auto-negotiation is off while the other device has it on.
24.6	AUTO_SW	R/W	1	Write a '1' to this bit to enable auto switching.
24.5	MDIX	R/W	0	Indicates state of the MDI pair or force configuration: 1 = MDIX (cross over) 0 = MDI When auto_sw is a '1', this bit will only be readable. When auto_sw is a '0' this bit can be written to set the configuration.
24.4	MDIX_CM	R	0	Indicates completion of auto-switch sequence. 1 = Sequence completed. 0 = Sequence in progress or auto-switch is disabled.
24.3:0	MDIX_SD	R/W	<0000>	Write initial pattern seed for switching algorithm. The initial seed directly affects attempts [5,4] respectively to write bits [3:0]. Setting to [0000] will result in device using its own seed of [0101].

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Operation above maximum rating may permanently damage the device.

Parameter	Rating
DC Supply Voltage (Vcc)	-0.5 to 4.0 VDC
Storage Temperature	-65 to 150 °C
Pin Voltage (except TXOP/N)	-0.3 to (Vcc+0.6) VDC
Pin Voltage (TXOP/N only)	-0.3 to (Vcc+1.4) VDC
Pin Current	± 120 mA

4.2 Recommended Operating Conditions

Unless otherwise noted, all specifications are valid over these temperatures and supply voltage ranges.

Parameter	Rating
DC Voltage Supply (Vcc)	3.3 ± 0.3 VDC
78Q2123 Ambient Operating Temperature (Ta)	0 to 70 °C
78Q2133 Ambient Operating Temperature (Ta)	-40 to 85 °C
Maximum Junction Temperature	125 °C
Package Thermal Conductivity (θja)	50 °C/W

4.3 DC Characteristics

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Supply Current	I_{CC}	Vcc = 3.3V; Auto-Negotiation 10BT (Idle) 10BT (Normal Activity) 100BTX		 48 26 88 88	 56 35 110 110	mA
Supply Current	I_{CC}	Power-down mode			6	mA

4.4 Digital I/O Characteristics

Pins of type CI, CIU, CID, CIO

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Input Voltage Low	Vil				0.8	V
Input Voltage High	Vih		2.0		3.6	V
Input Current	Iil, Iih		-1		1	μA
Pull-up Resistance	Rpu	Type CIU only	38	56	78	kΩ
Input Capacitance	Cin			8		pF

Pins of type CIS

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Low-to-High Threshold	Vt+				2.0	V
High-to-Low Threshold	Vt-		0.8			V
Input Current	Iil, Iih		-1		1	μA
Input Capacitance	Cin			8		pF
Input Hysteresis	Vhy		125			mV

Pins of type COZ

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Output Voltage Low	Vol	Iol = 4mA			0.4	V
Output Voltage High	Voh	Ioh = -4mA	2.4			V
Output Transition Time	Tt	CL = 20pF			6	ns
Tristate Output Leakage Current	Iz		-1		1	μA

Pins of type CO

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Output Voltage Low	Vol	Iol = 4mA			0.4	V
Output Voltage High	Voh	Ioh = -4mA	2.4			V
Output Transition Time	Tt	CL = 20pF			6	ns

Pins of type CIO

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Output Voltage Low	Vol	Iol = 4mA			0.4	V
Output Voltage High	Voh	Ioh = -4mA	2.4			V
Output Transition Time	Tt	CL = 20pF			6	ns

4.5 Digital Timing Characteristics

4.5.1 $\overline{\text{RST}}$ Characteristics

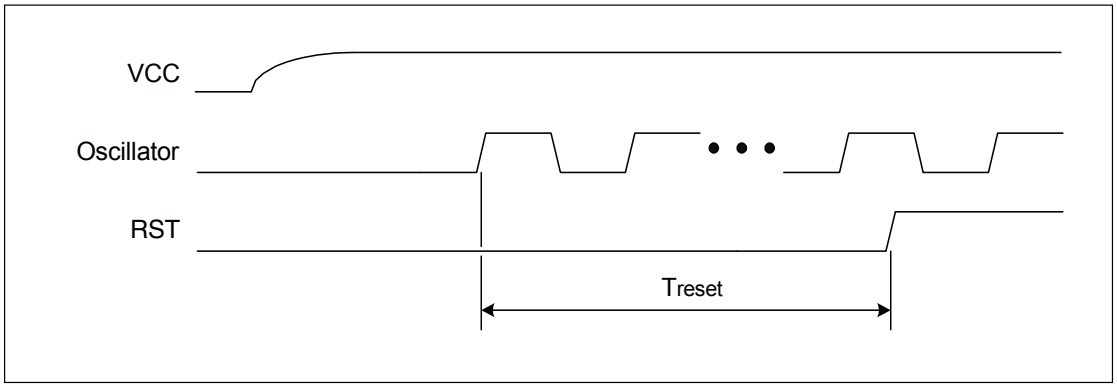


Figure 1: RST Pulse Duration

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
RST Pulse Assertion	Treset	VCC = 3.3V and oscillator stabilized	30			Oscillator Clock Cycles

4.5.2 MII Transmit Interface

Characteristics	Symbol	Conditions	Min	Nom	Max	Unit
Setup Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX_{SU}		15			ns
Hold Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX_{HD}		0			ns
CKIN-to-TX_CLK Delay	T_{CKIN}		0		40	ns
TX_CLK Duty-Cycle			40		60	%

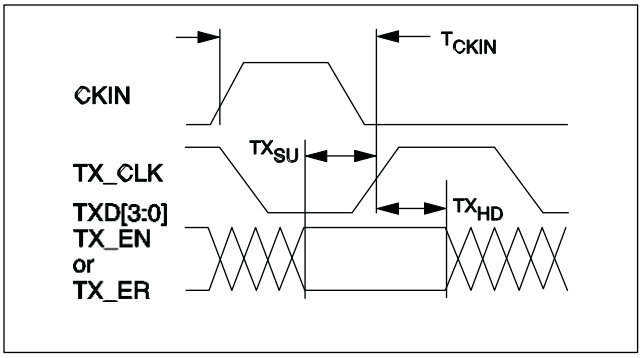


Figure 2: Transmit Inputs to the 78Q2123/78Q2133

4.5.3 MII Receive Interface

Characteristics	Symbol	Conditions	Min	Nom	Max	Unit
Receive Output Delay: RX_CLK to RXD[3:0], RX_DV, RX_ER	RX_{DLY}		10		30	ns
RX_CLK Duty-Cycle			40		60	%

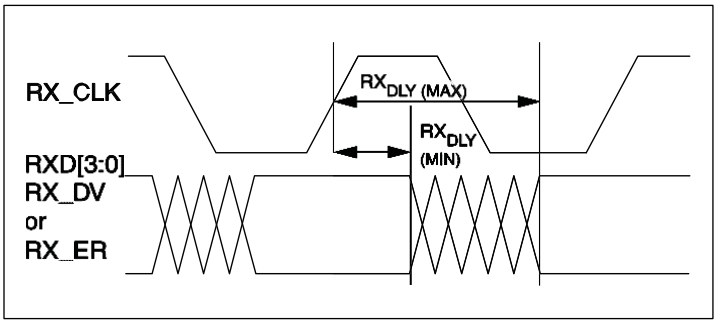


Figure 3: Receive Outputs from the 78Q2123/78Q2133

4.6 MDIO Interface Input Timing

Characteristics	Symbol	Conditions	Min	Nom	Max	Unit
Setup Time: MDC to MDIO	MIO_{SU}		10			ns
Hold Time: MDC to MDIO	MIO_{HD}		10			ns
Max Frequency: MDC	F_{max}				25	MHz

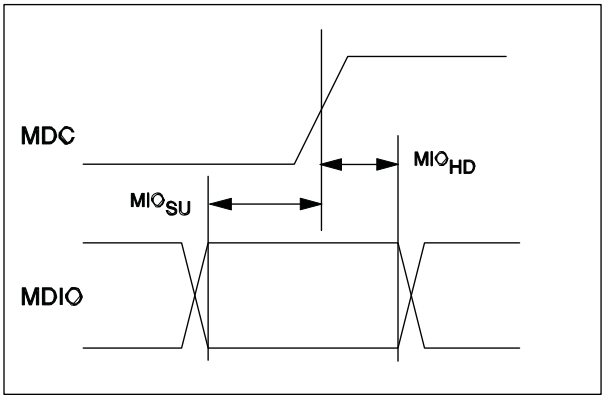


Figure 4: MDIO as an Input to the 78Q2123/78Q2133

4.6.1 MDIO Interface Output Timing

Characteristics	Symbol	Conditions	Min	Nom	Max	Unit
MDC to MDIO data delay	MC2D				30	ns
MDIO output from high Z to driven after MDC	MCZ2D				30	ns
MDIO output from driven to high Z after MDC	MCD2Z				30	ns

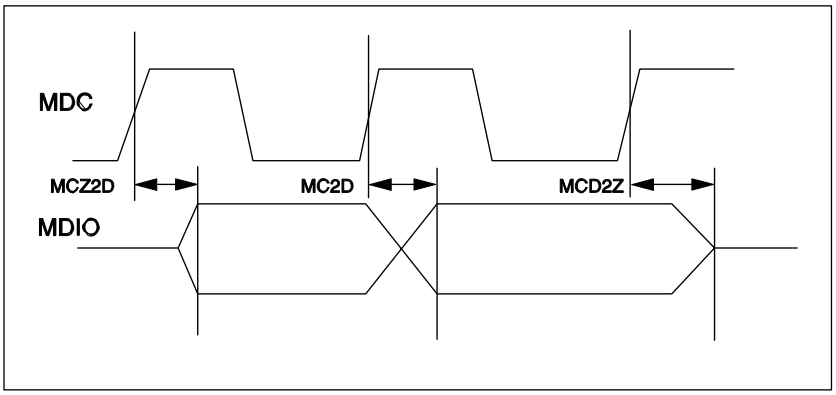


Figure 5: MDIO as an Output to the 78Q2123/78Q2133

4.6.2 MDIO Interface Output Timing

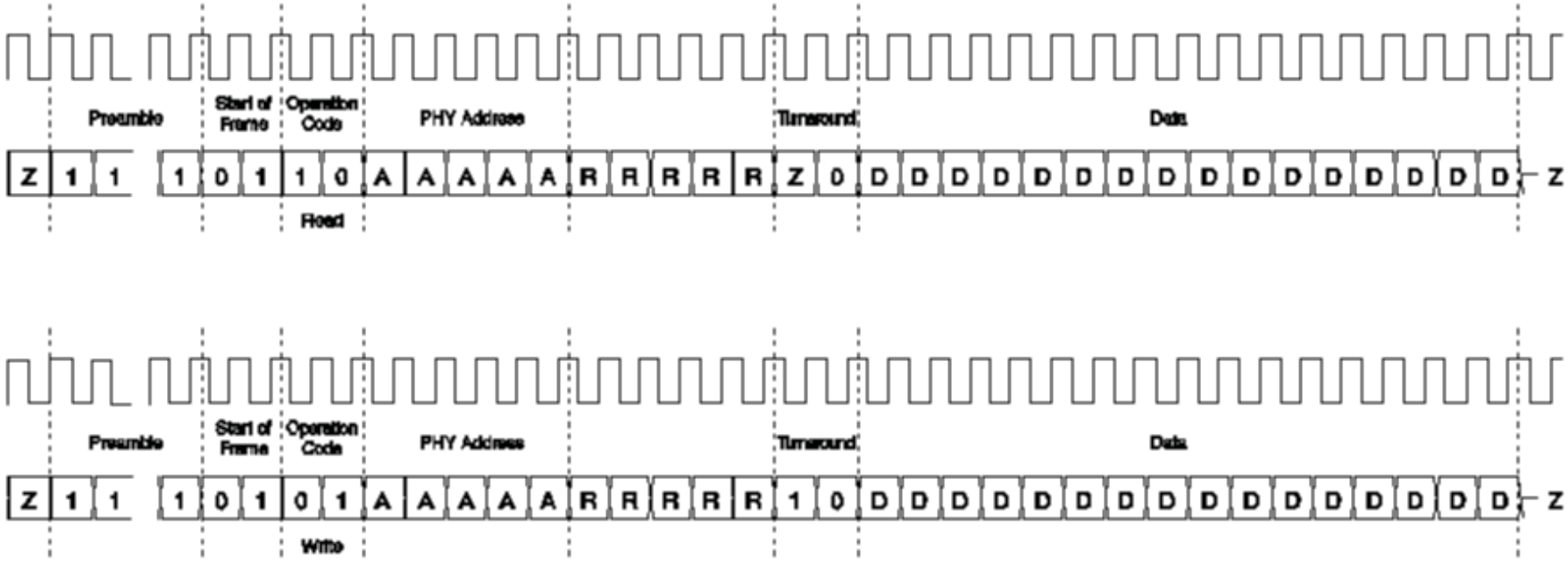


Figure 6: MDIO Interface Output Timing

4.6.3 100BASE-TX System Timing

System timing requirements for 100BASE-TX operation are listed in Table 24-2 of Clause 24 of IEEE 802.3.

Parameter	Condition	Nom	Unit
TX_EN Sampled to first bit of "J" on MDI output		12	BT
First bit of "J" on MDI input to CRS assert		16	BT
First bit of "T" on MDI input to CRS de-assert		23	BT
First bit of "J" on MDI input to COL assert		20	BT
First bit of "T" on MDI input to COL de-assert		24	BT
TX_EN Sampled to CRS assert	RPTR = low	6	BT
TX_EN sampled to CRS de-assert	RPTR = low	6	BT

4.6.4 10BASE-T System Timing

Parameter	Condition	Min	Nom	Max	Unit
TX_EN (MII) to TD Delay				6	BT
RD to RXD at (MII) Delay				6	BT
Collision delay				9	BT
SQE test wait			1		μs
SQE test duration			1		μs
Jabber on-time*		20		150	ms
Jabber off-time*		250		750	ms

***** Guarantee by design. The specifications in the following table are included for information only.

4.7 Analog Electrical Characteristics

4.7.1 100BASE-TX Transmitter

Parameter	Condition	Min	Nom	Max	Unit
Peak Output Amplitude (|Vp+|, |Vp-|) (see note below)	Best-fit over 14 bit times; 0.4 dB Transformer loss	950		1050	mVpk
Output Amplitude Symmetry	$\frac{\|Vp+\|}{\|Vp-\|}$	0.98		1.02	
Output Overshoot	Percent of Vp+, Vp-			5	%
Rise/Fall time (tr, tf)	10-90% of Vp+, Vp-	3		5	ns
Rise/Fall time Imbalance	$\|tr - tf\|$			500	ps
Duty Cycle Distortion	Deviation from best-fit time-grid; 010101... Sequence			±250	ps
Jitter	Scrambled Idle			1.4	ns

Note: Measured at the line side of the transformer.

Test Condition: Transformer P/N: TLA-6T103
Line Termination: 100 Ω ±1%

4.7.2 100BASE-TX Transmitter (Informative)

The specifications in the following table are included for information only. They are mainly a function of the external transformer and termination resistors used for measurements.

Parameter	Condition	Min	Max	Unit
Return Loss	2 < f < 30 MHz 30 < f < 60 MHz 60 < f < 80 MHz	16 $16 - 20\log\left(\frac{f}{30\,MHz}\right)$ 10		dB
Open-Circuit Inductance	-8 < Iin < 8 mA	350		μH

4.7.3 100BASE-TX Receiver

Parameter	Condition	Min	Nom	Max	Unit
Signal Detect Assertion Threshold		500	600	700	mVppd
Signal Detect De-assertion Threshold		275	350	425	mVppd
Differential Input Resistance			20		kΩ
Jitter Tolerance (pk-pk)	Not tested in production	4			ns
Baseline Wander Tracking		-75		+75	%
Signal Detect Assertion Time	Not tested			1000	μs
Signal Detect De-assertion Time	Not tested			4	μs

4.7.4 10BASE-T Transmitter

The Manchester-encoded data pulses, the link pulse and the start-of-idle pulse are tested against the templates and using the procedures found in Clause 14 of IEEE 802.3.

Parameter	Condition	Min	Nom	Max	Unit
Peak Differential Output Signal (see note below)	All data patterns	2.2		2.8	V
Harmonic Content (dB below fundamental)	Any harmonic All ones data Not tested	27			dB
Link Pulse Width			100		ns
Start-of-Idle Pulse Width	Last bit 0 Last bit 1		300 350		ns ns

Note: Measured at the line side of the transformer.

Test Condition: Transformer P/N: TLA-6T103
Line Termination: 100Ω ±1%

4.7.5 10BASE-T Transmitter (Informative)

The specifications in the following table are included for information only. They are mainly a function of the external transformer and termination resistors used for measurements.

Parameter	Condition	Min	Nom	Max	Unit
Output return loss		15			dB
Output Impedance Balance	1 MHz < freq < 20 MHz	$29-17\log\left(\frac{f}{10}\right)$			dB
Peak Common-mode Output Voltage				50	mV
Common-mode rejection	15 V_{pk}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			100	mV
Common-mode rejection jitter	15 V_{pk}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			1	ns

4.7.6 10BASE-T Receiver

Parameter	Condition	Min	Nom	Max	Unit
DLL Phase Acquisition Time			10		BT
Jitter Tolerance (pk-pk)		30			ns
Input Squelched Threshold		500	600	700	mVppd
Input Unsquelched Threshold		275	350	425	mVppd
Differential Input Resistance			20		kΩ
Bit Error Ratio			10^{-10}		
Common-mode rejection	Square wave 0 < f < 500 kHz Not tested	25			V

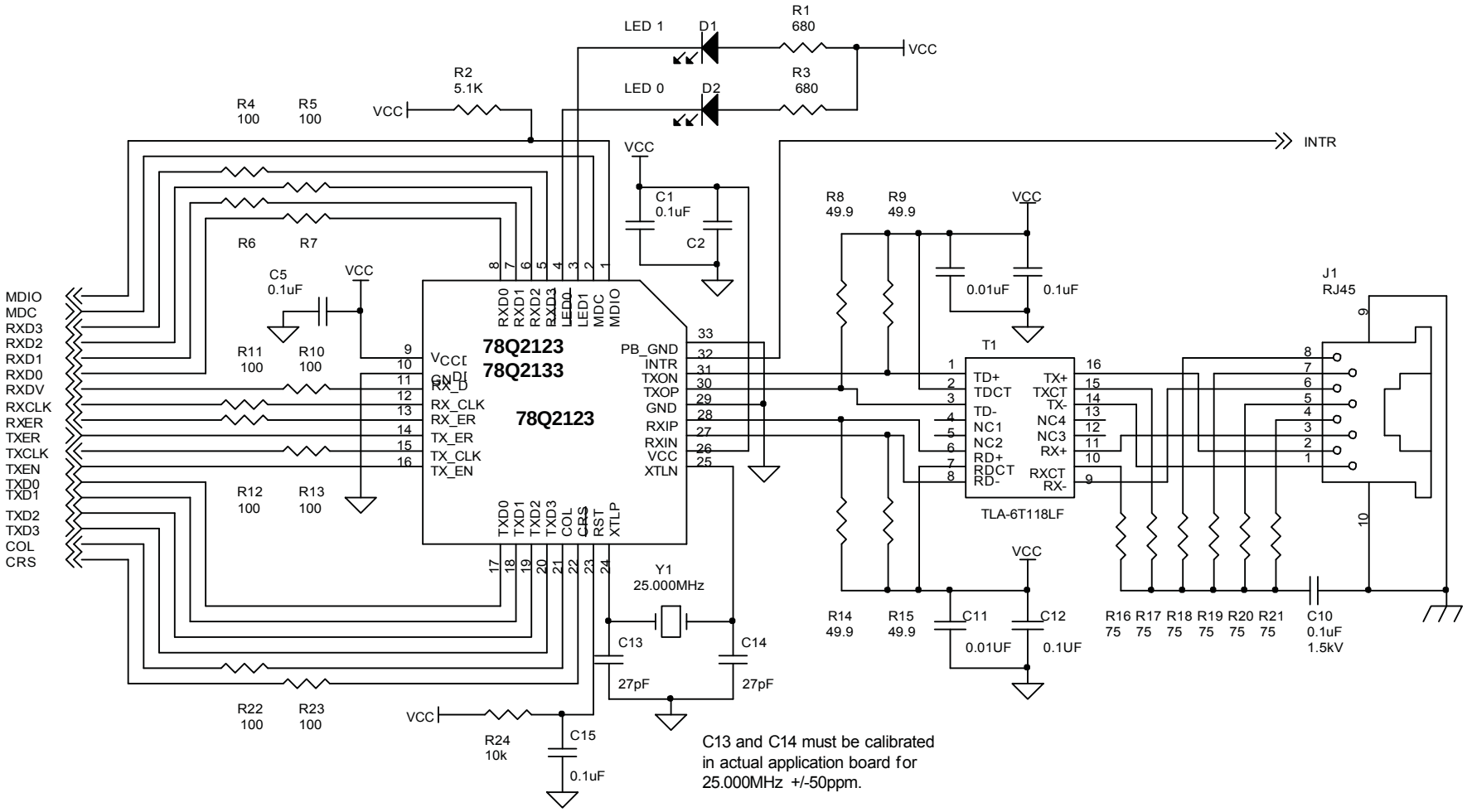


Figure 7: Application Diagram for 78Q2123/78Q2133

4.8 Isolation Transformers

Two simple 1:1 isolation transformers are required at the line interface. Transformers with integrated common-mode chokes are recommended for exceeding FCC requirements. This table gives the recommended line transformer characteristics.

Name	Value	Condition
Turns Ratio	1 CT : 1 CT ± 5%	
Open-Circuit Inductance	350 μH (min)	@ 10 mV, 10 kHz
Leakage Inductance	0.40 μH (max)	@ 1 MHz (min)
Inter-Winding Capacitance	25 pF (max)	
D.C. Resistance	0.9 Ω (max)	
Insertion Loss	0.4 dB (typ)	0 - 65 MHz
HIPOT	1500 Vrms	

Note: The 100Base-TX amplitude specifications assume a transformer loss of 0.4 dB. For the transmit line transformer with higher insertion losses, up to 1.2 dB of insertion loss can be compensated by selecting the appropriate setting in the Transmit Amplitude Selection bits in register MR19.15:14.

4.9 Reference Crystal

If the internal crystal oscillator is to be used, a crystal with the following characteristics should be chosen.

Name	Value	Units
Frequency	25.00000	MHz
Load Capacitance*	4**	pF
Frequency Tolerance	±50	PPM
Aging	±2	PPM/yr
Temperature Stability (0 - 70°C)	±5	PPM
Oscillation Mode	Parallel Resonance, Fundamental Mode	
Parameters at 25°C ± 2°C ; Drive Level = 0.5 mW		
Drive Level (typ)	50-100	μW
Shunt Capacitance (max)	10	pF
Motional Capacitance (min)	10	pF
Series Resistance (max)	60	Ω
Spurious Response (max)	> 5 dB below main within 500 kHz	

***** Equivalent differential capacitance across the XTLP/XTLN pins.

** If crystal with a larger load is used, external shunt capacitors to ground should be added to make up the equivalent capacitance difference.

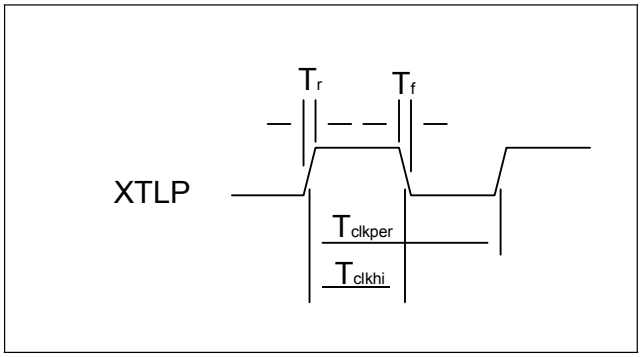


Figure 8: External XTLP Oscillator Characteristics

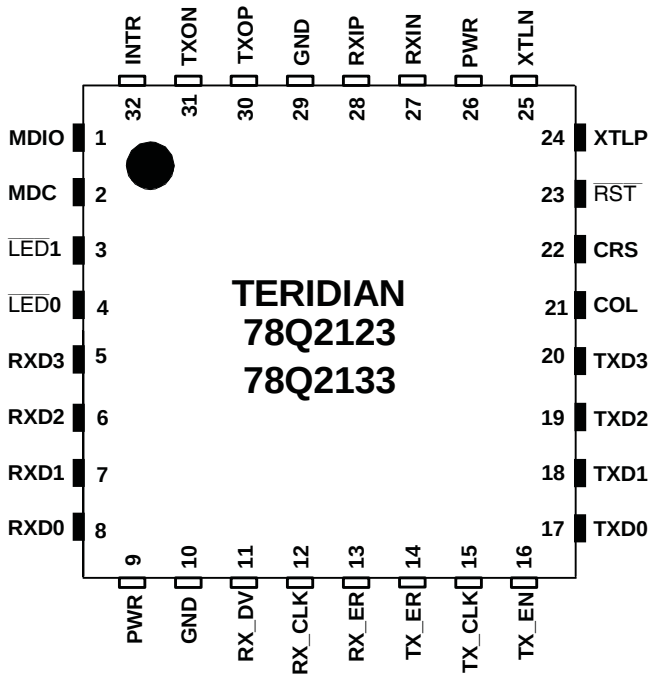
4.9.1 External XTLP Oscillator Characteristics

Parameter	Symbol	Condition	Min	Nom	Max	Unit
XTLP Input Level		See specification for CIS-type input				
XTLN Input Low Voltage					0.8	V
XTLP Frequency	f	See Note 1		25.000		MHz
XTLP Period	Tclkper	See Note 1		40		ns
XTLP Duty Cycle		Tclkhi / Tclkper	40		60	%
Rise / Fall Time	Tr, Tf				4.0	ns
Absolute Jitter		Input signaling requirements = CIS			0.1	ns

Note 1: IEEE 802.3 frequency tolerance ±50 ppm.

5 Package Pin Designations

(Top View)



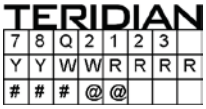
Note: For information only, actual package outline will vary depending on package type.

Figure 9: Package Pin Designations

6 Package Information

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32-QFN	G3255+3	21-0697	90-0434
32-TQFN	T3255+4	21-0140	90-0012

7 Ordering Information

Part	Package	Option	Ordering Number	IC Marking
78Q2123, Lead-Free, Commercial Temp	32-QFN	Bulk	78Q2123/F	
		Tape & Reel	78Q2123R/F	
	32-TQFN	Bulk	78Q2123S/F	
		Tape & Reel	78Q2123SR/F	
78Q2133, Lead-Free, Industrial Temp	32-QFN	Bulk	78Q2133/F	
		Tape & Reel	78Q2133R/F	
	32-TQFN	Bulk	78Q2133S/F	
		Tape & Reel	78Q2133SR/F	

YY: Last two digits of year of assembly
WW: Week of assembly
RRRR:Die Rev Code from Reliability Database
###: Will be substituted with the last 3 numeric characters from the lot number
@@: Will be substituted with the first two alpha characters after the numeric characters from the lot number

Revision History

Rev. #	Date	Comments
1.0	9/15/2005	First publication.
1.6	4/16/2010	Removed the 32-pin TQFP option.
2.0	9/24/2014	Added 32-TQFN package.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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