19-5735; Rev 3/11

DS1100
5-Tap Economy Timing Element (Delay Line)

GENERAL DESCRIPTION

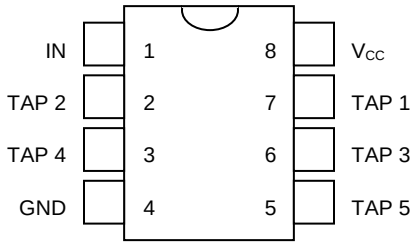
The DS1100 series delay lines have five equally spaced taps providing delays from 4ns to 500ns. These devices are offered in surface-mount packages to save PCB area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry-standard µMAX and SO packaging. The DS1100 5-tap silicon delay line reproduces the input-logic state at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1100 is designed to reproduce both leading and trailing edges with equal precision. Each tap can drive up to 10 74LS loads.

Maxim can customize standard products to meet special needs.

FEATURES

- All-Silicon Timing Circuit
- Five Taps Equally Spaced
- 5V Operation
- Delays are Stable and Precise
- Both Leading- and Trailing-Edge Accuracy
- Improved Replacement for DS1000
- Low-Power CMOS
- TTL/CMOS-Compatible
- Vapor-Phase, IR, and Wave Solderable
- Custom Delays Available
- Fast-Turn Prototypes
- Delays Specified Over Both Commercial and Industrial Temperature Ranges

PIN ASSIGNMENT



DS1100Z SO (150 mils)
DS1100U µMAX®

PIN DESCRIPTION

TAP 1 to TAP 5	- TAP Output Number
V_{CC}	- +5V
GND	- Ground
IN	- Input

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground ..... -0.5V to +6.0V
Short-Circuit Output Current ..... 50mA for 1s
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow)
Lead(Pb)-free ..... +260°C
Containing lead(Pb) ..... +240°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	5
High-Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.3	V	5
Low-Level Input Voltage	V_{IL}		-0.3		0.8	V	5
Input-Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = Max; Freq = 1MHz		30	50	mA	6, 8
High-Level Output Current	I_{OH}	V_{CC} = Min; V_{OH} = 4			-1	mA	
Low-Level Output Current	I_{OL}	V_{CC} = Min; V_{OL} = 0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}		20% of Tap 5 t_{PLH}			ns	9
Input-to-Tap Delay Tolerance (Delays ≤ 40ns)	t_{PLH}, t_{PHL}	+25°C 5V	-2	Table 1	+2	ns	1, 3, 4, 7
		0°C to +70°C	-3	Table 1	+3	ns	1, 2, 3, 4, 7
		-40°C to +85°C	-4	Table 1	+4	ns	1, 2, 3, 4, 7
Input-to-Tap Delay Tolerance (Delays > 40ns)	t_{PLH}, t_{PHL}	+25°C 5V	-5	Table 1	+5	%	1, 3, 4, 7
		0°C to +70°C	-8	Table 1	+8	%	1, 2, 3, 4, 7
		-40°C to +85°C	-13	Table 1	+13	%	1, 2, 3, 4, 7
Power-Up Time	t_{PU}				200	µs	
Input Period	Period		$2(t_{WI})$			ns	9

CAPACITANCE

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	10	pF	

NOTES:

1) Initial tolerances are ± with respect to the nominal value at +25°C and 5V for both leading and trailing edge.
2) Temperature and voltage tolerance is with respect to the nominal delay value over the stated temperature range, and a supply-voltage range of 4.75V to 5.25V.
3) All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP1 slows down, all other taps also slow down; TAP3 can never be faster than TAP2.
4) Intermediate delay values are available on a custom basis. For further information, email the factory at custom.oscillators@maxim-ic.com.
5) All voltages are referenced to ground.
6) Measured with outputs open.
7) See *Test Conditions* section at the end of this data sheet.
8) Frequencies higher than 1MHz result in higher I_{CC} values.
9) At or near maximum frequency the delay accuracy can vary and will be application sensitive (i.e., decoupling, layout).

Figure 1. LOGIC DIAGRAM

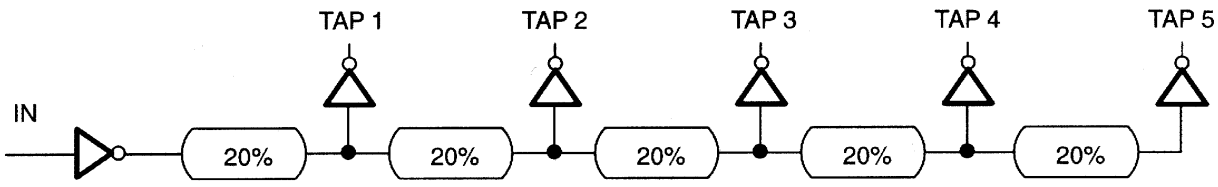
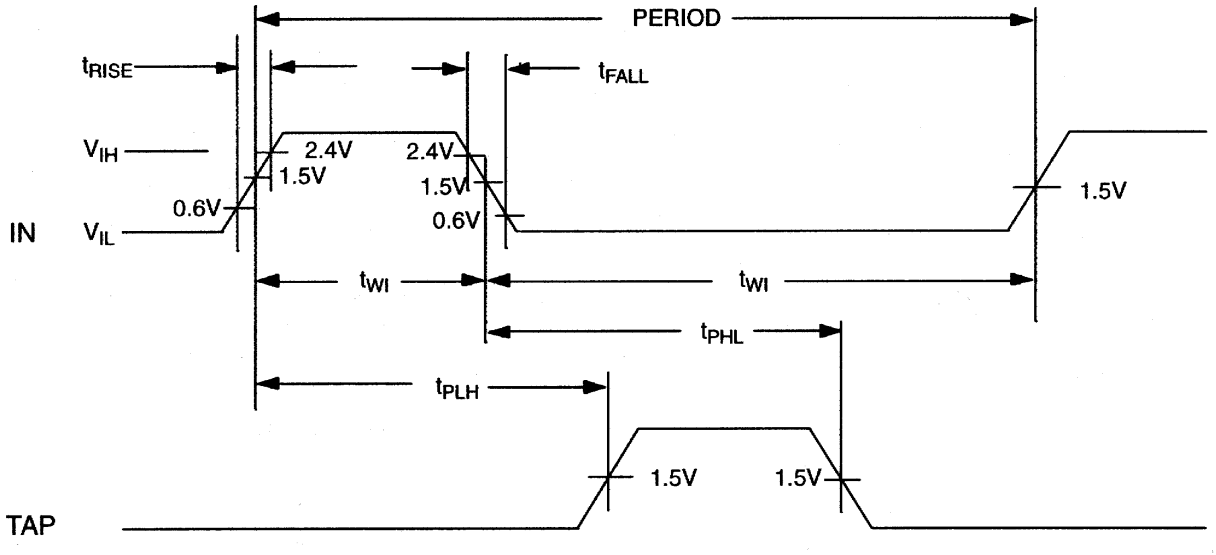


Figure 2. TIMING DIAGRAM: SILICON DELAY LINE



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1100. The input waveform is produced by a precision-pulse generator under software control. Time delays are measured by a time interval counter (20ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS INPUT

Ambient Temperature:	+25°C ±3°C
Supply Voltage (V_{CC}):	5.0V ±0.1V
Input Pulse:	High = 3.0V ±0.1V
	Low = 0.0V ±0.1V
Source Impedance:	50Ω max
Rise and Fall Time:	3.0ns max (measured between 0.6V and 2.4V)
Pulse Width:	500ns (1µs for -500 version)
Period:	1µs (2µs for -500 version)

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

Note: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

Figure 3. TEST CIRCUIT

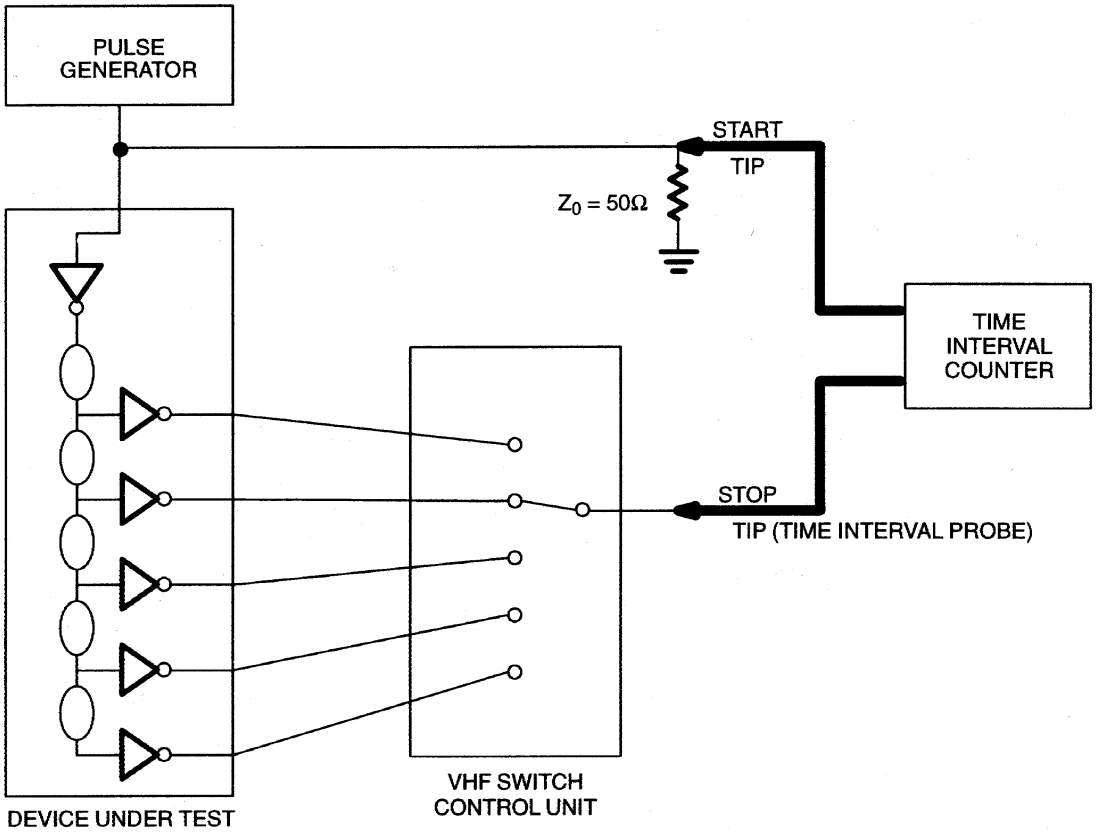


Table 1. DS1100 PART NUMBER DELAY

PART	NOMINAL DELAYS (ns)				
DS1100-xxx	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
-20	4	8	12	16	20
-25	5	10	15	20	25
-30	6	12	18	24	30
-35	7	14	21	28	35
-40	8	16	24	32	40
-45	9	18	27	36	45
-50	10	20	30	40	50
-60	12	24	36	48	60
-75	15	30	45	60	75
-100	20	40	60	80	100
-125	25	50	75	100	125
-150	30	60	90	120	150
-175	35	70	105	140	175
-200	40	80	120	160	200
-250	50	100	150	200	250
-300	60	120	180	240	300
-500	100	200	300	400	500

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS1100Z-xxx	-40°C to +85°C	8 SO
DS1100Z-xxx/T&R	-40°C to +85°C	8 SO
DS1100Z-xxx+	-40°C to +85°C	8 SO
DS1100Z-xxx+T	-40°C to +85°C	8 SO
DS1100U-xxx	-40°C to +85°C	8 μMAX
DS1100U-xxx/T&R	-40°C to +85°C	8 μMAX
DS1100U-xxx+	-40°C to +85°C	8 μMAX
DS1100U-xxx+T	-40°C to +85°C	8 μMAX

xxx *Denotes total time delay (ns) (see Table 1).*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R and T = Tape and reel.

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO (150 mils)	S8+4	**21-0041**	**90-0096**
8 μMAX	U8+1	**21-0036**	**90-0092**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
3/11	Removed the DIP package from *General Description*, *Pin Assignment*, and *Ordering Information* (no longer available); changed µSOP package type to µMAX; updated the *Absolute Maximum Ratings* section; added the customer support email address to the electrical characteristics Note 4; added the *Ordering Information* and *Package Information* tables	1–6

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