Rev 1; 11/03

DALLAS SEMICONDUCTOR MAXIM

10-Tap Silicon Delay Line

General Description

The DS1110 delay line is an improved replacement for the DS1010. It has ten equally spaced taps providing delays from 5ns to 500ns. The devices are offered in a standard 16-pin SO or 14-pin TSSOP. The DS1110 series delay lines provide a nominal accuracy of ±5% or ±2ns, whichever is greater, at 5V and +25°C. The DS1110 reproduces the input logic state at the tap 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1110 is designed to produce both leading- and trailing-edge delays with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs.

Applications

Communications Equipment

Medical Devices

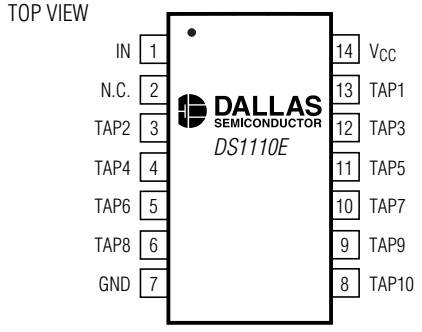
Automated Test Equipment

PC Peripheral Devices

Features

- **All-Silicon, 5V, 10-Tap Delay Line**
- **Improved, Drop-In Replacement for the DS1010**
- **10 Taps Equally Spaced**
- **Delays are Stable and Precise**
- **Leading- and Trailing-Edge Accuracy**
- **Delay Tolerance ±5% or ±2ns, whichever is Greater, at 5V and +25°C**
- **Economical**
- **Auto-Insertable, Low Profile**
- **Low-Power CMOS**
- **TTL/CMOS Compatible**
- **Vapor Phase, IR, and Wave Solderable**
- **Fast-Turn Prototypes**
- **Delays Specified Over Commercial and Industrial Temperature Ranges**
- **Custom Delays Available**
- **Standard 16-Pin SO or 14-Pin TSSOP**

Pin Configurations



TSSOP

Pin Configurations continued at end of data sheet.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1110E-XXX	-40°C to +85°C	14 TSSOP
DS1110S-XXX	-40°C to +85°C	16 SO

Selector Guide appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

10-Tap Silicon Delay Line

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground .....-0.5V to +6.0V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....See IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	4.75	5.0	5.25	V
High-Level Input Voltage	V_{IH}	(Note 1)	2.4		V_{CC} + 0.3	V
Low-Level Input Voltage	V_{IL}	(Note 1)	-0.3		+0.8	V
Input Leakage Current	I_I	$0V \le V_I \le V_{CC}$	-1.0		+1.0	µA
Active Current	I_{CC}	V_{CC} = max, period = min (Note 2)		40	150	mA
High-Level Output Current	I_{OH}	V_{CC} = min, V_{OH} = 2.3V			-1.0	mA
Low-Level Output Current	I_{OL}	V_{CC} = min, V_{OL} = 0.5V	12			mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pulse Width	t_{WI}	(Note 6)	10% of tap 10			ns
Input-to-Tap Delay (Delays ≤ 40ns)	t_{PLH} t_{PHL}	+25°C, 5.0V (Notes 3, 5, 6, 7, 9)	-2	Table 1	+2	ns
		0°C to +70°C (Notes 4–7)	-3	Table 1	+3	
		-40°C to +85°C (Notes 4–7)	-4	Table 1	+4	
Input-to-Tap Delay (Delays > 40ns)	t_{PLH} t_{PHL}	+25°C, 5.0V (Notes 3, 5, 6, 7, 9)	-5	Table 1	+5	%
		0°C to +70°C (Notes 4–7)	-8	Table 1	+8	
		-40°C to +85°C (Notes 4–7)	-13	Table 1	+13	
Power-Up Time	t_{PU}				200	ms
Input Period	Period	(Note 8)	2 (t_{WI}) or 20, whichever is greater			ns

CAPACITANCE

(T_A = +25°C.)

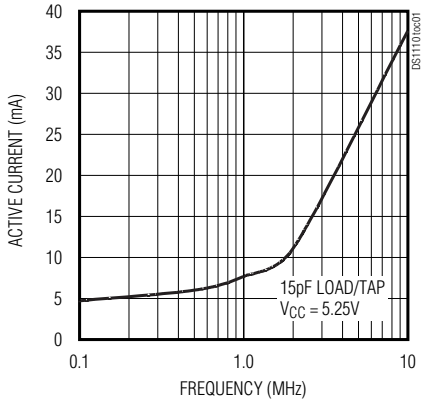
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}			5	10	pF

Note 1: All voltages are referenced to ground.
Note 2: Measured with outputs open.
Note 3: Initial tolerances are ± with respect to the nominal value at +25°C and V_{CC} = 5.0V for both leading and trailing edges.
Note 4: Temperature and voltage tolerances are with respect to the actual delay measured over stated temperature range and a 4.75V to 5.25V range.
Note 5: Intermediate delay values are available on a custom basis.
Note 6: See *Test Conditions* section.
Note 7: All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if tap 1 slows down, all other taps also slow down; tap 3 can never be faster than tap 2.
Note 8: Pulse width and period specifications may be exceeded; however, accuracy is application sensitive (decoupling, layout, etc.)
Note 9: For Tap 1 delays greater than 20ns, the tolerance is ±3ns or ±5%, whichever is greater.

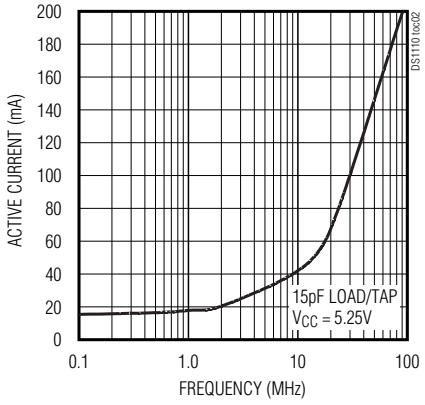
Typical Operating Characteristics

(V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

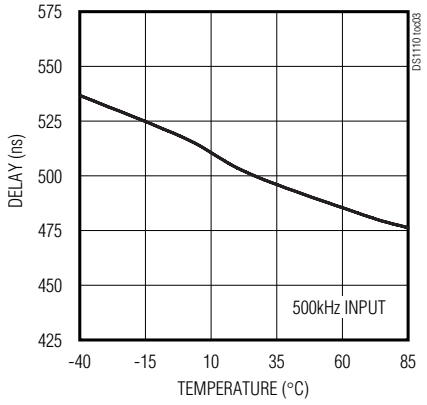
DS1110-500 ACTIVE CURRENT vs. INPUT FREQUENCY



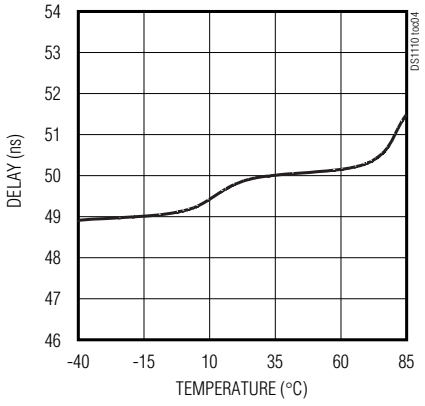
DS1110-50 ACTIVE CURRENT vs. INPUT FREQUENCY



DS1110-500 TAP 10 DELAY vs. TEMPERATURE



DS1110-50 TAP 10 DELAY vs. TEMPERATURE

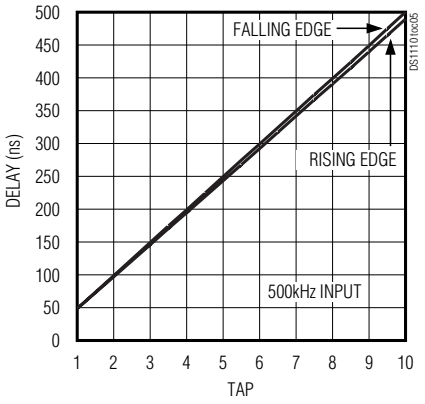


10-Tap Silicon Delay Line

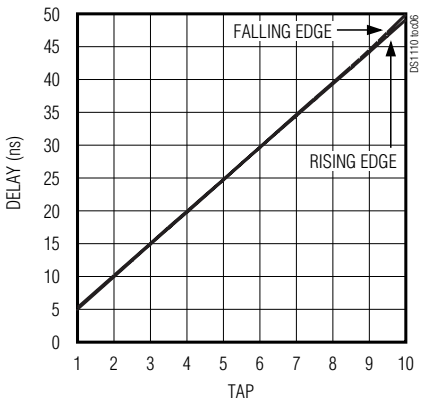
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

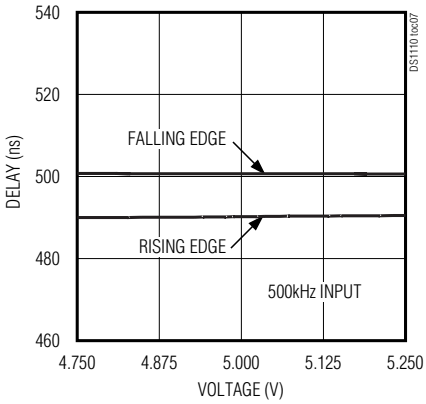
DS1110-500 DELAY vs. TAP



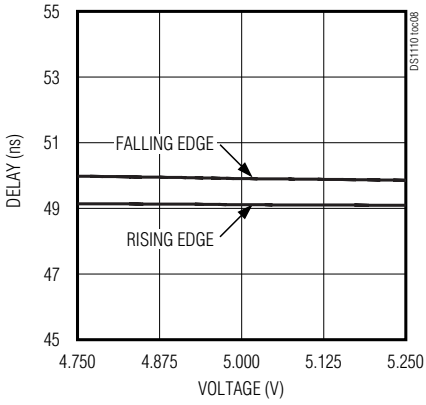
DS1110-50 DELAY vs. TAP



DS1110-500 TAP 10 DELAY vs. VOLTAGE



DS1110-50 TAP 10 DELAY vs. VOLTAGE



Pin Description

PIN		NAME	FUNCTION
TSSOP	SO		
1	1	IN	Input
2	2, 3, 15	N.C.	No Connection
7	8	GND	Ground
13, 3, 12, 4, 11, 5, 10, 6, 9, 8	14, 4, 13, 5, 12, 6, 11, 7, 10, 9	Tap 1–Tap 10	Tap Output Number
14	16	V_{CC}	5.0V

Detailed Description

The DS1110 delay line is an improved replacement for the DS1010. It has ten equally spaced taps providing delays from 5ns to 500ns. The devices are offered in a standard 16-pin SO or 14-pin TSSOP. The DS1110 series delay lines provide a nominal accuracy of ±5% or ±2ns, whichever is greater, at 5V and +25°C. The DS1110 reproduces the input logic state at the tap 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1110 is designed to produce both leading- and trailing-edge delays with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests call 972-371-4348.

Table 1. Part Number by Delay (t_{PHL}, t_{PLH})

PART	TOTAL DELAY* (ns)	DELAY/TAP (ns)
DS1110-50	50	5
DS1110-60	60	6
DS1110-75	75	7.5
DS1110-80	80	8
DS1110-100	100	10
DS1110-125	125	12.5
DS1110-150	150	15
DS1110-175	175	17.5
DS1110-200	200	20
DS1110-250	250	25
DS1110-300	300	30
DS1110-350	350	35
DS1110-400	400	40
DS1110-450	450	45
DS1110-500	500	50

**Custom delays are available.*

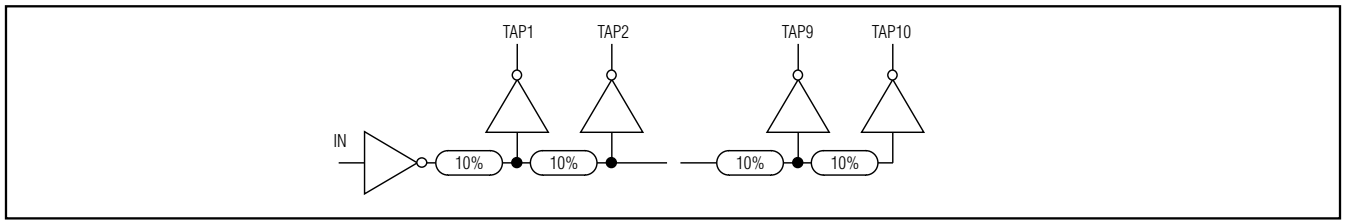


Figure 1. Logic Diagram

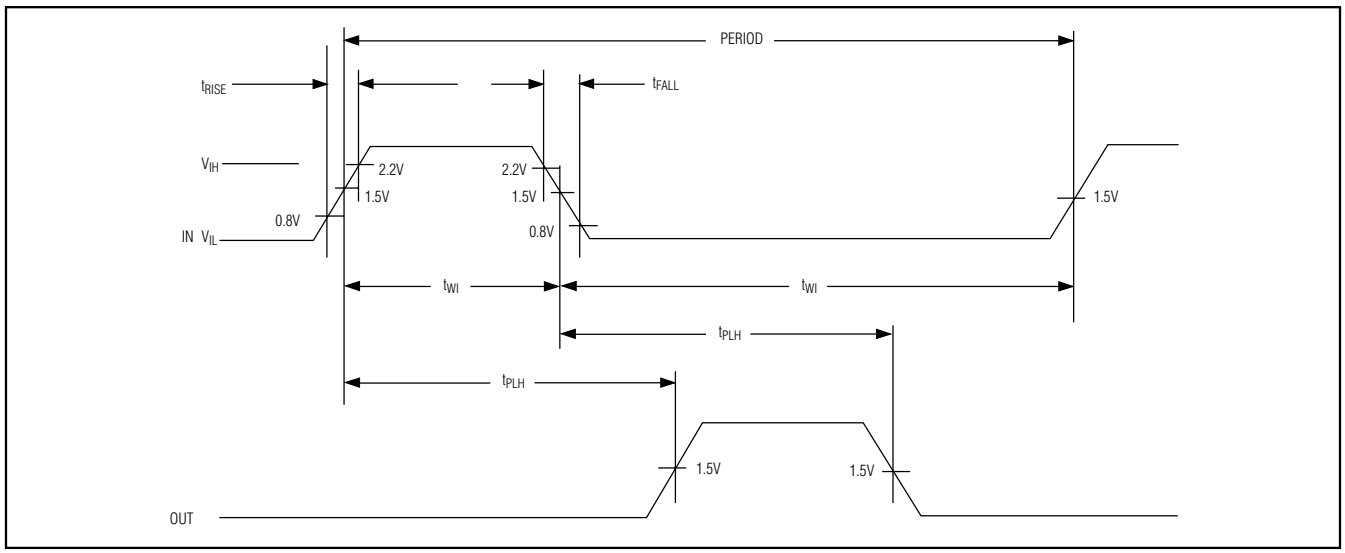


Figure 2. Timing Diagram: Silicon Delay Line

10-Tap Silicon Delay Line

Terminology

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

Test Setup Description

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1110. A precision pulse generator under software control produces the input waveform. Time delays are measured by a time interval counter (20ps resolution) connected

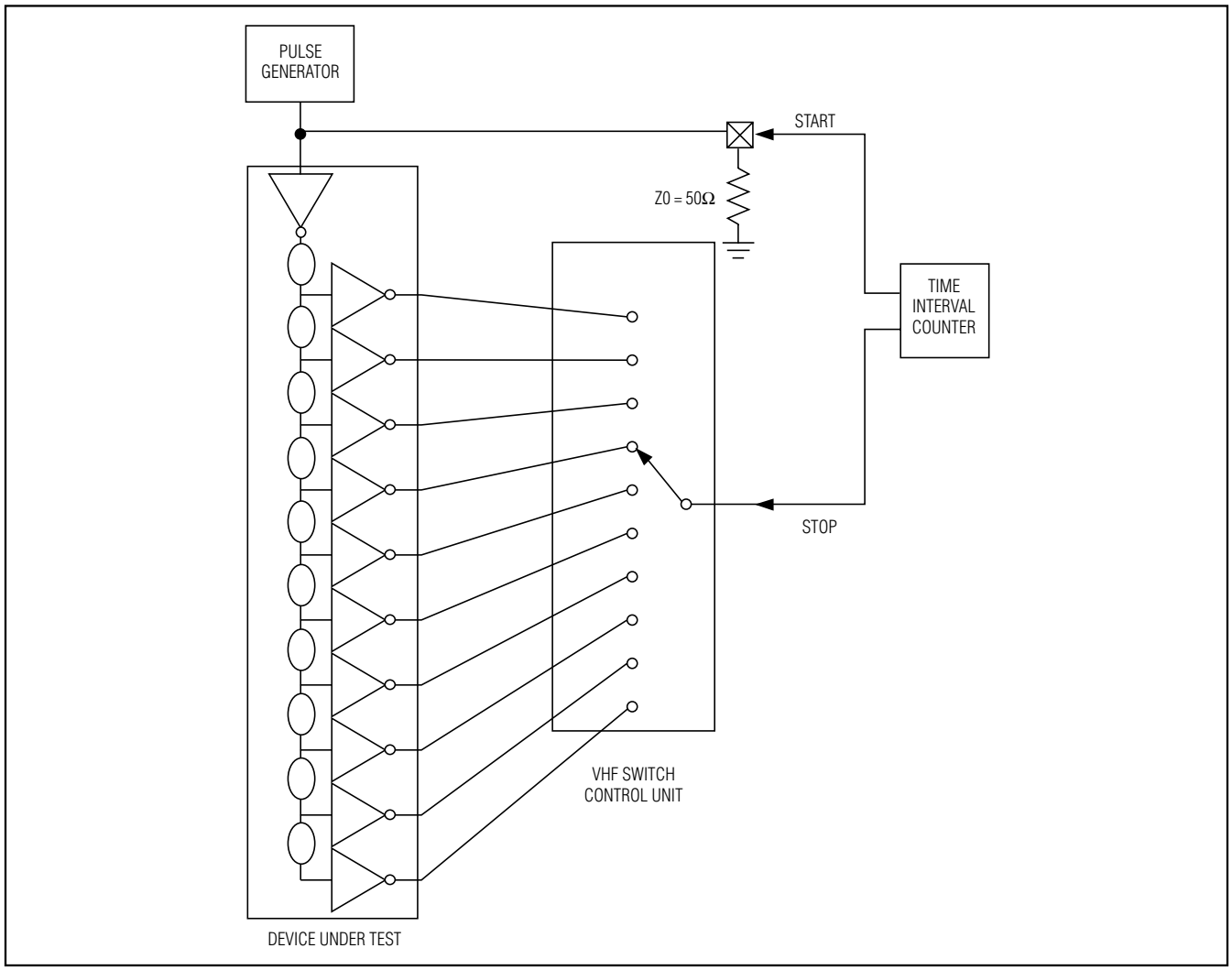


Figure 3. Test Circuit

between the input and each tap. Each tap is selected and connected to the counter by a VHF switch-control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE-488 bus.

Output

Each output is loaded with the equivalent of one 74FO4 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

Chip Information

TRANSISTOR COUNT: 6813

Table 2. Test Conditions

INPUT	CONDITION
Ambient Temperature	+25°C ±3°C
Supply Voltage (V_{CC})	5.0V ±0.1V
Input Pulse	High = 3.0V ±0.1V
	Low = 0.0V ±0.1V
Source Impedance	50Ω max
Rise and Fall Time	3ns max
Pulse Width	500ns (1µs for -500ns)
Period	1µs (2µs for -500ns)

Note: *The above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.*

Selector Guide

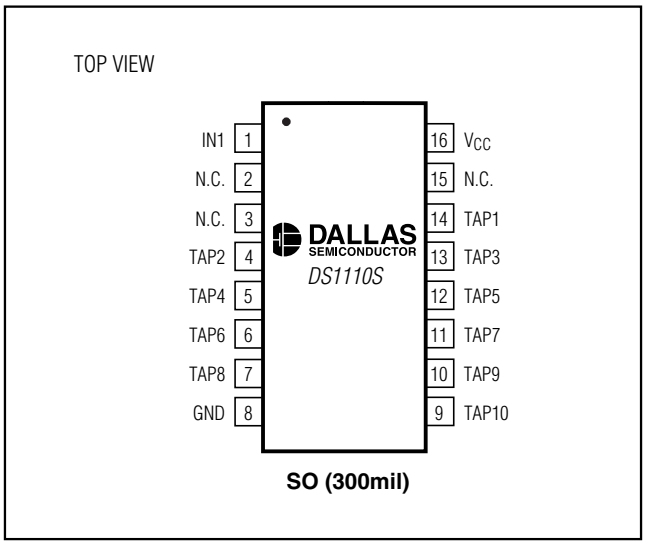
PART	TEMP RANGE	PIN-PACKAGE	TOTAL DELAY (ns)*
DS1110E-50	-40°C to +85°C	14 TSSOP	50
DS1110E-60	-40°C to +85°C	14 TSSOP	60
DS1110E-75	-40°C to +85°C	14 TSSOP	75
DS1110E-80	-40°C to +85°C	14 TSSOP	80
DS1110E-100	-40°C to +85°C	14 TSSOP	100
DS1110E-125	-40°C to +85°C	14 TSSOP	125
DS1110E-150	-40°C to +85°C	14 TSSOP	150
DS1110E-175	-40°C to +85°C	14 TSSOP	175
DS1110E-200	-40°C to +85°C	14 TSSOP	200
DS1110E-250	-40°C to +85°C	14 TSSOP	250
DS1110E-300	-40°C to +85°C	14 TSSOP	300
DS1110E-350	-40°C to +85°C	14 TSSOP	350
DS1110E-400	-40°C to +85°C	14 TSSOP	400
DS1110E-450	-40°C to +85°C	14 TSSOP	450
DS1110E-500	-40°C to +85°C	14 TSSOP	500

PART	TEMP RANGE	PIN-PACKAGE	TOTAL DELAY (ns)*
DS1110S-50	-40°C to +85°C	16 SO	50
DS1110S-60	-40°C to +85°C	16 SO	60
DS1110S-75	-40°C to +85°C	16 SO	75
DS1110S-80	-40°C to +85°C	16 SO	80
DS1110S-100	-40°C to +85°C	16 SO	100
DS1110S-125	-40°C to +85°C	16 SO	125
DS1110S-150	-40°C to +85°C	16 SO	150
DS1110S-175	-40°C to +85°C	16 SO	175
DS1110S-200	-40°C to +85°C	16 SO	200
DS1110S-250	-40°C to +85°C	16 SO	250
DS1110S-300	-40°C to +85°C	16 SO	300
DS1110S-350	-40°C to +85°C	16 SO	350
DS1110S-400	-40°C to +85°C	16 SO	400
DS1110S-450	-40°C to +85°C	16 SO	450
DS1110S-500	-40°C to +85°C	16 SO	500

**Custom delays are available.*

10-Tap Silicon Delay Line

Pin Configurations (continued)



SO (300mil)

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

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