19-5593; Rev 10/10

DS1330Y/AB
256k Nonvolatile SRAM with Battery Monitor

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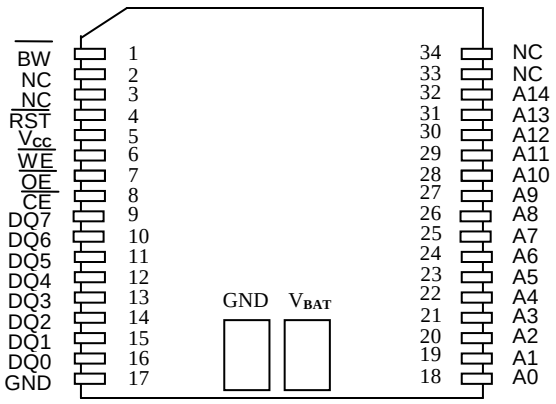
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Power supply monitor resets processor when V_{CC} power loss occurs and holds processor in reset during V_{CC} ramp-up
- Battery monitor checks remaining capacity daily
- Read and write access times of 70ns
- Unlimited write cycle endurance
- Typical standby current 50µA
- Upgrade for 32k x 8 SRAM, EEPROM or Flash
- Lithium battery is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1330Y) or optional ±5% V_{CC} operating range (DS1330AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND
- PowerCap Module (PCM) package
  - Directly surface-mountable module
  - Replaceable snap-on PowerCap provides lithium backup battery
  - Standardized pinout for all nonvolatile (NV) SRAM products
  - Detachment feature on PowerCap allows easy removal using a regular screwdriver

PIN ASSIGNMENT



34-Pin POWERCAP MODULE (PCM)
(Uses DS9034PC+ or DS9034PCI+ PowerCap)

PIN DESCRIPTION

A0 – A14	- Address Inputs
DQ0 – DQ7	- Data In/Data Out
$\overline{CE}$	- Chip Enable
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
$\overline{RST}$	- Reset Output
$\overline{BW}$	- Battery Warning
V_{CC}	- Power (+5V)
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS1330 256k NV SRAMs are 262,144-bit, fully static, NV SRAMs organized as 32,768 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. Additionally, the DS1330 devices have dedicated circuitry for monitoring the status of V_{CC} and the status of the internal lithium battery. DS1330 devices in the PowerCap module package are directly surface mountable and are normally paired with a DS9034PC PowerCap to form a complete NV SRAM module. The devices can be used in place of 32k x 8 SRAM, EEPROM, or Flash components.

READ MODE

The DS1330 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 15 address inputs ($A_0 - A_{14}$) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1330 devices execute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later-occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1330AB provides full-functional capability for V_{CC} greater than 4.75V and write protects by 4.5V. The DS1330Y provides full-functional capability for V_{CC} greater than 4.5V and write protects by 4.25V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The NV SRAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high-impedance. As V_{CC} falls below approximately 2.7V, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 2.7V, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75V for the DS1330AB and 4.5V for the DS1330Y.

SYSTEM POWER MONITORING

DS1330 devices have the ability to monitor the external V_{CC} power supply. When an out-of-tolerance power supply condition is detected, the NV SRAMs warn a processor-based system of impending power failure by asserting $\overline{RST}$. On power-up, $\overline{RST}$ is held active for 200ms nominal to prevent system operation during power-on transients and to allow t_{REC} to elapse. $\overline{RST}$ has an open drain output driver.

BATTERY MONITORING

The DS1330 devices automatically perform periodic battery voltage monitoring on a 24-hour time interval. Such monitoring begins within t_{REC} after V_{CC} rises above V_{TP} and is suspended when power failure occurs.

After each 24-hour period has elapsed, the battery is connected to an internal 1MΩ test resistor for one second. During this one second, if battery voltage falls below the battery voltage trip point (2.6V), the battery warning output $\overline{BW}$ is asserted. Once asserted, $\overline{BW}$ remains active until the module is replaced. The battery is still retested after each V_{CC} power-up, however, even if $\overline{BW}$ is active. If the battery voltage is found to be higher than 2.6V during such testing, $\overline{BW}$ is de-asserted and regular 24-hour testing resumes. $\overline{BW}$ has an open drain output driver.

PACKAGES

The 34-pin PowerCap module integrates SRAM memory and NV control along with contacts for connection to the lithium battery in the DS9034PC PowerCap. The PowerCap module package design allows a DS1330 PCM device to be surface mounted without subjecting its lithium backup battery to destructive high-temperature reflow soldering. After a DS1330 PCM is reflow soldered, a DS9034PC is snapped on top of the PCM to form a complete NV SRAM module. The DS9034PC is keyed to prevent improper attachment. DS1330 PowerCap modules and DS9034PC PowerCaps are ordered separately and shipped in separate containers. See the DS9034PC data sheet for further information.

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature Range	
Commercial:	0°C to +70°C
Industrial:	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+260°C
Soldering Temperature (reflow)	+260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1330AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1330Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5% for DS1330AB)

(T_A: See Note 10) (V_{CC} = 5V ± 10% for DS1330Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	14
Output Current @ 0.4V	I_{OL}	2.0			mA	14
Standby Current $\overline{CE}$ =2.2V	I_{CCS1}		200	600	µA	
Standby Current $\overline{CE}$ =V_{CC}-0.5V	I_{CCS2}		50	150	µA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1330AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1330Y)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(T_A = +25°C)

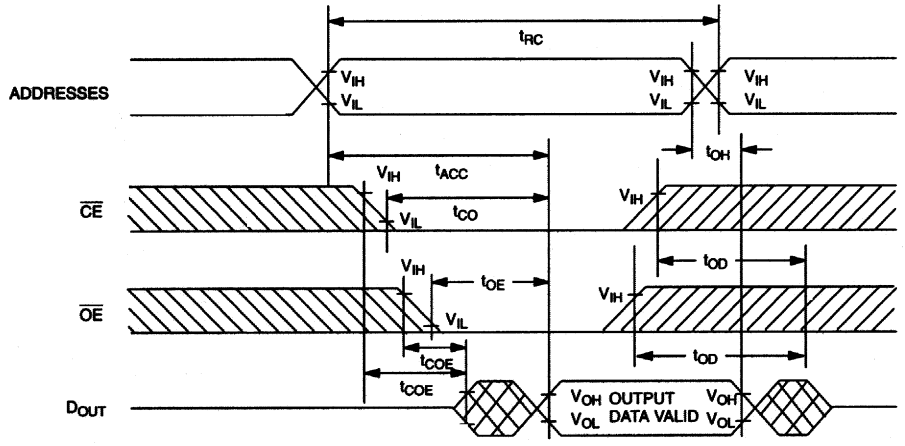
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 5% for DS1330AB)
(T_A: See Note 10) (V_{CC} = 5V ± 10% for DS1330Y)

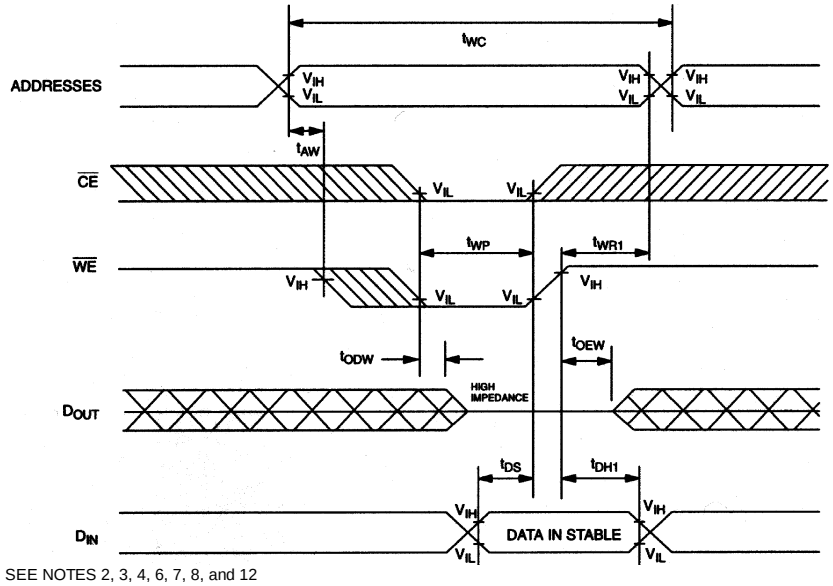
PARAMETER	SYMBOL	DS1330AB-70 DS1330Y-70		UNITS	NOTES
		MIN	MAX		
Read Cycle Time	t_{RC}	70		ns	
Access Time	t_{ACC}		70	ns	
$\overline{OE}$ to Output Valid	t_{OE}		45	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		ns	5
Output High Z from Deselection	t_{OD}		25	ns	5
Output Hold from Address Change	t_{OH}	5		ns	
Write Cycle Time	t_{WC}	70		ns	
Write Pulse Width	t_{WP}	55		ns	3
Address Setup Time	t_{AW}	0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 12		ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		25	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		ns	5
Data Setup Time	t_{DS}	30		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 7		ns	12 13

READ CYCLE



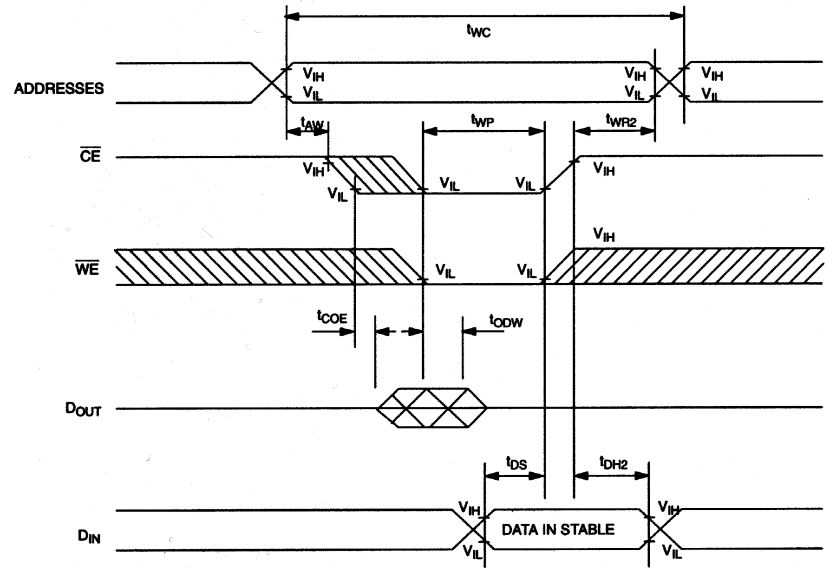
SEE NOTE 1

WRITE CYCLE 1



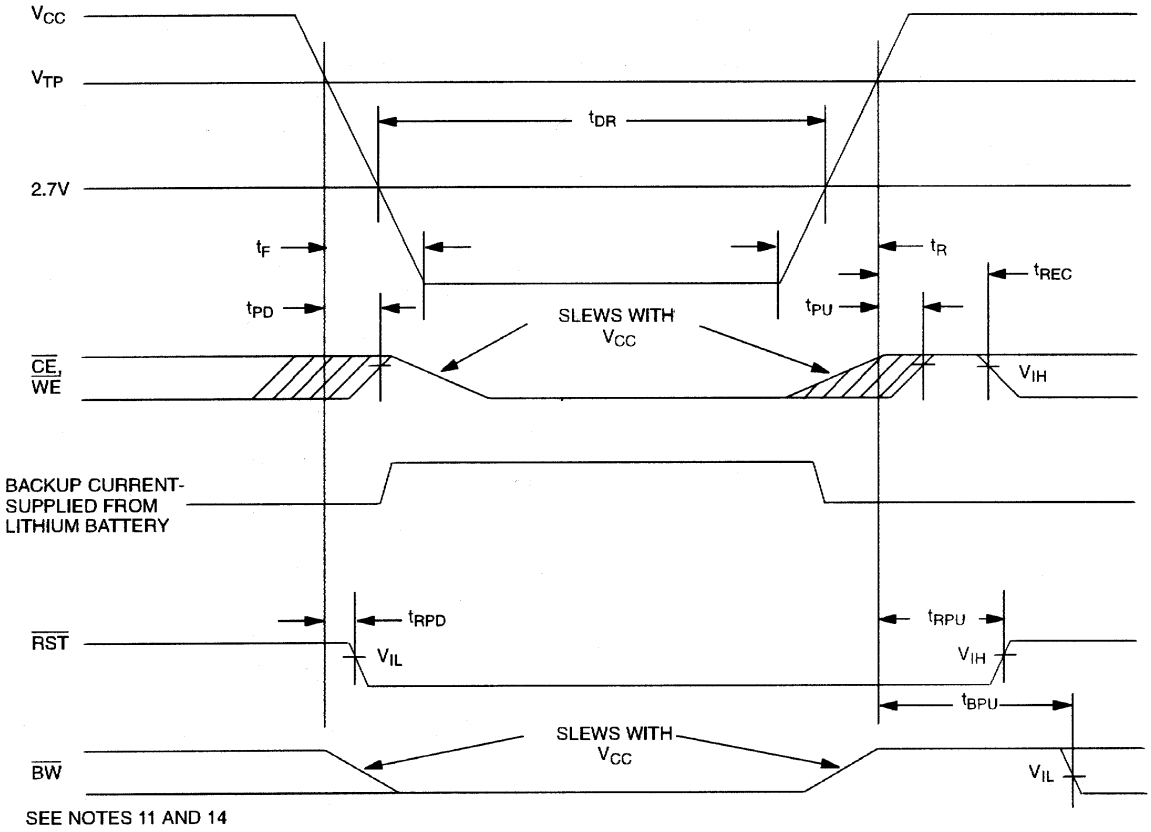
SEE NOTES 2, 3, 4, 6, 7, 8, and 12

WRITE CYCLE 2



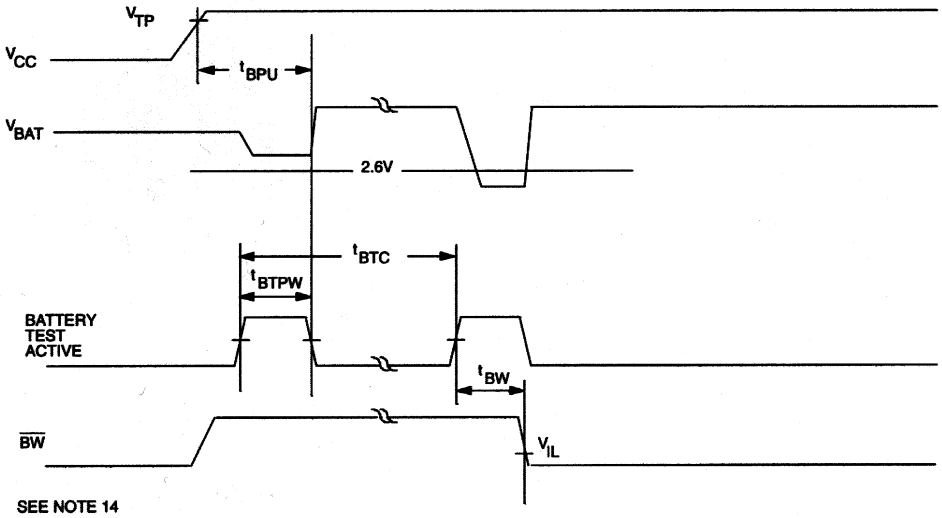
SEE NOTES 2, 3, 4, 6, 7, 8, and 13

POWER-DOWN/POWER-UP CONDITION



SEE NOTES 11 AND 14

BATTERY WARNING DETECTION



SEE NOTE 14

POWER-DOWN/POWER-UP TIMING

(T_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PD}			1.5	µs	11
V_{CC} slew from V_{TP} to 0V	t_F	150			µs	
V_{CC} Fail Detect to $\overline{RST}$ Active	t_{RPD}			15	µs	14
V_{CC} slew from 0V to V_{TP}	t_R	150			µs	
V_{CC} Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	
V_{CC} Valid to $\overline{RST}$ Inactive	t_{RPU}	150	200	350	ms	14
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	s	14

BATTERY WARNING TIMING

(T_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test Cycle	t_{BTC}		24		hr	
Battery Test Pulse Width	t_{BTPW}			1	s	
Battery Test to $\overline{BW}$ Active	t_{BW}			1	s	

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high-impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high-impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.

9. Each DS1330 has a built-in switch that disconnects the lithium source until the user first applies V_{CC}. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user. This parameter is assured by component selection, process control, and design. It is not measured directly during production testing.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to +70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power-down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1} and t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2} and t_{DH2} are measured from $\overline{CE}$ going high.
14. $\overline{RST}$ and $\overline{BW}$ are open drain outputs and cannot source current. External pull-up resistors should be connected to these pins for proper operation. Both pins will sink 10mA.
15. DS1330 modules are recognized by Underwriters Laboratories (UL) under file E99151.

DC TEST CONDITIONS

Outputs Open
Cycle = 200ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 – 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5ns

ORDERING INFORMATION

PART	TEMP RANGE	SUPPLY TOLERANCE	PIN-PACKAGE
DS1330ABP-70+	0°C to +70°C	5V ± 5%	34 PCAP*
DS1330ABP-70IND+	-40°C to +85°C	5V ± 5%	34 PCAP*
DS1330YP-70+	0°C to +70°C	5V ± 10%	34 PCAP*
DS1330YP-70IND+	-40°C to +85°C	5V ± 10%	34 PCAP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**DS9034PC+ or DS9034PCI+ (PowerCap) required. Must be ordered separately.*

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
34 PCAP	PC2+4	**21-0246**	—

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
10/10	Updated the storage, lead, and soldering information in the *Absolute Maximum Ratings* section, removed the unused AC timing specs in the *AC Electrical Characteristics* table, updated the *Ordering Information* table, replaced the package outline drawing with the *Package Information* table	1, 4, 5, 9