DS1672
I²C 32-Bit Binary Counter RTC

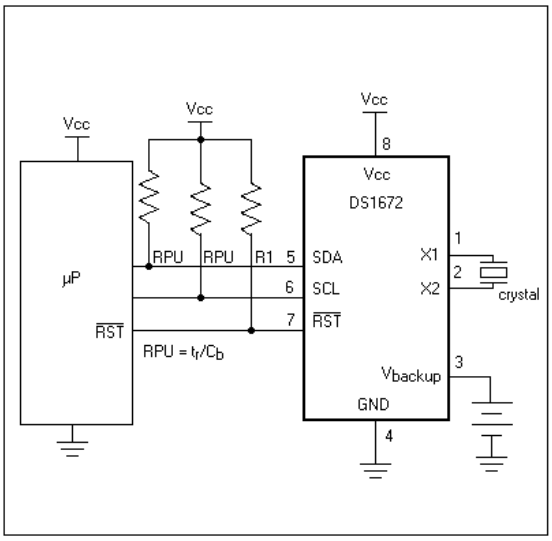
GENERAL DESCRIPTION

The DS1672 incorporates a 32-bit counter and power-monitoring functions. The 32-bit counter is designed to count seconds and can be used to derive time-of-day, week, month, month, and year by using a software algorithm. A precision, temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power-fail signal is generated that forces the reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for a period of time to allow the power supply and processor to stabilize.

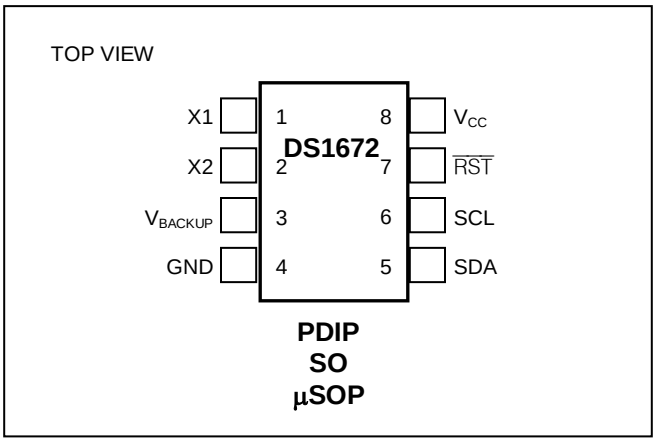
FEATURES

- 32-Bit Counter
- I^2C Serial Interface
- Automatic Power-Fail Detect and Switch Circuitry
- Power-Fail Reset Output
- Low-Voltage Oscillator Operation (1.3V min)
- Trickle-Charge Capability
- Underwriters Laboratories (UL) Recognized
- -40°C to +85°C Operating Range

TYPICAL OPERATING CIRCUIT



PIN CONFIGURATION



.

ORDERING INFORMATION

PART	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK*
DS1672-2+	-40°C to +85°C	2.0	8 PDIP (300 mils)	DS1672-2
DS1672-3+	-40°C to +85°C	3.0	8 PDIP (300 mils)	DS1672-3
DS1672-33+	-40°C to +85°C	3.3	8 PDIP (300 mils)	DS1672-33
DS1672S-2+	-40°C to +85°C	2.0	8 SO (150 mils)	D1672-2
DS1672S-3+	-40°C to +85°C	3.0	8 SO (150 mils)	D1672-3
DS1672S-33+	-40°C to +85°C	3.3	8 SO (150 mils)	D167233
DS1672S-3+T&R	-40°C to +85°C	3.0	8 SO (150 mils)/Tape and Reel	D1672-3
DS1672S-33+T&R	-40°C to +85°C	3.3	8 SO (150 mils)/Tape and Reel	D167233
DS1672U-2+	-40°C to +85°C	2.0	8 µSOP(3mm)	1672 rr -2
DS1672U-3+	-40°C to +85°C	3.0	8 µSOP(3mm)	1672 rr -3
DS1672U-33+	-40°C to +85°C	3.3	8 µSOP(3mm)	1672 rr -33
DS1672U-33+T&R	-40°C to +85°C	3.3	8 µSOP(3mm)/Tape and Reel	1672 rr -33

+ Denotes a lead-free/RoHS-compliant device.
** A "+" anywhere on the top mark denotes a lead-free device. rr = 2-digit alphanumeric revision code.*

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.5V to +6.0V
Operating Temperature Range (noncondensing) ...……-40°C to +85°C
Storage Temperature Range…….-55°C to +125°C
Soldering Temperature (reflow)…….……. +260°C
Lead Temperature (soldering, 10s) …….. +260°C

This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C) (Note 1)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	DS1672-2	V_{CC}	1.8	2.0	5.5	V
	DS1672-3	V_{CC}	2.7	3.0	5.5	
	DS1672-33	V_{CC}	2.97	3.3	5.5	
Logic 1		V_{IH}	0.7 x V_{CC}		V_{CC} + 0.5	V
Logic 0		V_{IL}	-0.5		+0.3 x V_{CC}	V
Backup Supply Voltage		V_{BACKUP}	1.3	3.0	3.63	V

Note 1: All voltages referenced to ground.

DC ELECTRICAL CHARACTERISTICS

(V_{CCMIN} < V_{CC} < V_{CCMAX}, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Supply Current (Note 2)	I_{CCA}	-2: V_{CC} = 2.2V			600	µA
		-3: V_{CC} = 3.3V				
		-33: V_{CC} = 3.63V				
Standby Current (Note 3)	I_{CCS}	-2: V_{CC} = 2.2V			500	µA
		-3: V_{CC} = 3.3V				
		-33: V_{CC} = 3.63V				
Power-Fail Voltage	V_{PF}	-2:	2.70	2.88	2.97	V
		-3:	2.45	2.60	2.70	
		-33:	1.58	1.70	1.80	
V_{BACKUP} Leakage Current	$I_{BACKUPLKG}$			25	50	nA
Logic 0 Output (Note 4)	I_{OL}	V_{OL} = 0.4V			3	mA
Logic 0 Output (Note 4, DS1672-2 Only)	I_{OL}	V_{CC} > 2V; V_{OL} = 0.4V			3	mA
		V_{CC} < 2V; V_{OL} = V_{CC} * 0.2				

Note 1: All voltages referenced to ground.

Note 2: I_{CCA} specified with SCL clocking at max frequency (400kHz), trickle charger disabled.

Note 3: I_{CCS} specified with V_{CC} = V_{CCTYP} and SDA, SCL = V_{CCTYP}, trickle charger disabled.

Note 4: SDA and $\overline{RST}$.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 0V, T_A = -40°C to +85°C.) (Note 5)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{BACKUP} Current (Oscillator On)	$I_{BACKUPOSC}$		0.425	1	µA
V_{BACKUP} Current (Oscillator Off)	I_{BACKUP}			200	nA

Note 5: Using the recommended crystal on X1 and X2.

CRYSTAL SPECIFICATIONS*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			45	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications*

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 0V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode			100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 6)	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
HIGH Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time (Notes 7, 8)	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time (Note 9)	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals (Note 10)	t_R	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode			1000	
Fall Time of Both SDA and SCL Signals (Note 10)	t_F	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode			300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load for Each Bus Line (Note 10)	C_B				400	pF
I/O Capacitance	$C_{I/O}$			10		pF

Note 6: After this period, the first clock pulse is generated.

Note 7: A device must internally provide a hold time of at least 300ns for the SDA signal (referenced to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

Note 8: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 9: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

Note 10: C_B–Total capacitance of one bus line in pF.

POWER-UP/POWER-DOWN CHARACTERISTICS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{CC} Detect to $\overline{RST}$ (V_{CC} Falling)	t_{RPD}			10	µs
V_{CC} Detect to $\overline{RST}$ (V_{CC} Rising) (Note 11)	t_{RPU}		250		ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs

Note 11: If the $\overline{EOSC}$ bit in the control register is set to logic 1, t_{RPU} is equal to 250ms plus the startup time of the crystal oscillator.

Warning: Negative undershoots below –0.3V while the part is in battery-backed mode can cause loss of data.

Figure 1. Timing Diagram

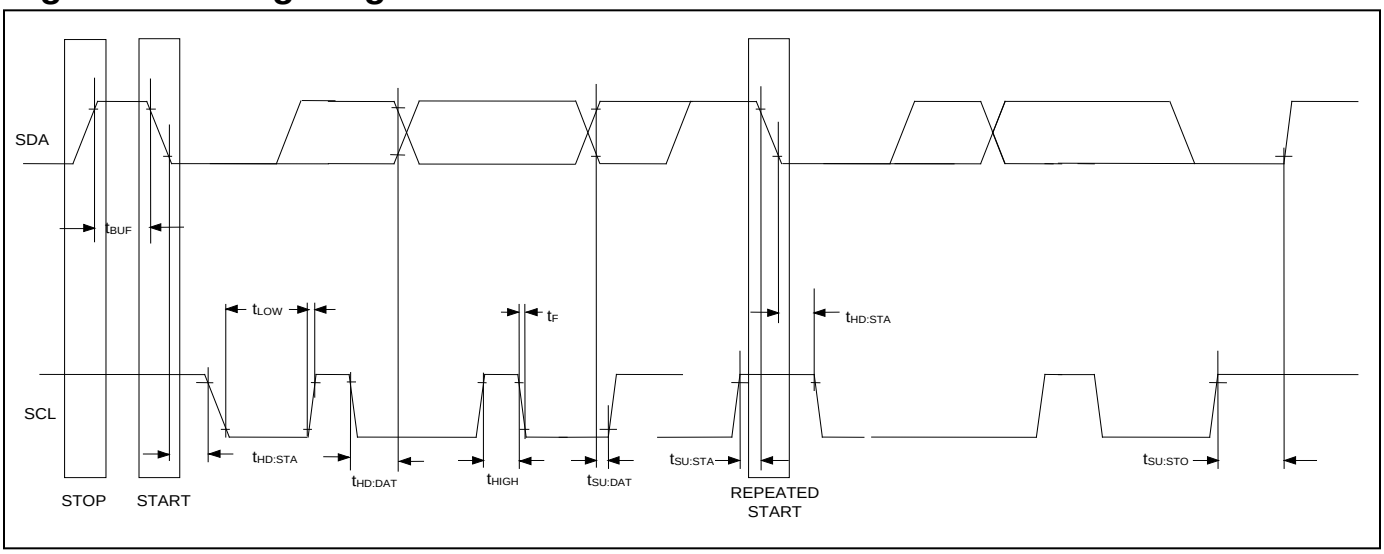
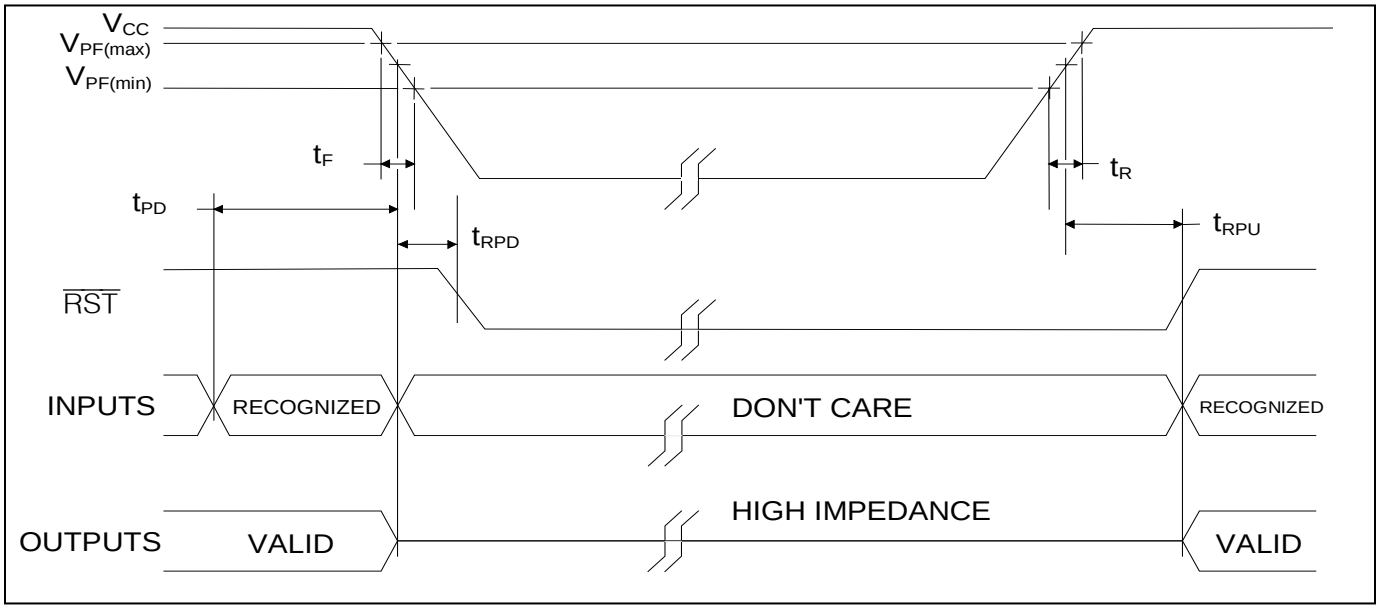


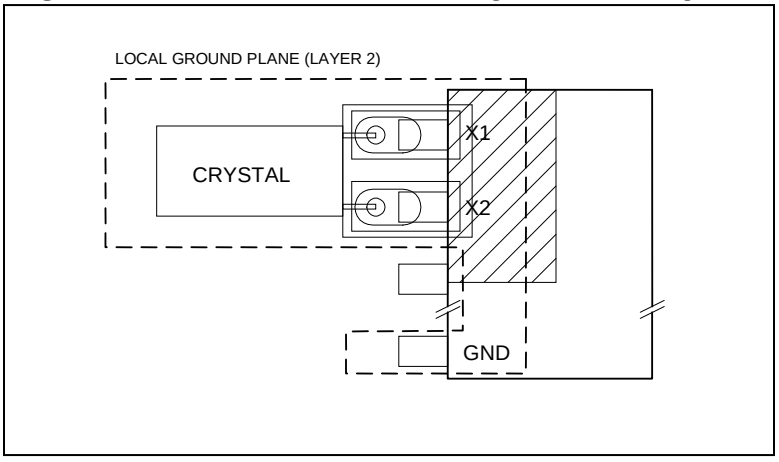
Figure 2. Power-Up/Power-Down Timing



PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	X1, X2	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6pF. For more information about crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks.* The DS1672 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left unconnected.
3	V_{BACKUP}	Battery Input for Any Standard 3V Lithium Cell or Other Energy Source. Battery voltage must be held between 1.3V and 3.63V for proper operation. Diodes placed in series between the power source and the V_{BACKUP} pin may result in improper operation. If a backup supply is not required, V_{BACKUP} must be grounded. UL recognized to ensure against reverse charging current when used in conjunction with a lithium battery (charger disabled). See "Conditions of Acceptability" at www.maxim-ic.com/qa/info/ul.
4	GND	Ground.
5	SDA	Serial-Data Input/Output. SDA is the input/output pin for the I^2C serial interface. The SDA pin is open drain and requires an external pullup resistor.
6	SCL	I^2C Serial-Clock Input. SCL is used to synchronize data movement on the serial interface and requires an external pullup resistor.
7	$\overline{RST}$	Active-Low Reset Output. It functions as a microprocessor reset signal. This pin is an open-drain output and requires an external pullup resistor.
8	V_{CC}	Power pin for Primary Power Supply. When V_{CC} is applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below V_{PF}, reads and writes are inhibited.

Figure 3. Recommended Layout for Crystal

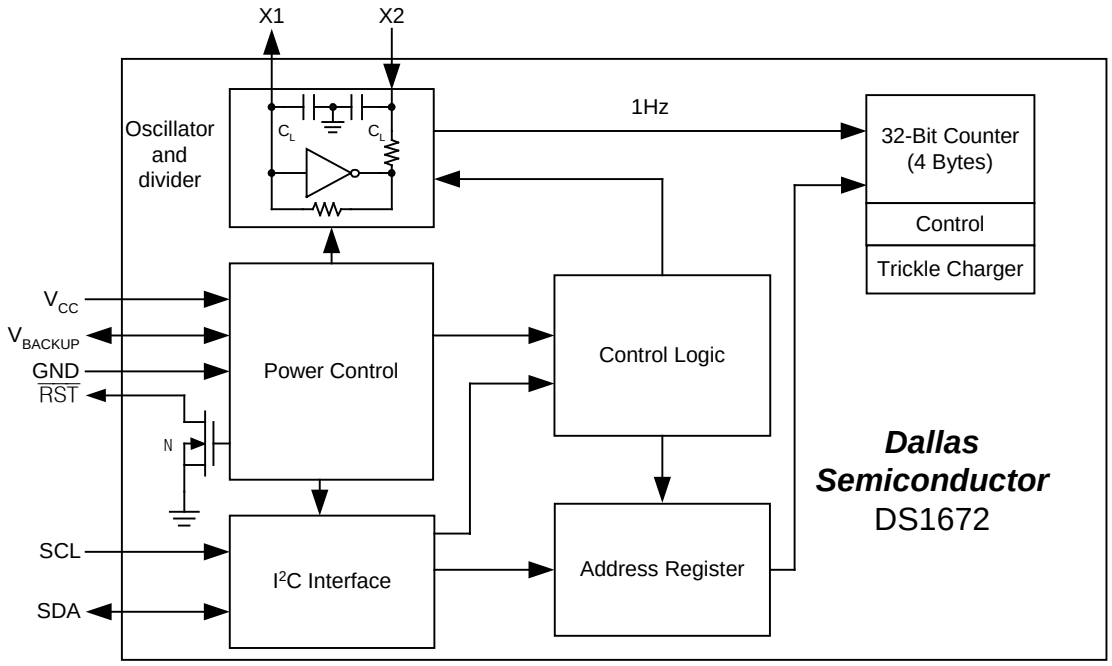


Detailed Description

The DS1672 provides a 32-bit counter that increments once-per-second. The counter data is accessible via an I^2C serial interface. A precision, temperature-compensated, voltage reference and comparator circuit monitors V_{CC}. When V_{CC} drops below V_{PF}, $\overline{RST}$ becomes active and the interface is disabled to prevent data corruption. The device switches to the backup supply input, which maintains oscillator and counter operation while V_{CC} is absent. When V_{CC} rises above V_{PF}, $\overline{RST}$ remains low for a period of time (t_{RPU}) to allow V_{CC} to stabilize.

The block diagram in Figure 4 shows the main elements of the DS1672. As shown, communications to and from the DS1672 occur serially over a I^2C, bidirectional bus. The DS1672 operates as a slave device on the I^2C bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed.

Figure 4. Block Diagram



Oscillator Circuit

The DS1672 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 4 shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Nominal Frequency	F_O		32.768		kHz	
Series Resistance	ESR			45	kΩ	
Load Capacitance	C_L		6		pF	

* The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58:

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was

trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. Refer to *Application Note 5: "Crystal Considerations with Dallas Real-Time Clocks"* for detailed information.

Address Map

The counter is accessed by reading or writing the first 4 bytes of the DS1672 (00h–03h). The control register and trickle charger are accessed by reading or writing the appropriate register bytes as illustrated in Table 2. If the master continues to send or request more data after the address pointer has reached 05h, the address pointer will wrap around to location 00h.

Table 2. Registers

ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0	FUNCTION
00h								LSB	Counter Byte 1
01h									Counter Byte 2
02h									Counter Byte 3
03h	MSB								Counter Byte 4
04h	$\overline{\text{EOSC}}$								Control
05h	TCS	TCS	TCS	TCS	DS	DS	RS	RS	Trickle Charger

Power Control

The device is fully accessible and data can be written and ready only when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, (point at which write protection occurs) the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. Oscillator and counter operation are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels (see Table 3).

Table 3. Power Control

SUPPLY CONDITION	READ/WRITE ACCESS	$\overline{\text{RST}}$	POWERED BY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKUP}$	No	Active	V_{BACKUP}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	Active	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	Inactive	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	Inactive	V_{CC}

Oscillator Control

The $\overline{\text{EOSC}}$ bit (bit 7 of the control register) controls the oscillator when in back-up mode. This bit when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped and the DS1672 is placed into a low-power standby mode (I_{BACKUP}) when in back-up mode. When the DS1672 is powered by $V_{CC,}$ the oscillator is always on regardless of the status of the $\overline{\text{EOSC}}$ bit; however, the counter is incremented only when $\overline{\text{EOSC}}$ is a logic 0.

Microprocessor Monitor

A temperature-compensated comparator circuit monitors the level of V_{CC}. When V_{CC} falls to the power-fail trip point, the $\overline{\text{RST}}$ signal (open drain) is pulled active, and read/write access is inhibited. When V_{CC} returns to nominal levels, the $\overline{\text{RST}}$ signal is kept in the active state for t_{RPU} (typically) to allow the power supply and microprocessor to stabilize. Note, however, that if the $\overline{\text{EOSC}}$ bit is set to a logic 1 (to disable the oscillator during write protection), the reset signal will be kept in an active state for t_{RPU} plus the startup time of the oscillator.

Trickle Charger

The trickle charger is controlled by the trickle charge register. The simplified schematic of Figure 5 shows the basic components of the trickle charger. The trickle charge select (TCS) bit (bits 4–7) controls the selection of the trickle charger. In order to prevent accidental enabling, only a pattern on 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The DS1672 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2, 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. If DS is 01, no diode is selected or if DS is 10, a diode is selected. The RS bits (bits 0, 1) select whether a resistor is connected between V_{CC} and V_{BACKUP} and what the value of the resistor is. The resistor selected by the resistor select (RS) bits and the diode selected by the diode select (DS) bits are as follows:

TCS	TCS	TCS	TCS	DS	DS	RS	RS	FUNCTION
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Initial default value--disabled

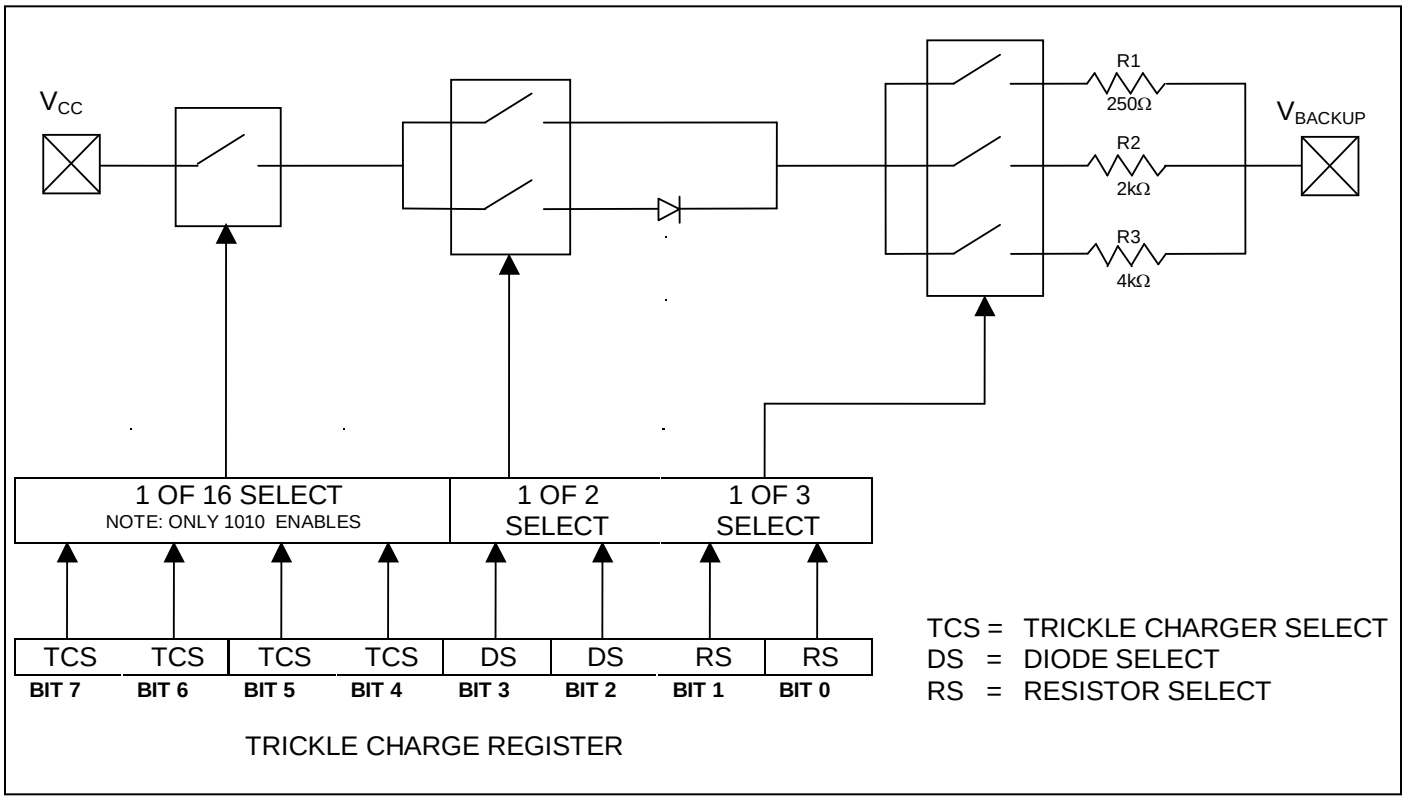
Warning: The resistor value of 250Ω must not be selected whenever V_{CC} is greater than 3.63V.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 3V is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would, therefore, be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.6V) / 2k\Omega \approx 2.2mA$$

As the super cap changes, the voltage drop between V_{CC} and V_{BACKUP} will decrease and, therefore, the charge current will decrease.

Figure 5. Programmable Trickle Charger



I²C Serial Data Bus

The DS1672 supports a bidirectional I²C bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1672 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS1672 operates in both modes.

The following bus protocol has been defined (Figure 6):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Stop data transfer: A change in the state of the data line from low to high, while the clock line is high, defines a STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the I^2C bus specifications a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figures 7 and 8 detail how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1672 can operate in the following two modes:

1) **Slave receiver mode (DS1672 write mode):** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (Figure 7). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1672 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which for a write is a 0. After receiving and decoding the slave address byte the DS1672 outputs an acknowledge on the SDA line. After the DS1672 acknowledges the slave address + write bit, the master transmits a word address to the DS1672. This will set the register pointer on the DS1672, with the DS1672 acknowledging the transfer. The master may then transmit zero or more bytes of data,

with the DS1672 acknowledging each byte received. The register pointer will increment after each byte is transferred. The master will generate a stop condition to terminate the data write.

2) **Slave transmitter mode (DS1672 read mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1672 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 8). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit DS1672 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which for a read is a 1. After receiving and decoding the slave address byte the DS1672 outputs an acknowledge on the SDA line. The DS1672 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1672 must receive a "not acknowledge" to end a read.

Figure 6. Data Transfer on I²C Serial Bus

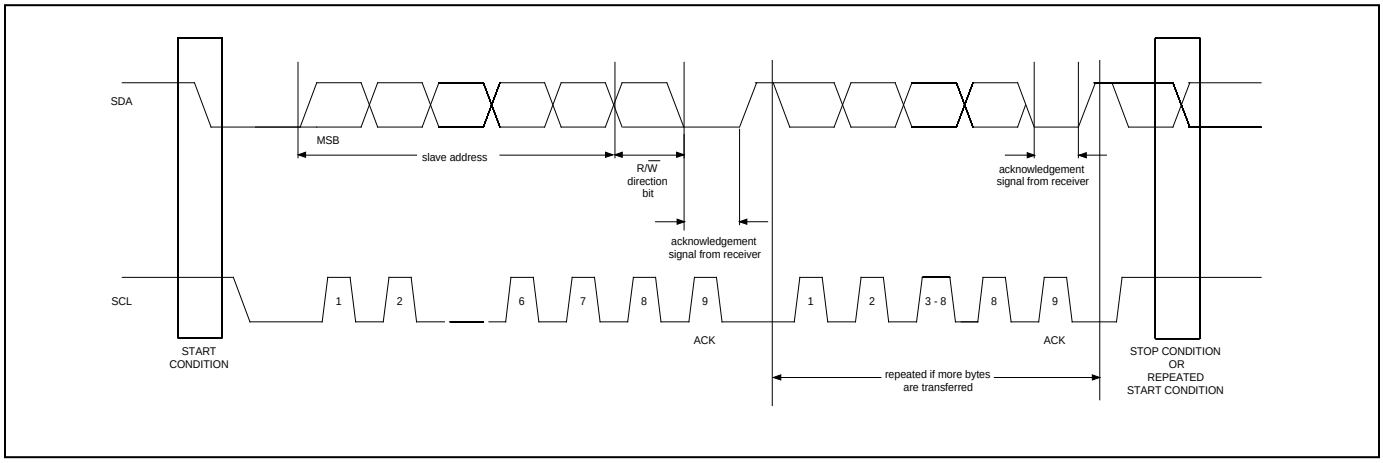
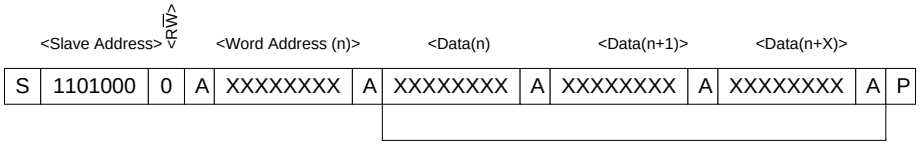


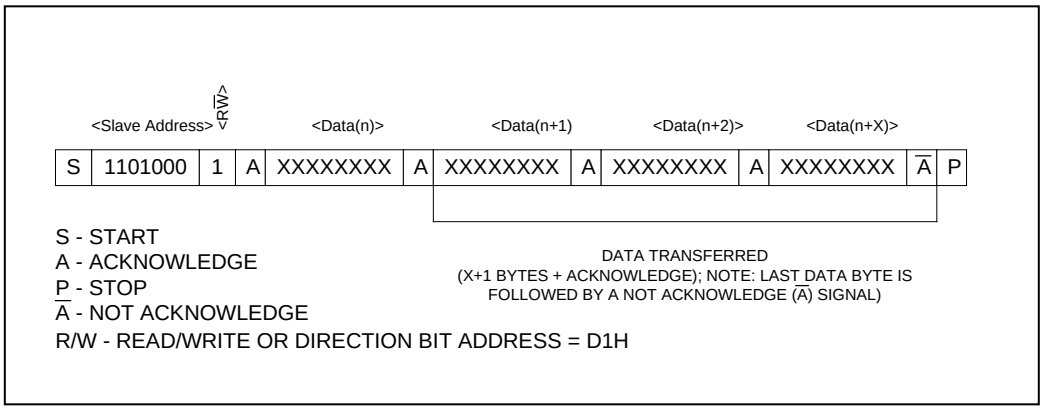
Figure 7. Data Write: Slave Receiver Mode



S - START
A - ACKNOWLEDGE
P - STOP

R/W - READ/WRITE OR DIRECTION BIT ADDRESS = D0H

Figure 8. Data Read: Slave Transmitter Mode



THERMAL INFORMATION

PACKAGE	THETA-JA	THETA-JC
8 PDIP (300 mils)	110°C/W	40°C/W
8 SO (150 mils)	128.4°C/W	36°C/W
8 µSOP (3mm)	206.3°C/W	42°C/W

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 PDIP (300 mils)	P8+1	21-0043	—
8 SO (150 mils)	S8+5	21-0041	90-0096
8 µSOP (3mm)	U8+1	21-0036	90-0092

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
9/11	Updated the *Ordering Information*, *Absolute Maximum Ratings*, *Recommended Operating Conditions*, *DC Electrical Characteristics*, *AC Electrical Characteristics*, *Pin Description*, *Trickle Charger*, *Thermal Information*, and *Package Information*	2, 3, 5, 7, 10, 15

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