DS1685/DS1687
3V/5V Real-Time Clocks

FEATURES

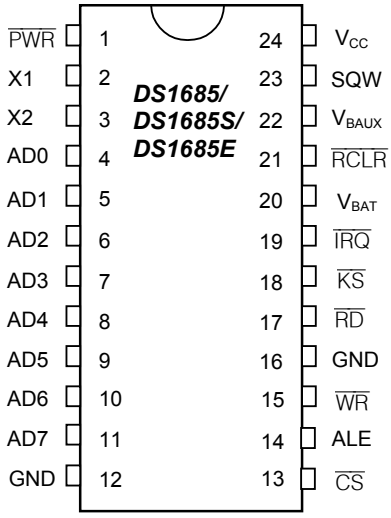
- **Incorporates Industry-Standard DS1287 PC Clock plus Enhanced Features Such as Y2K Compliant**
- **+3V or +5V Operation**
- **64-Bit Silicon Serial Number**
- **Power-Control Circuitry Supports System Power-On from Date/Time Alarm or Key Closure**
- **32kHz Output for Power Management**
- **Crystal-Select Bit Allows RTC to Operate with 6pF or 12.5pF Crystal**
- **SMI Recovery Stack**
- **242 Bytes Battery-Backed NV RAM**
- **Auxiliary Battery Input**
- **RAM Clear Input**
- **Century Register**
- **Date Alarm Register**
- **Compatible with Existing BIOS for Original DS1287 Functions**
- **Available as Chip (DS1685) or Stand-Alone Encapsulated DIP (EDIP) with Embedded Battery and Crystal (DS1687)**
- **Timekeeping Algorithm Includes Leap-Year Compensation Valid Through 2099**
- **Underwriters Laboratory (UL) Recognized**

APPLICATIONS

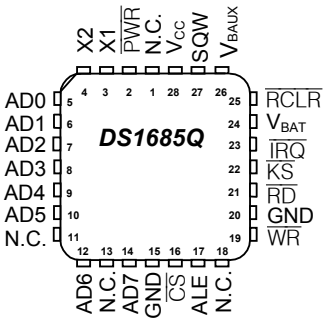
Embedded Systems
Utility Meters
Security Systems
Network Hubs, Bridges, and Routers

PIN CONFIGURATIONS

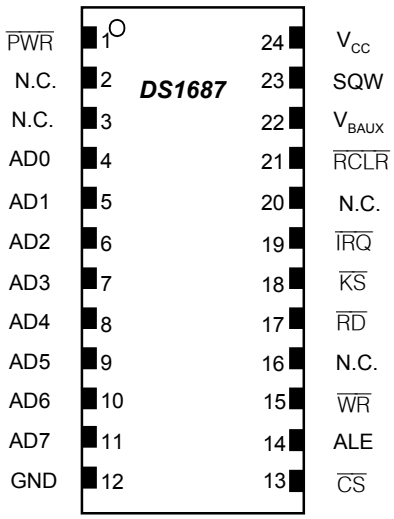
TOP VIEW



PDIP (0.600″)/
SO (0.300″)/
TSSOP (0.173″)



PLCC



EDIP (0.740″)

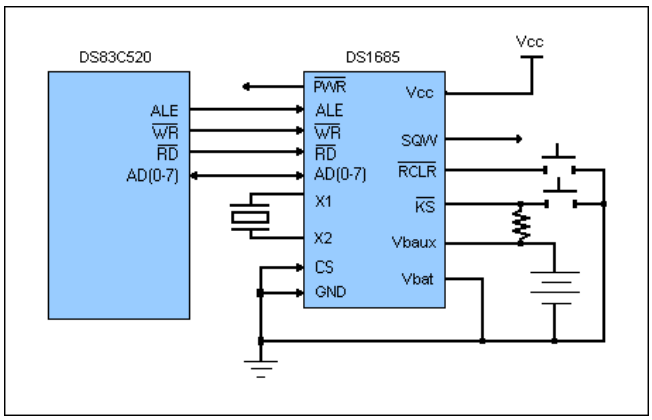
19-5215; Rev 10/12

ORDERING INFORMATION

PART*	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK*
DS1685-3+	0°C to +70°C	3	24 PDIP (0.600”)	DS1685-3
DS1685-5+	0°C to +70°C	5	24 PDIP (0.600”)	DS1685-5
DS1685-5IND+	-40°C to +85°C	5	24 PDIP (0.600”)	DS1685-5
DS1685E-3+	0°C to +70°C	3	24 TSSOP (0.173”)	DS1685E-3
DS1685E-5+	0°C to +70°C	5	24 TSSOP (0.173”)	DS1685E
DS1685EN-3+	-40°C to +85°C	3	24 TSSOP (0.173”)	DS1685E-3
DS1685EN-5+	-40°C to +85°C	5	24 TSSOP (0.173”)	DS1685E
DS1685E-3+T&R	0°C to +70°C	3	24 TSSOP (0.173”)/Tape & Reel	DS1685E-3
DS1685E-5+T&R	0°C to +70°C	5	24 TSSOP (0.173”)/Tape & Reel	DS1685E
DS1685EN-3+T&R	-40°C to +85°C	3	24 TSSOP (0.173”)/Tape & Reel	DS1685E-3
DS1685EN-5+T&R	-40°C to +85°C	5	24 TSSOP (0.173”) /T&R	DS1685E
DS1685Q-3+	0°C to +70°C	3	28 PLCC	DS1685Q-3
DS1685Q-5+	0°C to +70°C	5	28 PLCC	DS1685Q-5
DS1685QN-3+	-40°C to +85°C	3	28 PLCC	DS1685Q-3
DS1685QN-5+	-40°C to +85°C	5	28 PLCC	DS1685Q-5
DS1685Q-3+T&R	0°C to +70°C	3	28 PLCC/Tape & Reel	DS1685Q-3
DS1685Q-5+T&R	0°C to +70°C	5	28 PLCC/Tape & Reel	DS1685Q-5
DS1685S-3+	0°C to +70°C	3	24 SO (0.300”)	DS1685S-3
DS1685S-5+	0°C to +70°C	5	24 SO (0.300”)	DS1685S-5
DS1685S-3+T&R	0°C to +70°C	3	24 SO (0.300”)/Tape & Reel	DS1685S-3
DS1685S-5+T&R	0°C to +70°C	5	24 SO (0.300”)/Tape & Reel	DS1685S-5
DS1687-3+	0°C to +70°C	3	24 EDIP (0.740”)	DS1687-3
DS1687-5+	0°C to +70°C	5	24 EDIP (0.740”)	DS1687-5
DS1687-3IND+	-40°C to +85°C	3	24 EDIP (0.740”)	DS1687-3
DS1687-5IND+	-40°C to +85°C	5	24 EDIP (0.740”)	DS1687-5

+Denotes a lead(Pb)-free/RoHS-compliant device. A “+” anywhere on the top mark indicates a lead-free/RoHS-compliant device.
**An “N” or “IND” denotes an industrial temperature grade device.*

TYPICAL OPERATING CIRCUIT



DETAILED DESCRIPTION

The DS1685/DS1687 are real-time clocks (RTC) designed as successors to the industry-standard DS1285, DS1385, DS1485, and DS1585 PC RTCs. These devices provide the industry-standard DS1285 clock function with either +3.0V or +5.0V operation. The DS1685 also incorporates a number of enhanced features including a silicon serial number, power-on/off control circuitry, 242 bytes of user NV SRAM, and 32.768kHz output for sustaining power management activities.

The DS1685/DS1687 power-control circuitry allows the system to be powered on by an external stimulus such as a keyboard or by a time and date (wake-up) alarm. The PWR output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The PWR pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS1685 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. The DS1687 incorporates the DS1685 chip, a 32.768kHz crystal, and a lithium battery in a complete, self-contained timekeeping EDIP. The entire unit is fully tested at Maxim Integrated such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1685/DS1687. The following paragraphs describe the function of each pin.

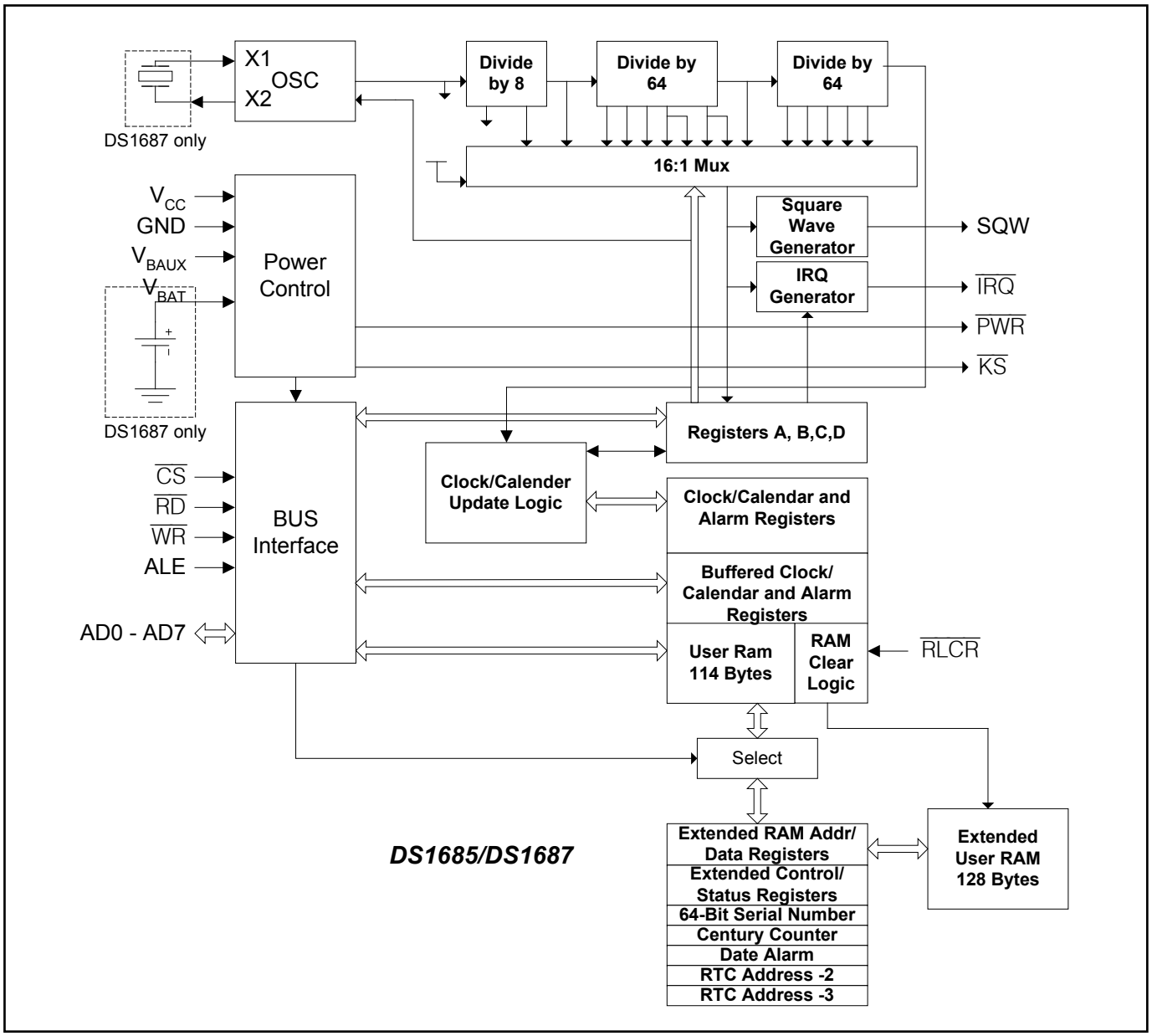
PIN DESCRIPTIONS

PIN			NAME	FUNCTION
DS1685		DS1687		
PDIP, SO, TSSOP	PLCC	EDIP		
1	2	1	$\overline{PWR}$	Active Low Power-On Output, Open Drain. The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS1685/DS1687, $\overline{PWR}$ can be automatically activated from a kickstart input by the $\overline{KS}$ pin or from a wake-up interrupt. Once the system is powered on, the state of $\overline{PWR}$ can be controlled by bits in the Maxim Integrated registers. The $\overline{PWR}$ pin can be connected through a pullup resistor to a positive supply. The voltage of the pullup supply should be no greater than 5.5V.
—	1, 11, 13, 18	2, 3, 16, 20	N.C.	No Connection. Pins missing by design.
2	3	—	X1	Connections for Standard 32.768kHz Quartz Crystal. For greatest accuracy, the DS1685 must be used with a crystal that has a specified load capacitance of either 6pF or 12.5pF. The crystal-select ($\overline{CS}$) bit in Extended Control Register 4B is used to select operation with a 6pF or 12.5pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high-impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high-frequency signals be kept away from the crystal area.
3	4	—	X2	
4–11	5–10, 12, 14	4–11	AD0–AD7	Multiplexed, Bidirectional Address/Data Bus. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1685 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, at which time the DS1685/DS1687 latches the address. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ pulse. In a read cycle, the DS1685/DS1687 outputs 8 bits of data during the latter portion of the $\overline{RD}$ pulse. The read cycle is terminated and the bus returns to a high-impedance state as $\overline{RD}$ transitions high. The address/data bus also serves as a bidirectional data path for the extended RAM.
12, 16	15, 20	12	GND	Ground
13	16	13	$\overline{CS}$	Chip-Select Input, Active-Low. The chip-select signal must be asserted low during a bus cycle for the RTC portion of the DS1685/DS1687 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles that take place with ALE asserted but without asserting $\overline{CS}$ will latch addresses. However, no data transfer will occur.
14	17	14	ALE	Address-Strobe Input, Active High. A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1685/DS1687.
15	19	15	$\overline{WR}$	Write Input, Active Low. The $\overline{WR}$ signal is an active-low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed register.
17	21	17	$\overline{RD}$	Read Input, Active Low. $\overline{RD}$ identifies the time period when the DS1685/DS1687 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

PIN DESCRIPTIONS (continued)

PIN			NAME	FUNCTION
DS1685		DS1687		
PDIP, SO, TSSOP	PLCC	EDIP		
18	22	18	$\overline{KS}$	Kickstart Input, Active Low. When V_{CC} is removed from the DS1685/DS1687, the system can be powered on in response to an active-low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and the auxiliary-battery enable bit (ABE) and kick-start enable bit (KSE) must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input. If not used, connect to V_{CC}, or to V_{BAUX} if V_{BAUX} is used.
19	23	19	$\overline{IRQ}$	Interrupt-Request Output, Open Drain, Active Low. The $\overline{IRQ}$ pin is an active-low output of the DS1685/DS1687 that can be connected to the interrupt input of a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all the enabled flag bits contributing to $\overline{IRQ}$'s active state asserted but without asserting $\overline{CS}$ latch addresses. However, no data transfer occurs.
20	24	—	V_{BAT}	Battery Input for Any Standard 3V Lithium Cell or Other Energy Source. Battery voltage must be held between 2.5V and 3.7V for proper operation. V_{BAT} must be grounded if not used. Diodes should not be placed between V_{BAT} and the battery. See "Conditions of Acceptability" at www.maximintegrated.com/UL.
21	25	21	$\overline{RCLR}$	RAM Clear Input, Active Low. If enabled by software, taking $\overline{RCLR}$ low clears the 242 bytes of user RAM to FFh. When enabled, $\overline{RCLR}$ can be activated whether or not V_{CC} is present. The $\overline{RCLR}$ function is designed to be used by a human interface (shorting to ground manually or by a switch) and not to be driven with external buffers. This pin is internally pulled up. Do not use an external pullup resistor on this pin.
22	26	22	V_{BAUX}	Auxiliary Battery Input. Required for kickstart and wake-up features. This input also supports clock/ calendar and user RAM if V_{BAT} is at lower voltage or is not present. A standard +3V lithium cell or other energy source can be used. Battery voltage must be held between +2.5V and +3.7V for proper operation. If V_{BAUX} is not going to be used it should be grounded, and Auxiliary-Battery Enable bit bank 1, register 4BH, should be written to 0. See "Conditions of Acceptability" at www.maximintegrated.com/UL.
23	27	23	SQW	Square-Wave Output. The SQW pin provides a 32kHz square-wave output, t_{REC}, after a power-up condition has been detected. This condition sets the following bits, enabling the 32kHz output; DV1 = 1, and E32K = 1. A square wave is output on this pin if either SQWE = 1 or E32K = 1. If E32K = 1, then 32kHz is output regardless of the other control bits. If E32K = 0, then the output frequency is dependent on the control bits in register A. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the RTC. The frequency of the SQW pin can be changed by programming Register A as shown in Table 3. The SQW signal can be turned on and off using the SQWE bit in register B or the E32K bit in extended register 4Bh. A 32kHz SQW signal is output when the enable-32kHz (E32K) bit in extended register 4Bh is a logic 1 and V_{CC} is above V_{PF}. A 32kHz square wave is also available when V_{CC} is less than V_{PF} if E32K = 1, ABE = 1, and voltage is applied to the V_{BAUX} pin.
24	28	24	V_{CC}	DC Power for Primary Power Supply. When V_{CC} is applied within the normal limits, the device sis fully accessible and data can be written and read. When V_{CC} is below V_{PF} reads and writes are inhibited.

Figure 1. Block Diagram



OSCILLATOR CIRCUIT

The DS1685 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal, and Figure 2 shows a functional schematic of the oscillator circuit. The oscillator is controlled by an enable bit in the control register. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within one second.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6, 12.5		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

CLOCK ACCURACY

The accuracy of the clock is dependent on the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 3 shows a typical PC board layout for isolation of the crystal and oscillator from noise. Refer to Application Note 58: *Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

The DS1685 can also be driven by an external 32.768 kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated. Refer to Application Note 58: *Crystal Considerations with Dallas Real-Time Clocks* for detailed information about crystal selection and crystal layout.

Figure 2. Oscillator Circuit Showing Internal Bias Network

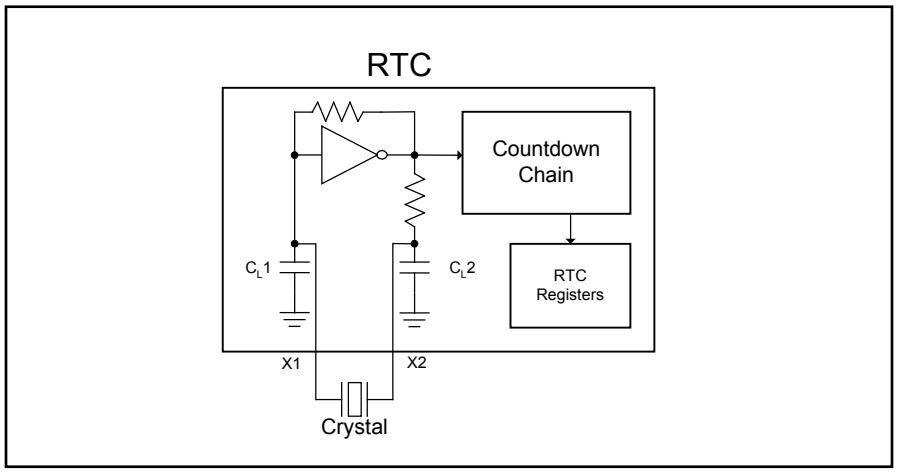
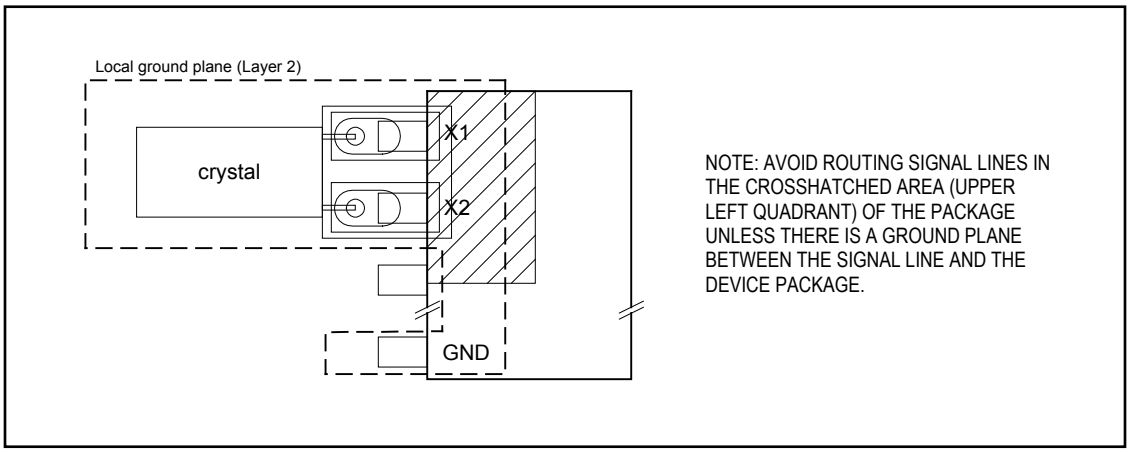


Figure 3. Typical Crystal Layout



POWER-DOWN/POWER-UP CONSIDERATIONS

The RTC function continues to operate, and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. . At least one back up supply must remain within the minimum and maximum limits whenever V_{CC} is not at a valid level. When V_{CC} is applied and exceeds V_{PF} (power-fail trip point), the device becomes accessible after t_{REC}, provided that the oscillator is running and the oscillator countdown chain is not in reset (Register A). This time period allows the system to stabilize after power is applied. If the oscillator is not enabled, the oscillator enable bit will be enabled on power up, and the device becomes immediately accessible.

The DS1685/DS1687 is available in either a 3V or a 5V device.

The 5V device is fully accessible and data can be written and read only when V_{CC} is greater than 4.5V. When V_{CC} falls below V_{PF}, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below the greater of V_{BAT} and V_{BAUX}, the RAM and timekeeper are switched over to a lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin.

The 3V device is fully accessible and data can be written or read only when V_{CC} is greater than 2.7V. When V_{CC} falls below V_{PF}, reads and writes are inhibited. If V_{PF} is less than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply (the greater of V_{BAT} and V_{BAUX}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply when V_{CC} drops below the larger of V_{BAT} and V_{BAUX}.

When V_{CC} falls below V_{PF}, the device inhibits access by internally disabling the $\overline{CS}$ input. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, and SQW pins, all inputs are ignored and all outputs are in a high-impedance state.

TIME, CALENDAR, AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 2. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either binary or binary coded decimal (BCD) format. Table 2 shows the binary and BCD formats of the 10 time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching are explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic 1 to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD) should be set by the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. Invalid time and date entries will result in undefined operation. The set bit in Register B should be cleared after the data mode bit has been written to allow the RTC to update the time and calendar bytes. If the oscillator is running, the time and date registers will update 500ms after the countdown chain is enabled.

Once initialized, the RTC makes all updates in the selected mode. The data mode cannot be changed without reinitializing the 10 data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic 1. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the 10 bytes are advanced by one second and checked for an alarm condition

If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc., might not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later.

The three time alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high.

The second use condition is to insert a “don’t care” state in one or more of the three time-alarm bytes. The “don’t care” code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the “don’t care” condition when at logic 1. An alarm is generated each hour when the “don’t care” bits are set in the hours byte. Similarly, an alarm is generated every minute with “don’t care” codes in the hours and minute alarm bytes. The

"don't care" codes in all three time alarm bytes create an interrupt every second. The three time-alarm bytes can be used with the date alarm as described in the *Wake-Up/Kickstart* section. The century counter is discussed later in this text.

All registers can be directly written or read except for the following:

1) Registers C and D are read-only.
2) Bit 7 of Register A is read-only.
3) Bit 7 of the seconds byte is read-only.

Table 2A. Time, Calendar, and Alarm Data Modes—BCD Mode (DM = 0)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	10 Seconds			Seconds				Seconds	00-59
01H	0	10 Seconds			Seconds				Seconds Alarm	00-59
02H	0	10 Minutes			Minutes				Minutes	00-59
03H	0	10 Minutes			Minutes				Minutes Alarm	00-59
04H	AM/PM	0	0	10 Hour	Hours				Hours	1-12 +AM/PM 00-23
	0		10 Hour							
05H	AM/PM	0	0	10 Hour	Hours				Hours Alarm	1-12 +AM/PM 00-23
	0		10 Hr							
06H	0	0	0	0	0	Day			Day	01-07
07H	0	0	10 Date		Date				Date	01-31
08H	0	0	0	10 Month	Month				Month	01-12
09H	10 Year				Year				Year	00-99
0AH	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	
0BH	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	
0CH	IRQF	PF	AF	UF	0	0	0	0	Control	
0DH	VRT	0	0	0	0	0	0	0	Control	
48H	Century								Bank 1 Century	00-99
49H			10 Date		Date				Bank 1 Date Alarm	01-31

X = Read/Write Bit.

Note 1: Unless otherwise specified, the state of the registers is not defined when power is first applied.

Note 2: Except for the seconds register, 0 bits in the time and date registers can be written to a 1, but may be modified when the clock updates. 0 bits should always be written to 0 except for alarm mask bits.

Table 2. Time, Calendar, and Alarm Data Modes—Binary Mode (DM = 1)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	0	Seconds						Seconds	00-3B
01H	0	0	Seconds						Seconds Alarm	00-3B
02H	0	0	Minutes						Minutes	00-3B
03H	0	0	Minutes						Minutes Alarm	00-3B
04H	AM/PM	0	0	0	Hours				Hours	1-0C +AM/PM
	0			Hours						00-17
05H	AM/PM	0	0	0	Hours				Hours Alarm	1-0C +AM/PM
	0			Hours						00-17
06H	0	0	0	0	0	Day			Day	01-07
07H	0	0	0	Date					Date	01-1F
08H	0	0	0	0	Month				Month	01-0C
09H	0	Year							Year	00-63
0AH	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	
0BH	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	
0CH	IRQF	PF	AF	UF	0	0	0	0	Control	
0DH	VRT	0	0	0	0	0	0	0	Control	
48H	Century								Bank 1 Century	00-63
49H			10 Date		Date				Bank 1 Date Alarm	01-1F

CONTROL REGISTERS

The four control registers A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

Register A (0Ah)

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP – The update-in-progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a 1, the update transfer occurs soon. When UIP is a 0, the update transfer does not occur for at least 244μs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read-only. Writing the SET bit in Register B to a 1 inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500ms after a pattern of 01X is written to DV0, DV1, and DV2. The oscillator enable bit, DV1, will be set to a 1 when V_{CC} is applied.

DV2 = Countdown Chain
- 1 – resets countdown chain only if DV1=1
- 0 – countdown chain enabled

DV1 = Oscillator Enable
- 1 – oscillator on
- 0 – oscillator off

DV0 = Bank Select
- 1 – extended registers
- 0 – original bank

RS3, RS2, RS1, RS0 – These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1) Enable the interrupt with the PIE bit;
2) Enable the SQW output pin with the SQWE or E32K bits;
3) Enable both at the same time and the same rate; or
4) Enable neither.

Table 3 lists the periodic interrupt rates and the square-wave frequencies that can be chosen with the RS bits.

Register B (0Bh)

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET – When the SET bit is a 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a 1, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1685/DS1687.

PIE – The periodic-interrupt enable bit is a read/write bit that allows the periodic-interrupt flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3–RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1685/DS1687 functions.

AIE – The alarm-interrupt enable (AIE) bit is a read/write bit which, when set to a 1, permits the alarm flag (AF) bit in Register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes, including a “don’t care” alarm code of binary 11XXXXXX. When the AIE bit is set to 0, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1685/DS1687 do not affect the AIE bit.

UIE – The update-ended interrupt-enable (UIE) bit is a read/write bit that enables the update-end flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE – When the square-wave enable (SQWE) bit is set to a 1 and E32K = 0, a square-wave signal at the frequency set by the rate-selection bits RS3–RS0 is driven out on the SQW pin. When the SQWE bit is set to 0 and E32K = 0, the SQW pin is held low. SQWE is a read/write bit.

DM – The data mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A 1 in DM signifies binary data while a 0 in DM specifies BCD data.

24/12 – The 24/12 control bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit that enables two daylight savings adjustments when DSE is set to 1. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. When DSE is enabled, the internal logic tests for the first/last Sunday condition at 1:59:59 AM. If the DSE bit is not set when the test occurs, the daylight savings function will not operate correctly. These adjustments do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

Register C (0Ch)

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IQRF	PF	AF	UF	0	0	0	0

IRQF – The interrupt-request flag (IRQF) bit is set to a 1 when one or more of the following are true:
PF = PIE = 1 WF = WIE = 1
AF = AIE = 1 KF = KSE = 1
UF = UIE = 1 RF = RIE = 1

Any time the IRQF bit is a 1, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF – The periodic-interrupt flag (PF) is a read-only bit that is set to a 1 when an edge is detected on the selected tap of the divider chain. The RS3–RS0 bits establish the periodic rate. PF is set to a 1 independently of the state of the PIE bit. When both PF and PIE are 1's, the $\overline{IRQ}$ signal is active and sets the IRQF bit. This bit may be cleared by reading Register C.

AF – A 1 in the alarm-interrupt flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a 1, the $\overline{IRQ}$ pin goes low and a 1 appears in the IRQF bit. This bit may be cleared by reading Register C.

UF – The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is set to 1, the one in UF causes the IRQF bit to be a 1, which asserts the $\overline{IRQ}$ pin. This bit may be cleared by reading Register C.

BIT 3, BIT2, BIT 1, BIT 0 - These are unused bits of the status Register C. These bits always read 0 and cannot be written.

Register D (0Dh)

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT – The valid RAM and time (VRT) bit indicates the condition of the battery connected to the V_{BAT} pin or the battery connected to V_{BAUX}, whichever is at a higher voltage. This bit is not writable and should always be a 1 when read. If a 0 is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6, BIT 5, BIT 4, BIT 3, BIT 2, BIT 1, BIT 0 – The remaining bits of Register D are not usable. They cannot be written and when read will always read 0.

NV RAM—RTC

The 242 general-purpose NV RAM bytes are not dedicated to any special function within the DS1685/DS1687. They can be used by the application program as nonvolatile memory and are fully available during the update cycle.

The user RAM is divided into two separate memory banks. When the bank 0 is selected, the 14 RTC registers and 114 bytes of user RAM are accessible. When bank 1 is selected, an additional 128 bytes of user RAM are accessible through the extended RAM address and data registers.

INTERRUPT CONTROL

The DS1685/DS1687 includes six separate, fully automatic sources of interrupt for a processor:

1) Alarm Interrupt
2) Periodic Interrupt
3) Update-Ended Interrupt
4) Wake-Up Interrupt
5) Kickstart Interrupt
6) RAM Clear Interrupt

The conditions that generate each of these independent interrupt conditions are described in detail in other sections of this text. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of 6 bits, including 3 bits in Register B and 3 bits in Extended Register 4B, that enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the IRQ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, IRQ is immediately set at an active level, even though the event initiating the interrupt condition might have occurred much earlier. As a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register 4A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register 4B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that set bits remain stable throughout the read cycle. All bits that were set are cleared when read and new interrupts that are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each used flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register 4A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the IRQ line is driven low when an interrupt flag bit is set and its corresponding enable bit is also set. IRQ is held low as long as at least one of the six possible interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the IRQ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS1685/DS1687 initiated an interrupt is accomplished by reading Register C and finding IRQF = 1. IRQF remains set until all enabled interrupt flag bits are cleared to 0.

SQUARE-WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768kHz crystal tied to X1 and X2. The square-wave output is enabled and disabled by the SQWE bit in Register B or the E32K bit in extended register 4Bh. If the square wave is enabled (SQWE = 1 or E32K = 1), then the output frequency is determined by the settings of the E32K bit in Extended Register 4Bh and by the RS3–0 bits in Register A. If E32K = 1, then a 32.768kHz square wave is output on the SQW pin regardless of the settings of RS3–0 and SQWE.

If E32K = 0, then the square-wave output frequency is determined by the RS3–0 bits. These bits control a 1-of-16 decoder, which selects one of 13 taps that divide the 32.768kHz frequency. The RS3–0 bits establish the SQW output frequency as shown in Table 3. In addition, RS3–0 bits control the periodic interrupt selection as described below.

If E32K = 1 and the auxiliary-battery enable bit (ABE, bank 1; register 04Bh) is enabled, and voltage is applied to V_{BAUX}, then the 32kHz square-wave output signal is output on the SQW pin in the absence of V_{CC}. This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square-wave output signal is generated on the SQW pin in the absence of V_{CC}.

A pattern of 01X in the DV2, DV1, and DV0 bits respectively turns the oscillator on and enables the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a “don’t care” because it is used for selection between register banks 0 and 1.

A pattern of 11X turns the oscillator on, but the oscillator’s countdown chain is held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 keeps the oscillator off.

OSCILLATOR CONTROL BITS

When the DS1687 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 01X in bits 4 through 6 of Register A turns the oscillator on and enables the countdown chain. A pattern of 11X turns the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

PERIODIC INTERRUPT SELECTION

The periodic interrupt causes the $\overline{IRQ}$ pin to go to an active state from once every 500ms to once every 122µs. This function is separate from the alarm interrupt, which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3–0 bits in Register A, which select the square-wave frequency (Table 3). Changing the bits affects both the square-wave frequency and the periodic-interrupt output. However, each function has a separate enable bit in Register B. The SQWE and E32K bits control the square-wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

Table 3. Periodic Interrupt Rate and Square-Wave Output Frequency

EXT. REG B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625ms	256Hz
0	0	0	1	0	7.8125ms	128Hz
0	0	0	1	1	122.070µs	8.192kHz
0	0	1	0	0	244.141µs	4.096kHz
0	0	1	0	1	488.281µs	2.048kHz
0	0	1	1	0	976.5625µs	1.024kHz
0	0	1	1	1	1.953125ms	512Hz
0	1	0	0	0	3.90625ms	256Hz
0	1	0	0	1	7.8125ms	128Hz
0	1	0	1	0	15.625ms	64Hz
0	1	0	1	1	31.25ms	32Hz
0	1	1	0	0	62.5ms	16Hz
0	1	1	0	1	125ms	8Hz
0	1	1	1	0	250ms	4Hz
0	1	1	1	1	500ms	2Hz
1	X	X	X	X	*	32.768kHz

**RS3–RS0 determine periodic interrupt rates as listed for E32K = 0.*

UPDATE CYCLE

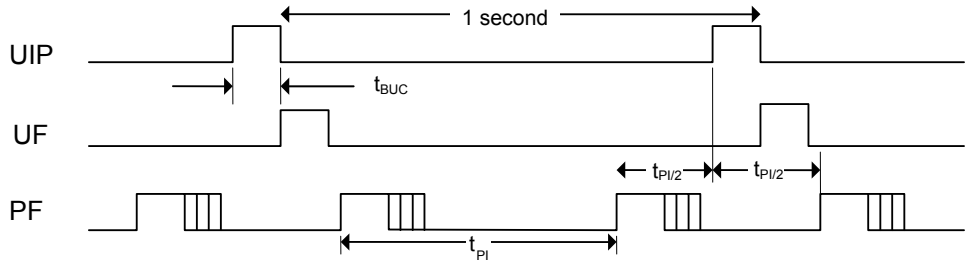
The RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to 1, the user copy of the double-buffered time, calendar, alarm, and elapsed time byte is frozen and does not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a “don’t care” code is present in all alarm locations.

There are three methods that can handle access of the RTC that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999ms is available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the UIP bit in Register A to determine if the update cycle is in progress. The UIP bit pulses once per second. After the UIP bit goes high, the update transfer occurs 244µs later. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data is changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (Figure 4). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2 + t_{BUC}) to ensure that data is not read during the update cycle.

Figure 4. Update-Ended And Periodic-Interrupt Relationship

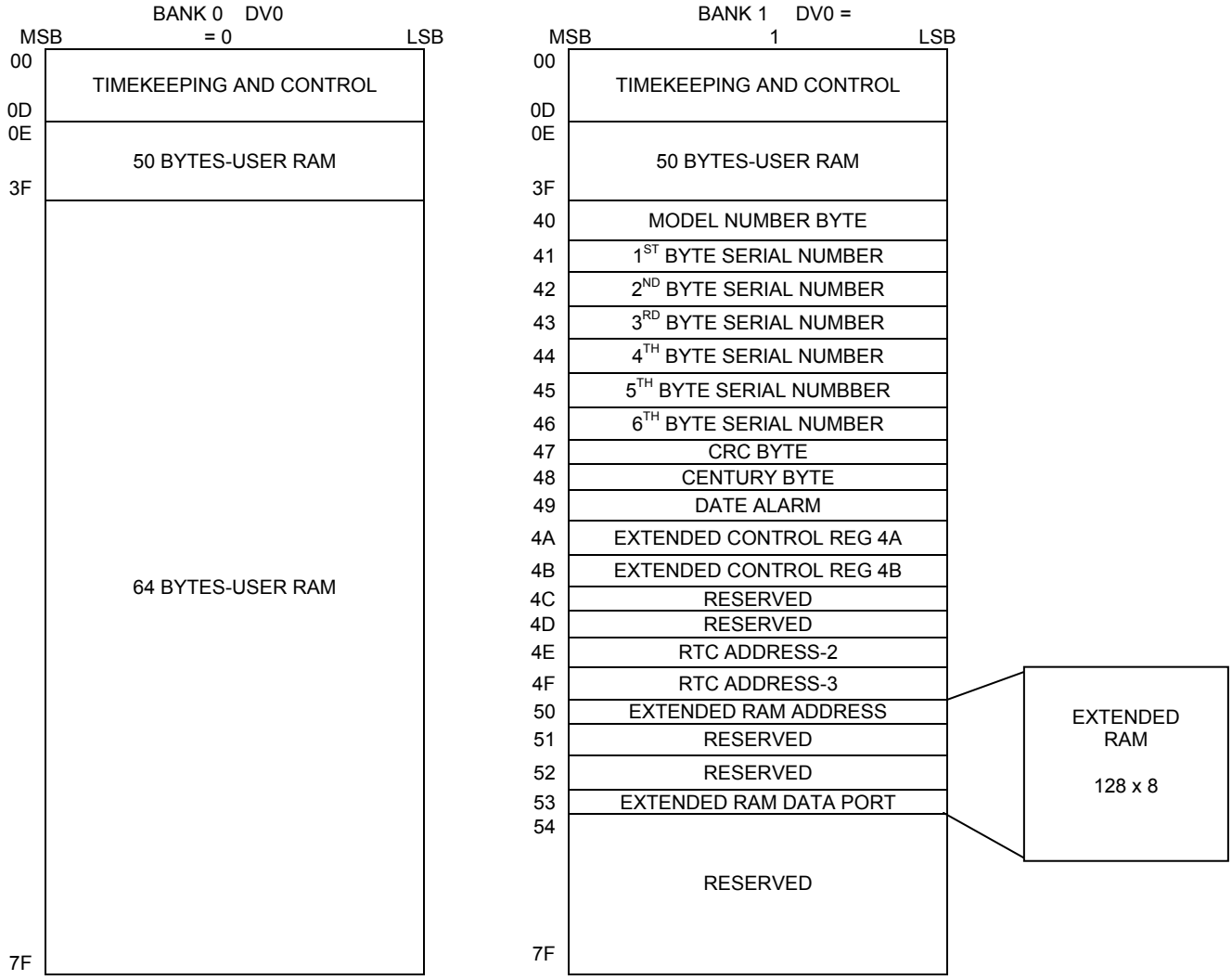


t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 3.
t_{BUC} = DELAY BEFORE UPDATE CYCLE = 244µs.

EXTENDED FUNCTIONS

The extended functions provided by the DS1685/DS1687 that are new to the RAMified RTC family are accessed by a software-controlled bank-switching scheme, as illustrated in Figure 5. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS1685/DS1687 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

Figure 5. DS1685/DS1687 Register Map and Extended Register Bank Definition



When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the registers that provide control and status for the extended functions are accessed in place of the additional 64 bytes of user RAM. The major functions controlled by the extended registers are listed below:

1) 64-Bit Silicon Serial Number
2) Century counter
3) Date Alarm
4) Auxiliary Battery Control/Status
5) Wake Up
6) Kickstart
7) RAM Clear Control/Status
8) 128 Bytes Extended RAM Access

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0, the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Maxim Integrated. Bits in these locations cannot be written and return a 0 if read.

SILICON SERIAL NUMBER

A unique 64-bit lasered serial number is located in bank 1, registers 40h to 47h. This serial number is divided into three parts. The first byte in register 40h contains a model number, 71h, to identify the device type. Registers 41h to 46h contain a unique binary number. Register 47h contains a CRC byte used to validate the data in registers 40h to 46h. All 8 bytes of the serial number are read-only registers.

The DS1685/DS1687 is manufactured such that no two devices contain an identical number in locations 41h to 47h.

CENTURY COUNTER

A register has been added in bank 1, location 48h, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS1685/DS1687 kickstart, wake-up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The auxiliary-battery enable (ABE; bank 1, register 04Bh) bit in extended control register 4B is used to turn on and off the auxiliary battery for the above functions in the absence of V_{CC}. When set to a 1, V_{BAUX} battery power is enabled, and when cleared to 0, V_{BAUX} battery power is disabled to these functions.

In the DS1685/DS1687, this auxiliary battery can be used as the primary backup-power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS1685 is to be backed-up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and V_{BAT} should be grounded. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

WAKE-UP/KICKSTART

The DS1685/DS1687 incorporates a wake-up feature that can power the system on at a predetermined date and time through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature allows the system to be powered up in response to a low-going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power can be applied upon such events as a key closure or modem-ring detect signal. In order to use either the wake-up or the kickstart features, the DS1685/DS1687 must have an auxiliary battery connected to the V_{BAUX} pin and the oscillator must be running, and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin does not drive low in response to a kickstart or wake-up condition, while in battery-backed mode.

The wake-up feature is controlled through the wake-up interrupt-enable bit in extended control register 4B (WIE, bank 1, 04Bh). Setting WIE to 1 enables the wake-up feature, clearing WIE to 0 disables it. Similarly, the kick-start feature is controlled through the kickstart-interrupt-enable bit in extended control register 4B (KSE, bank 1, 04Bh).

A wake-up sequence occurs as follows: When wake-up is enabled by WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar monitors the current date for a match condition with the date alarm register (bank 1, register 049h). In conjunction with the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05h, 03h, and 01h) are also monitored. As a result, a wake-up occurs at the date and time specified by the date, hours, minutes, and seconds alarm-register values. This additional alarm occurs regardless of the programming of the AIE bit (bank 0, register B, 0Bh). When the match condition occurs, the $\overline{PWR}$ pin automatically drives low. This output can be used to turn on the main system power supply, which provides V_{CC} voltage to the DS1685/DS1687 as well as the other major components in the system. Also at this time, the wake-up flag (WF, bank 1, register 04Ah) is set, indicating that a wake-up condition has occurred.

A kickstart sequence occurs when kickstarting is enabled by KSE = 1. While the system is powered down, the $\overline{KS}$ input pin is monitored for a low-going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line pulls low, as it does for a wake-up condition. Also at this time, the kickstart flag (KF, bank 1, register 04Ah) is set, indicating that a kickstart condition has occurred.

The timing associated with both the wake-up and kickstarting sequences is illustrated in the “Wake-Up/Kickstart Timing Diagram” in the *Electrical Specifications* section of this data sheet. The timing associated with these functions is divided into five intervals, labeled 1 to 5 on the diagram.

The occurrence of either a kickstart or wake-up condition causes the $\overline{PWR}$ pin to be driven low, as described above. During Interval 1, if the supply voltage on the DS1685/DS1687 V_{CC} pin rises above the greater of V_{BAT} or V_{PF} before the power on timeout period (t_{POTO}) expires, then $\overline{PWR}$ remains at the active-low level. If V_{CC} does not rise above the greater of V_{BAT} or V_{PF} in this time, then the $\overline{PWR}$ output pin is turned off and returns to its high-impedance level. In this event, the $\overline{IRQ}$ pin also remains three-stated. The interrupt flag bit (either WF or KF) associated with the attempted power-on sequence remains set until cleared by software during a subsequent system power-on.

If V_{CC} is applied within the timeout period, then the system power-on sequence continues as shown in Intervals 2 to 5 in the timing diagram. During Interval 2, $\overline{PWR}$ remains active and $\overline{IRQ}$ is driven to its active-low level, indicating that either WF or KF was set in initiating the power-on. In the diagram, $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit is automatically cleared to 0 in response to a successful power-on. The $\overline{PWR}$ line remains active as long as the PAB remains cleared to 0.

At the beginning of Interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing 0’s to both of these control bits. As long as no other interrupt within the DS1685/DS1687 is pending, the $\overline{IRQ}$ line is taken inactive once these bits are reset. Execution of the application software can proceed. During this time, both the wake-up and kickstart functions can be used to generate status and interrupts. WF is set in response to a date, hours, minutes, and seconds match condition. KF is set in response to a low-going transition on $\overline{KS}$. If the associated interrupt-enable bit is set (WIE and/or KSE), then the $\overline{IRQ}$ line is driven active-low in response to enabled event. In addition, the other possible interrupt sources within the DS1685/DS1687 can cause $\overline{IRQ}$ to be driven low. While system power is applied, the on-chip logic always attempts to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake-up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake-up or kickstart.

The system can be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high-impedance state, as shown at the beginning of Interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin is placed in a high-impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake-up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During Interval 5, the system is fully powered down. Battery backup of the clock calendar and NV RAM is in effect and $\overline{IRQ}$ is three-stated, and monitoring of wake-up and kickstart takes place. If PRS = 1, $\overline{PWR}$ stays active; otherwise, if PRS = 0, $\overline{PWR}$ is three-stated.

RAM CLEAR

The DS1685/DS1687 provides a RAM clear function for the 242 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled by the RAM clear-enable bit (RCE; bank 1, register 04Bh). When RCE is set to a logic 1 and RF=0, the 242 bytes of user RAM is cleared (all bits set to 1) when an active-low transition is sensed on the $\overline{RCLR}$ pin. This action has no affect on either the clock/calendar settings or upon the contents of the extended RAM. The RAM clear flag (RF, bank 1, register 04Ah) is set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE = 1, the IRQ line is also driven low upon completion. The interrupt condition can be cleared by writing a 0 to the RF bit. The IRQ line then returns to its inactive high level, provided there is no other pending interrupts. Once the $\overline{RCLR}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in the *Electrical Characteristics* section.

When RCE is cleared to 0, the RAM clear function is disabled. The state of the $\overline{RCLR}$ pin has no affect on the contents of the user RAM, and transitions on the $\overline{RCLR}$ pin have no affect on RF.

128 x 8 EXTENDED RAM

The DS1685/DS1687 provides 128 x 8 of on-chip SRAM, which is controlled as nonvolatile storage sustained by V_{BAT} and/or V_{BAUX}. On power-up, the RAM is accessible after T_{REC}.

The on-chip 128 x 8 NV SRAM is accessed by the eight multiplexed address/data lines AD7–AD0. Access to the SRAM is controlled by two on-chip latch registers. One register is used to hold the SRAM address and the other register is used to hold read/write data. The SRAM address space is from 00h to 7Fh.

Access to the extended 128 x 8 RAM is controlled by two of the registers shown in Figure 5. The registers in bank 1 must first be selected by setting the DV0 bit in register A to a logic 1. The 7-bit address of the RAM location to be accessed must be loaded into the extended RAM address register located at 50h. Data in the addressed location may be read by performing a read operation from location 53h, or written to by performing a write operation to location 53h. Data in any addressed location may be read or written repeatedly without changing the address in location 50h.

EXTENDED CONTROL REGISTERS

Two extended control registers are provided to supply controls and status information for the extended features offered by the DS1685/DS1687. These are designated as extended control registers 4A and 4B and are located in register bank 1, locations 04Ah and 04Bh, respectively. The functions of the bits within these registers are described as follows.

Extended Control Register 4A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	*	*	PAB	RF	WF	KF

VRT2 – This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the V_{BAUX}. If this bit is read as a logic 0, the external battery should be replaced.

INCR – Increment-in-Progress status bit. This bit is set to a 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR is set to a 1 at 122μs before the update cycle starts and is cleared to 0 at the end of each update cycle.

PAB – Power-Active Bar control bit. When this bit is 0, the PWR pin is in the active-low state. When this bit is 1, the PWR pin is in the high-impedance state. This bit can be written to a logic 1 or 0 by the user. If either WF and WIE = 1 or KF and KSE = 1, the PAB bit is cleared to 0.

RF – Ram Clear Flag. This bit is set to a logic 1 when a high-to-low transition occurs on the $\overline{RCLR}$ input if RCE = 1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF – Wake-Up Alarm Flag. This bit is set to 1 when a wake-up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF – Kickstart Flag. This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

**Reserved bits. These bits are reserved for future use by Maxim Integrated. They can be read and written, but have no affect on operation.*

Extended Control Register 4B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	CS	RCE	PRS	RIE	WIE	KSE

ABE – Auxiliary Battery Enable. This bit when written to a logic 1 enables the V_{BAUX} pin for extended functions.

E32K – Enable 32.768kHz output. This bit when written to a logic 1 enables the 32.768kHz oscillator frequency to be output on the SQW pin. This bit is set to a logic 1 when V_{CC} is applied.

CS – Crystal Select Bit. When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6pF specified load capacitance. When CS = 1, the oscillator is configured for a 12.5pF crystal. CS is disabled in the DS1687 EDIP and should be set to CS = 0.

RCE – RAM Clear-Enable bit. When set to a 1, this bit enables a low level on $\overline{RCLR}$ to clear all 242 bytes of user RAM. When RCE = 0, $\overline{RCLR}$ and the RAM clear function are disabled.

PRS – PAB Reset-Select Bit. When set to a 0, the $\overline{PWR}$ pin is set high-Z when the DS1685 goes into power-fail. When set to a 1, the PWR pin remains active upon entering power-fail.

RIE – Ram Clear-Interrupt Enable. When RIE is set to a 1, the $\overline{IRQ}$ pin is driven low when a RAM clear function is completed.

WIE – Wake-Up Alarm-Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin is driven active-low when a wake-up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin is also driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ are driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit has no affect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

KSE – Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin is driven active-low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin is also driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ are driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit has no affect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

SYSTEM MAINTENANCE INTERRUPT (SMI) RECOVERY STACK

An SMI recovery register stack is located in the extended register bank, locations 4Eh and 4Fh. This register stack, shown below, can be used by the BIOS to recover from an SMI occurring during an RTC read or write.

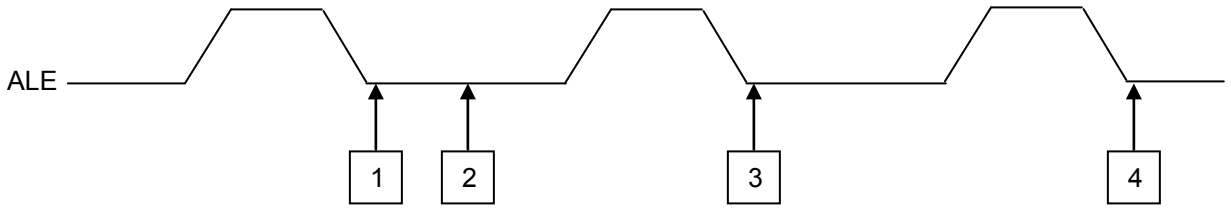
	RTC ADDRESS
	RTC ADDRESS-1
4Eh	RTC ADDRESS-2
4Fh	RTC ADDRESS-3

SMI RECOVERY STACK

7	6	5	4	3	2	1	0
DV0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

REGISTER BIT DEFINITION

The RTC address is latched on the falling edge of the ALE signal. Each time an RTC address is latched, the register address stack is pushed. The stack is only four registers deep, holding the three previous RTC addresses in addition to the current RTC address being accessed. The following waveform illustrates how the BIOS could recover the RTC address when an SMI occurs.



1) The RTC address is latched.
2) An SMI is generated before an RTC read or write occurs.
3) RTC address 0Ah is latched and the address from 1 is pushed to the RTC Address-1 stack location. This step is necessary to change the bank select bit, DV0 = 1.
4) RTC address 4Eh is latched and the address from “1” is pushed to location “4Eh,” “RTC Address-2” while 0Ah is pushed to the “RTC Address-1” location. The data in this register, 4Eh, is the RTC address lost due to the SMI.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……0.3V to +6V
Operating Temperature Range, Commercial ...……0°C to +70°C
Operating Temperature Range, Industrial……...-40°C to +85°C
Storage Temperature Range
EDIP……...……-40°C to +85°C
PDIP, SO, TSSOP……...……-55°C to +125°C
Lead Temperature (soldering, 10s)……...……..+260°C
(**Note:** EDIP is hand or wave-soldered only.)
Soldering Temperature (reflow)…….....……..…+260°C

This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C, T_A = -40°C to +85°C.)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power-Supply Voltage	(-5)	V_{CC}	4.5	5.0	5.5	V	1
	(-3)		2.7	3.0	3.7		
Input Logic 1		V_{IH}	2.2		V_{CC} + 0.3	V	1
Pullup Voltage	$\overline{PWR}$	V_{PUPWR}			5.5	V	1
	$\overline{IRQ}$				V_{CC} + 0.2		
Input Logic 0		V_{IL}	-0.3		0.6	V	1
Battery Voltage		V_{BAT}	2.5		3.7	V	1
Auxiliary Battery Voltage	(-5)	V_{BAUX}	2.5		5.2	V	1
	(-3)		2.5		3.7		

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V±10% or V_{CC} = 3.0V±10%, T_A = 0°C to +70°C, T_A = -40°C to +85°C.)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power-Supply Current	(-5)	I_{CC1}		7	15	mA	2, 3
	(-3)			5	10		
CMOS Standby Current ($\overline{CS}$ = V_{CC} - 0.2V)	(-5)	I_{CC2}		1	3	mA	2, 3
	(-3)			0.5	2		
Input Leakage Current (Any Input)		I_{IL}	-1		+1	µA	
Output Leakage Current		I_{OL}	-1		+1	µA	5
Output Logic 1 Voltage (I_{OUT} = -1.0mA)		V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1mA)		V_{OL}			0.4	V	
Power-Fail Trip Point	(-5)	V_{PF}	4.25	4.37	4.5	V	
	(-3)		2.5	2.6	2.7		
Battery Switch Voltage	(-5)	V_{SW}		V_{BAT}, V_{BAUX}		V	8
Battery Leakage Current		I_{BATLKG}		10	100	nA	12
I/O Leakage		I_{LO}	-1		+1	µA	4
$\overline{PWR}$ Output at 0.4V	(-5)	I_{OLPWR}			10.0	mA	1
	(-3)				4		
$\overline{IRQ}$ Output at 0.4V	(-5)	I_{OLIRQ}			2.1	mA	1
	(-3)				0.8		

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = 0V**, T_A = 0°C to +70°C, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{BAT}, V_{BAUX} Current (OSC ON, E32K = 0)	I_{BAT1}			500	nA	12
V_{BAT}, V_{BAUX} Current (OSC OFF)	I_{BAT2}			200	nA	12

RTC AC TIMING CHARACTERISTICS

(V_{CC} **= 3.0V±10%**, T_A = 0°C to +70°C, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	260		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{RWL}	100			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	100			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip-Select Setup Time Before $\overline{WR}$ or $\overline{RD}$	t_{CS}	20			ns	
Chip-Select Hold Time	t_{CH}	0			ns	
Read-Data Hold Time	t_{DHR}	10		50	ns	
Write-Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE Fall	t_{AHL}	15			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	30			ns	
Pulse-Width ALE High	PW_{ASH}	80			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	30			ns	
Output-Data Delay Time from $\overline{RD}$	t_{DDR}	20		80	ns	6
Data Setup Time	t_{DSW}	60			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

AC TEST CONDITIONS

Output Load: 50pF

Input Pulse Levels: 0 to 3.0V

Timing Measurement Reference Levels
Input : 1.5V
Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

RTC AC TIMING CHARACTERISTICS

(V_{CC} **= 5.0V±10%**, T_A = 0°C to +70°C, T_A = -40°C to 85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	195		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{RWL}	75			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	75			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip-Select Setup Time Before $\overline{WR}$ or $\overline{RD}$	t_{CS}	20			ns	
Chip-Select Hold Time	t_{CH}	0			ns	
Read-Data Hold Time	t_{DHR}	10		50	ns	
Write-Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE Fall	t_{AHL}	15			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse-Width ALE High	PW_{ASH}	40			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	30			ns	
Output-Data Delay Time from $\overline{RD}$	t_{DDR}	20		60	ns	6
Data Setup Time	t_{DSW}	60			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

AC TEST CONDITIONS

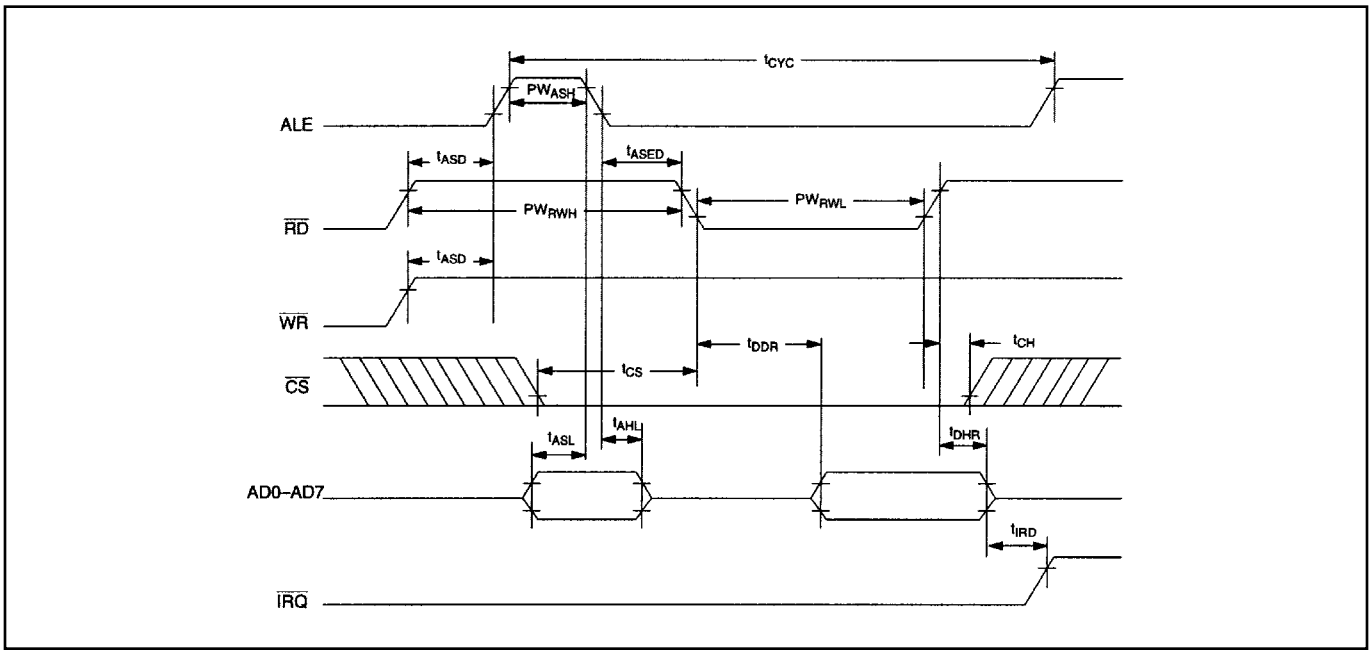
Output Load: 50pF

Input Pulse Levels: 0 to 3.0V

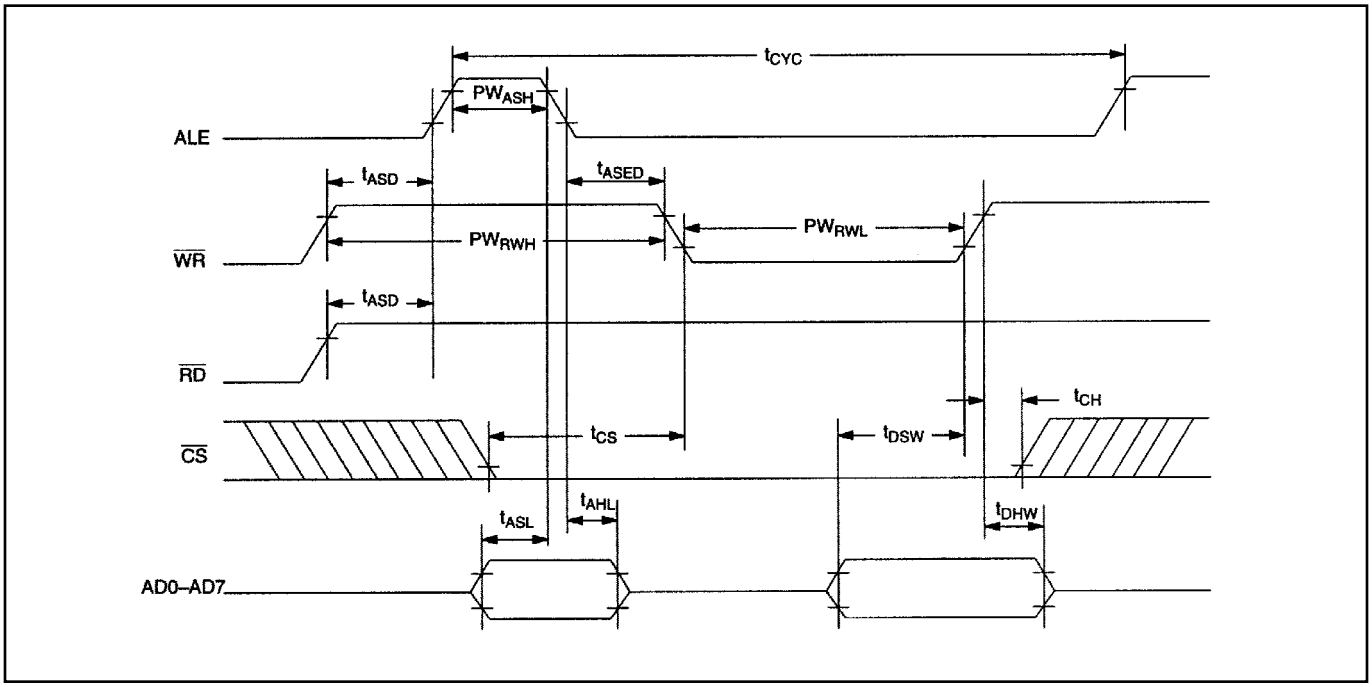
Timing Measurement Reference Levels
Input : 1.5V
Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

DS1685/DS1667 BUS TIMING FOR READ CYCLE TO RTC AND RTC REGISTERS



DS1685/DS1687 BUS TIMING FOR WRITE CYCLE TO RTC AND RTC REGISTERS



POWER-UP/DOWN TIMING—5V

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power-Fail	t_{PF}			0	ns	
Recovery at Power-Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power-Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power-Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power-Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	9, 10

POWER-UP/DOWN TIMING—3V

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power-Fail	t_{PF}			0	ns	
Recovery at Power-Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power-Down	t_F $2.5 \le V_{CC} \le 2.7V$	300			µs	
V_{CC} Slew Rate Power-Up	t_R $2.7V \ge V_{CC} \ge 2.5V$	0			µs	
Expected Data Retention	t_{DR}	10			years	9, 10

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

CAPACITANCE

(T_A = +25°C)

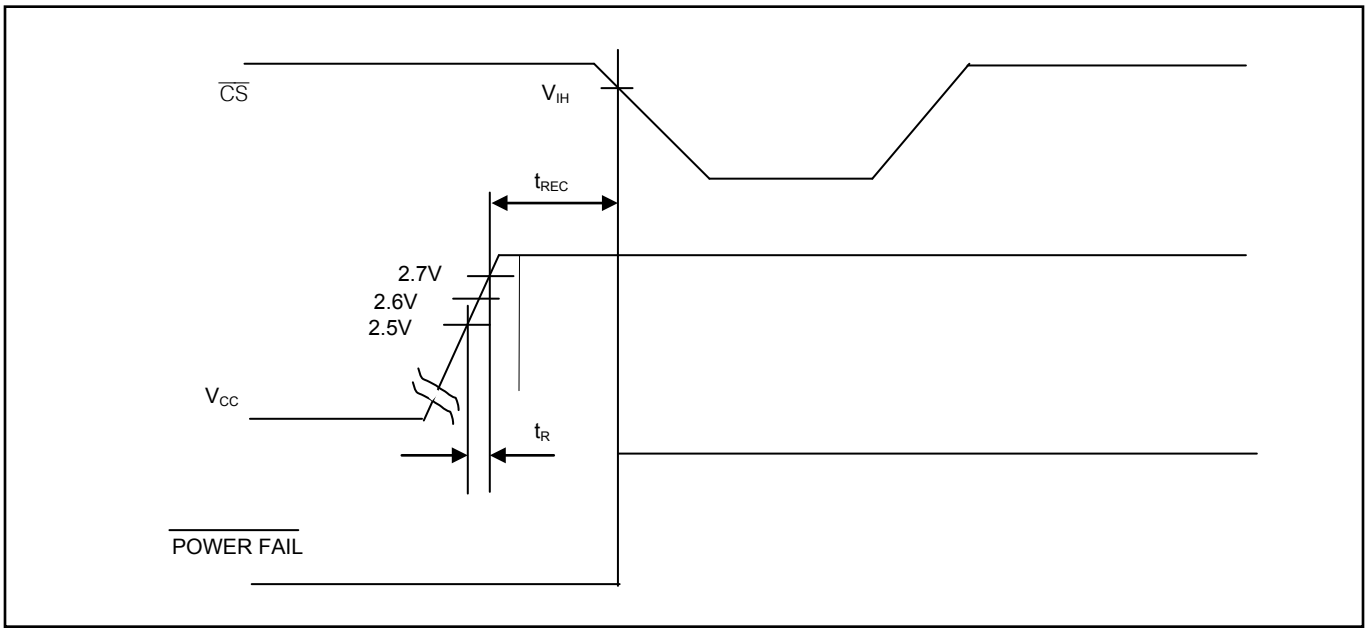
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance on All Inputs Except X1 and X2	C_{IN}			12	pF	
Output Capacitance on $\overline{IRQ}$, SQW and DQ pins	C_{OUT}			12	pF	

WAKE-UP/KICKSTART TIMING

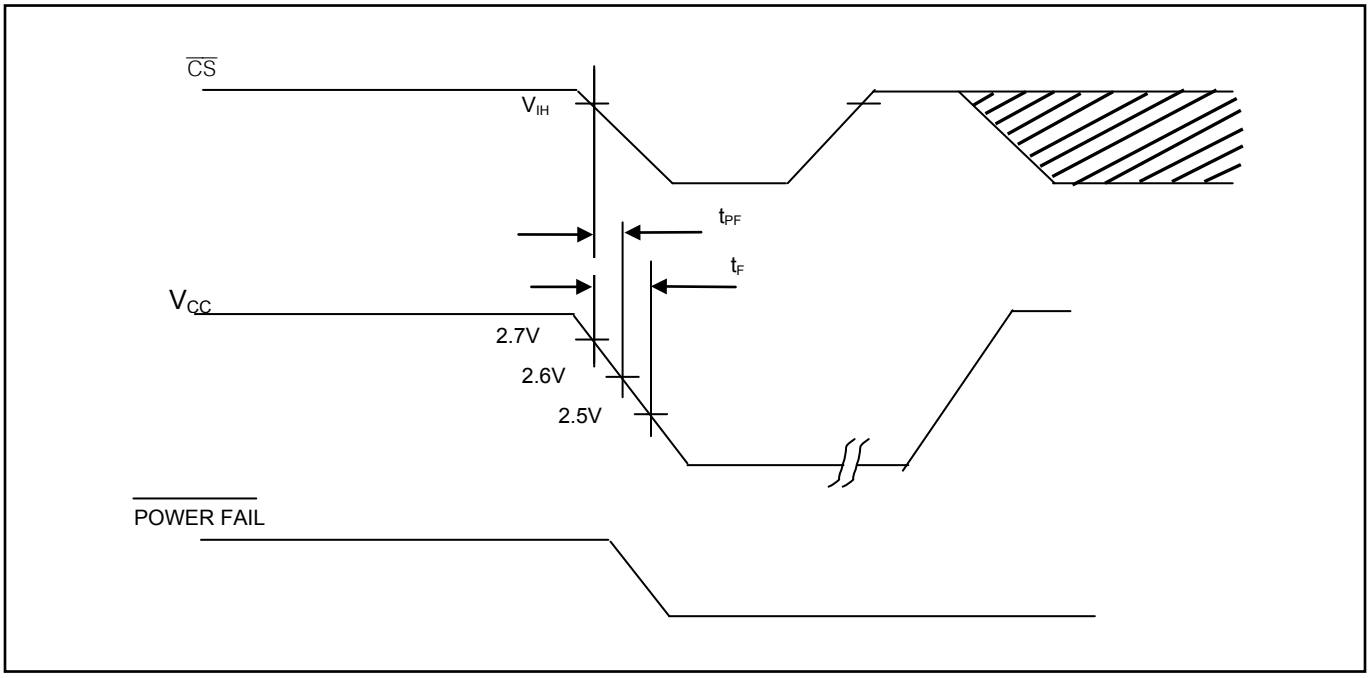
(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake-Up/Kickstart Power On Timeout	t_{POTO}	2			seconds	7

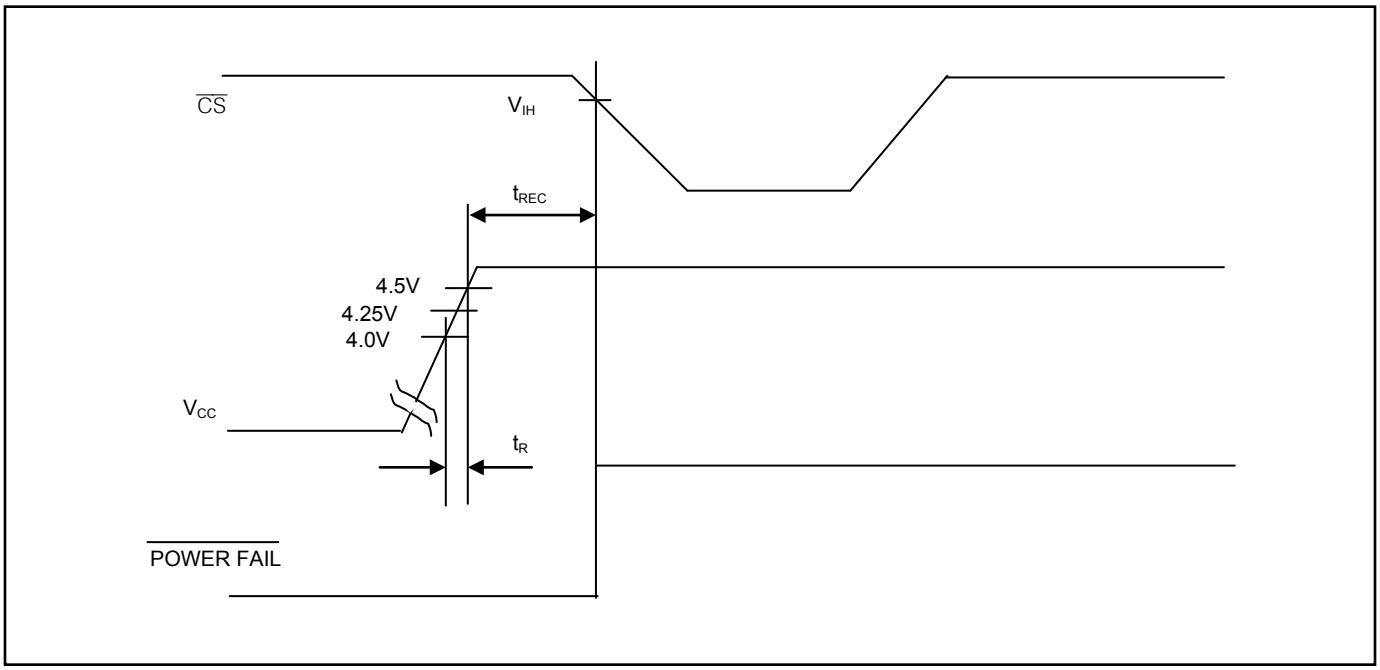
POWER-UP CONDITION—3V



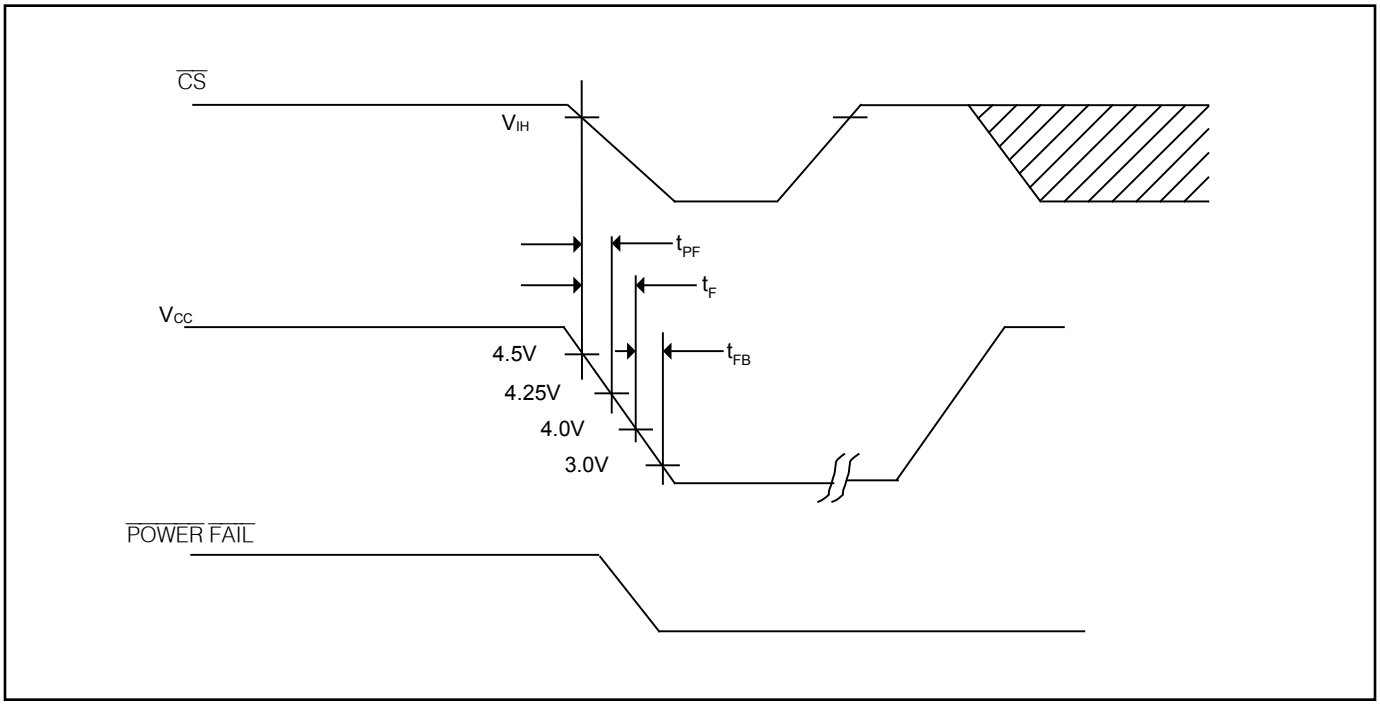
POWER-DOWN CONDITION—3V



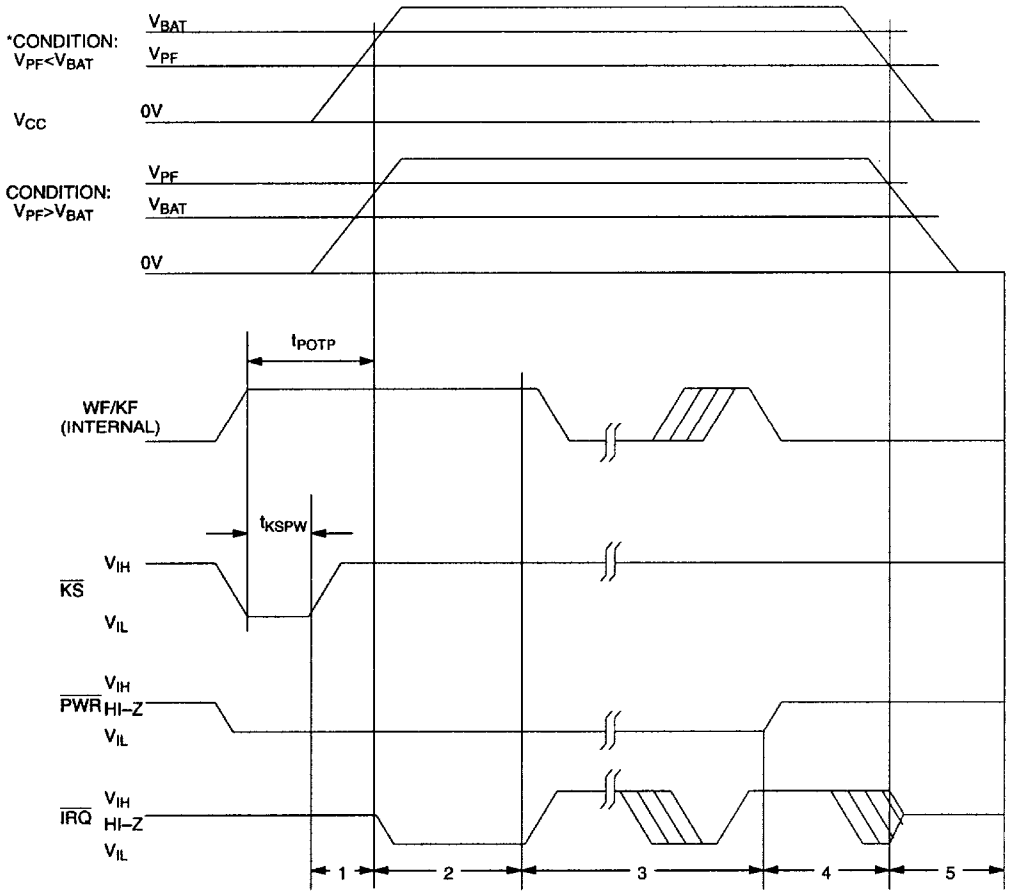
POWER-UP CONDITION—5V



POWER-DOWN CONDITION—5V



WAKE-UP/KICKSTART TIMING



*THIS CONDITION CAN OCCUR WITH THE 3V DEVICE.
NOTE: TIME INTERVALS SHOWN ABOVE ARE REFERENCED IN *WAKE-UP/KICKSTART* SECTION.

Note 1: All voltages are referenced to ground.

Note 2: Typical values are at +25°C and nominal supplies.

Note 3: Outputs are open.

Note 4: Applies to the AD0–AD7 pins and the SQW pin when each is in a high-impedance state.

Note 5: The $\overline{IRQ}$ and $\overline{PWR}$ pins are open-drain outputs.

Note 6: Measured with a load of 50pF + 1 TTL gate.

Note 7: Wake-up kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.

Note 8: V_{SW} is determined by the larger of V_{BAT} and V_{BAUX}.

Note 9: The DS1687 keeps time to an accuracy of ±1 minute per month at 25°C during data retention time for the period of t_{DR}.

Note 10: t_{DR} is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS1687 at 25°C.

Note 11: RTC Encapsulate DIP modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water washing techniques is acceptable, if ultrasonic vibration is not used.

Note 12: I_{BAT1} and I_{BAT2} are measured at V_{BAT} or V_{BAUX} = 3.5V and with recommended crystal type on X1 and X2.

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 PDIP	P24+3	21-0044
28 PLCC	Q28+4	21-0049
24 TSSOP	U24+1	21-0066
24 SO	W24+7	21-0042
24 EDIP	MDP24+2	21-0241

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
4/10	Removed the leaded parts from the *Ordering Information* table; updated the storage temperature ranges, added the lead temperature, and updated the soldering temperature for all packages in the *Absolute Maximum Ratings*.	2, 24
10/12	Correct Silicon Model number, correct hex address formatting.	15, 19, 20, 21

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000

© 2012 Maxim Integrated Products, Inc. Maxim Integrated and the Maxim Integrated logo are trademarks of Maxim Integrated Products, Inc.