# DS1922E

# iButton High-Temperature Logger with 8KB Datalog Memory

## General Description

The iButton® high-temperature logger (DS1922E) is a rugged, self-sufficient system that measures temperature and records the result in a protected memory section. The recording is done at a user-defined rate. A total of 8192 8-bit readings or 4096 16-bit readings, taken at equidistant intervals ranging from 1s to 273hr, can be stored. Additionally, 576 bytes of SRAM store application-specific information. A mission to collect data can be programmed to begin immediately, after a user-defined delay, or after a temperature alarm. Access to the memory and control functions can be password protected. The DS1922E is configured and communicates with a host-computing device through the serial 1-Wire® protocol, which requires only a single data lead and a ground return. Every DS1922E is factory lasered with a guaranteed unique 64-bit registration number that allows for absolute traceability. The durable stainless-steel package is highly resistant to environmental hazards such as dirt, moisture, and shock.

## Application

High-Temperature Logging (Process Monitoring, Industrial Temperature Monitoring)

Steam Sterilization

## Benefits and Features

- High Accuracy, Full-Featured Digital Temperature Logger Simplifies Temperature Data Collection and Dissemination of Electronic Temperature Record
  - Temperature Accuracy: ±1.5°C from +110°C to +140°C, ±7°C typical from +15°C to +110°C
  - Measures Temperature with 8-Bit (0.5°C) or 11-Bit (0.0625°C) Resolution
  - Operating Temperature Range: +15°C to +140°C
  - Automatically Wakes Up, Measures Temperature, and Stores Values in 8KB of Data-Log Memory in 8- or 16-Bit Format
  - Sampling Rate from 1s Up to 273hr
  - Programmable High and Low Trip Points for Temperature Alarms
  - Programmable Recording Start Delay After Elapsed Time or Upon a Temperature Alarm Trip Point
  - 576 Bytes of General-Purpose Memory
  - Two-Level Password Protection of All Memory and Configuration Registers
- Rugged Construction Survives Harsh Environments
  - Water Resistant or Waterproof if Placed Inside DS9107 iButton Capsule (Exceeds Water Resistant 3 ATM Requirements)
- Simple Serial Port Interfaces to Most Microcontrollers for Rapid Data Transfer
  - Communicates to Host with a Single Digital Signal Up to 15.4kbps at Standard Speed or Up to 125kbps in Overdrive Mode Using 1-Wire Protocol
  - Quick Access to Alarmed Devices Through 1-Wire Conditional Search Function

## Common iButton Device Features

- Rugged Chip-Based Data Carrier with Fast, Simple Access to Information
  - Digital Identification and Information by Momentary Contact
  - Unique Factory-Lasered 64-Bit Registration Number Ensures Error-Free Device Selection and Absolute Traceability Because No Two Parts Are Alike
  - Built-In Multidrop Controller for 1-Wire Net
  - Chip-Based Data Carrier Compactly Stores Information
  - Data Can Be Accessed While Affixed to an Object
  - Button Shape is Self-Aligning with Cup-Shaped Probes
  - Durable Stainless-Steel Case Engraved with Registration Number Withstands Harsh Environments
  - Easily Affixed with Self-Stick Adhesive Backing, Latched by Its Flange, or Locked with a Ring Pressed Onto Its Rim
  - Presence Detector Acknowledges When Reader First Applies Voltage

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| DS1922E-F5# | +15°C to +140°C | F5 Can |

*# Denotes a RoHS-compliant device that may include lead(Pb) that is exempt under the RoHS requirements.*

## Examples of Accessories

| PART | ACCESSORY |
|---|---|
| DS9093RA | Mounting Lock Ring |
| DS9107 | iButton Capsule |
| DS9490B | USB to 1-Wire Adapter |

***Pin Configuration* appears at end of data sheet.**

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## Absolute Maximum Ratings

I/O Voltage Range to GND .....-0.3V to +6V
I/O Sink Current.....20mA
Operating Temperature Range .....+15°C to +140°C
Junction Temperature.....+150°C
Storage Temperature Range.....-25°C to +140°C*

**Storage or operation above +50°C significantly reduces battery life with an upper limit of 300hr cumulative at +140°C. The recommended storage temperature for maximum battery lifetime is between +5°C and +35°C.*

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Characteristics

($V_{PUP}$ = 3.0V to 5.25V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Operating Temperature | $T_A$ | DS1922E (Note 1) | +15 | | +140 | °C |
| **I/O PIN GENERAL DATA** | | | | | | |
| 1-Wire Pullup Resistance | $R_{PUP}$ | (Notes 2, 3) | | | 2.2 | kΩ |
| Input Capacitance | $C_{IO}$ | (Note 4) | | 100 | 800 | pF |
| Input Load Current | $I_L$ | I/O pin at $V_{PUP}$ | | 6 | 10 | µA |
| High-to-Low Switching Threshold | $V_{TL}$ | (Notes 5, 6) | 0.4 | | 3.2 | V |
| Input Low Voltage | $V_{IL}$ | (Notes 2, 7) | | | 0.3 | V |
| Low-to-High Switching Threshold | $V_{TH}$ | (Notes 5, 8) | 0.7 | | 3.4 | V |
| Switching Hysteresis | $V_{HY}$ | (Note 9) | 0.09 | | N/A | V |
| Output Low Voltage | $V_{OL}$ | At 4mA (Note 10) | | | 0.4 | V |
| Recovery Time (Note 2) | $t_{REC}$ | Standard speed, $R_{PUP}$ = 2.2kΩ | 5 | | | µs |
| | | Overdrive speed, $R_{PUP}$ = 2.2kΩ | 2 | | | |
| | | Overdrive speed, directly prior to reset pulse; $R_{PUP}$ = 2.2kΩ | 5 | | | |
| Rising-Edge Hold-Off Time | $t_{REH}$ | (Note 11) | 0.6 | | 2.0 | µs |
| Time Slot Duration (Note 2) | $t_{SLOT}$ | Standard speed | 65 | | | µs |
| | | Overdrive speed, $V_{PUP}$ > 4.5V | 8 | | | |
| | | Overdrive speed (Note 12) | **9.5** | | | |
| **I/O PIN 1-Wire RESET, PRESENCE-DETECT CYCLE** | | | | | | |
| Reset Low Time (Note 2) | $t_{RSTL}$ | Standard speed, $V_{PUP}$ > 4.5V | 480 | | 720 | µs |
| | | Standard speed (Note 12) | **690** | | 720 | |
| | | Overdrive speed, $V_{PUP}$ > 4.5V | 48 | | 80 | |
| | | Overdrive speed (Note 12) | **70** | | 80 | |
| Presence-Detect High Time | $t_{PDH}$ | Standard speed, $V_{PUP}$ > 4.5V | 15 | | 60 | µs |
| | | Standard speed (Note 12) | 15 | | **63.5** | |
| | | Overdrive speed (Note 12) | 2 | | **7** | |

## Electrical Characteristics (continued)

($V_{PUP}$ = 3.0V to 5.25V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Presence-Detect Fall Time (Note 13) | $t_{FPD}$ | Standard speed, $V_{PUP}$ > 4.5V | 1.5 | | 5 | µs |
| | | Standard speed | 1.5 | | 8 | |
| | | Overdrive speed | 0.15 | | 1 | |
| Presence-Detect Low Time | $t_{PDL}$ | Standard speed, $V_{PUP}$ > 4.5V | 60 | | 240 | µs |
| | | Standard speed (Note 12) | 60 | | **287** | |
| | | Overdrive speed, $V_{PUP}$ > 4.5V (Note 12) | **7** | | 24 | |
| | | Overdrive speed (Note 12) | **7** | | **28** | |
| Presence-Detect Sample Time (Note 2) | $t_{MSP}$ | Standard speed, $V_{PUP}$ > 4.5V | 65 | | 75 | µs |
| | | Standard speed | 71.5 | | 75 | |
| | | Overdrive speed | 8 | | 9 | |
| **I/O PIN 1-Wire WRITE** | | | | | | |
| Write-Zero Low Time (Notes 2, 14) | $t_{W0L}$ | Standard speed | 60 | | 120 | µs |
| | | Overdrive speed, $V_{PUP}$ > 4.5V (Note 12) | 6 | | **12** | |
| | | Overdrive speed (Note 12) | **7.5** | | **12** | |
| Write-One Low Time (Notes 2, 14) | $t_{W1L}$ | Standard speed | 5 | | 15 | µs |
| | | Overdrive speed | 1 | | 1.95 | |
| **I/O PIN 1-Wire READ** | | | | | | |
| Read Low Time (Notes 2, 15) | $t_{RL}$ | Standard speed | 5 | | 15 - $\delta$ | µs |
| | | Overdrive speed | 1 | | 1.95 - $\delta$ | |
| Read Sample Time (Notes 2, 15) | $t_{MSR}$ | Standard speed | $t_{RL}$ + $\delta$ | | 15 | µs |
| | | Overdrive speed | $t_{RL}$ + $\delta$ | | 1.95 | |
| **REAL-TIME CLOCK (RTC)** | | | | | | |
| Accuracy | | | See the *RTC Accuracy* graph | | | Min/ Month |
| Frequency Deviation | $\Delta_F$ | 0°C to +125°C | -600 | | +60 | ppm |
| **TEMPERATURE CONVERTER** | | | | | | |
| Conversion Time (Note 16) | $t_{CONV}$ | 8-bit mode | 30 | | 75 | ms |
| | | 16-bit mode (11 bits) | 240 | | 600 | |
| Thermal Response Time Constant (Note 17) | $\tau_{RESP}$ | Can package | | 130 | | s |
| Conversion Error (Notes 18, 19) | $\Delta\vartheta$ | +15°C to +110°C (Note 20) | | ±7 | | °C |
| | | +110°C to +140°C | -1.5 | | +1.5 | |
| Temperature Cycles | $N_{TCY}$ | Cycle = ramp from +25°C to > +125°C and back to +25°C (Note 21) | | | 300 | Cycles |
| Operating Lifetime | $t_{LIFE}$ | Temperature > +125°C (Note 21) | | | 300 | Hours |

**Note 1:** Operation above +125°C is restricted to mission operations only. Communication and 1-Wire pin specifications are not specified for operation above +125°C.

**Note 2:** System requirement.

**Note 3:** Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that in the DS2480B can be required.

**Note 4:** Capacitance on the data pin could be 800pF when $V_{PUP}$ is first applied. If a 2.2k  resistor is used to pull up the data line 2.5µs after $V_{PUP}$ has been applied, the parasite capacitance does not affect normal communications.

**Note 5:** $V_{TL}$ and $V_{TH}$ are a function of the internal supply voltage, which is a function of $V_{PUP}$ and the 1-Wire recovery times. The $V_{TH}$ and $V_{TL}$ maximum specifications are valid at $V_{PUPMAX}$ (5.25V). In any case, $V_{TL} < V_{TH} < V_{PUP}$.

**Note 6:** Voltage below which, during a falling edge on I/O, a logic 0 is detected.

**Note 7:** The voltage on I/O must be less than or equal to $V_{ILMAX}$ whenever the master drives the line low.

**Note 8:** Voltage above which, during a rising edge on I/O, a logic 1 is detected.

**Note 9:** After $V_{TH}$ is crossed during a rising edge on I/O, the voltage on I/O must drop by $V_{HY}$ to be detected as logic 0.

**Note 10:** The I-V characteristic is linear for voltages less than 1V.

**Note 11:** The earliest recognition of a negative edge is possible at $t_{REH}$ after $V_{TH}$ has been previously reached.

**Note 12:** Numbers in **bold** are **not** in compliance with the published iButton device standards. See the *Comparison Table*.

**Note 13:** Interval during the negative edge on I/O at the beginning of a presence-detect pulse between the time at which the voltage is 90% of $V_{PUP}$ and the time at which the voltage is 10% of $V_{PUP}$.

**Note 14:** e in Figure 13 represents the time required for the pullup circuitry to pull the voltage on I/O up from $V_{IL}$ to $V_{TH}$. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - e$ and $t_{W0LMAX} + t_F - e$, respectively.

**Note 15:** d in Figure 13 represents the time required for the pullup circuitry to pull the voltage on I/O up from $V_{IL}$ to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.

**Note 16:** To conserve battery power, use 8-bit temperature logging whenever possible.

**Note 17:** This number was derived from a test conducted by Cemagref in Antony, France, in July 2000: www.cemagref.fr/English/index.htm Test Report No. E42.

**Note 18:** Includes +0.1°C/-0.2°C calibration chamber measurement uncertainty.

**Note 19:** **Warning:** Maxim data-logger products are 100% tested and calibrated at time of manufacture to ensure that they meet all data sheet parameters, including temperature accuracy. As with any sensor-based product, user shall be responsible for occasionally rechecking the temperature accuracy of the product to ensure it is still operating properly. Furthermore, as with all products of this type, when deployed in the field and subjected to handling, harsh environments, or other hazards/use conditions, there may be some extremely small but nonzero logger failure rate. In applications where the failure of any logger is a concern, user shall assure that redundant (or other primary) methods of testing and determining the handling methods, quality, and fitness of the articles and products are implemented to further mitigate any risk.

**Note 20:** Guaranteed by design and not production tested.

**Note 21:** Devices leave the factory after having been run through a few cycles above +125°C. This is required for calibration of the device but should not affect lifetime of the device as specified. However, this process results in a nonzero value in the Device Samples Counter register (0223h–0225h), which provides evidence the device has been factory calibrated.

## Comparison Table

| PARAMETER | LEGACY VALUES | | | | DS1922E VALUES | | | |
|---|---|---|---|---|---|---|---|---|
| | STANDARD SPEED (µs) | | OVERDRIVE SPEED (µs) | | STANDARD SPEED (µs) | | OVERDRIVE SPEED (µs) | |
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| $t_{SLOT}$ (including $t_{REC}$) | 61 | (undefined) | 7 | (undefined) | 65* | (undefined) | **9.5** | (undefined) |
| $t_{RSTL}$ | 480 | (undefined) | 48 | 80 | **690** | 720 | **70** | 80 |
| $t_{PDH}$ | 15 | 60 | 2 | 6 | 15 | **63.5** | 2 | **7** |
| $t_{PDL}$ | 60 | 240 | 8 | 24 | 60 | **287** | **7** | **28** |
| $t_{W0L}$ | 60 | 120 | 6 | 16 | 60 | 120 | **7.5** | **12** |

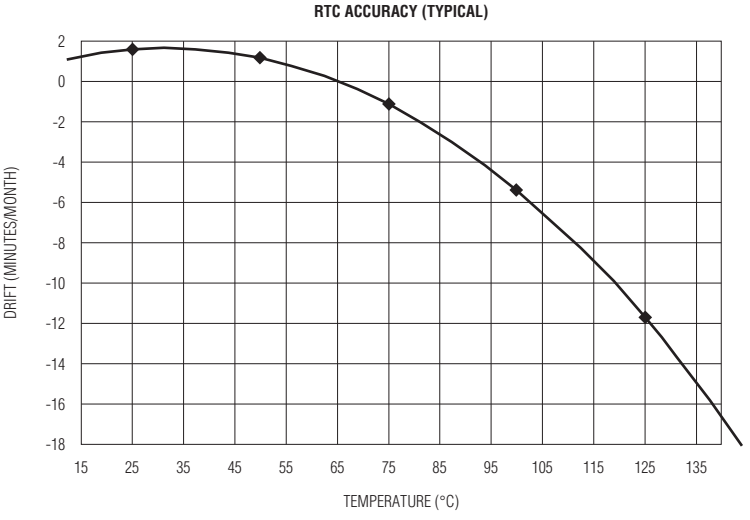
**Intentional change; longer recovery time requirement due to modified 1-Wire front-end.*

***Note:*** *Numbers in* ***bold*** *are* ***not*** *in compliance with the published iButton device standards.*

## iButton Can Physical Specification

| | |
|---|---|
| **SIZE** | See the *Package Information* section. |
| **WEIGHT** | Ca. 3.3 grams |

## RTC Accuracy



## Detailed Description

With its extended temperature range, the DS1922E is well suited to monitor processes that require temperatures well above the boiling point of water, such as pasteurization of food items. Note that the initial sealing level of the DS1922E achieves the equivalent of IP56. Aging and use conditions can degrade the integrity of the seal over time, so for applications with significant exposure to liquids, sprays, or other similar environments, it is recommended to place the DS1922E in the DS9107 iButton capsule. The DS9107 provides a watertight enclosure that has been rated to IP68 (refer to Application Note 4126: *Understanding the IP (Ingress Protection) Ratings of iButton Data Loggers and Capsules*). Software for setup and data retrieval through the 1-Wire interface is available for free download from the iButton device website (**www.ibutton.com**). This software also includes drivers for the serial and USB port of a PC and routines to access the general-purpose memory for storing application- or equipment-specific data files.

All iButton data loggers are calibrated/validated against NIST traceable reference devices. Maxim offers a web application to generate validation certificates for the DS1922L, DS1922T, DS1922E, and DS1923 (temperature portion only) data loggers. Input is the device's ROM code (or list of codes) and the output is a validation certificate in PDF format. For more information, refer to Application Note 4629: *iButton Data-Logger Calibration and NIST Certificate FAQs*.

### Overview

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS1922E. The device has five main data components: 64-bit lasered ROM; 256-bit scratchpad; 576-byte general-purpose SRAM; two 256-bit register pages of timekeeping, control, status, and counter registers, and passwords; and 8192 bytes of data-logging memory. Except for the ROM and the scratchpad, all other memory is arranged in a single linear address space. The data-logging memory, counter registers, and several other registers are read only for the user. Both register pages are write protected while the device is programmed for a mission. The password registers, one for a read password and another one for a read/write password, can only be written, never read.

Figure 2 shows the hierarchical structure of the 1-Wire protocol. The bus master must first provide one of the eight ROM function commands: Read ROM, Match ROM, Search ROM, Conditional Search ROM, Skip ROM, Overdrive-Skip ROM, Overdrive-Match ROM, or Resume Command. Upon completion of an Overdrive ROM command byte executed at standard speed, the device enters Overdrive Mode, where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 11. After a ROM function command is successfully executed, the memory and control functions become accessible and the master can provide any one of the eight available commands. The protocol for these memory and control function commands is described in Figure 9. **All data is read and written least significant bit first.**

### Parasite Power

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O input is high. I/O provides sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) By parasiting off this input, battery power is not consumed for 1-Wire ROM function commands, and 2) if the battery is exhausted for any reason, the ROM can still be read normally. The remaining circuitry of the DS1922E is solely operated by battery energy.

### 64-Bit Lasered ROM

Each DS1922E contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits (see Figure 3 for details). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products*.

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the last bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC returns the shift register to all 0s.

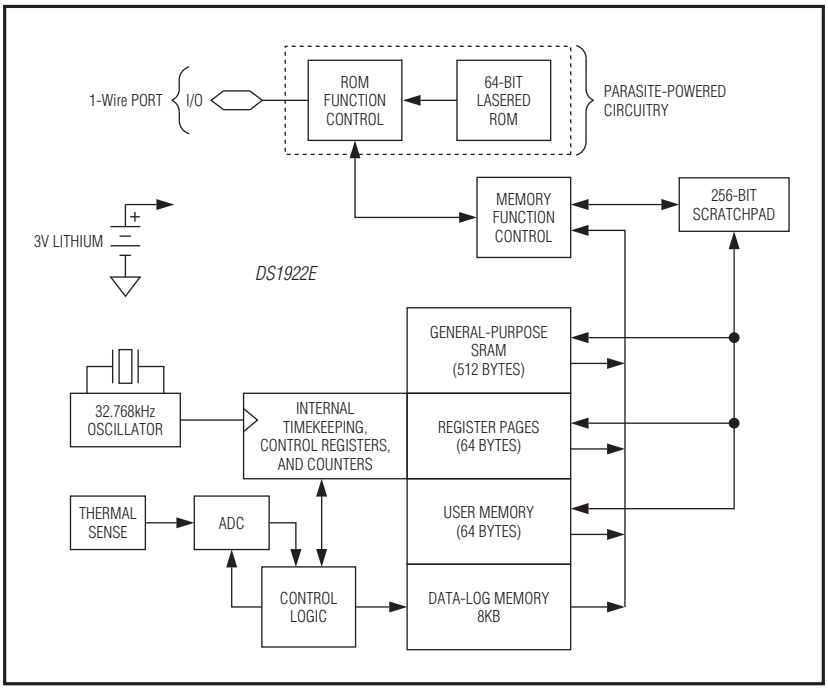



*Figure 1. Block Diagram*

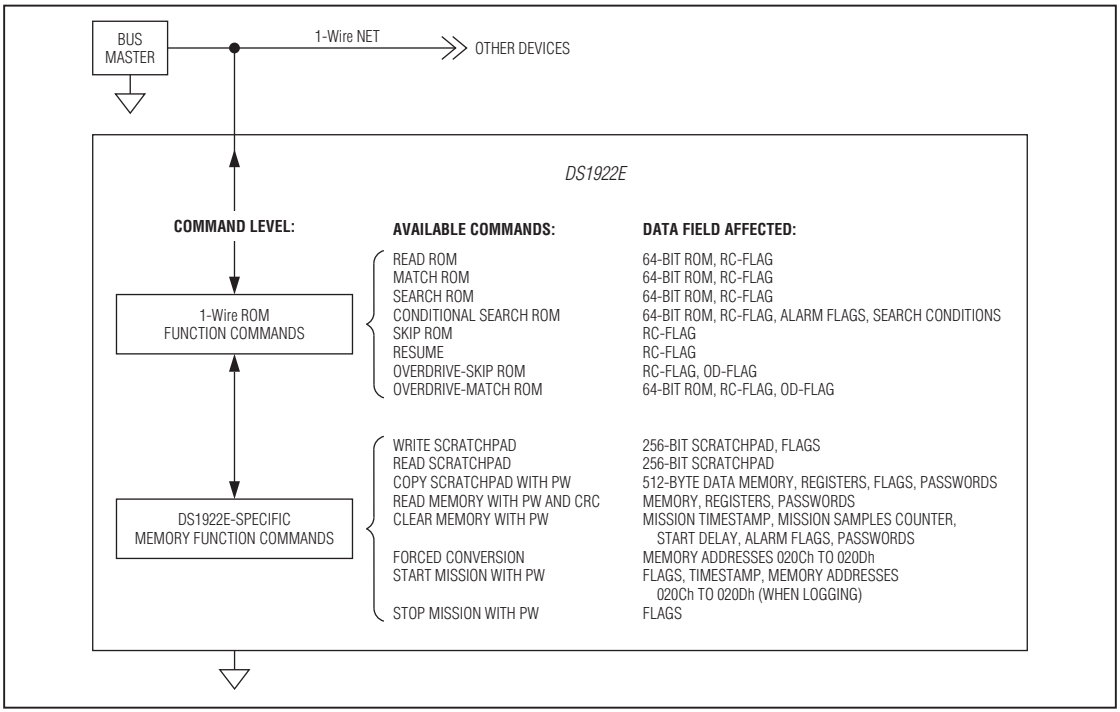



*Figure 2. Hierarchical Structure for 1-Wire Protocol*

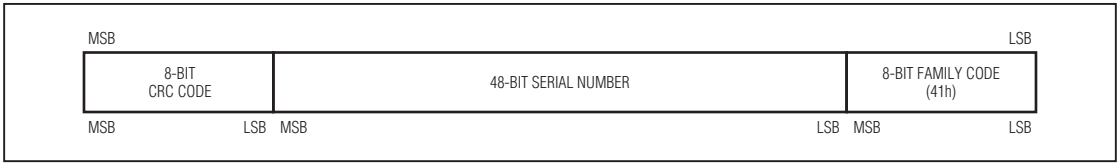



*Figure 3. 64-Bit Lasered ROM*

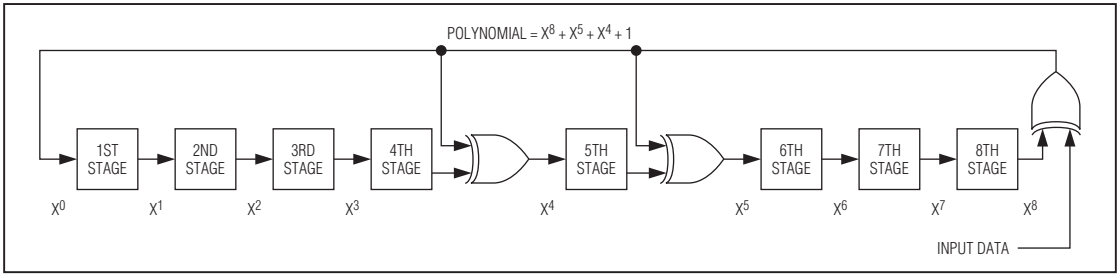



*Figure 4. 1-Wire CRC Generator*

## Memory

Figure 5 shows the DS1922E memory map. Pages 0 to 15 contain 512 bytes of general-purpose SRAM. The various registers to set up and control the device fill pages 16 and 17, called register pages 1 and 2 (see Figure 6 for details). Pages 18 and 19 can be used as extension of the general-purpose memory. The data-log logging memory starts at address 1000h (page 128) and extends over 256 pages. The memory pages 20 to 127 are reserved for future extensions. The scratchpad is an additional page that acts as a buffer when writing to the SRAM memory or the register page. The data memory can be written at any time. The access type for the register pages is register-specific and depends on whether the device is programmed for a mission. Figure 6 shows the details. The data-log memory is read only for the user. It is written solely under supervision of the on-chip control logic. Due to the special behavior of the write access logic (write scratchpad, copy scratchpad), it is recommended to only write full pages at a time. This also applies to the register pages. See the *Address Registers and Transfer Status* section for details.

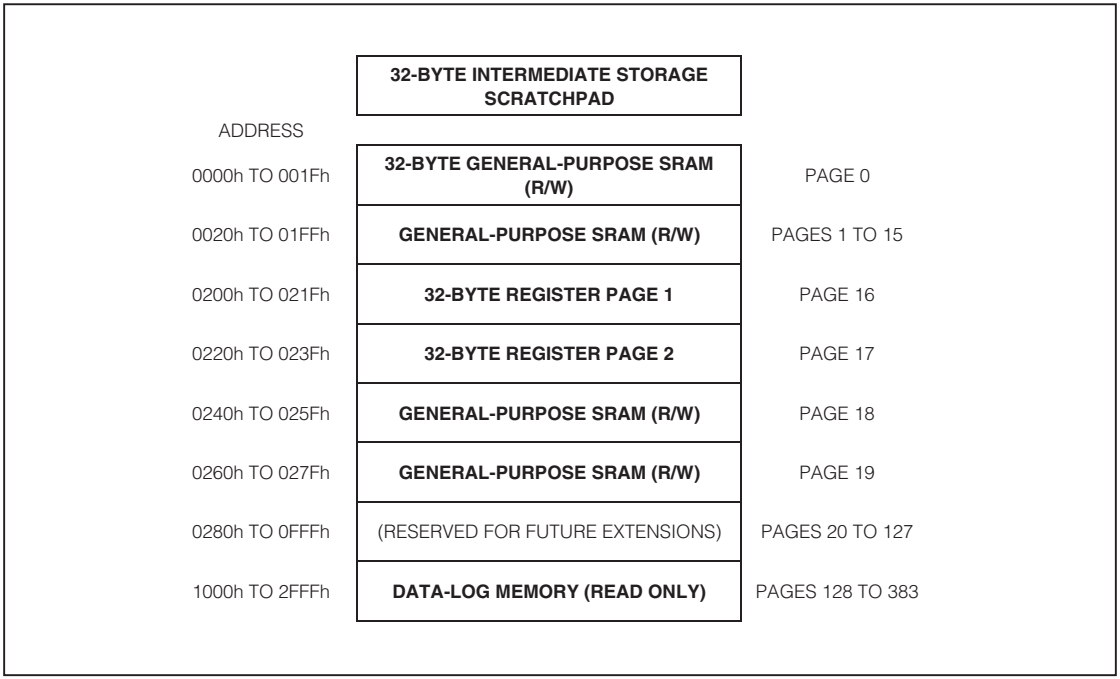



*Figure 5. Memory Map*

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | FUNCTION | ACCESS* | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0200h | 0 | 10 Seconds | | | Single Seconds | | | | Real-Time Clock Registers | R/W | R |
| 0201h | 0 | 10 Minutes | | | Single Minutes | | | | | | |
| 0202h | 0 | 12/24 | 20 Hour AM/PM | 10 Hour | Single Hours | | | | | | |
| 0203h | 0 | 0 | 10 Date | | Single Date | | | | | | |
| 0204h | CENT | 0 | 0 | 10 Months | Single Months | | | | | | |
| 0205h | 10 Years | | | | Single Years | | | | | | |
| 0206h | Low Byte | | | | | | | | Sample Rate | R/W | R |
| 0207h | 0 | 0 | High Byte | | | | | | | | |
| 0208h | Low Threshold | | | | | | | | Temperature Alarms | R/W | R |
| 0209h | High Threshold | | | | | | | | | | |
| 020Ah | (No Function with the DS1922E) | | | | | | | | — | R/W | R |
| 020Bh | (No Function with the DS1922E) | | | | | | | | | | |
| 020Ch | Low Byte | | | 0 | 0 | 0 | 0 | 0 | Latest Temperature | R | R |
| 020Dh | High Byte | | | | | | | | | | |
| 020Eh | (No Function with the DS1922E) | | | | | | | | — | R | R |
| 020Fh | (No Function with the DS1922E) | | | | | | | | | | |
| 0210h | 0 | 0 | 0 | 0 | 0 | 0 | ETHA | ETLA | Temperature Alarm Enable | R/W | R |
| 0211h | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | — | R/W | R |
| 0212h | 0 | 0 | 0 | 0 | 0 | 0 | EHSS | EOSC | RTC Control | R/W | R |
| 0213h | 1 | 1 | SUTA | RO | (X) | TLFS | 0 | ETL | Mission Control | R/W | R |
| 0214h | BOR | 1 | 1 | 1 | 0 | 0 | THF | TLF | Alarm Status | R | R |
| 0215h | 1 | 1 | 0 | WFTA | MEMCLR | 0 | MIP | 0 | General Status | R | R |
| 0216h | Low Byte | | | | | | | | Start Delay Counter | R/W | R |
| 0217h | Center Byte | | | | | | | | | | |
| 0218h | High Byte | | | | | | | | | | |

**The left entry in the ACCESS column is valid between missions. The right entry shows the applicable access type while a mission is in progress.*

*Figure 6. DS1922E Register Pages Map*

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | FUNCTION | ACCESS* | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0219h | 0 | 10 Seconds | | | Single Seconds | | | | Mission Timestamp | R | R |
| 021Ah | 0 | 10 Minutes | | | Single Minutes | | | | | | |
| 021Bh | 0 | 12/24 | 20 Hour AM/PM | 10 Hour | Single Hours | | | | | | |
| 021Ch | 0 | 0 | 10 Date | | Single Date | | | | | | |
| 021Dh | CENT | 0 | 0 | 10 Months | Single Months | | | | | | |
| 021Eh | 10 Years | | | | Single Years | | | | | | |
| 021Fh | (No Function; Reads 00h) | | | | | | | | — | R | R |
| 0220h | Low Byte | | | | | | | | Mission Samples Counter | R | R |
| 0221h | Center Byte | | | | | | | | | | |
| 0222h | High Byte | | | | | | | | | | |
| 0223h | Low Byte | | | | | | | | Device Samples Counter | R | R |
| 0224h | Center Byte | | | | | | | | | | |
| 0225h | High Byte | | | | | | | | | | |
| 0226h | Configuration Code | | | | | | | | Flavor | R | R |
| 0227h | EPW | | | | | | | | PW Control | R/W | R |
| 0228h | First Byte | | | | | | | | Read Access Password | W | — |
| … | … | | | | | | | | | | |
| 022Fh | Eighth Byte | | | | | | | | | | |
| 0230h | First Byte | | | | | | | | Full Access Password | W | — |
| … | … | | | | | | | | | | |
| 0237h | Eighth Byte | | | | | | | | | | |
| 0238h | (No Function; All These Bytes Read 00h) | | | | | | | | — | R | R |
| … | | | | | | | | | | | |
| 023Fh | | | | | | | | | | | |

**The left entry in the ACCESS column is valid between missions. The right entry shows the applicable access type while a mission is in progress.*

*Figure 6. DS1922E Register Pages Map (continued)*

## Detailed Register Descriptions

### Timekeeping and Calendar

The RTC and calendar information is accessed by reading/writing the appropriate bytes in the register page, address 0200h to 0205h. For readings to be valid, all RTC registers must be read sequentially starting at address 0200h. Some of the RTC bits are set to 0. These bits always read 0 regardless of how they are written. The number representation of the RTC registers is binary-coded decimal (BCD) format.

The DS1922E's RTC can run in either 12hr or 24hr mode. Bit 6 of the Hours register (address 0202h) is defined as the 12hr or 24hr mode select bit. When high, the 12hr mode is selected. In the 12hr mode, bit 5 is the AM/PM bit with logic 1 being PM. In the 24hr mode, bit 5 is the 20hr bit (20hr to 23hr). The CENT bit, bit 7 of the Months register, can be written by the user. This bit changes its state when the years counter transitions from 99 to 00.

The calendar logic is designed to automatically compensate for leap years. For every year value that is either 00 or a multiple of 4, the device adds a 29th of February. This works correctly up to (but not including) the year 2100.

### Sample Rate

The content of the Sample Rate register (addresses 0206h, 0207h) specifies the time elapse (in seconds if EHSS = 1, or minutes if EHSS = 0) between two temperature-logging events. The sample rate can be any value from 1 to 16,383, coded as an unsigned 14-bit binary number. If EHSS = 1, the shortest time between logging events is 1s and the longest (sample rate = 3FFFh) is 4.55hr. If EHSS = 0, the shortest is 1min and the longest time is 273.05hr (sample rate = 3FFFh). The EHSS bit is located in the RTC Control register at address 0212h. It is important that the user sets the EHSS bit accordingly while setting the Sample Rate register. **Writing a sample rate of 0000h results in a sample rate = 0001h, causing the DS1922E to log the temperature either every minute or every second depending upon the state of the EHSS bit.**

### RTC Registers

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0200h | 0 | 10 Seconds | | | Single Seconds | | | |
| 0201h | 0 | 10 Minutes | | | Single Minutes | | | |
| 0202h | 0 | 12/24 | 20 Hour AM/PM | 10 Hour | Single Hours | | | |
| 0203h | 0 | 0 | 10 Date | | Single Date | | | |
| 0204h | CENT | 0 | 0 | 10 Months | Single Months | | | |
| 0205h | 10 Years | | | | Single Years | | | |

***Note:*** *During a mission, there is only read access to these registers. Bit cells marked "0" always read 0 and cannot be written to 1.*

### Sample Rate Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0206h | Sample Rate Low | | | | | | | |
| 0207h | 0 | 0 | Sample Rate High | | | | | |

***Note:*** *During a mission, there is only read access to these registers. Bit cells marked "0" always read 0 and cannot be written to 1.*

### Temperature Conversion

The DS1922E's temperature range begins at +15°C and ends at +140°C. Temperature values are represented as an 8- or 16-bit unsigned binary number with a resolution of 0.5°C in 8-bit mode and 0.0625°C in 16-bit mode.

The higher temperature byte TRH is always valid. In 16-bit mode, only the three highest bits of the lower byte TRL are valid. The five lower bits all read 0. TRL is undefined if the device is in 8-bit temperature mode. An out-of-range temperature reading is indicated as 00h or 0000h when too cold and FFh or FFE0h when too hot.

With TRH and TRL representing the decimal equivalent of a temperature reading, the temperature value is calculated as:

$$J(°C) = TRH/2 + 14 + TRL/512 \text{ (16-bit mode, TLFS = 1, see address 0213h)}$$

$$J(°C) = TRH/2 + 14 \text{ (8-bit mode, TLFS = 0, see address 0213h)}$$

This equation is valid for converting temperature readings stored in the data-log memory as well as for data read from the Latest Temperature Conversion Result register.

To specify the temperature alarm thresholds, the previous equations are resolved to:

$$TALM = 2 \times J(°C) - 28$$

Because the temperature alarm threshold is only one byte, the resolution or temperature increment is limited to 0.5°C. The TALM value must be converted into hexadecimal format before it can be written to one of the Temperature Alarm Threshold registers (Low Alarm address 0208h; High Alarm address 0209h). Independent of the conversion mode (8- or 16-bit), only the most significant byte of a temperature conversion is used to determine whether an alarm is generated.

### Latest Temperature Conversion Result Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | BYTE |
|---|---|---|---|---|---|---|---|---|---|
| 020Ch | T2 | T1 | T0 | 0 | 0 | 0 | 0 | 0 | TRL |
| 020Dh | T10 | T9 | T8 | T7 | T6 | T5 | T4 | T3 | TRH |

## Table 1. Temperature Conversion Examples

| MODE | TRH | | TRL | | ϑ(°C) |
|---|---|---|---|---|---|
| | HEX | DECIMAL | HEX | DECIMAL | |
| 8-Bit | 54h | 84 | — | — | 56.0 |
| 8-Bit | 17h | 23 | — | — | 25.5 |
| 16-Bit | 54h | 84 | 00h | 0 | 56.0000 |
| 16-Bit | 17h | 23 | 60h | 96 | 25.6875 |

## Table 2. Temperature Alarm Threshold Examples

| ϑ(°C) | TALM | |
|---|---|---|
| | HEX | DECIMAL |
| 65.5 | 67h | 103 |
| 30.0 | 20h | 32 |

### Temperature Sensor Control Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0210h | 0 | 0 | 0 | 0 | 0 | 0 | ETHA | ETLA |

***Note:*** *During a mission, there is only read access to this register. Bits 2 to 7 have no function. They always read 0 and cannot be written to 1.*

### RTC Control Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0212h | 0 | 0 | 0 | 0 | 0 | 0 | EHSS | EOSC |

***Note:*** *During a mission, there is only read access to this register. Bits 2 to 7 have no function. They always read 0 and cannot be written to 1.*

### Temperature Sensor Alarm

The DS1922E has two Temperature Alarm Threshold registers (address 0208h, 0209h) to store values that determine whether a critical temperature has been reached. A temperature alarm is generated if the device measures an alarming temperature and the alarm signaling is enabled. The bits ETLA and ETHA that enable the temperature alarm are located in the Temperature Sensor Control register. The temperature alarm flags TLF and THF are found in the Alarm Status register at address 0214h.

**Bit 1: Enable Temperature High Alarm (ETHA).** This bit controls whether, during a mission, the temperature high alarm flag (THF) may be set, if a temperature conversion results in a value equal to or higher than the value in the Temperature High Alarm Threshold register. If ETHA is 1, temperature high alarms are enabled. If ETHA is 0, temperature high alarms are not generated.

**Bit 0: Enable Temperature Low Alarm (ETLA).** This bit controls whether, during a mission, the temperature low alarm flag (TLF) may be set, if a temperature conversion results in a value equal to or lower than the value in the Temperature Low Alarm Threshold register. If ETLA is 1, temperature low alarms are enabled. If ETLA is 0, temperature low alarms are not generated.

### RTC Control

To minimize the power consumption of a DS1922E, the RTC oscillator should be turned off when the device is not in use. The oscillator on/off bit is located in the RTC Control register. This register also includes the EHSS bit, which determines whether the sample rate is specified in seconds or minutes.

**Bit 1: Enable High-Speed Sample (EHSS).** This bit controls the speed of the sample rate counter. When set to logic 0, the sample rate is specified in minutes. When set to logic 1, the sample rate is specified in seconds.

**Bit 0: Enable Oscillator (EOSC).** This bit controls the crystal oscillator of the RTC. When set to logic 1, the oscillator starts. When written to logic 0, the oscillator stops and the device is in a low-power data-retention mode. This bit must be 1 for normal operation. A Forced Conversion or Start Mission command automatically starts the RTC by changing the EOSC bit to logic 1.

### Mission Control Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0213h | 1 | 1 | SUTA | RO | (X) | TLFS | 0 | ETL |

***Note:*** *During a mission, there is only read access to this register. Bits 6 and 7 have no function. They always read 1 and cannot be written to 0. Bits 1 and 3 control functions that are not available with the DS1922E. Bit 1 must be set to 0. Under this condition the setting of bit 3 becomes a "don't care."*

## Mission Control

The DS1922E is set up for its operation by writing appropriate data to its special function registers, which are located in the two register pages. The settings in the Mission Control register determine which format (8 or 16 bits) applies and whether old data can be overwritten by new data once the data-log memory is full. An additional control bit can be set to tell the DS1922E to wait with logging data until a temperature alarm is encountered.

**Bit 5: Start Mission Upon Temperature Alarm (SUTA).** This bit specifies whether a mission begins immediately (includes delayed start) or if a temperature alarm is required to start the mission. If this bit is 1, the device performs an 8-bit temperature conversion at the selected sample rate and begins with data logging only if an alarming temperature (high alarm or low alarm) was found. The first logged temperature is when the alarm occurred. However, the mission sample counter does not increment. This functionality is guaranteed by design and not production tested.

**Bit 4: Rollover Control (RO).** This bit controls whether, during a mission, the data-log memory is overwritten with new data or whether data logging is stopped once the data-log memory is full. Setting this bit to 1 enables the rollover and data logging continues at the beginning, overwriting previously collected data. If this bit is 0, the logging and conversions stop once the data-log memory is full. However, the RTC continues to run and the MIP bit remains set until the Stop Mission command is performed.

**Bit 2: Temperature Logging Format Selection (TLFS).** This bit specifies the format used to store temperature readings in the data-log memory. If this bit is 0, the data is stored in 8-bit format. If this bit is 1, the 16-bit format is used (higher resolution). With 16-bit format, the most significant byte is stored at the lower address.

**Bit 0: Enable Temperature Logging (ETL).** To set up the device for a temperature-logging mission, this bit must be set to logic 1. The recorded temperature values start at address 1000h.

### Alarm Status Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0214h | BOR | 1 | 1 | 1 | 0 | 0 | THF | TLF |

***Note:*** *There is only read access to this register. Bits 4 to 6 have no function. They always read 1. Bits 2 and 3 have no function with the DS1922E. They always read 0. The alarm status bits are cleared simultaneously when the Clear Memory Function is invoked. See memory and control functions for details.*

### General Status Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0215h | 1 | 1 | 0 | WFTA | MEMCLR | 0 | MIP | 0 |

***Note:*** *There is only read access to this register. Bits 0, 2, 5, 6, and 7 have no function.*

## Alarm Status

The fastest way to determine whether a programmed temperature threshold was exceeded during a mission is through reading the Alarm Status register. In a networked environment that contains multiple DS1922E devices, the devices that encountered an alarm can quickly be identified by means of the Conditional Search command (see the *1-Wire ROM Function Commands* section). The temperature alarm only occurs if enabled (see the *Temperature Sensor Alarm* section). The BOR alarm is always enabled.

**Bit 7: Battery-On Reset Alarm (BOR).** If this bit reads 1, the device has performed a power-on reset. This indicates that the device has experienced a shock big enough to interrupt the internal battery power supply. The device may still appear functional, but it has lost its factory calibration. Any data found in the data-log memory should be disregarded.

**Bit 1: Temperature High Alarm Flag (THF).** If this bit reads 1, there was at least one temperature conversion during a mission revealing a temperature equal to or higher than the value in the Temperature High Alarm register. A forced conversion can affect the THF bit. This bit can also be set with the initial alarm in the SUTA = 1 mode.

**Bit 0: Temperature Low Alarm Flag (TLF).** If this bit reads 1, there was at least one temperature conversion during a mission revealing a temperature equal to or lower than the value in the Temperature Low Alarm register. A forced conversion can affect the TLF bit. This bit can also be set with the initial alarm in the SUTA = 1 mode.

## General Status

The information in the General Status register tells the host computer whether a mission-related command was executed successfully. Individual status bits indicate whether the DS1922E is performing a mission, waiting for a temperature alarm to trigger the logging of data or whether the data from the latest mission has been cleared.

**Bit 4: Waiting for Temperature Alarm (WFTA).** If this bit reads 1, the Mission Start Upon Temperature Alarm was selected and the Start Mission command was successfully executed, but the device has not yet experienced the temperature alarm. This bit is cleared after a temperature alarm event, but is not affected by the Clear Memory command. Once set, WFTA remains set if a mission is stopped before a temperature alarm occurs. To clear WFTA manually before starting a new mission, set the high temperature alarm (address 0209h) to +15°C and perform a forced conversion.

**Bit 3: Memory Cleared (MEMCLR).** If this bit reads 1, the Mission Timestamp, mission samples counter, and all the alarm flags of the Alarm Status register have been cleared in preparation of a new mission. Executing the Clear Memory command clears these memory sections. The MEMCLR bit returns to 0 as soon as a new mission is started by using the Start Mission command. The memory must be cleared for a mission to start.

**Bit 1: Mission in Progress (MIP).** If this bit reads 1, the device has been set up for a mission and this mission is still in progress. The MIP bit returns from logic 1 to logic 0 when a mission is ended. See the Start Mission and Stop Mission function commands.

### Mission Start Delay Counter Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0216h | Delay Low Byte | | | | | | | |
| 0217h | Delay Center Byte | | | | | | | |
| 0218h | Delay High Byte | | | | | | | |

***Note:*** *During a mission, there is only read access to this register.*

### Mission Timestamp Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0219h | 0 | 10 Seconds | | | Single Seconds | | | |
| 021Ah | 0 | 10 Minutes | | | Single Minutes | | | |
| 021Bh | 0 | 12/24 | 20 Hours AM/PM | 10 Hours | Single Hours | | | |
| 021Ch | 0 | 0 | 10 Date | | Single Date | | | |
| 021Dh | CENT | 0 | 0 | 10 Months | Single Months | | | |
| 021Eh | 10 Years | | | | Single Years | | | |

***Note:*** *There is only read access to this register.*

### Mission Samples Counter Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0220h | Low Byte | | | | | | | |
| 0221h | Center Byte | | | | | | | |
| 0222h | High Byte | | | | | | | |

***Note:*** *There is only read access to this register.*

### Mission Start Delay

The content of the Mission Start Delay Counter register tells how many minutes must expire from the time a mission was started until the first measurement of the mission takes place (SUTA = 0) or until the device starts testing the temperature for a temperature alarm (SUTA = 1). The Mission Start Delay is stored as an unsigned 24-bit integer number. The maximum delay is 16,777,215min, equivalent to 11,650 days or roughly 31yr. If the start delay is nonzero and the SUTA bit is set to 1, first the delay must expire before the device starts testing for temperature alarms to begin logging data.

For a typical mission, the Mission Start Delay is 0. If a mission is too long for a single DS1922E to store all readings at the selected sample rate, one can use several devices and set the Mission Start Delay for the second device to start recording as soon as the memory of the first device is full, and so on. The RO bit in the Mission Control register (address 0213h) must be set to 0 to prevent overwriting of collected data once the data-log memory is full.

### Mission Timestamp

The Mission Timestamp register indicates the date and time of the first temperature sample of the mission. There is only read access to the Mission Timestamp register.

### Mission Progress Indicator

Depending on settings in the Mission Control register (address 0213h), the DS1922E logs temperature in 8-bit or 16-bit format. The Mission Samples Counter together with the starting address and the logging format (8 or 16 bits) provide the information to identify valid blocks of data that have been gathered during the current (MIP = 1) or latest mission (MIP = 0). See the *Data-Log Memory Usage* section for an illustration.

The number read from the mission samples counter indicates how often the DS1922E woke up during a mission to measure temperature. The number format is 24-bit unsigned integer. The mission samples counter is reset through the Clear Memory command.

### Device Samples Counter Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0223h | Low Byte | | | | | | | |
| 0224h | Center Byte | | | | | | | |
| 0225h | High Byte | | | | | | | |

***Note:*** *There is only read access to this register.*

### Device Configuration Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | PART |
|---|---|---|---|---|---|---|---|---|---|
| 0226h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DS2422 |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | DS1923 |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | DS1922L |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | DS1922T |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DS1922E |

***Note:*** *There is only read access to this register.*

### Password Control Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0227h | EPW | | | | | | | |

***Note:*** *During a mission, there is only read access to this register.*

## Other Indicators

The Device Samples Counter register is similar to the Mission Samples Counter register. During a mission this counter increments whenever the DS1922E wakes up to measure and log data and when the device is testing for a temperature alarm in SUTA mode. Between missions the counter increments whenever the Forced Conversion command is executed. This way the Device Samples Counter register functions like a gas gauge for the battery that powers the device.

The Device Samples Counter register is reset to zero when the device is assembled. The number format is 24-bit unsigned integer. The maximum number that can be represented in this format is 16,777,215. Due to the calibration and tests at the factory, new devices can have a count value of up to 35,000. The typical value is well below 10,000.

The code in the Device Configuration register allows the master to distinguish between the DS2422 chip and different versions of the DS1922 devices. The *Device Configuration Register* table shows the codes assigned to the various devices.

## Security by Password

The DS1922E is designed to use two passwords that control read access and full access. Reading from or writing to the scratchpad as well as the forced conversion command does not require a password. The password must be transmitted immediately after the command code of the memory or control function. If password checking is enabled, the password transmitted is compared to the passwords stored in the device. The data pattern stored in the Password Control register determines whether password checking is enabled.

To enable password checking, the EPW bits need to form a binary pattern of 10101010 (AAh). The default pattern of EPW is different from AAh. If the EPW pattern is different from AAh, any pattern is accepted as long as it has a length of exactly 64 bits. Once enabled, changing the passwords and disabling password checking requires the knowledge of the current full-access password.

### Read Access Password Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0228h | RP7 | RP6 | RP5 | RP4 | RP3 | RP2 | RP1 | RP0 |
| 0229h | RP15 | RP14 | RP13 | RP12 | RP11 | RP10 | RP9 | RP8 |
| … | … | | | | | | | |
| 022Eh | RP55 | RP54 | RP53 | RP52 | RP51 | RP50 | RP49 | RP48 |
| 022Fh | RP63 | RP62 | RP61 | RP60 | RP59 | RP58 | RP57 | RP56 |

***Note:*** *There is only write access to this register. Attempting to read the password reports all zeros. The password cannot be changed while a mission is in progress.*

### Full Access Password Register

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0230h | FP7 | FP6 | FP5 | FP4 | FP3 | FP2 | FP1 | FP0 |
| 0231h | FP15 | FP14 | FP13 | FP12 | FP11 | FP10 | FP9 | FP8 |
| … | … | | | | | | | |
| 0236h | FP55 | FP54 | FP53 | FP52 | FP51 | FP50 | FP49 | FP48 |
| 0237h | FP63 | FP62 | FP61 | FP60 | FP59 | FP58 | FP57 | FP56 |

***Note:*** *There is only write access to this register. Attempting to read the password reports all zeros. The password cannot be changed while a mission is in progress.*

**Before enabling password checking, passwords for read-only access as well as for full access (read/write/control) must be written to the password registers. Setting up a password or enabling/disabling the password checking is done in the same way as writing data to a memory location; only the address is different. Since they are located in the same memory page, both passwords can be redefined at the same time.**

The Read Access Password must be transmitted exactly in the sequence RP0, RP1…RP62, RP63. This password only applies to the Read Memory with CRC function. The DS1922E delivers the requested data only if the password transmitted by the master was correct or if password checking is not enabled.

The Full Access Password must be transmitted exactly in the sequence FP0, FP1…FP62, FP63. It affects the functions Read Memory with CRC, Copy Scratchpad, Clear Memory, Start Mission, and Stop Mission. The DS1922E executes the command only if the password transmitted by the master was correct or if password checking is not enabled.

Due to the special behavior of the write-access logic, the Password Control register and both passwords must be written at the same time. When setting up new passwords, always verify (read back) the scratchpad before sending the Copy Scratchpad command. After a new password is successfully copied from the scratchpad to its memory location, erase the scratchpad by filling it with new data (Write Scratchpad command). Otherwise, a copy of the passwords remains in the scratchpad for public read access.

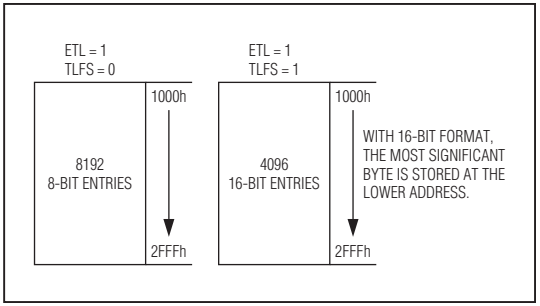



*Figure 7. Temperature Logging*

## Data-Log Memory Usage

Once set up for a mission, the DS1922E logs the temperature measurements at equidistant time points entry after entry in its data-log memory. The data-log memory can store 8192 entries in 8-bit format or 4096 entries in 16-bit format (Figure 7). In 16-bit format, the higher 8 bits of an entry are stored at the lower address. Knowing the starting time point (Mission Timestamp) and the interval between temperature measurements, one can reconstruct the time and date of each measurement.

There are two alternatives to the way the DS1922E behaves after the data-log memory is filled with data. The user can program the device to either stop any further recording (disable rollover) or overwrite the previously recorded data (enable rollover), one entry at a time, starting again at the beginning of the respective memory section. The contents of the Mission Samples Counter in conjunction with the sample rate and the Mission Timestamp allow reconstructing the time points of all values stored in the data-log memory. This gives the exact history over time for the most recent measurements taken. Earlier measurements cannot be reconstructed.

## Missioning

The typical task of the DS1922E is recording temperature. Before the device can perform this function, it needs to be set up properly. This procedure is called missioning.

First, the DS1922E must have its RTC set to a valid time and date. This reference time can be the local time, or, when used inside of a mobile unit, UTC (also called GMT, Greenwich Mean Time), or any other time standard that was agreed upon. The RTC oscillator must be running (EOSC = 1). The memory assigned to store the mission timestamp, mission samples counter, and alarm flags must be cleared using the Memory Clear command. To enable the device for a mission, the ETL bit must be set to 1. These are general settings that must be made in any case, regardless of the type of object to be monitored and the duration of the mission.

If alarm signaling is desired, the temperature alarm low and high thresholds must be defined. See the *Temperature Conversion* section for how to convert a temperature value into the binary code to be written to the threshold registers. In addition, the temperature alarm must be enabled for the low and/or high threshold. This makes the device respond to a Conditional Search command (see the *1-Wire ROM Function Commands* section), provided that an alarming condition has been encountered.

The setting of the RO bit (rollover enable) and sample rate depends on the duration of the mission and the monitoring requirements. If the most recently logged data is important, the rollover should be enabled (RO = 1). Otherwise, one should estimate the duration of the mission in minutes and divide the number by 8192 (8-bit format) or 4096 (16-bit format) to calculate the value of the sample rate (number of minutes between conversions). For example, if the estimated duration of a mission is 10 days (= 14400min), the 8192-byte capacity of the data-log memory would be sufficient to store a new 8-bit value every 1.8min (110s). If the DS1922E's data-log memory is not large enough to store all readings, one can use several devices and set the mission start delay to values that make the second device start logging as soon as the memory of the first device is full, and so on. The RO bit must be set to 0 to disable rollover that would otherwise overwrite the logged data.

After the RO bit and the mission start delay are set, the sample rate must be written to the Sample Rate register. The sample rate can be any value from 1 to 16,383, coded as an unsigned 14-bit binary number. The fastest sample rate is one sample per second (EHSS = 1, sample rate = 0001h) and the slowest is one sample every 273.05hr (EHSS = 0, sample rate = 3FFFh). To get one sample every 6min, for example, the sample rate value must be set to 6 (EHSS = 0) or 360 decimal (equivalent to 0168h at EHSS = 1).

If there is a risk of unauthorized access to the DS1922E or manipulation of data, one should define passwords for read access and full access. Before the passwords become effective, their use must be enabled. See the *Security by Password* section for more details.

The last step to begin a mission is to issue the Start Mission command. As soon as it has received this command, the DS1922E sets the MIP flag and clears the MEMCLR flag. With the Immediate/Delayed Start Mode (SUTA = 0), after as many minutes as specified by the mission start delay are over, the device wakes up, copies the current date and time to the Mission Timestamp register, and logs the first entry of the mission. This increments both the mission samples counter and device samples counter. All subsequent log entries are made as specified by the value in the Sample Rate register and the EHSS bit.

If the Start Upon Temperature Alarm mode is chosen (SUTA = 1) and temperature logging is enabled (ETL = 1), the DS1922E first waits until the start delay is over. Then the device wakes up in intervals as specified by the sample rate and EHSS bit and measures the temperature. This increments the Device Samples Counter register only. The first sample of the mission is logged when the temperature alarm occurred. However, the Mission Sample Counter does not increment. One sample period later the Mission Timestamp register is set. From then on, both the Mission Samples Counter and Device Samples Counter registers increment at the same time. All subsequent log entries are made as specified by the value in the Sample Rate register and the EHSS bit.

The general-purpose memory operates independently of the other memory sections and is not write protected during a mission. All the DS1922E's memory can be read at any time, e.g., to watch the progress of a mission. Attempts to read the passwords read 00h bytes instead of the data that is stored in the password registers.

## Memory Access

### Address Registers and Transfer Status

Because of the serial data transfer, the DS1922E employs three address registers called TA1, TA2, and E/S (Figure 8). Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is sent to the master upon a Read command. Register E/S acts like a byte counter and transfer status register. It is used to verify data integrity with Write commands. Therefore, the master only has read access to this register. The lower 5 bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called ending offset. **The DS1922E requires that the ending offset is always 1Fh for a Copy Scratchpad to function.** Bit 5 of the E/S register, called PF or partial byte flag, is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 is always a 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad, where intermediate storage of data begins. This address is called byte offset. If the target address for a Write command is 13Ch, for example, the scratchpad stores incoming data beginning at the byte offset 1Ch and is full after

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TARGET ADDRESS (TA1) | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| TARGET ADDRESS (TA2) | T15 | T14 | T13 | T12 | T11 | T10 | T9 | T8 |
| ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY) | AA | 0 | PF | E4 | E3 | E2 | E1 | E0 |

*Figure 8. Address Registers*

only 4 bytes. The corresponding ending offset in this example is 1Fh. For best economy of speed and efficiency, the target address for writing should point to the beginning of a page, i.e., the byte offset is 0. Thus, the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1Fh. The ending offset together with the PF flag are a means to support the master checking the data integrity after a Write command. The highest valued bit of the E/S register, called authorization accepted (AA), indicates that a valid Copy command for the scratchpad has been received and executed. Writing data to the scratchpad clears this flag.

### Writing with Verification

To write data to the DS1922E, the scratchpad must be used as intermediate storage. First, the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. In the next step, the master sends the Read Scratchpad command to read the scratchpad and to verify data integrity. As preamble to the scratchpad data, the DS1922E sends the requested target address TA1 and TA2 and the contents of the E/S Register. If the PF flag is set, data did not arrive correctly in the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the Write command was not recognized by the device. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue verifying every data bit. After the master has verified the data, it must send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2, and E/S, as the master has read them verifying the scratchpad. As soon as the DS1922E has received these bytes, it copies the data to the requested location beginning at the target address.

## Memory and Control Function Commands

Figure 9 shows the protocols necessary for accessing the memory and the special function registers of the DS1922E. An example on how to use these and other functions to set up the DS1922E for a mission is included in the *Mission Example: Prepare and Start a New Mission* section. The communication between the master and the DS1922E takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into the Overdrive Mode the DS1922E assumes standard speed. Internal memory access during a mission has priority over external access through the 1-Wire interface. This affects several commands in this section. See the *Memory Access Conflicts* section for details and solutions.

### Write Scratchpad Command [0Fh]

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset T[4:0]. The master must send as many bytes as are needed to reach the ending offset of 1Fh. If a data byte is incomplete, its content is ignored and the partial byte flag PF is set.

When executing the Write Scratchpad command, the CRC generator inside the DS1922E calculates a CRC of the entire data stream, starting at the command code and ending at the last data byte sent by the master (Figure 15). This CRC is generated using the CRC-16 polynomial by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses TA1 and TA2 as supplied by the master, and all the data bytes. If the ending offset is 11111b, the master can send 16 read time slots and receive the inverted CRC-16 generated by the DS1922E.

Note that both register pages are write protected during a mission. Although the Write Scratchpad command works normally at any time, the subsequent copy scratchpad to a register page fails during a mission.

### Read Scratchpad Command [AAh]

This command is used to verify scratchpad data and target address. After issuing the Read Scratchpad command, the master begins reading. The first 2 bytes are the target address. The next byte is the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset T[4:0], as shown in Figure 8. The master can continue reading data until the end of the scratchpad after which it receives an inverted CRC-16 of the command code, target addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. After the CRC is read, the bus master reads logic 1s from the DS1922E until a reset pulse is issued.

### Copy Scratchpad with Password [99h]

This command is used to copy data from the scratchpad to the writable memory sections. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern, which can be obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). Next, the master must transmit the 64-bit full-access password. If passwords are enabled and the transmitted password is different from the stored full-access password, the Copy Scratchpad with Password command fails. The device stops communicating and waits for a reset pulse. If the password was correct or if passwords were not enabled, the device tests the 3-byte authorization code. If the authorization code pattern matches, the AA flag is set and the copy begins. A pattern of alternating 1s and 0s is transmitted after the data has been copied until the master issues a reset pulse. While the copy is in progress, any attempt to reset the part is ignored. Copy typically takes 2µs per byte.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset are copied, starting at the target address. The AA flag remains at logic 1 until it is cleared by the next Write Scratchpad command. With suitable password, the copy scratchpad always functions for the 16 pages of data memory and the 2 pages of calibration memory. While a mission is in progress, write attempts to the register pages are not successful. The AA bit remaining at 0 indicates this.

### Read Memory with Password and CRC [69h]

The Read Memory with CRC command is the general function to read from the device. This command generates and transmits a 16-bit CRC following the last data byte of a memory page.

After having sent the command code of the Read Memory with CRC command, the bus master sends a 2-byte address that indicates a starting byte location. Next, the master must transmit one of the 64-bit passwords. If passwords are enabled and the transmitted password does not match one of the stored passwords, the Read Memory with Password and CRC command fails. The device stops communicating and waits for a reset pulse. If the password was correct or if passwords were not enabled, the master reads data from the DS1922E beginning from the starting address and continuing until the end of a 32-byte page is reached. At that point the bus master sends 16 additional read data time slots and receives the inverted 16-bit CRC. With subsequent read data time slots the master receives data starting at the beginning of the next memory page followed again by the CRC for that page. This sequence continues until the bus master resets the device. When trying to read the passwords or memory areas that are marked as “reserved,” the DS1922E transmits 00h or FFh bytes, respectively. The CRC at the end of a 32-byte memory page is based on the data as it was transmitted.

With the initial pass through the Read Memory with CRC flow, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator followed by the two address bytes and the contents of the data memory. Subsequent passes through the Read Memory with CRC flow generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the contents of the data memory page. After the 16-bit CRC of the last page is read, the bus master receives logic 1s from the DS1922E until a reset pulse is issued. The Read Memory with CRC command sequence can be ended at any point by issuing a reset pulse.

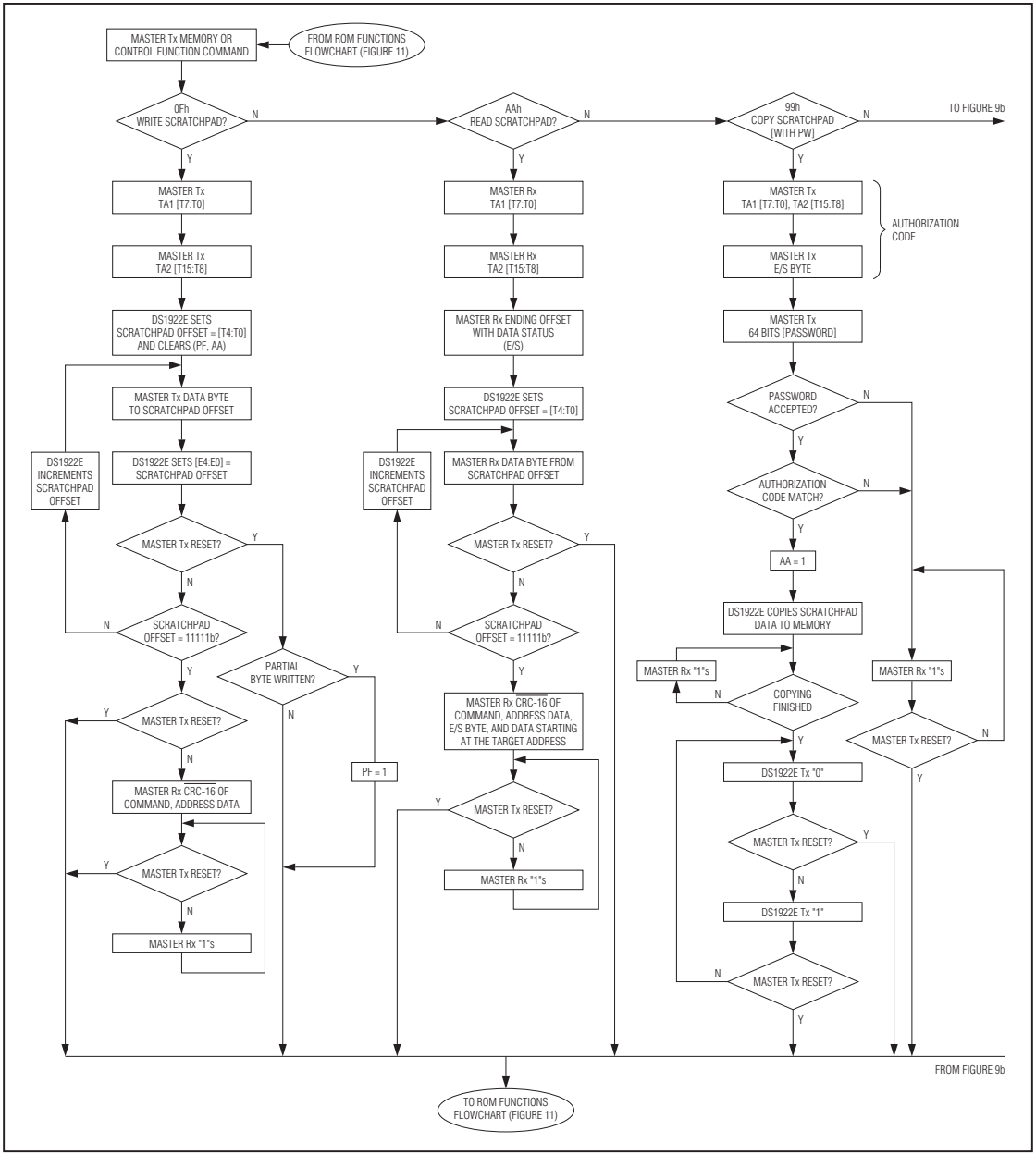



*Figure 9a. Memory/Control Function Flowchart*

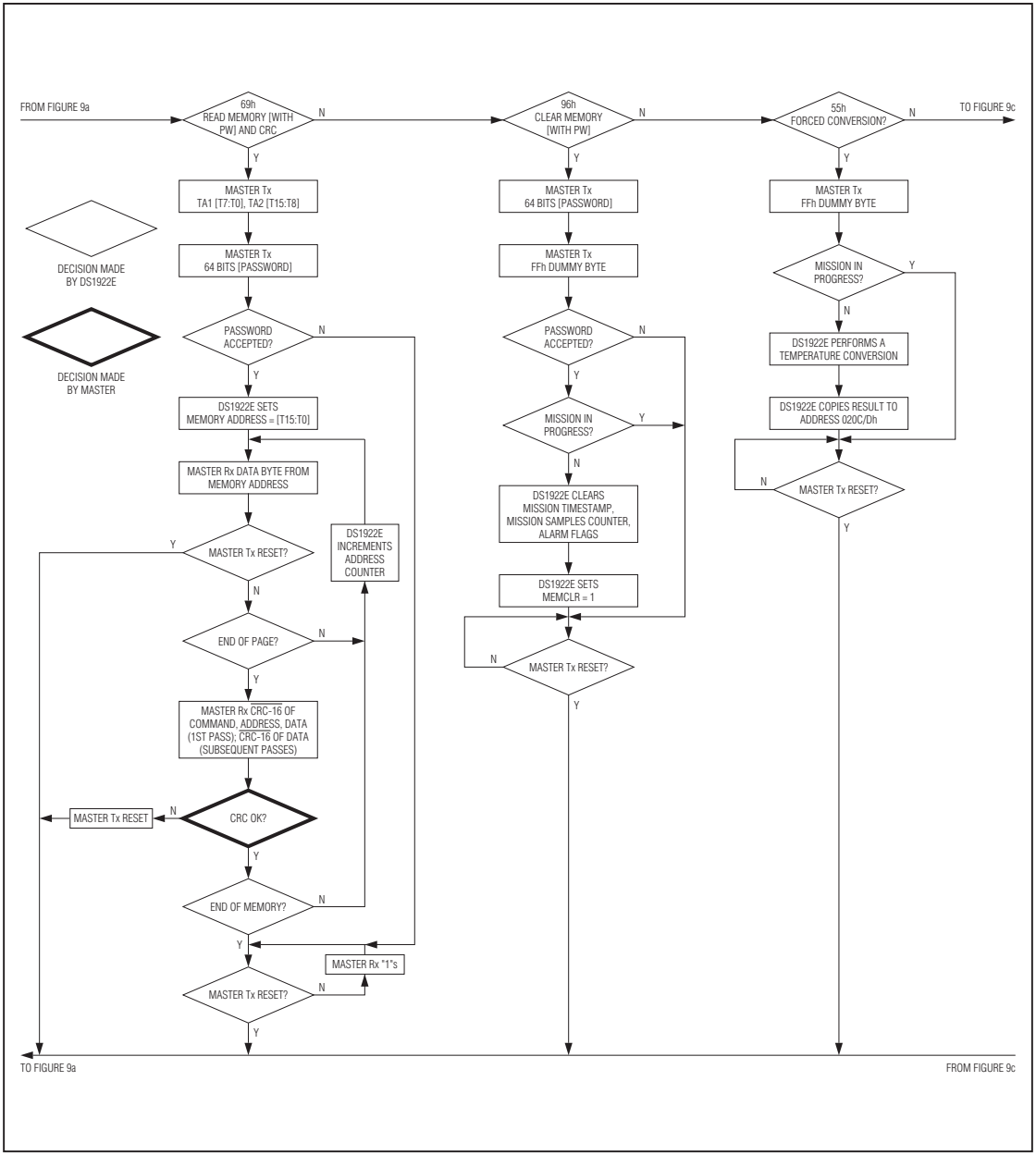



*Figure 9b. Memory/Control Function Flowchart (continued)*

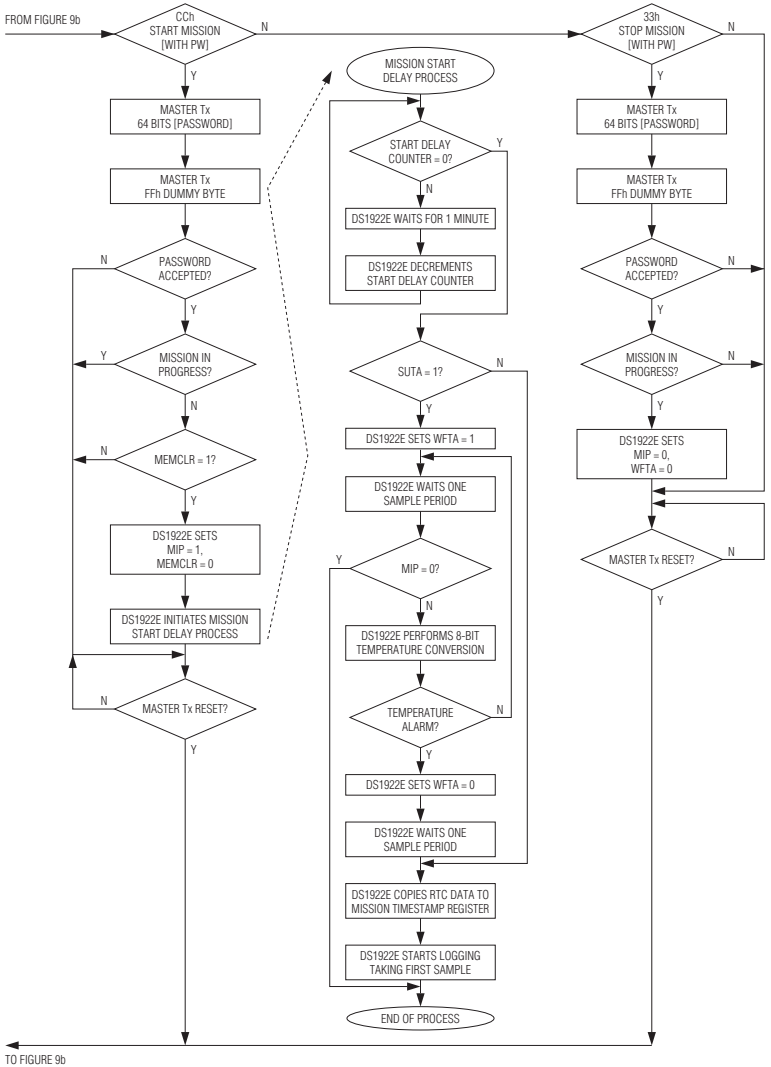



*Figure 9c. Memory/Control Function Flowchart (continued)*

### Clear Memory with Password [96h]

The Clear Memory with Password command is used to prepare the device for another mission. This command is only executed if no mission is in progress. After the command code the master must transmit the 64-bit full-access password followed by an FFh dummy byte. If passwords are enabled and the transmitted password is different from the stored full-access password or a mission is in progress, the Clear Memory with Password command fails. The device stops communicating and waits for a reset pulse. If the password was correct or if passwords were not enabled, the device clears the Mission Timestamp register, Mission Samples Counter register, and all alarm flags of the Alarm Status register. After these cells are cleared, the MEMCLR bit of the General Status register reads 1 to indicate the successful execution of the Clear Memory with Password command. Clearing of the data-log memory is not necessary because the mission samples counter indicates how many entries in the data-log memory are valid.

### Forced Conversion [55h]

The Forced Conversion command can be used to measure the temperature without starting a mission. After the command code, the master must send one FFh byte to get the conversion started. The conversion result is found as a 16-bit value in the Latest Temperature Conversion Result register. This command is only executed if no mission is in progress (MIP = 0). It cannot be interrupted and takes maximum 600ms to complete. During this time memory access through the 1-Wire interface is blocked. The device behaves the same way as during a mission when the sampling interferes with a memory/control function command. See the *Memory Access Conflicts* section for details.

### Start Mission with Password [CCh]

The DS1922E uses a control function command to start a mission. A new mission can only be started if the previous mission has been ended and the memory has been cleared. After the command code, the master must transmit the 64-bit full-access password followed by an FFh dummy byte. If passwords are enabled and the transmitted password is different from the stored full-access password or a mission is in progress, the Start Mission with Password command fails. The device stops communicating and waits for a reset pulse. If the password was correct or if passwords were not enabled, the device starts a mission. If SUTA = 0, the sampling begins as soon as the mission start delay is over. If SUTA = 1, the first sample is written to the data-log memory at the time the temperature alarm occurred. However, the mission sample counter does **not** increment. One sample period later, the Mission Timestamp register is set and the regular sampling and logging begins. While the device is waiting for a temperature alarm to occur, the WFTA flag in the General Status register reads 1. During a mission there is only read access to the register pages.

### Stop Mission with Password [33h]

The DS1922E uses a control function command to stop a mission. Only a mission that is in progress can be stopped. After the command code, the master must transmit the 64-bit full-access password followed by a FFh dummy byte. If passwords are enabled and the transmitted password is different from the stored full-access password or a mission is not in progress, the Stop Mission with Password command fails. The device stops communicating and waits for a reset pulse. If the password was correct or if passwords were not enabled, the device clears the MIP bit in the General Status register and restores write access to the register pages. The WFTA bit is not cleared. See the description of the General Status register for a method to clear the WFTA bit.

## Memory Access Conflicts

While a mission is in progress or while the device is waiting for a temperature alarm to start a mission, periodically a temperature sample is taken and logged. This “internal activity” has priority over 1-Wire communication. As a consequence, device-specific commands (excluding ROM function commands and 1-Wire reset) do not perform properly when internal and “external” activities interfere with each other. Not affected are the commands Start Mission, Forced Conversion, and Clear Memory, because they are not applicable while a mission is in progress or while the device is waiting for a temperature alarm. Table 3 explains how the remaining five commands are affected by internal activity, how to detect this interference, and how to work around it.

The interference is more likely to be seen with a high-sample rate (one sample every second) and with high-resolution logging, which can last up to 600ms. With lower sample rates, interference may hardly be visible at all. In any case, when writing driver software it is important to know about the possibility of interference and to take measures to work around it.

## Table 3. Memory Access Conflicts and Solutions

| COMMAND | INDICATION OF INTERFERENCE | SOLUTION |
|---|---|---|
| Write Scratchpad | The CRC-16 at the end of the command flow reads FFFFh. | Wait 0.5s, 1-Wire reset, address the device, repeat Write Scratchpad with the same data, and check the validity of the CRC-16 at the end of the command flow. Alternatively, use Read Scratchpad to verify data integrity. |
| Read Scratchpad | The data read changes to FFh bytes or all bytes received are FFh, including the CRC at the end of the command flow. | Wait 0.5s, 1-Wire reset, address the device, repeat Read Scratchpad, and check the validity of the CRC-16 at the end of the command flow. |
| Copy Scratchpad | The device behaves as if the authorization code or password was not valid, or as if the copy function would not end. | Wait 0.5s, 1-Wire reset, address the device, issue Read Scratchpad, and check the AA bit of the E/S byte. If the AA bit is set, Copy Scratchpad was successful. |
| Read Memory with CRC | The data read changes to all FFh bytes or all bytes received are FFh, including the CRC at the end of the command flow, despite a valid password. | Wait 0.5s, 1-Wire reset, address the device, repeat Read Memory with CRC, and check the validity of the CRC-16 at the end of the memory page. |
| Stop Mission | The General Status register at address 0215h reads FFh or the MIP bit is 1 while bits 0, 2, and 5 are 0. | Wait 0.5s, 1-Wire reset, address the device, and repeat Stop Mission. Perform a 1-Wire reset, address the device, read the General Status register at address 0215h, and check the MIP bit. If the MIP bit is 0, Stop Mission was successful. |

## 1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS1922E is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

## Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS1922E is open drain with an internal circuit equivalent to that shown in Figure 10.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At standard speed the 1-Wire bus has a maximum data rate of 16.3kbps. The speed can be boosted to 142kbps by activating the Overdrive Mode. The DS1922E is not guaranteed to be fully compliant to the iButton device standard. Its maximum data rate in standard speed is 15.4kbps and 125kbps in overdrive speed. The value of the pullup resistor primarily depends on the network size and load conditions. The DS1922E requires a pullup resistor of maximum 2.2kW at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus **must** be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus may be reset. Note that the DS1922E does not quite meet the full 16µs maximum low time of the normal 1-Wire bus overdrive timing. With the DS1922E the bus must be left low for no longer than 12µs at overdrive to ensure that no DS1922E on the 1-Wire bus performs a reset. The DS1922E communicates properly when used in conjunction with a DS2480B or DS2490 1-Wire driver and adapters that are based on these driver chips.

## Transaction Sequence

The protocol for accessing the DS1922E through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory/Control Function Command
- Transaction/Data

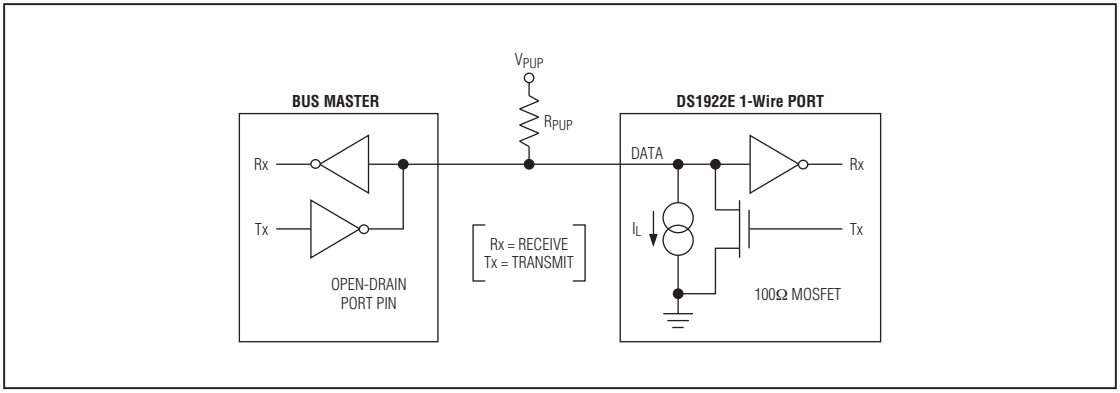



*Figure 10. Hardware Configuration*

## Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1922E is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

## 1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the eight ROM function commands that the DS1922E supports. All ROM function commands are 8 bits long. A list of these commands follows (see the flowchart in Figure 11).

### Read ROM [33h]

This command allows the bus master to read the DS1922E's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number results in a mismatch of the CRC.

### Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1922E on a multidrop bus. Only the DS1922E that exactly matches the 64-bit ROM sequence responds to the following memory function command. All other slaves wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

### Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to Application Note 187: *1-Wire Search Algorithm* for a detailed discussion, including an example.

### Conditional Search ROM [ECh]

The Conditional Search ROM command operates similarly to the Search ROM command except that only those devices that fulfill certain conditions participate in the search. This function provides an efficient means for the bus master to identify devices on a multidrop system that have to signal an important event. After each pass of the conditional search that successfully determined the 64-bit ROM code for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM had been issued, since all other devices have dropped out of the search process and are waiting for a reset pulse.

The DS1922E responds to the Conditional Search ROM command if one of the three alarm flags of the Alarm Status register (address 0214h) reads 1. The temperature alarm only occurs if enabled (see the *Temperature Sensor Alarm* section). The BOR alarm is always enabled. The first alarm that occurs makes the device respond to the Conditional Search ROM command.

### Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. For example, if more than one slave is present on the bus and a Read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

### Resume [A5h]

The DS1922E must be accessed several times before a mission starts. In a multidrop environment this means that the 64-bit ROM code after a Match ROM command must be repeated for every access. To maximize the data throughput in a multidrop environment, the Resume function was implemented. This function checks the status of the RC bit and, if it is set, directly transfers control to the memory/control functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive-Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command function. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command function.

### Overdrive-Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory/control functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive-Skip ROM command sets the DS1922E in the Overdrive Mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 690µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into Overdrive Mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a Read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

### Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS1922E on a multidrop bus and to simultaneously set it in Overdrive Mode. Only the DS1922E that exactly matches the 64-bit ROM sequence responds to the subsequent memory/control function command. Slaves already in Overdrive Mode from a previous Overdrive-Skip ROM or successful Overdrive-Match ROM command remain in Overdrive Mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 690µs duration. The Overdrive-Match ROM command can be used with a single or multiple devices on the bus.

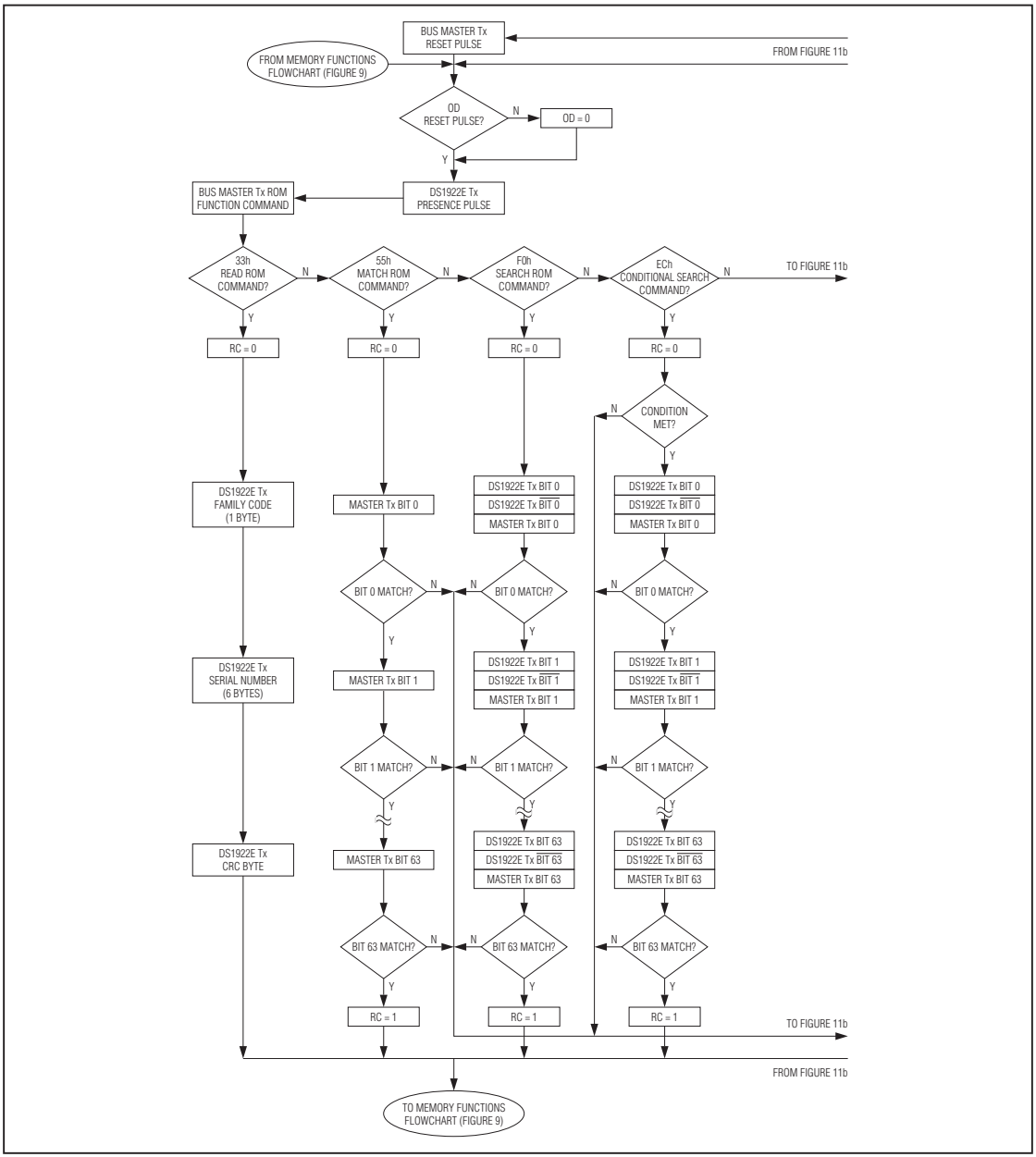



*Figure 11a. ROM Functions Flowchart*

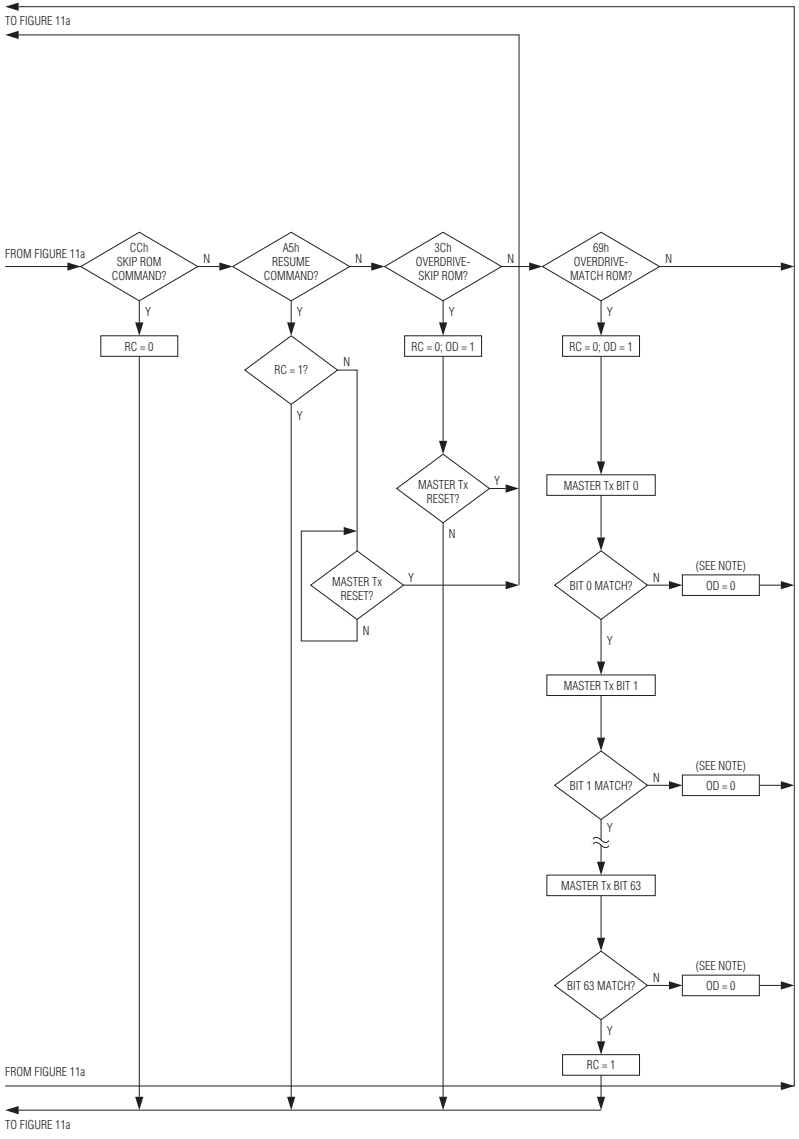



*Figure 11b. ROM Functions Flowchart (continued)*

## 1-Wire Signaling

The DS1922E requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all these signals. The DS1922E can communicate at two different speeds: standard speed and overdrive speed. If not explicitly set into the Overdrive Mode, the DS1922E communicates at standard speed. While in Overdrive Mode the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from $V_{PUP}$ below the threshold $V_{TL}$. To get from active to idle, the voltage needs to rise from $V_{ILMAX}$ past the threshold $V_{TH}$. The time it takes for the voltage to make this rise is seen in Figure 12 as "$\varepsilon$" and its duration depends on the pullup resistor ($R_{PUP}$) used and the capacitance of the 1-Wire network attached. The voltage $V_{ILMAX}$ is relevant for the DS1922E when determining a logical level, not triggering any events.

The initialization sequence required to begin any communication with the DS1922E is shown in Figure 12. A reset pulse followed by a presence pulse indicates the DS1922E is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. A $t_{RSTL}$ duration of 690µs or longer exits the Overdrive Mode, returning the device to standard speed. If the DS1922E is in Overdrive Mode and $t_{RSTL}$ is no longer than 80µs, the device remains in Overdrive Mode.

After the bus master has released the line, it goes into receive mode (Rx). Now the 1-Wire bus is pulled to $V_{PUP}$ through the pullup resistor or, in the case of a DS2480B driver, through active circuitry. When the threshold $V_{TH}$ is crossed, the DS1922E waits for $t_{PDH}$ and then transmits a presence pulse by pulling the line low for $t_{PDL}$. To detect a presence pulse, the master must test the logical state of the 1-Wire line at $t_{MSP}$.

The $t_{RSTH}$ window must be at least the sum of $t_{PDHMAX}$, $t_{PDLMAX}$, and $t_{RECMIN}$. Immediately after $t_{RSTH}$ is expired, the DS1922E is ready for data communication. In a mixed population network, $t_{RSTH}$ should be extended to minimum 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

### Read/Write Time Slots

Data communication with the DS1922E takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. The definitions of the write and read time slots are illustrated in Figure 13.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold $V_{TL}$, the DS1922E starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

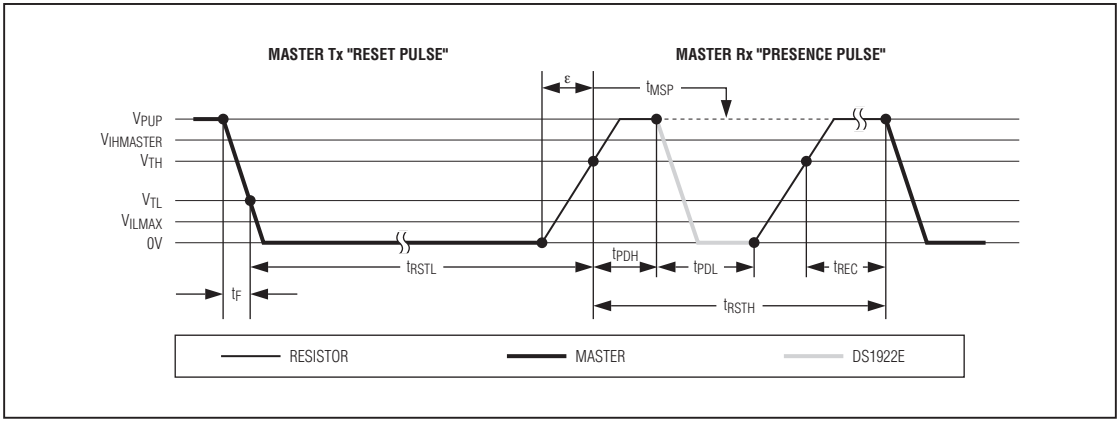



*Figure 12. Initialization Procedure: Reset and Presence Pulse*

**Master-to-Slave**
For a **write-one** time slot, the voltage on the data line must have crossed the $V_{TH}$ threshold before the write-one low time $t_{W1LMAX}$ is expired. For a **write-zero** time slot, the voltage on the data line must stay below the $V_{TH}$ threshold until the write-zero low time $t_{W0LMIN}$ is expired. The voltage on the data line should not exceed $V_{ILMAX}$ during the entire $t_{W0L}$ or $t_{W1L}$ window. After the $V_{TH}$ threshold has been crossed, the DS1922E needs a recovery time $t_{REC}$ before it is ready for the next time slot.

**Slave-to-Master**
A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below $V_{TL}$ until the read low time $t_{RL}$ is expired. During the $t_{RL}$ window, when responding with a 0, the DS1922E starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS1922E does not hold the data line low at all, and the voltage starts rising as soon as $t_{RL}$ is over.

The sum of $t_{RL}$ + d (rise time) on one side and the internal timing generator of the DS1922E on the other side define the master sampling window ($t_{MSRMIN}$ to $t_{MSRMAX}$) in which the master must perform a read from the data line. For most reliable communication, $t_{RL}$ should be as short as permissible and the master should read close to but no later than $t_{MSRMAX}$. After reading from the data line, the master must wait until $t_{SLOT}$ is expired. This guarantees sufficient recovery time $t_{REC}$ for the DS1922E to get ready for the next time slot. Note that $t_{REC}$ specified herein applies only to a single DS1922E attached to a 1-Wire line. For multiple device configurations, $t_{REC}$ must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the DS2482-x00 or DS2480B 1-Wire line drivers can be used.

## Improved Network Behavior (Switchpoint Hysteresis)

In a 1-Wire environment line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, as a consequence, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS1922E uses a new 1-Wire front-end, which makes it less sensitive to noise and also reduces the magnitude of noise injected by the slave device itself.

The DS1922E's 1-Wire front-end differs from traditional slave devices in four characteristics:

1) The falling edge of the presence pulse has a controlled slew rate. This provides a better match to the line impedance than a digitally switched transistor, converting the high-frequency ringing known from traditional devices into a smoother low-bandwidth transition. The slew-rate control is specified by the parameter $t_{FPD}$, which has different values for standard and overdrive speed.
2) There is additional lowpass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at overdrive speed.
3) There is a hysteresis at the low-to-high switching threshold $V_{TH}$. If a negative glitch crosses $V_{TH}$ but does not go below $V_{TH}$ - $V_{HY}$, it is not recognized (Figure 14, Case A). The hysteresis is effective at any 1-Wire speed.
4) There is a time window specified by the rising edge hold-off time $t_{REH}$ during which glitches are ignored, even if they extend below $V_{TH}$ - $V_{HY}$ threshold (Figure 14, Case B, $t_{GL} < t_{REH}$). Deep voltage droops or glitches that appear late after crossing the $V_{TH}$ threshold and extend beyond the $t_{REH}$ window cannot be filtered out and are taken as the beginning of a new time slot (Figure 14, Case C, $t_{GL} \geq t_{REH}$).

Devices that have the parameters $t_{FPD}$, $V_{HY}$, and $t_{REH}$ specified in their electrical characteristics use the improved 1-Wire front-end.

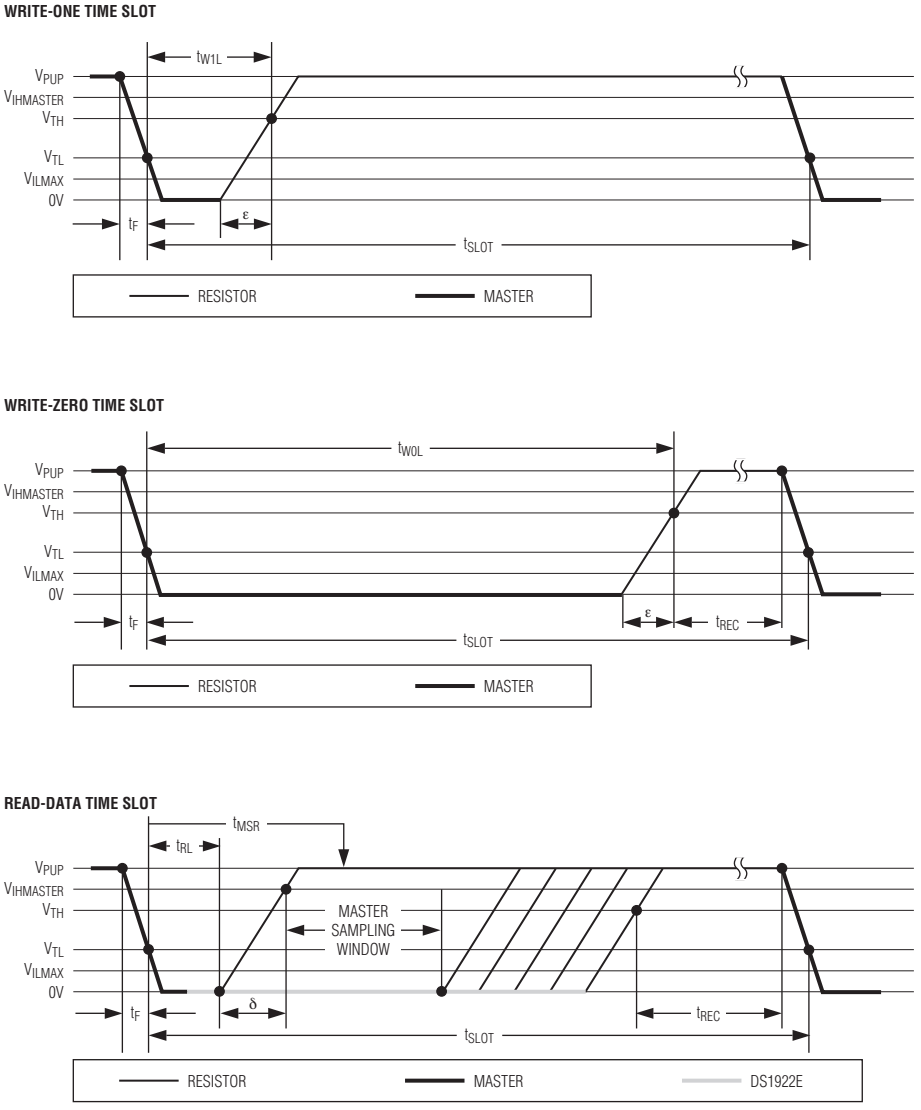



*Figure 13. Read/Write Timing Diagrams*

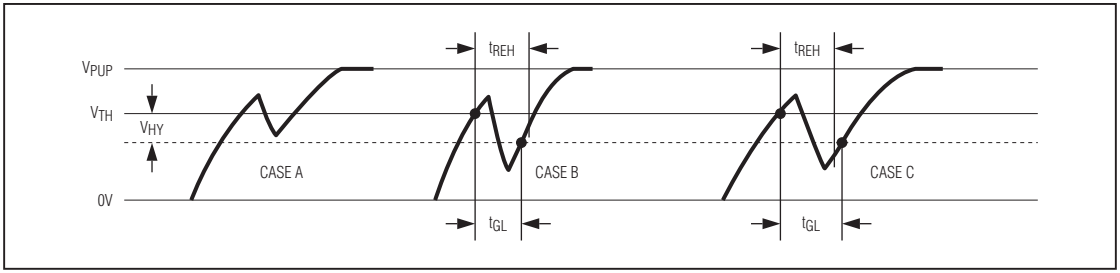



*Figure 14. Noise Suppression Scheme*

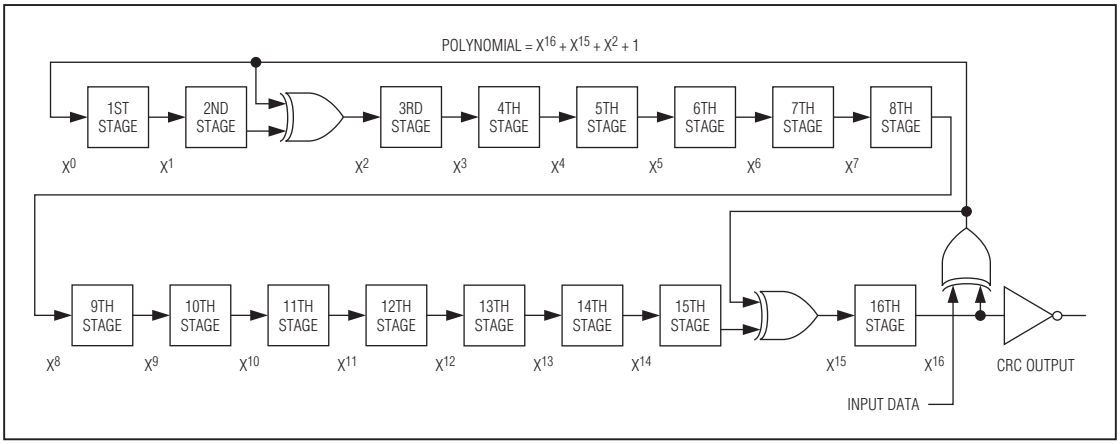



*Figure 15. CRC-16 Hardware Description and Polynomial*

## CRC Generation

The DS1922E uses two types of CRCs. One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS1922E to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (noninverted) form, and it is computed at the factory and lasered into the ROM.

The other CRC is a 16-bit type, generated according to the standardized CRC-16 polynomial function $x^{16} + x^{15} + x^2 + 1$. This CRC is used for error detection when reading register pages or the data-log memory using the Read Memory with CRC command and for fast verification of a data transfer when writing to or reading from the scratchpad. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC generator inside the DS1922E (Figure 15) calculates a new 16-bit CRC as shown in the command flowchart of Figure 9. The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to reread the portion of the data with the CRC error. With the initial pass through the Read Memory with CRC flowchart, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the data bytes. The password is excluded from the CRC calculation. Subsequent passes through the Read Memory with CRC flowchart generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the data bytes.

With the Write Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, and all the data bytes. The DS1922E transmits this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data can start at any location within the scratchpad.

With the Read Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. The DS1922E transmits this CRC only if the reading continues through the end of the scratchpad, regardless of the actual ending offset. For more information on generating CRC values, refer to Application Note 27.

## Command-Specific 1-Wire Communication Protocol—Legend

| SYMBOL | DESCRIPTION |
|---|---|
| RST | 1-Wire reset pulse generated by master. |
| PD | 1-Wire presence pulse generated by slave. |
| Select | Command and data to satisfy the ROM function protocol. |
| WS | Command "Write Scratchpad." |
| RS | Command "Read Scratchpad." |
| CPS | Command "Copy Scratchpad with Password." |
| RMC | Command "Read Memory with Password and CRC." |
| CM | Command "Clear Memory with Password." |
| FC | Command "Forced Conversion." |
| SM | Command "Start Mission with Password." |
| STP | Command "Stop Mission with Password." |
| TA | Target Address TA1, TA2. |
| TA–E/S | Target Address TA1, TA2 with E/S byte. |
| <Data to EOS> | Transfer of as many data bytes as are needed to reach the scratchpad offset 1Fh. |
| <Data to EOP> | Transfer of as many data bytes as are needed to reach the end of a memory page. |
| <PW/Dummy> | Transfer of 8 bytes that either represent a valid password or acceptable dummy data. |
| <32 Bytes> | Transfer of 32 bytes. |
| <Data> | Transfer of an undetermined amount of data. |
| FFh | Transmission of one FFh byte. |
| $\overline{\text{CRC-16}}$ | Transfer of an inverted CRC-16. |
| FF Loop | Indefinite loop where the master reads FF bytes. |
| AA Loop | Indefinite loop where the master reads AA bytes. |
| Busy | Interval during Copy Scratchpad where the DS1922E does not respond. Any bits read during this time are logic 1. |

## Command-Specific 1-Wire Communication Protocol—Color Codes

| Master-to-Slave | Slave-to-Master |
|---|---|

## 1-Wire Communication Examples

**Write Scratchpad, Reaching the End of the Scratchpad (Cannot Fail)**

| RST | PD | Select | WS | TA | <Data to EOS> | $\overline{\text{CRC-16}}$ | FF Loop |
|---|---|---|---|---|---|---|---|

**Read Scratchpad (Cannot Fail)**

| RST | PD | Select | RS | TA-E/S | <Data to EOS> | $\overline{\text{CRC-16}}$ | FF Loop |
|---|---|---|---|---|---|---|---|

**Copy Scratchpad with Password (Success)**

| RST | PD | Select | CPS | TA-E/S | <PW/Dummy> | Busy | AA Loop |
|---|---|---|---|---|---|---|---|

**Copy Scratchpad with Password (Fail TA-E/S or Password)**

| RST | PD | Select | CPS | TA-E/S | <PW/Dummy> | FF Loop |
|---|---|---|---|---|---|---|

**Read Memory with Password and CRC (Success)**

| RST | PD | Select | RMC | TA | <PW/Dummy> | <Data to EOP> | $\overline{\text{CRC-16}}$ |
|---|---|---|---|---|---|---|---|

| <32 Bytes> | $\overline{\text{CRC-16}}$ | FF Loop |
|---|---|---|

Loop

**Read Memory with Password and CRC (Fail Password or Address)**

| RST | PD | Select | RMC | TA | <PW/Dummy> | FF Loop |
|---|---|---|---|---|---|---|

**Clear Memory with Password**

| RST | PD | Select | CM | <PW/Dummy> | FFh | FF Loop |
|---|---|---|---|---|---|---|

To verify success, read the General Status register at address 0215h. If MEMCLR is 1, the command was executed successfully.

## 1-Wire Communication Examples (continued)

**Forced Conversion**

| RST | PD | Select | FC | FFh | FF Loop |
|---|---|---|---|---|---|

To read the result and to verify success, read the addresses 020Ch to 020Fh (results) and the device samples counter at address 0223h to 0225h. If the count has incremented, the command was executed successfully.

**Start Mission with Password**

| RST | PD | Select | SM | <PW/Dummy> | FFh | FF Loop |
|---|---|---|---|---|---|---|

To verify success, read the General Status register at address 0215h. If MIP is 1 and MEMCLR is 0, the command was executed successfully.

**Stop Mission with Password**

| RST | PD | Select | STP | <PW/Dummy> | FFh | FF Loop |
|---|---|---|---|---|---|---|

To verify success, read the General Status register at address 0215h. If MIP is 0, the command was executed successfully.

## Mission Example: Prepare and Start a New Mission

Assumption: The previous mission has been ended by using the Stop Mission command. Passwords are not enabled.

Starting a mission requires three steps:

Step 1: Clear the data of the previous mission.

Step 2: Write the setup data to register page 1.

Step 3: Start the new mission.

**Step 1: Clear the data of the previous mission.**

With only a single device connected to the bus master, the communication of step 1 looks like this:

| MASTER MODE | DATA (LSB FIRST) | COMMENTS |
|---|---|---|
| Tx | (Reset) | Reset pulse |
| Rx | (Presence) | Presence pulse |
| Tx | CCh | Issue “Skip ROM” command |
| Tx | 96h | Issue “Clear Memory” command |
| Tx | <8 FFh bytes> | Send dummy password |
| Tx | FFh | Send dummy byte |
| Tx | (Reset) | Reset pulse |
| Rx | (Presence) | Presence pulse |

**Step 2: Write the setup data to register page 1.**

During the setup, the device needs to learn the following information:

- Time and Date
- Sample Rate
- Alarm Thresholds
- Alarm Controls (Response to Conditional Search)
- General Mission Parameters (e.g., Channels to Log and Logging Format, Rollover, Start Mode)
- Mission Start Delay

The following data sets up the DS1922E for a mission that logs temperature using 8-bit format.

| ADDRESS | DATA | EXAMPLE VALUES | FUNCTION |
|---|---|---|---|
| 0200h | 00h | 15:30:00 hours | Time |
| 0201h | 30h | | |
| 0202h | 15h | | |
| 0203h | 01h | 1st of April in 2008 | Date |
| 0204h | 04h | | |
| 0205h | 08h | | |
| 0206h | 0Ah | Every 10 minutes (EHSS = 0) | Sample rate |
| 0207h | 00h | | |
| 0208h | 08h | 18°C low<br>135°C high | Temperature alarm thresholds |
| 0209h | F2h | | |
| 020Ah | 00h | (Don't care) | (Not applicable with DS1922E) |
| 020Bh | FFh | | |
| 020Ch | FFh | (Don't care) | Clock through read-only registers |
| 020Dh | FFh | | |
| 020Eh | FFh | | |
| 020Fh | FFh | | |
| 0210h | 02h | Enable high alarm | Temperature alarm control |
| 0211h | FCh | Disabled | (Not applicable with DS1922E) |
| 0212h | 01h | On (enabled), EHSS = 0 (low sample rate) | RTC oscillator control, sample rate selection |
| 0213h | C1h | Normal start; no rollover; 8-bit temperature log | General mission control |
| 0214h | FFh | (Don't care) | Clock through read-only registers |
| 0215h | FFh | | |
| 0216h | 5Ah | 90 minutes | Mission start delay |
| 0217h | 00h | | |
| 0218h | 00h | | |

With only a single device connected to the bus master, the communication of step 2 looks like this:

| MASTER MODE | DATA (LSB FIRST) | COMMENTS |
|---|---|---|
| Tx | (Reset) | Reset pulse |
| Rx | (Presence) | Presence pulse |
| Tx | CCh | Issue “Skip ROM” command |
| Tx | 0Fh | Issue “Write Scratchpad” command |
| Tx | 00h | TA1, beginning offset = 00h |
| Tx | 02h | TA2, address = 0200h |
| Tx | <25 Data Bytes> | Write 25 bytes of data to scratchpad |
| Tx | <7 FFh Bytes> | Write through the end of the scratchpad |
| Tx | (Reset) | Reset pulse |
| Rx | (Presence) | Presence pulse |
| Tx | CCh | Issue “Skip ROM” command |
| Tx | AAh | Issue “Read Scratchpad” command |
| Rx | 00h | Read TA1, beginning offset = 00h |
| Rx | 02h | Read TA2, address = 0200h |
| Rx | 1Fh | Read E/S, ending offset = 1Fh, flags = 0h |
| Rx | <32 Data Bytes> | Read scratchpad data and verify |
| Tx | (Reset) | Reset pulse |
| Rx | (Presence) | Presence pulse |
| Tx | CCh | Issue “Skip ROM” command |
| Tx | 99h | Issue “Copy Scratchpad” command |
| Tx | 00h | TA1 (AUTHORIZATION CODE) |
| Tx | 02h | TA2 |
| Tx | 1Fh | E/S |
| Tx | <8 FFh Bytes> | Send dummy password |
| Tx | (Reset) | Reset pulse |
| Rx | (Presence) | Presence pulse |

**Step 3: Start the new mission.**

With only a single device connected to the bus master, the communication of step 3 looks like this:

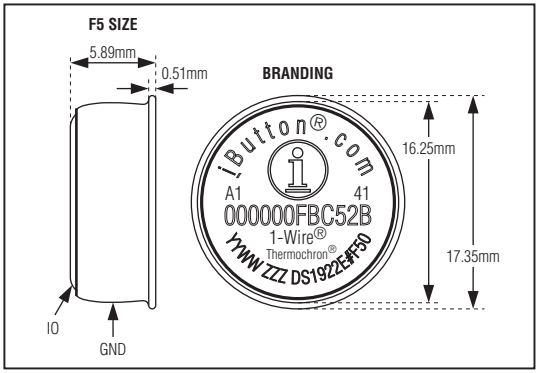
If step 3 was successful, the MIP bit in the General Status register is 1, the MEMCLR bit is 0, and the mission start delay counts down.

| MASTER MODE | DATA (LSB FIRST) | COMMENTS |
|---|---|---|
| Tx | (Reset) | Reset pulse |
| Rx | (Presence) | Presence pulse |
| Tx | CCh | Issue “Skip ROM” command |
| Tx | CCh | Issue “Start Mission” command |
| Tx | <8 FFh Bytes> | Send dummy password |
| Tx | FFh | Send dummy byte |
| Tx | (Reset) | Reset pulse |
| Rx | (Presence) | Presence pulse |

## Software Correction Algorithm or Temperature

The correction algorithm described in the DS1922L/DS1922T data sheet does not apply to the DS1922E. If attempted, the corrected result is generally less accurate than the raw temperature data read from the device. Therefore, with the DS1922E the memory pages 18 and 19 are available as additional user memory.

## Pin Configuration




## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| F5 Can | IB#6CB | **21-0266** | — |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 7/08 | Initial release | — |
| 1 | 10/08 | Added the *Software Correction Algorithm for Temperature* section | 43 |
| 2 | 6/09 | Changed storage temperature range in *Absolute Maximum Ratings* and added a recommended storage temperature note for maximum battery lifetime | 2 |
| 3 | 4/11 | Updated UL certificate reference; added paragraph on validation certificates to *Detailed Description* section; added more details on the Device Samples Counter in the *Other Indicators* section | 1, 5, 6, 18 |
| 4 | 6/13 | Removed the UL 913 5th Ed. compliance statement from the *Common iButton Device Features* section and *iButton Can Physical Specification* table; reworded the *Electrical Characteristics* table Note 19 | 1, 4, 5 |
| 5 | 11/13 | Added the Busy state during Copy Scratchpad to the *Command-Specific 1-Wire Communication Protocol—Legend* and *1-Wire Communication Examples* sections | 38, 39 |
| 6 | 3/15 | Updated *Benefits and Features* and Common *iButton Device Features* sections | 1 |
| 7 | 7/17 | Added Note 20 | 4 |

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