19-4865; Rev 4/11

DS1992/DS1993
1Kb/4Kb Memory iButton

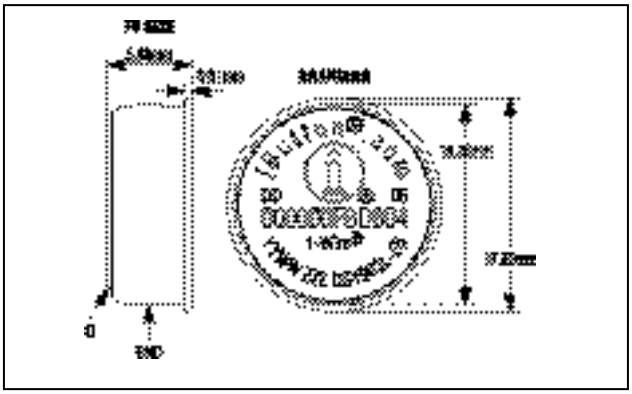
SPECIAL FEATURES
- 4096 bits of Read/Write Nonvolatile Memory (DS1993)
- 1024 bits of Read/Write Nonvolatile Memory (DS1992)
- 256-bit Scratchpad Ensures Integrity of Data Transfer
- Memory Partitioned into 256-bit Pages for Packetizing Data
- Data Integrity Assured with Strict Read/Write Protocols
- Operating Temperature Range from -40°C to +70°C
- Over 10 years of data retention

ORDERING INFORMATION
DS1992L-F5+	F5 MicroCan
DS1993L-F5+	F5 MicroCan

+Denotes a lead(Pb)-free/RoHS-compliant product.

EXAMPLES OF ACCESSORIES
DS9096P Self-Stick Adhesive Pad
DS9101 Multipurpose Clip
DS9093RA Mounting Lock Ring
DS9093F Snap-In Fob
DS9092 iButton Probe

F5 MicroCan



COMMON iButton FEATURES
- Unique, Factory-Lasered and Tested 64-bit Registration Number (8-bit Family Code + 48-bit Serial Number + 8-bit CRC Tester) Assures Absolute Traceability Because No Two Parts are Alike
- Multidrop Controller for MicroLAN
- Digital Identification and Information by Momentary Contact
- Chip-Based Data Carrier Compactly Stores Information
- Data Can be Accessed While Affixed to Object
- Economically Communicates to Bus Master with a Single Digital Signal at 16.3kbps
- Standard 16mm Diameter and 1-Wire® Protocol Ensure Compatibility with iButton® Family
- Button Shape is Self-Aligning with Cup-Shaped Probes
- Durable Stainless Steel Case Engraved with Registration Number Withstands Harsh Environments
- Easily Affixed with Self-Stick Adhesive Backing, Latched by its Flange, or Locked with a Ring Pressed onto its Rim
- Presence Detector Acknowledges When Reader First Applies Voltage
- Meets UL 913, 5th Ed., Rev. 1997-02-24; Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C, and D Locations

1-Wire and iButton are registered trademarks of Maxim Integrated Products, Inc.

iButton DESCRIPTION

The DS1992/DS1993 memory iButtons (hereafter referred to as DS199x) are rugged read/write data carriers that act as a localized database, easily accessible with minimal hardware. The nonvolatile memory and optional timekeeping capability offer a simple solution to storing and retrieving vital information pertaining to the object to which the iButton is attached. Data is transferred serially through the 1-Wire protocol that requires only a single data lead and a ground return.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command transfers the data to memory. This process ensures data integrity when modifying the memory. A 48-bit serial number is factory lasered into each DS199x to provide a guaranteed unique identity that allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact coin-shaped profile is self-aligning with mating receptacles, allowing the DS199x to be easily used by human operators. Accessories permit the DS199x to be mounted on almost any surface including plastic key fobs, photo-ID badges, and PC boards.

Applications include access control, work-in-progress tracking, electronic travelers, storage of calibration constants, and debit tokens.

OPERATION

The DS199x have three main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, and 3) 1024-bit (DS1992) or 4096-bit (DS1993) SRAM. All data is read and written least significant bit first.

The memory functions are not available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master can then provide any one of the four memory function commands (Figure 6).

PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry steals power whenever the data input is high. The data line provides sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, battery power is not consumed for 1-Wire ROM function commands, and 2) if the battery is exhausted for any reason, the ROM may still be read normally. The remaining circuitry of the DS1992 and DS1993 is solely operated by battery energy.

64-BIT LASERED ROM

Each DS199x contain a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits (see Figure 2). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Maxim 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards. The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all zeros.

Figure 1. DS1992/DS1993 BLOCK DIAGRAM

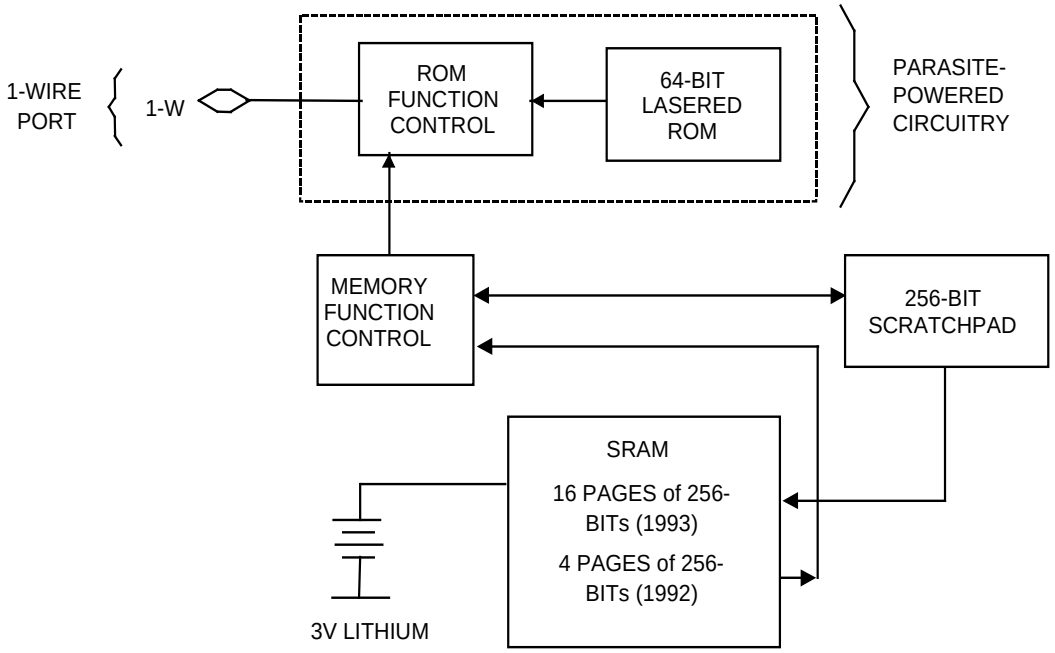


Figure 2. 64-BIT LASERED ROM

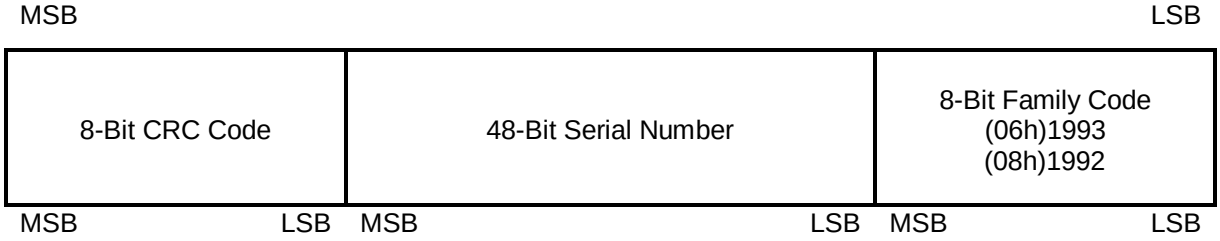


Figure 3. 1-Wire CRC CODE

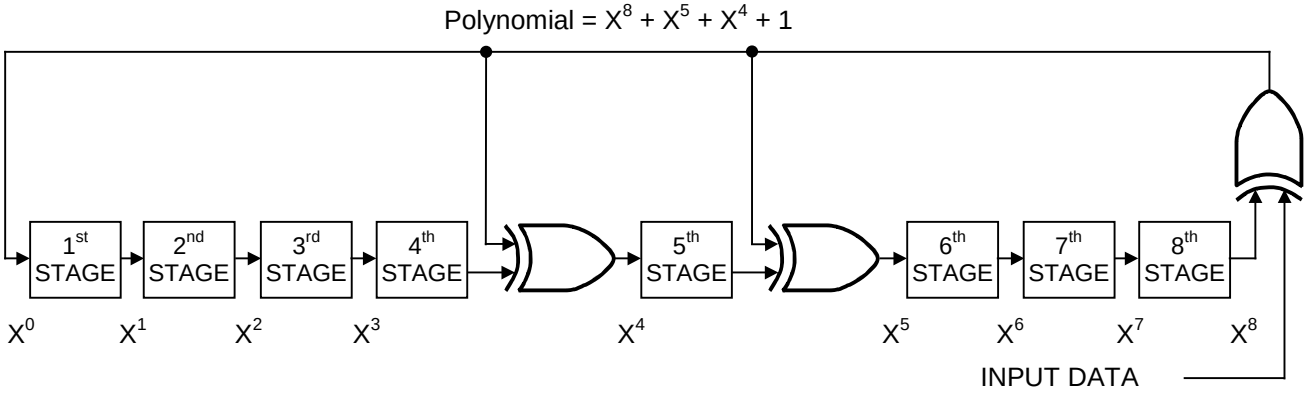
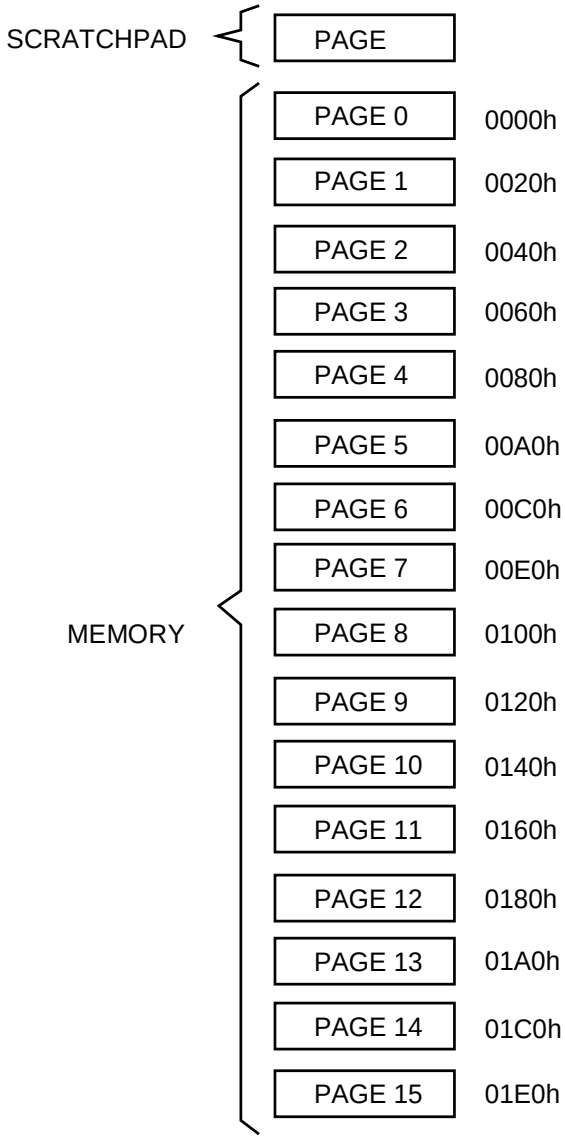
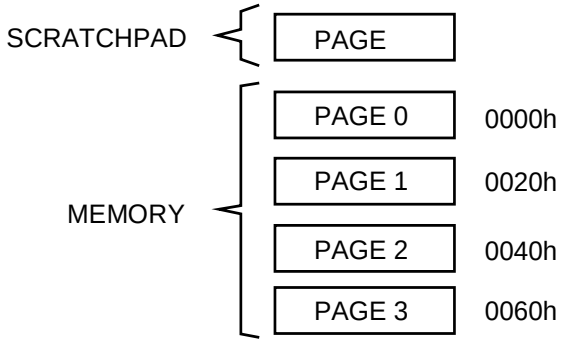


Figure 4a. DS1993 MEMORY MAP



NOTE: Each page is 32 bytes (256 bits). The hex values represent the starting address for each page or register.

Figure 4b. DS1992 MEMORY MAP



NOTE: Each page is 32 bytes (256 bits). The hex values represent the starting address for each page or register.

MEMORY

The memory map in Figure 4 shows a 32-Byte page called the scratchpad, and additional 32-Byte pages called memory. The DS1992 contains pages 0 though 3 that make up the 1024-bit SRAM. The DS1993 contain pages 0 through 15 that make up the 4096-bit SRAM.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command transfers the data to memory. This process ensures data integrity when modifying the memory.

MEMORY FUNCTION COMMANDS

The Memory Function Flow Chart (Figure 6) describes the protocols necessary for accessing the memory. An example follows the flow chart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique Byte location in memory. The first 5 bits of the target address (T4:T0) represent the Byte offset within a page. This Byte offset points to one of 32 possible Byte locations within a given page. For instance, 00000b points to the first Byte of a page where as 11111b would point to the last Byte of a page.

The third register (E/S) is a read only register. The first 5 bits (E4: E0) of this register are called the ending offset. The ending offset is a Byte offset within a page (1 of 32 Bytes). Bit 5 (PF) is the partial Byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

Figure 5. ADDRESS REGISTERS

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-Byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4:E0) is the Byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) is set and the remaining data is ignored. If the user writes an incomplete Byte and an overflow has not occurred, the partial Byte flag (PF) is set.

Read Scratchpad Command [AAh]

This command can be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user can begin reading. The first two Bytes are the target address. The next Byte is the ending offset/data status Byte (E/S) followed by the scratchpad data beginning at the Byte offset (T4: T0). The user can read data until the end of the scratchpad, after which the data read is all logic 1’s.

Copy Scratchpad [55h]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag is set and the copy begins. A logic 0 is transmitted after the data has been copied until the user issues a reset pulse. Any attempt to reset the part is ignored while the copy is in progress. Copy typically takes 30µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset is copied to memory, starting at the target address. Anywhere from 1 to 32 Bytes can be copied to memory with this command. Whole Bytes are copied even if only partially written. The AA flag is cleared only by executing a write scratchpad command.

Read Memory [F0h]

The read memory command can be used to read the entire memory. After issuing the command, the user must provide the 2-Byte target address. After the two Bytes, the user reads data beginning from the target address and may continue until the end of memory, at which point logic 1's are read. It is important to realize that the target address registers contains the address provided. The ending offset/data status Byte is unaffected.

The hardware of the DS199x provides a means to accomplish error-free writing to the memory section. To safeguard reading data in the 1-Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See Application Note 114 for the recommended file structure to be used with the 1-Wire environment.)

Figure 6. MEMORY FUNCTIONS FLOW CHART

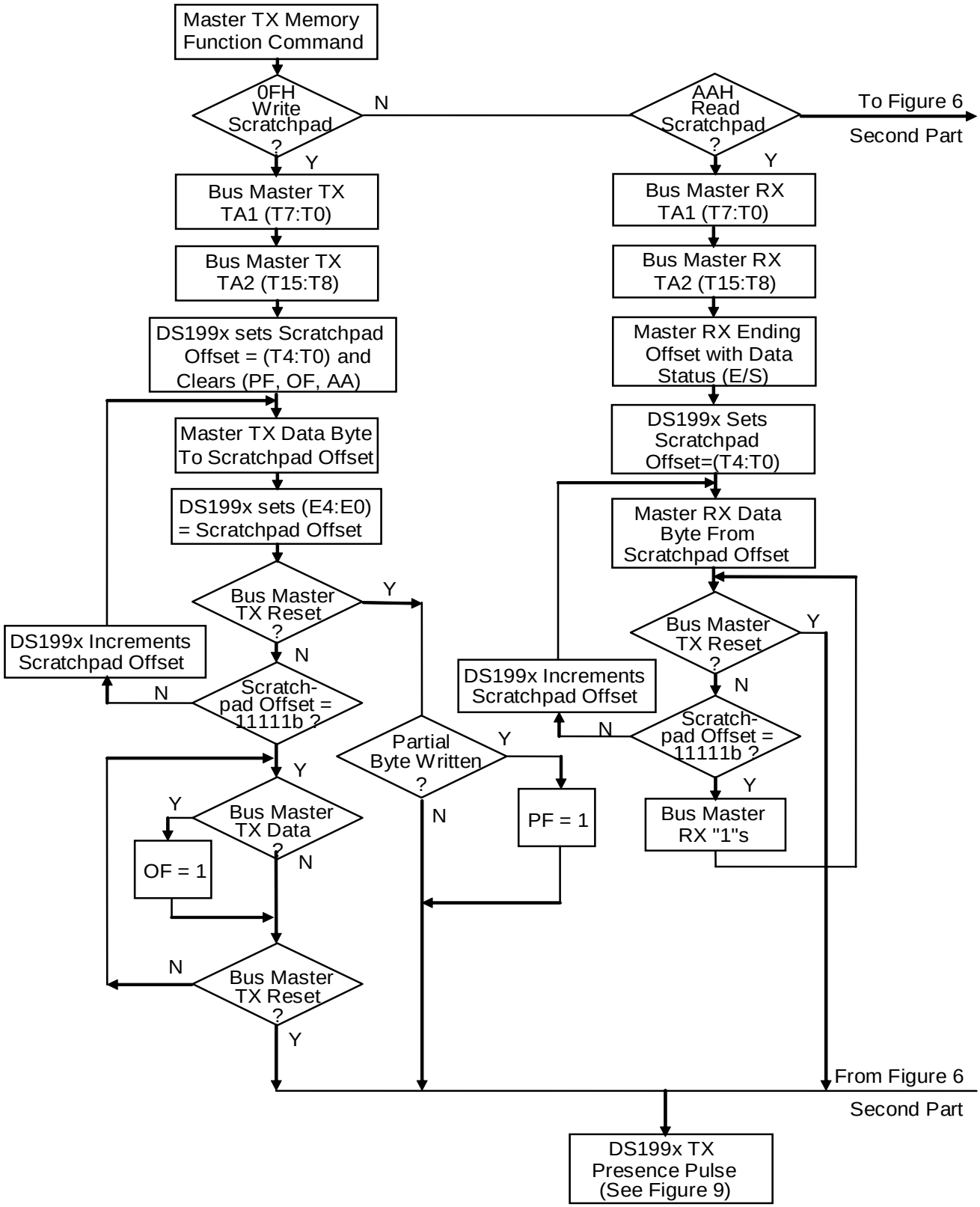
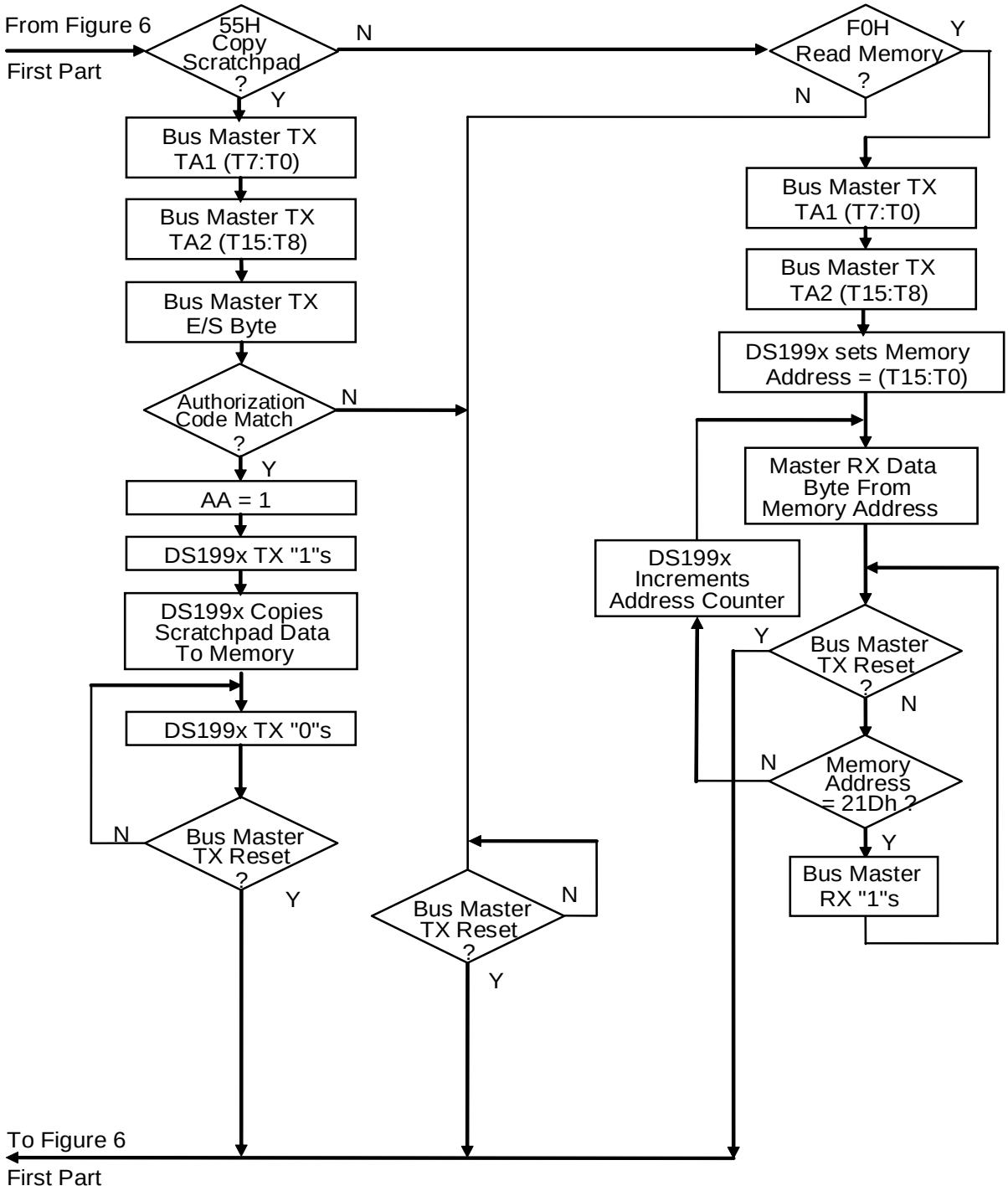


Figure 6. MEMORY FUNCTIONS FLOW CHART (continued)



MEMORY FUNCTION EXAMPLES

Example: Write two data Bytes to memory locations 0026h and 0027h (the seventh and eighth Bytes of page 1). Read entire memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480µs to 960µs)
RX	Presence	Presence pulse
TX	CCh	Issue skip ROM command
TX	0Fh	Issue write scratchpad command
TX	26h	TA1, beginning offset = 6
TX	00h	TA2, address = 0026h
TX	<2 data Bytes>	Write 2 Bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue skip ROM command
TX	Aah	Issue read scratchpad command
RX	26h	Read TA1, beginning offset = 6
RX	00h	Read TA2, address = 0026h
RX	07h	Read E/S, ending offset = 7, flags = 0
RX	<2 data Bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue skip ROM command
TX	55h	Issue copy scratchpad command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue skip ROM command
TX	F0h	Issue read memory command
TX	00h	TA1, beginning offset = 6
TX	00h	TA2, address = 0000h
RX	<128 Bytes (DS1992)> <512 Bytes (DS1993)>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1-Wire BUS SYSTEM

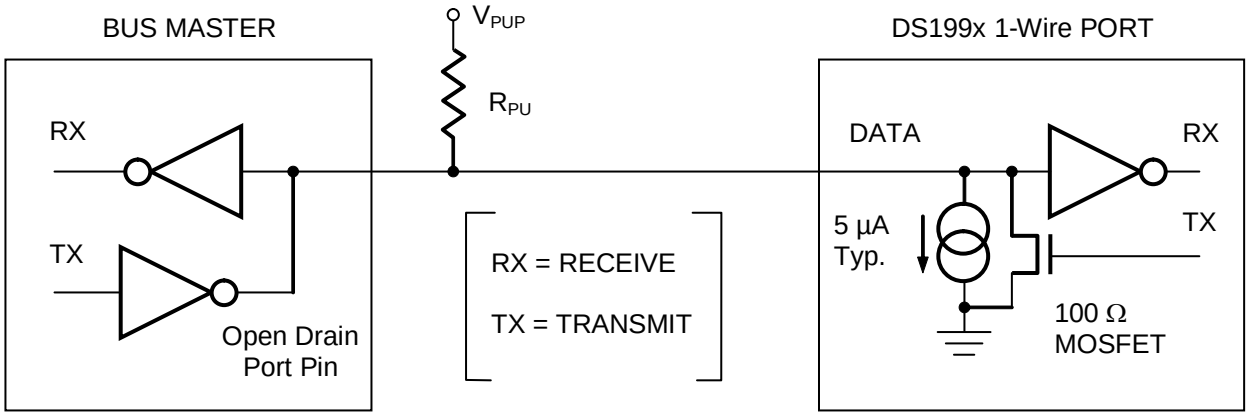
The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS199x is a slave device. The bus master is typically a microcontroller or PC. For small configurations the 1-Wire communication signals can be generated under software control using a single port pin. For multisensor networks, the DS2480B 1-Wire line driver chip or serial port adapters based on this chip (DS9097U series) are recommended. This simplifies the hardware design and frees the microprocessor from responding in real-time.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the *Book of DS19xx iButton Standards*.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS199x is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3kbps and requires a pullup resistor of approximately 5kΩ. The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus **must** be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120µs, one or more of the devices on the bus may be reset.

Figure 8. HARDWARE CONFIGURATION



TRANSACTION SEQUENCE

The protocol for accessing the DS199x through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the

slave(s). The presence pulse lets the bus master know that the DS199x is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (see the flow chart in Figure 9).

Read ROM [33h]

This command allows the bus master to read the DS199x's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command should only be used if there is a single DS199x on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number usually result in a mismatch of the CRC.

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS199x on a multidrop bus. Only the DS199x that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence wait for a reset pulse. This command can be used with single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master may not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the 64-bit ROM code of one device. Additional passes will identify the ROM codes of the remaining devices. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a search ROM, including an actual example.

1-Wire SIGNALING

The DS199x require strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write 0, write 1, and read data. The bus master initiates all these signals except presence pulse. The initialization sequence required to begin any communication with the DS199x is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS199x is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (Tx) a reset pulse (t_{RSTL}, minimum 480µs). The bus master then releases the line and goes into receive mode (Rx). The 1-Wire bus is pulled to a high state through the pullup resistor. After detecting the rising edge on the data line, the DS199x waits (t_{PDH}, 15µs to 60µs) and then transmits the presence pulse (t_{PDL}, 60µs to 240µs).

Figure 9. ROM FUNCTIONS FLOW CHART

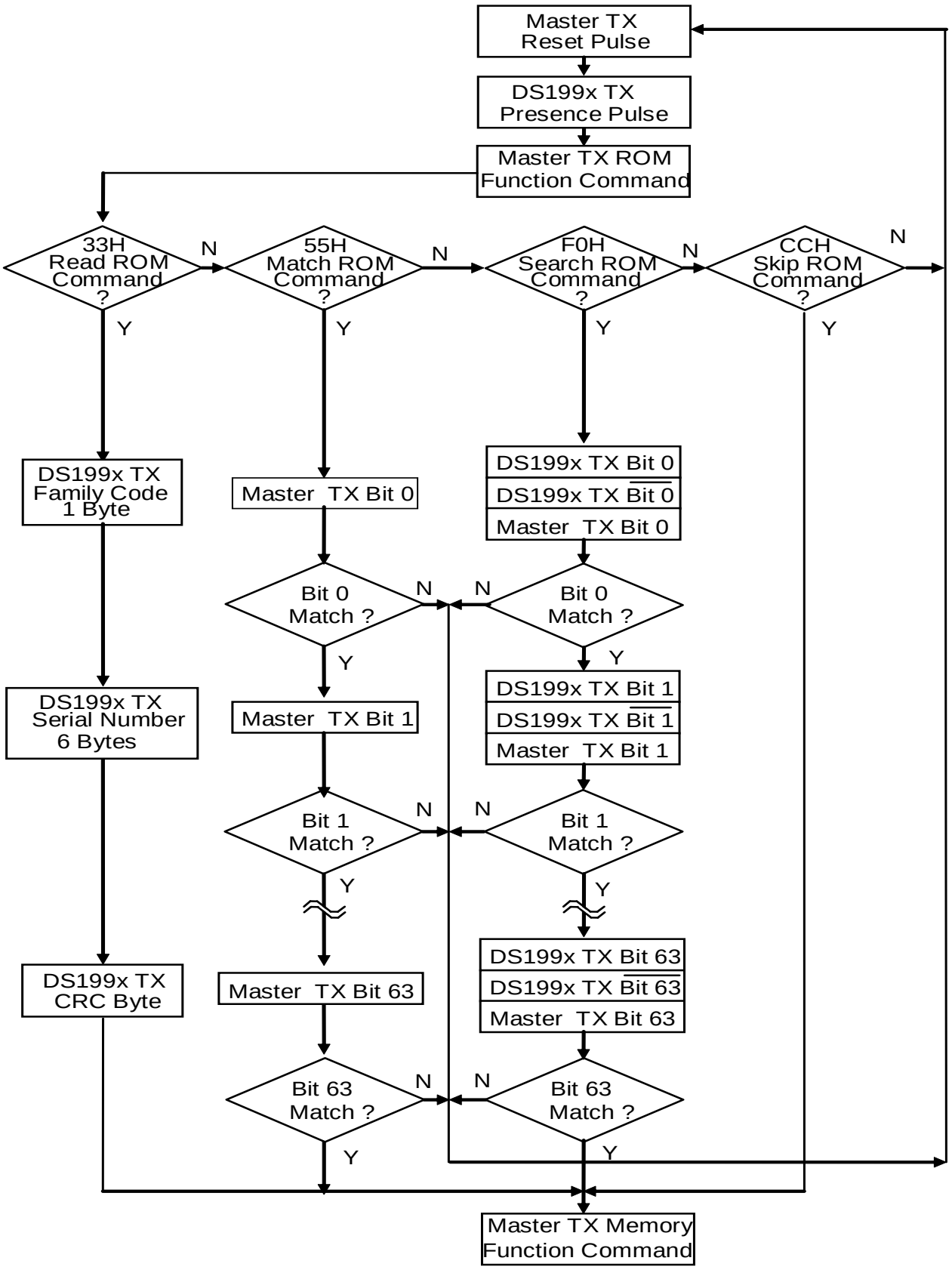
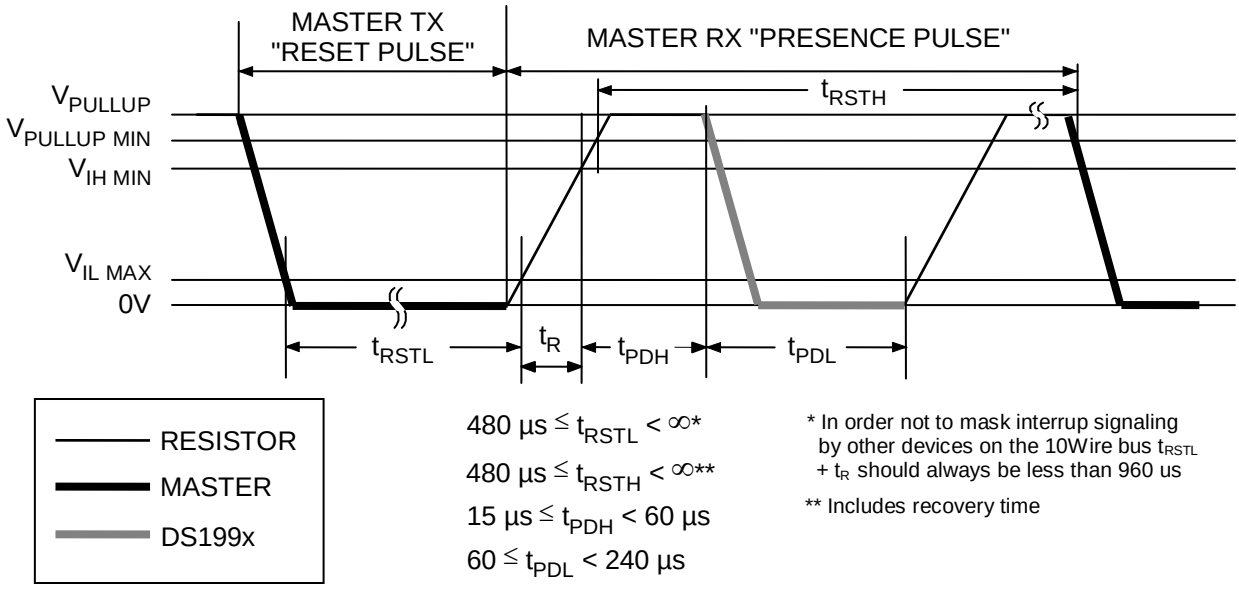


Figure 10. INITIALIZATION PROCEDURE RESET AND PRESENCE PULSE



READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. The master driving the data line low initiates all time slots. The falling edge of the data line synchronizes the DS199x to the master by triggering a delay circuit in the DS199x. During write time slots, the delay circuit determines when the DS199x samples the data line. For a read data time slot, if a 0 is to be transmitted, the delay circuit determines how long the DS199x holds the data line low overriding the 1 generated by the master. If the data bit is a 1, the iButton leaves the read data time slot unchanged.

Figure 11. READ/WRITE TIMING DIAGRAM

Write-One Time Slot

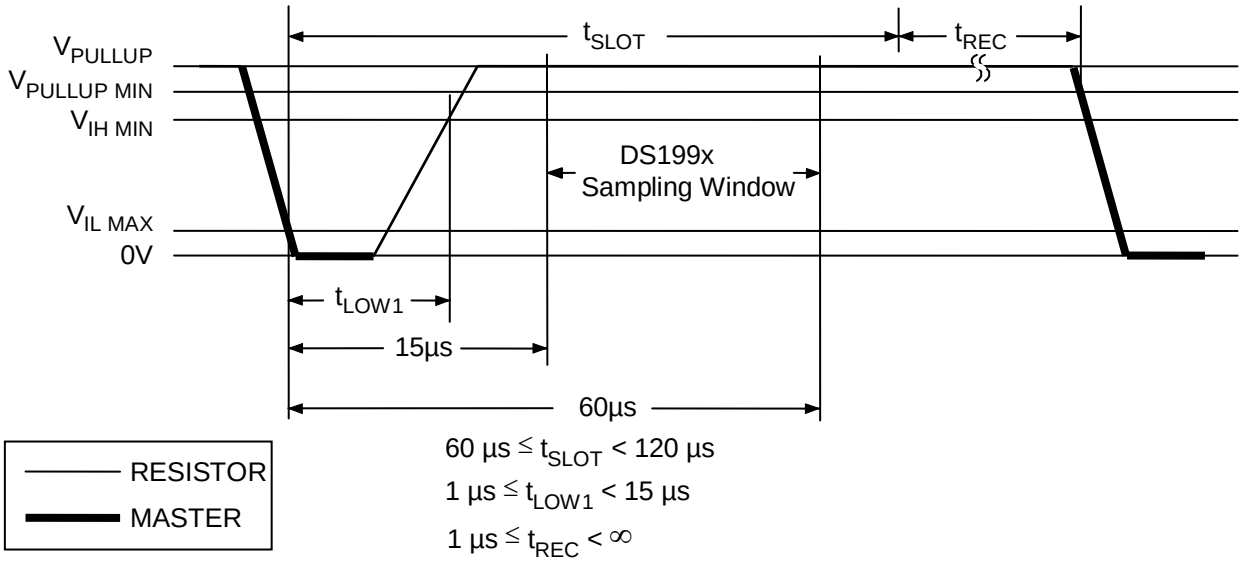
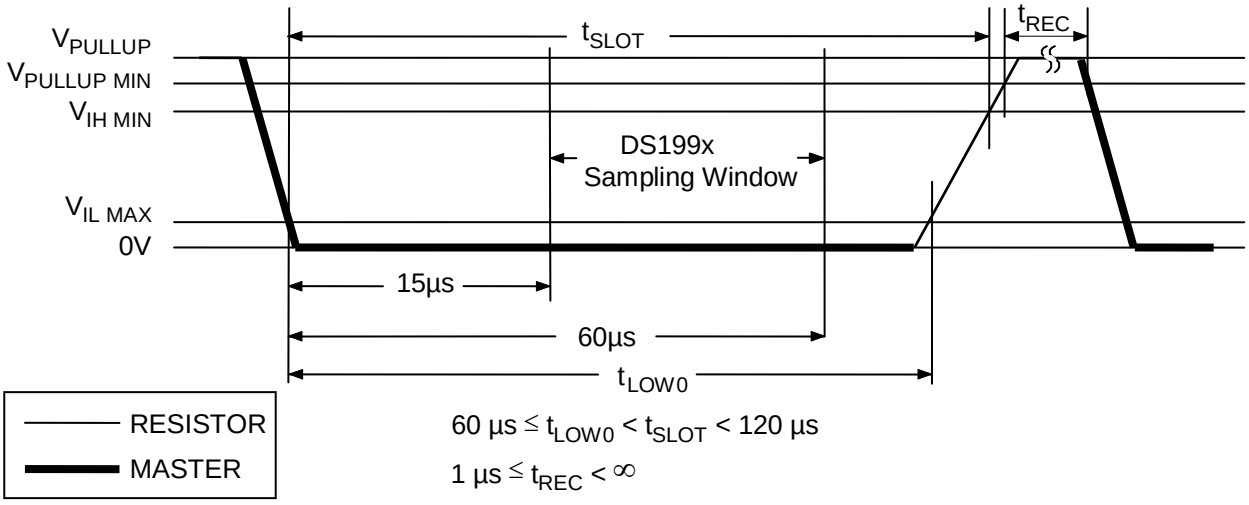
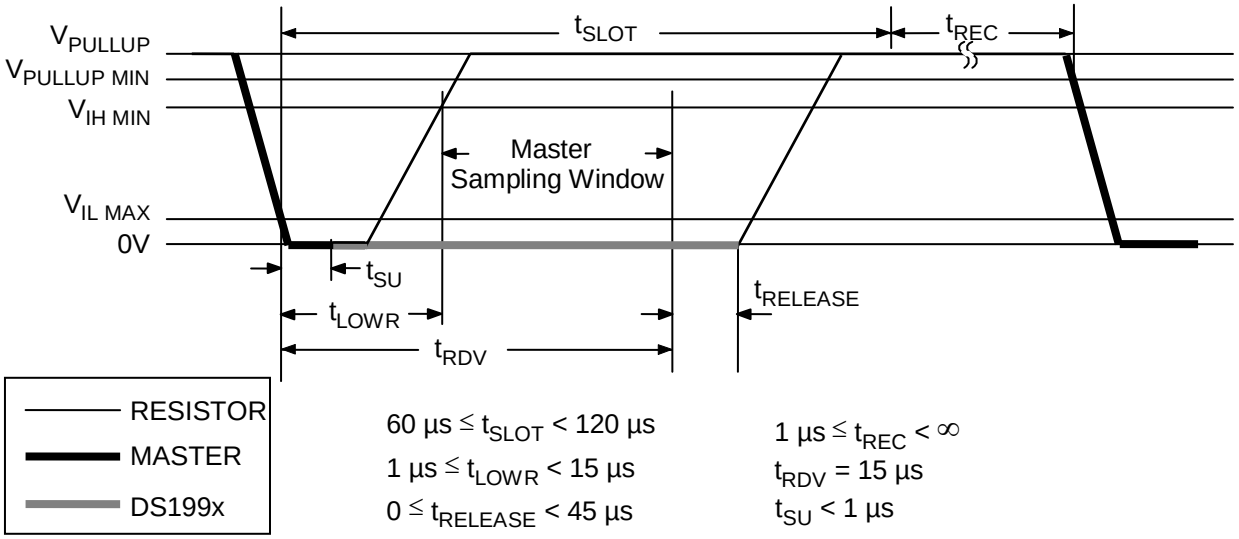


Figure 11. READ/WRITE TIMING DIAGRAM (continued)

Write-Zero Time Slot



Read-Data Time Slot



PHYSICAL SPECIFICATIONS

Size	See mechanical drawing
Weight	3.3 grams (F5 package)
Expected Service Life	10 years at +25°C
Safety	Meets UL 913, 5th Ed., Rev. 1997-02-24; Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C, and D Locations

ABSOLUTE MAXIMUM RATINGS

Voltage Range on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +70°C
Storage Temperature Range	-40°C to +70°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
1-Wire Pullup Voltage (Notes 1, 3)	V_{PUP}	2.8		6.0	V
Logic 1 (Notes 1, 2)	V_{IH}	2.2			V
Logic 0 (Note 1)	V_{IL}	-0.3		+0.3	V
Output Logic Low at 4mA (Note 1)	V_{OL}			0.4	V
Input Load Current (Note 4)	I_L		5		µA

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
I/O (1-Wire) (Notes 5, 6)	$C_{IN/OUT}$		100	800	pF

AC ELECTRICAL CHARACTERISTICS

(V_{PUP} = 2.8V to 6.0V, T_A = -40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Time Slot	t_{SLOT}	60		120	µs
Write 1 Low Time	t_{LOW1}	1		15	µs
Write 0 Low Time	t_{LOW0}	60		120	µs
Read Data Valid	t_{RDV}		exactly 15		µs
Release Time	$t_{RELEASE}$	0	15	45	µs
Read Data Setup (Note 7)	t_{SU}			1	µs
Recovery Time	t_{REC}	1			µs
Reset Time High (Note 8)	t_{RSTH}	480			µs
Reset Time Low (Note 9)	t_{RSTL}	480		960	µs
Presence Detect High	t_{PDH}	15		60	µs
Presence Detect Low	t_{PDL}	60		240	µs

Note 1: All voltages are referenced to ground.

Note 2: V_{IH} is a function of the external pullup resistor and the V_{CC} power supply.

Note 3: V_{PUP} = external pullup voltage.

Note 4: Input load is to ground.

Note 5: Capacitance on the data line could be 800pF when power is first applied. If a 5kΩ resistor is used to pull up the data line to V_{PUP}, 5µs after power has been applied, the parasite capacitance does not affect normal communications.

Note 6: Guaranteed by design; not production tested.

Note 7: Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1µs of this falling edge, and remains valid for 14µs minimum (15µs total from falling edge on 1-Wire bus).

Note 8: An additional reset or communication sequence cannot begin until the reset high time has expired.

Note 9: The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs, to allow interrupt signaling; otherwise, it could mask or conceal interrupt pulses.

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
F5 iButton	IB+5BW	**21-0266**	—

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
7/08	Updated the *F5 MicroCan* face brand with the latest per PCN H020201.	1
10/08	Change the last sentence of the *Parasite Power* section to "The advantages of parasite power are two-fold: 1) by parasiting off this input, battery power is not consumed for 1-Wire ROM function commands, and 2) if the battery is exhausted for any reason, the ROM may still be read normally. The remaining circuitry of the DS1992 and DS1993 is solely operated by battery energy."	2
	In the *DC Electrical Characteristics* section, relocated V_{PUP} from the header to the EC table, changed V_{ILMAX} from 0.8V to 0.3V, and removed the V_{OH} parameter for the 1-Wire pin.	15
8/09	Updated the part numbers in the *Ordering Information* table to indicate a lead(Pb)-free/RoHS compliant product.	1
4/11	Updated the UL certificate reference in the *Common iButton Features* and *Physical Specifications* sections; added the *Package Information* section.	1, 15, 16

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