# General-Purpose Timers

# ICM7555/ICM7556

## General Description

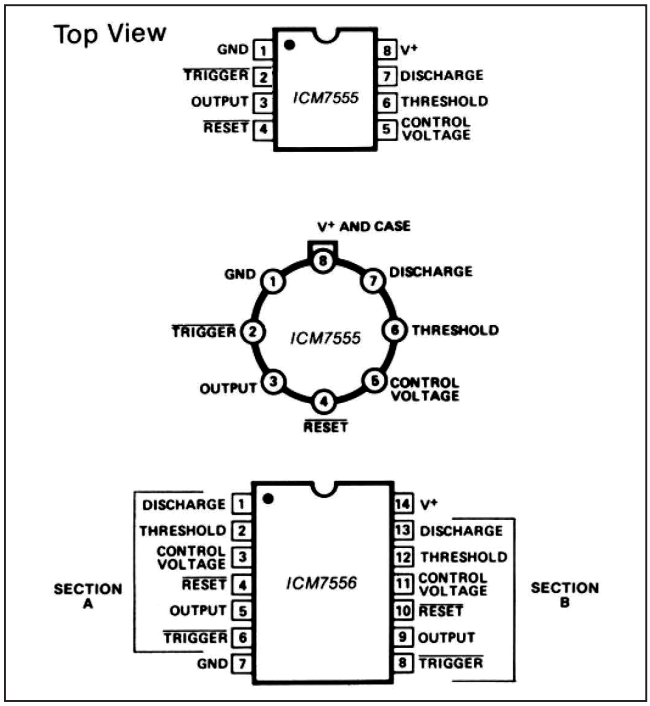
The Maxim ICM7555 and ICM7556 are respectively single and dual general-purpose RC timers capable of generating accurate time delays or frequencies. The primary feature is an extremely low supply current, making this device ideal for battery-powered systems. Additional features include low THRESHOLD, TRIGGER, and RESET currents, a wide operating supply voltage range, and improved performance at high frequencies.

These CMOS low-power devices offer significant performance advantages over the standard 555 and 556 bipolar timers. Low-power consumption, combined with the virtually nonexistent current spike during output transitions, make these timers the optimal solution in many applications.

## Applications

- Pulse Generator
- Precision Timing
- Time Delay Generation
- Pulse-Width Modulation
- Pulse Position Modulation
- Sequential Timing
- Missing Pulse Detector

## Pin Configurations



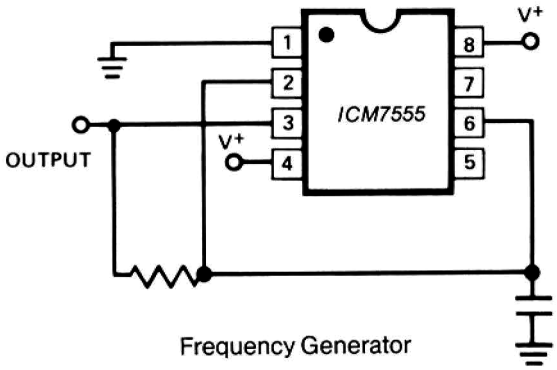

## Features

- Improved 2nd Source (See 4th Page for Maxim Advantage)
- Wide Supply Voltage Range: 2V to 18V
- No Crowbarring of Supply During Output Transition
- Adjustable Duty Cycle
- Low THRESHOLD, TRIGGER, and RESET Currents
- TTL Compatible
- Monolithic, Low-Power CMOS Design

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| ICM7555ESA | -40°C to +85°C | 8 SO |
| ICM7555IPA | -20°C to +85°C | 8 PDIP |
| ICM7555ISA | -20°C to +85°C | 8 SO |
| ICM7555MJA/HR | -55°C to +125°C | 8 CERDIP |
| ICM7555/D | 0°C to +70°C | Dice |
| ICM7556IPD | -20°C to +85°C | 14 PDIP |
| ICM7556ISD | -20°C to +85°C | 14 SO |
| ICM7556MJD | -55°C to +125°C | 14 CERDIP |
| ICM7556/D | 0°C to +70°C | Dice |

## Typical Operating Circuit




*(Detailed Circuit Diagram — Figure-1a)*

*19-0481; Rev 3; 3/13*

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## Absolute Maximum Ratings (Note 1)

Supply Voltage .....+18V
Input Voltage $\overline{\text{TRIGGER}}$
Control Voltage THRESHOLD.....< V+ +0.3V to ≥ -0.3V
$\overline{\text{RESET}}$
Output Current.....100mA
Power Dissipation (Note 2)
ICM7556 .....300mW
ICM7555 .....200mW
Operating Temperature Range
ICM75551JA (Maxim) ..... -20°C to +85°C
ICM75551SA (Maxim) ..... -20°C to +85°C
ICM75551PA..... -20°C to +85°C
ICM75551TV..... -20°C to +85°C
ICM75561PD ..... -20°C to +85°C
ICM7555MTV..... -55°C to +125°C
ICM7556MJD..... -55°C to +125°C
Storage Temperature..... -65°C to +150°C
Lead Temperature (soldering, 60s) .....+300°C

**Note 1:** Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ + 0.3V or less than V- - 0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established in multiple systems. The supply of the ICM7555/ICM7556 must be turned on first.

**Note 2:** Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at +125°C. Below 125°C, power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (ICM7556) or 2mW/°C (ICM7555).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Characteristics

(V+ = +2V to +15V; $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage | V+ | -20°C ≤ $T_A$ ≤ +70° | | 2 | | 18 | V |
| | | -55°C ≤ $T_A$ ≤ +125° | | 3 | | 16 | |
| Supply Current (Note 3) | I+ | ICM7555 | V+ = 2V | | 60 | 200 | µA |
| | | | V+ = 18V | | 120 | 300 | |
| | | ICM7556 | V+ = 2V | | 120 | 400 | |
| | | | V+ = 18V | | 240 | 600 | |
| Timing Error | | $R_A$, $R_B$ = 1kΩ to 100kΩ, C = 0.1µF | 5V ≤ V+ ≤ 15V | | | | |
| Initial Accuracy | | (Note 4) | | | 2.0 | 5.0 | % |
| Drift with Temperature | | (Note 4) | V+ = 5V | | 50 | | ppm/°C |
| | | | V+ = 10V | | 75 | | |
| | | | V+ = 15V | | 100 | | |
| Drift with Supply Voltage | | V+ = 5V | | | 1.0 | 3.0 | %/V |
| Threshold Voltage | $V_{TH}$ | V+ = 5V | | 0.63 | 0.66 | 0.67 | V+ |
| Trigger Voltage | $V_{TRIG}$ | V+ = 5V | | 0.29 | 0.33 | 0.34 | V+ |
| Trigger Current | $I_{TRIG}$ | V+ = 18V | | | 50 | | pA |
| | | V+ = 5V | | | 10 | | |
| | | V+ = 2V | | | 1 | | |
| Threshold Current | $I_{TH}$ | V+ = 18V | | | 50 | | pA |
| | | V+ = 5V | | | 10 | | |
| | | V+ = 2V | | | 1 | | |

## Electrical Characteristics (continued)

(V+ = +2V to +15V; $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Reset Current | $I_{RST}$ | $V_{REST}$ = Ground | | V+ = 18V | | 100 | | pA |
| | | | | V+ = 5V | | 20 | | |
| | | | | V+ = 2V | | 2 | | |
| Reset Voltage | $V_{RST}$ | V+ = 18V | | | 0.4 | 0.7 | 1.0 | V |
| | | V+ = 2V | | | 0.4 | 0.7 | 1.0 | |
| Control Voltage Lead | $V_{CV}$ | V+ = 5V | | | 0.62 | 0.66 | 0.67 | V |
| Output Voltage Drop | $V_O$ | Output Lo | V+ = 18V | $I_{SINK}$ = 3.2mA | | 0.1 | 0.4 | V |
| | | | V+ = 5V | $I_{SINK}$ = 3.2mA | | 0.15 | 0.4 | |
| | | Output Hi | V+ = 18V | $I_{SOURCE}$ = 1.0mA | 17.25 | 17.8 | | |
| | | | V+ = 5V | $I_{SOURCE}$ = 1.0mA | 4.0 | 4.5 | | |
| Rise Time of Output | $t_r$ | $R_L$ = 10MΩ | $C_L$ = 10pF | V+ = 5V | 35 | 40 | 75 | ns |
| Fall Time of Output | $t_f$ | $R_L$ = 10MΩ | $C_L$ = 10pF | V+ = 5V | 35 | 40 | 75 | |
| Guaranteed Max Osc. Frequency | $f_{max}$ | Astable operation | | | 500 | | | kHz |

**Note 3:** The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD, and $\overline{\text{RESET}}$ voltages.
**Note 4:** Parameter is not 100% tested. Majority of all units meet this specification.

## Maxim Advantage

- Lower Supply Current
- Increased Output Source Current
- Guaranteed THRESHOLD, $\overline{\text{TRIGGER}}$, and $\overline{\text{RESET}}$ Input Currents
- Guaranteed Discharge Output Voltage
- Supply Current Guaranteed Over Temperature
- Significantly Improved ESD Protection (Note 6)
- Maxim Quality and Reliability

## Absolute Maximum Ratings

This device conforms to the Absolute Maximum Ratings on adjacent page.

## Electrical Characteristics

Specifications below satisfy or exceed all “tested” parameters on adjacent page.
(V+ = +2V to +15V; $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage | V+ | -20°C ≤ $T_A$ ≤ +85° | | 2 | | 16.5 | V |
| | | -55°C ≤ $T_A$ ≤ +125° | | 3 | | 16 | |
| Supply Current (Note 3) | I+ | ICM7555 | V+ = 2V to 16.5V; $T_A$ = +25°C | | 30 | 250 | µA |
| | | | V+ = 5V; $T_A$ = +25°C | | | 120 | |
| | | | V+ = 5V; -20°C ≤ $T_A$ ≤ +85°C | | | 250 | |
| | | | V+ = 5V; -55°C ≤ $T_A$ ≤ +125°C | | | 300 | |
| | | ICM7556 | V+ = 2V to 16.5V; $T_A$ = +25°C | | 60 | 500 | µA |
| | | | V+ = 5V; $T_A$ = +25°C | | | 240 | |
| | | | V+ = 5V; -20°C ≤ $T_A$ ≤ +85°C | | | 500 | |
| | | | V+ = 5V; -55°C ≤ $T_A$ ≤ +125°C | | | 600 | |
| Timing Error (Note 4) | | Circuit of Figure 1b; $R_A$ = $R_B$ 100kΩ, C = 0.1µF, V+ = 5V | | | | | |
| Initial Accuracy (Note 5) | | | | | 2.0 | 5.0 | % |
| Drift with Temperature | | V+ = 5V | | | 50 | | ppm/°C |
| | | V+ = 10V | | | 75 | | |
| | | V+ = 15V | | | 100 | | |
| Drift with Supply Voltage | | V+ = 5V | | | 1.0 | 3.0 | %V |
| Threshold Voltage | $V_{TH}$ | V+ = 5V | | 0.63 | 0.66 | 0.67 | V+ |
| Trigger Voltage | $V_{TRIG}$ | V+ = 5V | | 0.29 | 0.33 | 0.34 | V+ |
| Trigger Current | $I_{TRIG}$ | V+ = 16.5V | | | 50 | | pA |
| | | V+ = 5V | | | 10 | | |
| | | V+ = 2V | | | 1 | | |
| Threshold Current | $I_{TH}$ | V+ = 16.5V | | | 50 | | pA |
| | | V+ = 5V | | | 10 | | |
| | | V+ = 2V | | | 1 | | |
| Reset Current | $I_{RST}$ | $V_{REST}$ = Ground | V+ = 16.5V | | 100 | | pA |
| | | | V+ = 5V | | 20 | | |
| | | | V+ = 2V | | 2 | | |

## Electrical Characteristics (continued)

Specifications below satisfy or exceed all “tested” parameters on adjacent page.
(V+ = +2V to +15V; $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Reset Voltage | $V_{RST}$ | V+ = 16.5V | | | 0.4 | 0.7 | 1.2 | V |
| | | V+ = 2V | | | 0.4 | 0.7 | 1.2 | |
| Control Voltage | $V_{CV}$ | V+ = 5V | | | 0.62 | 0.66 | 0.67 | V+ |
| Output Voltage Drop | $V_O$ | Output Lo | V+ = 16.5V | $I_{SINK}$ = 3.2mA | | 0.1 | 0.4 | V |
| | | | V+ = 5V | $I_{SINK}$ = 3.2mA | | 0.15 | 0.4 | |
| | | Output Hi | V+ = 16.5V | $I_{SOURCE}$ = 2.0mA | 15.75 | 16.25 | | |
| | | | V+ = 5V | $I_{SOURCE}$ = 2.0mA | 4.0 | 4.5 | | |
| Discharge Output Voltage | $V_{DIS}$ | V+ = 5V, $I_{DIS}$ = 3.2mA | | | | 0.1 | 0.4 | V |
| Rise Time of Output (Note 4) | $t_r$ | $R_L$ = 10MΩ | $C_L$ = 10pF | V+ = 5V | 35 | 40 | 75 | ns |
| Fall Time of Output (Note 4) | $t_f$ | $R_L$ = 10MΩ | $C_L$ = 10pF | V+ = 5V | 35 | 40 | 75 | |
| Guaranteed Max Osc. Frequency (Note 4) | $f_{max}$ | Astable Operation | | | 500 | | | kHz |

**Note 1:** Due to tho SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ + 3V or less than V- - 0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/ICM7556 must be turned on first.

**Note 2:** Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C, power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (ICM7556) or 2mW/°C (ICM7555).

**Note 3:** The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD, and $\overline{\text{RESET}}$ voltages.

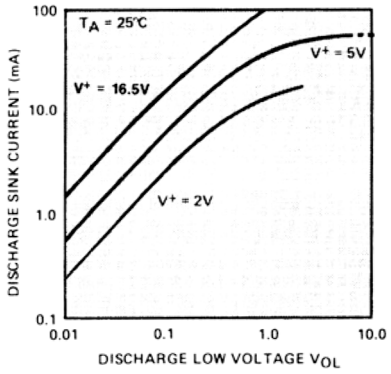
**Note 4:** Parameter is not 100% tested. Majority of all units meet this specification.

**Note 5:** Deviation from f = 1.46/($R_A$ + 2 $R_B$)C. V+ = 5V.

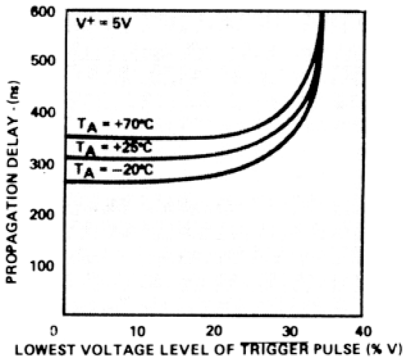
**Note 6:** All pins are designed to withstand electrostatic discharge (ESD) level in excess of 2000V. (Mil Std 883B Method 3015 1 Test Circuit).

## Typical Operating Characteristics

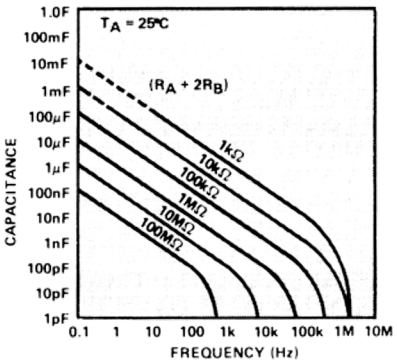
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



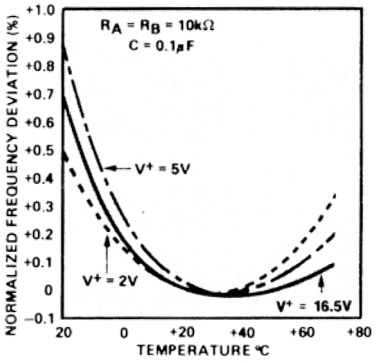

PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



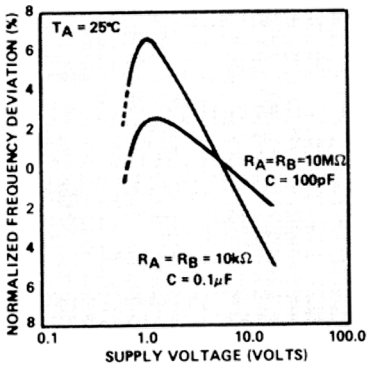

FREE RUNNING FREQUENCY AS A FUNCTION OF $R_A$, $R_B$ AND C



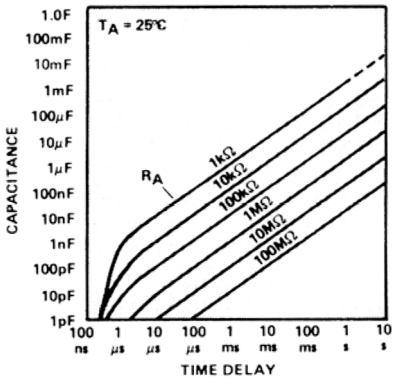

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE




NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE

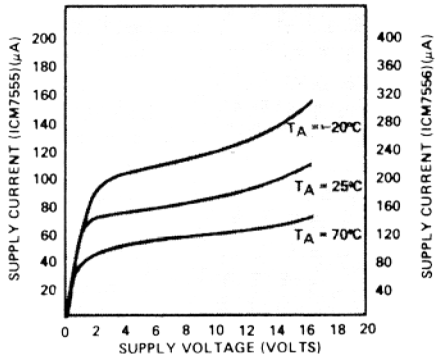



TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF $R_A$ AND C

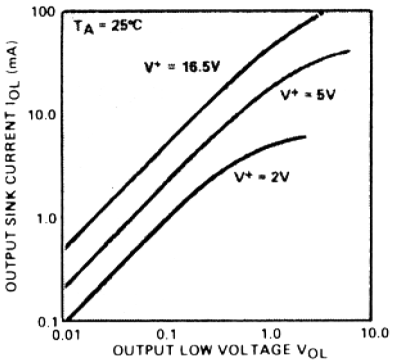


## Typical Operating Characteristics (continued)

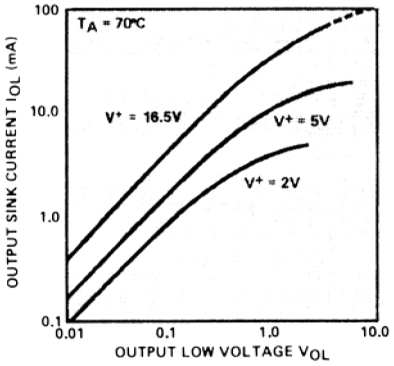
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



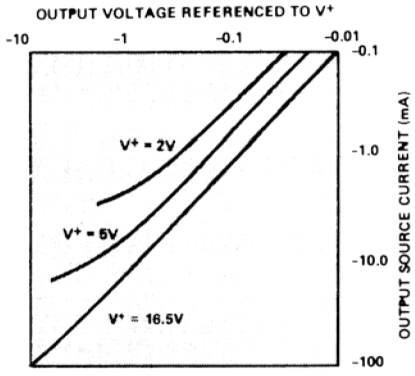

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



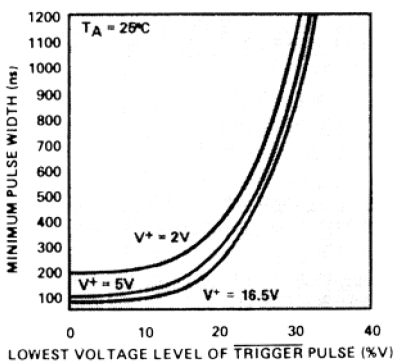

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



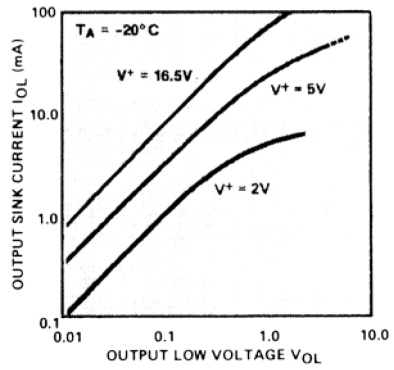

OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE




MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING




OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



## Detailed Description

Both the ICM7555 timer and the ICM7556 dual timer can be configured for either astable or monostable operation. In the astable mode, the free-running frequency and the duty cycle are controlled by two external resistors and one capacitor. Similarly, the pulse width in the monostable mode is precisely controlled by one external resistor and capacitor.

The external component count is decreased when replacing a bipolar timer with the ICM7555 or ICM7556. The bipolar devices produce large crowbar currents in the output driver. To compensate for this spike, a capacitor is used to decouple the power-supply lines. The CMOS timers produce supply spikes of only 2mA to 3mA vs. 300mA to 400mA (Bipolar), therefore supply decoupling is typically not needed. This current spike comparison is illustrated in Figure 3. Another component is eliminated at the control voltage pin. These CMOS timers, due to the high-impedance inputs of the comparators, do not require decoupling capacitors on the control voltage pin.

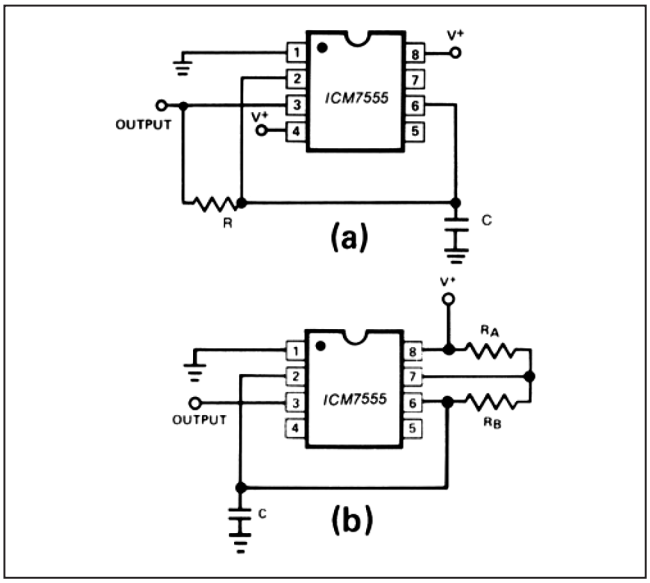



*Figure 1. Maxim ICM7555 Used in Two Different Astable Configurations*

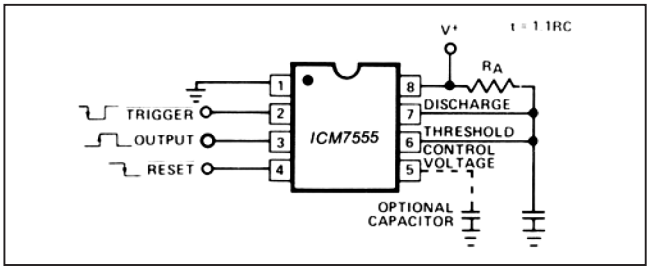



*Figure 2. Maxim ICM7555 in Monostable Operation*

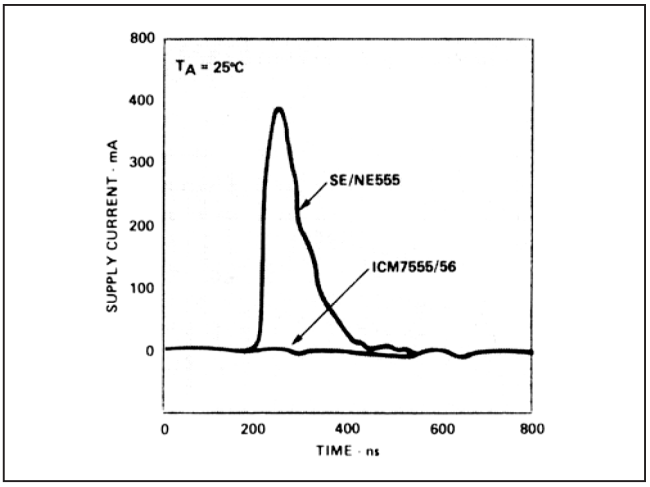



*Figure 3. Supply Current Transient Compared With A Standard Bipolar 555 During An Output Transition*

## Applications Information

### Astable Operation

Maxim recommends either of the two astable circuit configurations illustrated in Figure 1. The circuit in Figure 1a provides a 50% duty-cycle output using one timing resistor and capacitor. The oscillator waveform across the capacitor is symmetrical and triangular, swinging from 1/3 to 2/3 of the supply voltage. The frequency generated is defined by:

$$f = \frac{1}{1.4\,RC}$$

The circuit in Figure 1b provides a means of varying the duty cycle of the oscillator. The frequency is defined by:

$$f = \frac{1.46}{(R_A + 2R_B)C}$$

The duty cycle is:

$$D = \frac{R_B}{(R_A + 2R_B)}$$

### Monostable Operation

The circuit diagram in Figure 2 illustrates monostable operation. In this mode the timer acts as a one shot. Initially the external capacitor is held discharged by the discharge output. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the capacitor begins to charge exponentially through $R_A$. The device resets after the voltage across the capacitor reaches ⅔(V+).

$$t_{OUTPUT} = -\ln(1/3)R_AC = 1.1R_AC$$

### Reset

The reset function is significantly improved over the standard bipolar 555 and 556 in that it controls only the internal flip-flop, which in turn simultaneously controls the state of the Output and Discharge pins. This avoids the multiple threshold problems sometimes encountered with slow-falling edges of the bipolar devices. This input is designed to have essentially the same trip voltage as the standard bipolar devices (0.6V to 0.7V). At all supply voltages this input maintains an extremely high impedance.

### Control Voltage

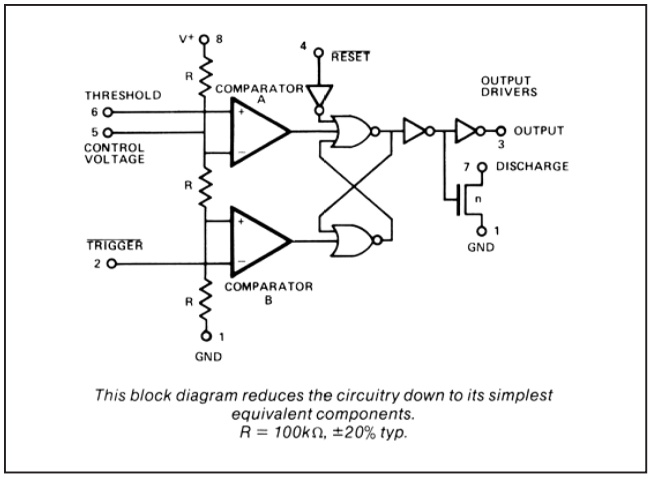
The control voltage regulates the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators. This pin can be used for frequency modulation in the astable mode. By varying the applied voltage to the control voltage pin, delay times can be changed in the monostable mode.

### Power-Supply Considerations

Since the $\overline{\text{TRIGGER}}$, THRESHOLD, and Discharge leakage currents are very low, high-impedance timing components may be used, keeping total system supply current at a minimum.

### Output Drive Capability

The CMOS output stage is capable of driving most logic families including CMOS and TTL. The ICM7555 and ICM7556 will drive at least two standard TTL loads at a supply voltage of 4.5V or greater. When driving CMOS, the output swing at all supply voltage levels will equal the supply voltage.




*This block diagram reduces the circuitry down to its simplest equivalent components.*
*R = 100kΩ, ±20% typ.*

*Figure 4. Block Diagram of ICM7555*

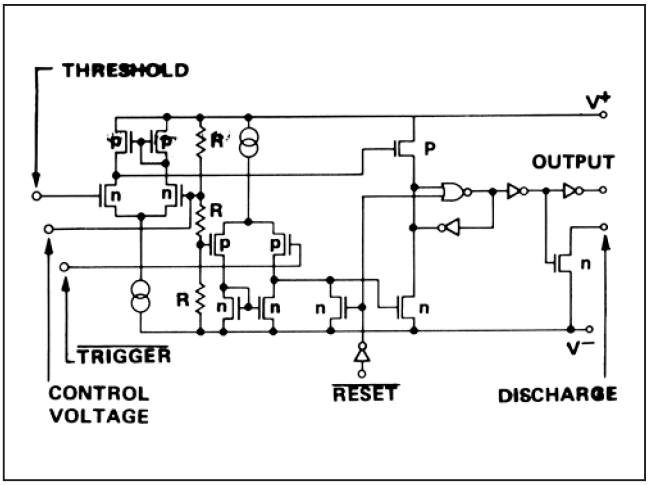



*Figure 5. Equivalent Circuit*

## Function Table

| $\overline{\text{RESET}}$ | $\overline{\text{TRIGGER}}$ VOLTAGE | THRESHOLD VOLTAGE | OUTPUT | DISCHARGE SWITCH |
|---|---|---|---|---|
| Low | Irrelevant | Irrelevant | Low | On |
| High | < 1/3 V+ | Irrelevant | High | Off |
| High | > 1/3 V+ | > 2/3 V+ | Low | On |
| High | > 1/3 V+ | < 2/3 V+ | As previously established | |

†*Voltage levels shown are nominal.*

***Note:*** *$\overline{\text{RESET}}$ will dominate all other inputs. $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.*

## Chip Information

PROCESS: CMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 8 PDIP | P8-1 | **21-0043** | — |
| 8 SO | S8-2 | **21-0041** | **90-0096** |
| 14 PDIP | P14-3 | **21-0043** | — |
| 14 CERDIP | J14-3 | **21-0045** | — |
| 14 SO | S14-1 | **21-0041** | **90-0112** |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 4/88 | Initial Release | — |
| 2 | 11/92 | Revised *Electrical Characteristics* | 3 |
| 3 | 3/13 | Updated *Ordering Information* | 1 |

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