MAX127/MAX128

Multirange, +5V, 12-Bit DAS with 2-Wire Serial Interface

General Description

The MAX127/MAX128 are multirange, 12-bit data acquisition systems (DAS) that require only a single +5V supply for operation, yet accept signals at their analog inputs that may span above the power-supply rail and below ground. These systems provide eight analog input channels that are independently software programmable for a variety of ranges: ±10V, ±5V, 0 to +10V, 0 to +5V for the MAX127; and $\pm V_{REF}$, $\pm V_{REF}/2$, 0 to $+V_{REF}$, 0 to $+V_{REF}/2$ for the MAX128. This range switching increases the effective dynamic range to 14 bits and provides the flexibility to interface 4–20mA, ±12V, and ±15V-powered sensors directly to a single +5V system. In addition, these converters are fault protected to ±16.5V; a fault condition on any channel will **not** affect the conversion result of the selected channel. Other features include a 5MHz bandwidth track/hold, an 8ksps throughput rate, and the option of an internal 4.096V or external reference.

The MAX127/MAX128 feature a 2-wire, I²C-compatible serial interface that allows communication among multiple devices using SDA and SCL lines.

A hardware shutdown input ($\overline{SHDN}$) and two software-programmable power-down modes (standby and full power-down) are provided for low-current shutdown between conversions. In standby mode, the reference buffer remains active, eliminating startup delays.

The MAX127/MAX128 are available in 24-pin narrow PDIP or space-saving 28-pin SSOP packages.

Applications

- Industrial Control Systems
- Data-Acquisition Systems
- Robotics
- Automatic Testing
- Battery-Powered Instruments
- Medical Instruments

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX127ACNG+	0°C to +70°C	24 Narrow PDIP	±1/2
MAX127ACNG+	0°C to +70°C	24 Narrow PDIP	±1

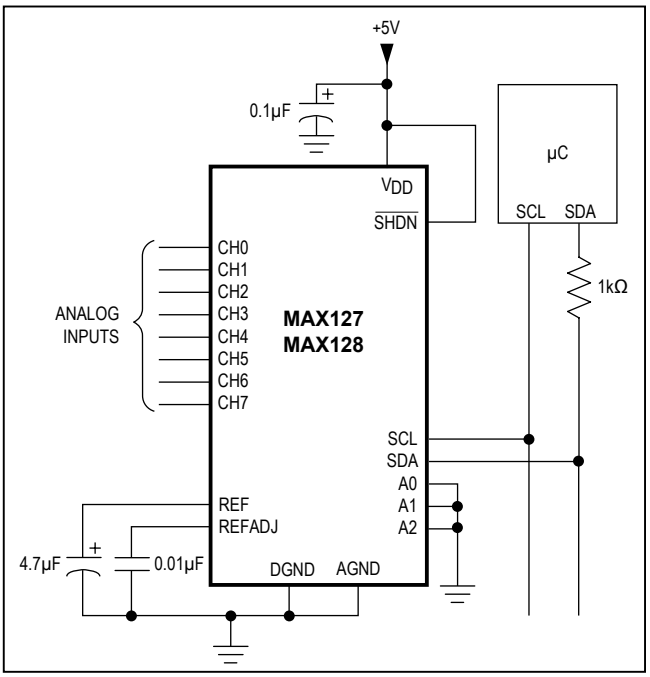
+Denotes a lead(Pb)-free/RoHS-compliant package.

Ordering Information continued at end of data sheet.

Features

- 12-Bit Resolution, 1/2 LSB Linearity
- +5V Single-Supply Operation
- I²C-Compatible, 2-Wire Serial Interface
- Four Software-Selectable Input Ranges
  - MAX127: 0 to +10V, 0 to +5V, ±10V, ±5V
  - MAX128: 0 to $+V_{REF}$, 0 to $+V_{REF}/2$, $\pm V_{REF}$, $\pm V_{REF}/2$
- 8 Analog Input Channels
- 8ksps Sampling Rate
- ±16.5V Overvoltage-Tolerant Input Multiplexer
- Internal 4.096V or External Reference
- Two Power-Down Modes
- 24-Pin Narrow PDIP or 28-Pin SSOP Packages

Typical Operating Circuit



Pin Configurations appear at end of data sheet.

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Absolute Maximum Ratings

V_{DD} to AGND .....-0.3V to +6V
AGND to DGND .....-0.3V to +0.3V
CH0–CH7 to AGND.....±16.5V
REF to AGND.....-0.3V to (V_{DD} + 0.3V)
REFADJ to AGND .....-0.3V to (V_{DD} + 0.3V)
A0, A1, A2 to DGND.....-0.3V to (V_{DD} + 0.3V)
$\overline{SHDN}$, SCL, SDA to DGND .....-0.3V to +6V
Max Current into Any Pin 50mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin Narrow PDIP
(derate 13.33mW/°C above +70°C) 1067mW
28-Pin SSOP (derate 15mW/°C above +70°C).....1201mW
Operating Temperature Ranges
MAX127_ C_ _/MAX128_ C_ _.....0°C to +70°C
MAX127_ E_ _/MAX128_ E_ _..... -40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = +5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF; external clock, f_{CLK} = 400kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				12			Bits
Integral Nonlinearity	INL	MAX127A				±1/2	LSB
		MAX127B/MAX128B				±1	
Differential Nonlinearity	DNL					±1	LSB
Offset Error		Unipolar	MAX127A			±3	LSB
			MAX127B/MAX128B			±5	
		Bipolar	MAX127A			±5	
			MAX127B/MAX128B			±10	
Channel-to-Channel Offset Error Matching		Unipolar			±0.1		LSB
		Bipolar			±0.3		
Gain Error (Note 2)		Unipolar	MAX127A			±7	LSB
			MAX127B/MAX128B			±10	
		Bipolar	MAX127A			±7	
			MAX127B/MAX128B			±10	
Gain Tempco (Note 2)		Unipolar			3		ppm/°C
		Bipolar			5		
DYNAMIC SPECIFICATIONS (800Hz sine-wave input, ±10V_{P-P} (MAX127) or ±4.096V_{P-P} (MAX128), f_{SAMPLE} = 8ksps)							
Signal-to-Noise Plus Distortion Ratio	SINAD			70			dB
Total Harmonic Distortion	THD	Up to the 5th harmonic			-87	-80	dB
Spurious-Free Dynamic Range	SFDR			81			dB
Channel-to-Channel Crosstalk		4kHz, V_{IN} = ±5V (Note 3)			-86		dB
		DC, V_{IN} = ±16.5V			-96		
Aperture Delay					200		ns
Aperture Jitter					10		ns

Electrical Characteristics (continued)

(V_{DD} = +5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF; external clock, f_{CLK} = 400kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG INPUT								
Track/Hold Acquisition Time							3	µs
Small-Signal Bandwidth		-3dB rolloff	±10V or ±V_{REF} range			5		MHz
			±5V or ±V_{REF}/2 range			2.5		
			0 to 10V or 0 to V_{REF} range			2.5		
			0 to 5V or 0 to V_{REF}/2 range			1.25		
Input Voltage Range	V_{IN}	Unipolar, Table 3	MAX127		0		10	V
					0		5	
			MAX128		0		V_{REF}	
					0		V_{REF}/2	
		Bipolar, Table 3	MAX127		-10		+10	
					-5		+5	
			MAX128		-V_{REF}		V_{REF}	
					-V_{REF}/2		V_{REF}/2	
Input Current	I_{IN}	Unipolar	MAX127	0 to 10V range	-10		+720	µA
				0 to 5V range	-10		+360	
			MAX128		-10	+0.1	+10	
		Bipolar	MAX127	±10V range	-1200		+720	
				±5V range	-600		+360	
			MAX128	±V_{REF} range	-1200		+10	
				±V_{REF}/2 range	-600		+10	
Input Resistance	$\Delta V_{IN}/\Delta I_{IN}$	Unipolar				21		kΩ
		Bipolar				16		
Input Capacitance		(Note 4)					40	pF
INTERNAL REFERENCE								
REFOUT Voltage	V_{REF}	T_A = +25°C			4.076	4.096	4.116	V
REFOUT Tempco	TC V_{REF}	MAX127_C/MAX128_C				±15		ppm/°C
		MAX127_E/MAX128_E				±30		
Output Short-Circuit Current							30	mA
Load Regulation (Note 5)		0 to 0.5mA output current					10	mV
Capacitive Bypass at REF					4.7			µF
REFADJ Output Voltage					2.465	2.500	2.535	V
REFADJ Adjustment Range		Figure 12				±1.5		%
Buffer Voltage Gain						1.638		V/V

Electrical Characteristics (continued)

(V_{DD} = +5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF; external clock, f_{CLK} = 400kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT (buffer disabled, reference input applied to REF)							
Input Voltage Range				2.4		4.18	V
Input Current		V_{REF} = 4.18V	Normal, or STANDBY power-down mode			400	µA
			FULL power-down mode			1	
Input Resistance		Normal or STANDBY power-down mode		10			kΩ
		FULL power-down mode		5			MΩ
REFADJ Threshold for Buffer Disable				V_{DD} - 0.5			V
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
Supply Current	I_{DD}	Normal mode, bipolar ranges				18	mA
		Normal mode, unipolar ranges			6	10	
		STANDBY power-down mode (Note 6)			700	850	µA
		FULL power-down mode			120	220	
Power-Supply Rejection Ratio (Note 7)	PSRR	External reference = 4.096V			±0.1	±0.5	LSB
		Internal reference			±0.5		
TIMING							
External Clock Frequency Range	f_{CLK}					0.4	MHz
Conversion Time	t_{CONV}			6.0	7.7	10.0	µs
Throughput Rate						8	ksps
Bandgap Reference Startup Time		Power-up (Note 8)			200		µs
Reference Buffer Settling Time		To 0.1mV, REF bypass capacitor fully discharged	C_{REF} = 4.7µF		8		ms
			C_{REF} = 33µF		60		
DIGITAL INPUTS ($\overline{SHDN}$, A2, A1, A0)							
Input High Threshold Voltage	V_{IH}					2.4	V
Input Low Threshold Voltage	V_{IL}			0.8			V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			±0.1	±10	µA
Input Capacitance	C_{IN}	(Note 4)				15	pF
Input Hysteresis	V_{HYS}				0.2		V

Electrical Characteristics (continued)

(V_{DD} = +5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF; external clock, f_{CLK} = 400kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDA, SCL)						
Input High Threshold Voltage	V_{IH}				0.7 x V_{DD}	V
Input Low Threshold Voltage	V_{IL}		0.3 x V_{DD}			V
Input Hysteresis	V_{HYS}		0.05 x V_{DD}			V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		±0.1	±10	µA
Input Capacitance	C_{IN}	(Note 4)			15	pF
DIGITAL OUTPUTS (SDA)						
Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
		I_{SINK} = 6mA			0.6	
Three-State Output Capacitance	C_{OUT}	(Note 4)			15	pF

Timing Characteristics

(V_{DD} = +4.75V to +5.25V; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE FAST MODE						
SCL Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
Rise Time for Both SDA and SCL Signals (Receiving)	t_R	C_b = Total capacitance of one bus line in pF	20 + 0.1 x C_b		300	ns
Fall Time for Both SDA and SCL Signals (Receiving)	t_F	C_b = Total capacitance of one bus line in pF	20 + 0.1 x C_b		300	ns
Fall Time for Both SDA and SCL Signals (Transmitting)	t_F	C_b = Total capacitance of one bus line in pF	20 + 0.1 x Cb		250	ns
Set-Up Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF
Pulse Width of Spike Suppressed	t_{SP}		0		50	ns

Timing Characteristics (continued)

(V_{DD} = +4.75V to +5.25V; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

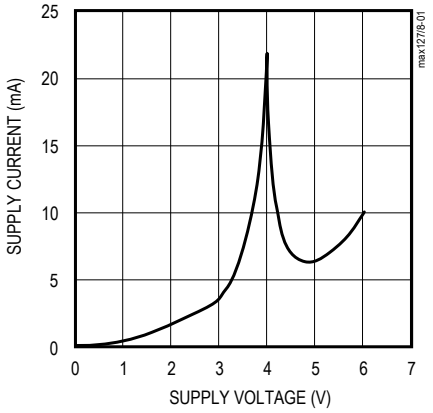
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE STANDARD MODE						
SCL Clock Frequency	f_{SCL}				100	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		4.7			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		4.0			µs
Low Period of the SCL Clock	t_{LOW}		4.7			µs
High Period of the SCL Clock	t_{HIGH}		4.0			µs
Setup Time for a Repeated START Condition	$t_{SU, STA}$		4.7			µs
Data Hold Time	$t_{HD, DAT}$		0		0.9	µs
Data Setup Time	$t_{SU, DAT}$		250			ns
Rise Time for Both SDA and SCL Signals (Receiving)	t_R				1000	ns
Fall Time for Both SDA and SCL Signals (Receiving)	t_F				300	ns
Fall Time for Both SDA and SCL Signals (Transmitting)	t_F	C_b = total capacitance of one bus line in pF, up to 6mA sink	20 + 0.1 x C_b		250	ns
Setup Time for STOP Condition	$t_{SU, STO}$		4.0			µs
Capacitive Load for Each Bus Line	C_b				400	pF
Pulse Width of Spike Suppressed	t_{SP}		0		50	ns

Note 1: Accuracy specifications tested at V_{DD} = 5.0V. Performance at power-supply tolerance limits is guaranteed by Power-Supply Rejection test.
Note 2: External reference: V_{REF} = 4.096V, offset error nulled, ideal last-code transition = FS - 3/2 LSB.
Note 3: Ground “on” channel, sine wave applied to all “off” channels.
Note 4: Guaranteed by design. Not tested.
Note 5: Use static external load during conversion for specified accuracy.
Note 6: Tested using internal reference.
Note 7: PSRR measured at full scale. Tested for the ±10V (MAX127) and ±4.096V (MAX128) input ranges.
Note 8: Not subject to production testing. Provided for design guidance only.

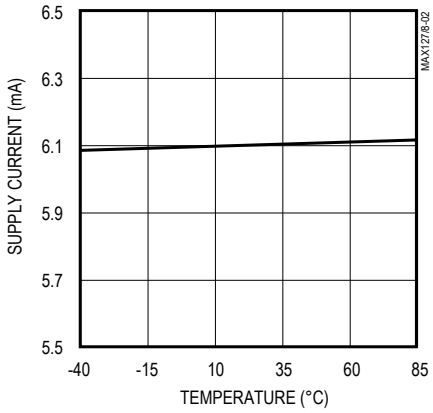
Typical Operating Characteristics

(V_{DD} = +5V, external reference mode, V_{REF} = 4.096V; 4.7µF at REF; external clock, f_{CLK} = 400kHz; T_A = +25°C, unless otherwise noted.)

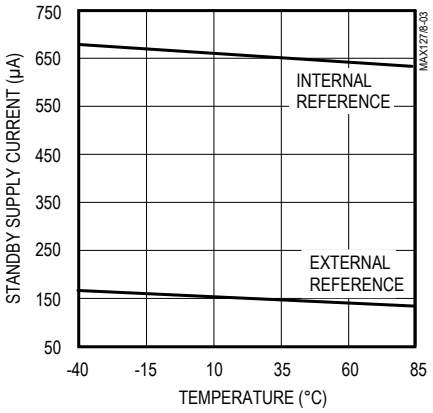
SUPPLY CURRENT vs. SUPPLY VOLTAGE



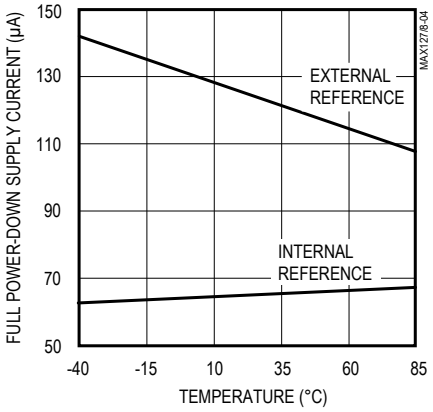
SUPPLY CURRENT vs. TEMPERATURE



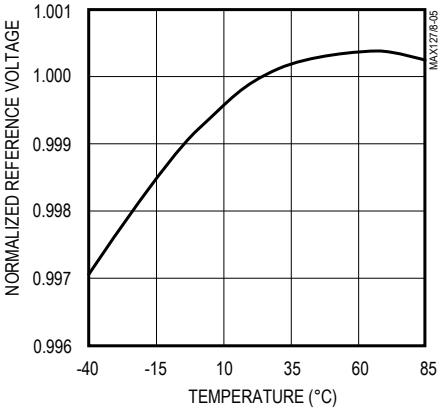
STANDBY SUPPLY CURRENT vs. TEMPERATURE



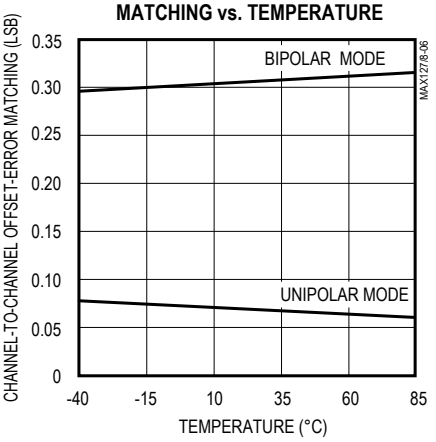
FULL POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



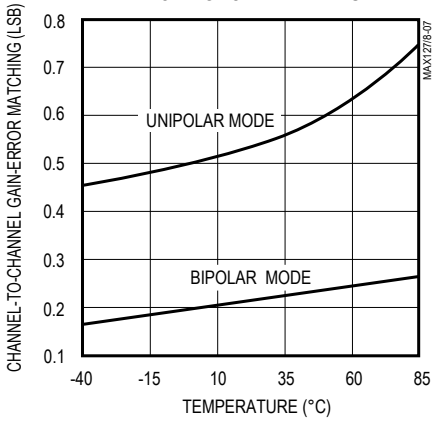
NORMALIZED REFERENCE VOLTAGE vs. TEMPERATURE



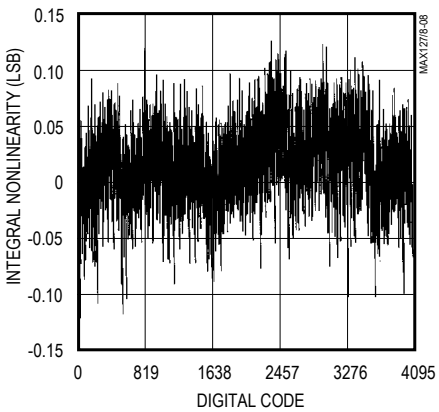
CHANNEL-TO-CHANNEL OFFSET-ERROR MATCHING vs. TEMPERATURE



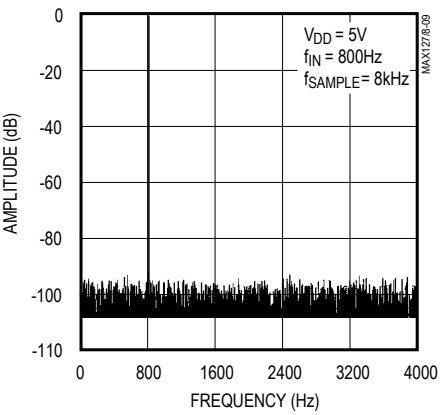
CHANNEL-TO-CHANNEL GAIN-ERROR MATCHING vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. DIGITAL CODE



FFT PLOT



Pin Description

PIN		NAME	FUNCTION
NARROW PDIP	SSOP		
1, 2	1, 2	V_{DD}	+5V Supply. Bypass with a 0.1µF capacitor to AGND.
3, 9, 22, 24	4, 7, 8, 11, 22, 24, 25, 28	N.C.	No Connection. No internal connection.
4	3	DGND	Digital Ground
5	5	SCL	Serial Clock Input
6, 8, 10	6, 10, 12	A0, A2, A1	Address Select Inputs
7	9	SDA	Open-Drain Serial Data I/O. Input data is clocked in on the rising edge of SCL, and output data is clocked out on the falling edge of SCL. External pullup resistor required.
11	13	$\overline{SHDN}$	Shutdown Input. When low, device is in full power-down (FULLPD) mode. Connect high for normal operation.
12	14	AGND	Analog Ground
13–20	15–21, 23	CH0–CH7	Analog Input Channels
21	26	REFADJ	Bandgap Voltage-Reference Output/External Adjust Pin. Bypass with a 0.01µF capacitor to AGND. Connect to V_{DD} when using an external reference at REF.
23	27	REF	Reference Buffer Output/ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal reference by pulling REFADJ to V_{DD} and applying the external reference to REF.

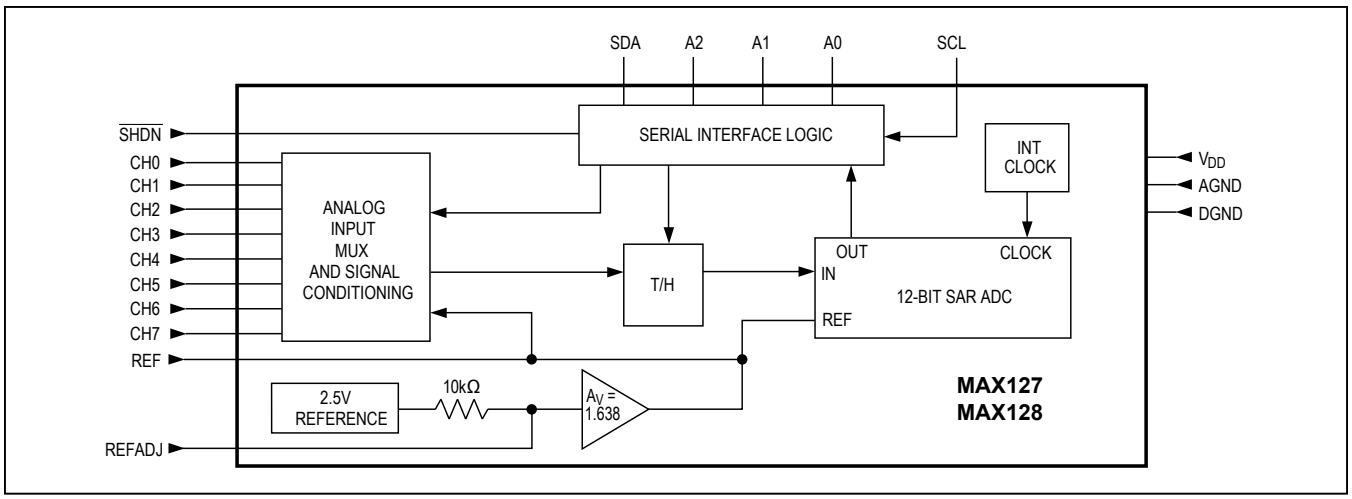


Figure 1. Block Diagram

Detailed Description

Converter Operation

The MAX127/MAX128 multirange, fault-tolerant ADCs use successive approximation and internal track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. Figure 1 shows the block diagram for these devices.

Analog-Input Track/Hold

The T/H circuitry enters its tracking/acquisition mode on the falling edge of the sixth clock in the 8-bit input control word and enters its hold/conversion mode when the master issues a STOP condition. For timing information, see the *Start a Conversion* section.

Input Range and Protection

The MAX127/MAX128 have software-selectable input ranges. Each analog input channel can be independently programmed to one of four ranges by setting the appropriate control bits (RNG, BIP) in the control byte (Table 1). The MAX127 has selectable input ranges extending to ±10V (±V_{REF} x 2.441), while the MAX128 has selectable input ranges extending to ±V_{REF}. Note that when an external reference is applied at REFADJ, the voltage at REF is given by V_{REF} = 1.638 x V_{REFADJ} (2.4 < V_{REF} < 4.18). Figure 2 shows the equivalent input circuit.

A resistor network on each analog input provides a ±16.5V fault protection for all channels. This circuit limits the current going into or out of the pin to less than 1.2mA, whether or not the channel is on. This provides an added layer of protection when momentary overvoltages occur at the selected input channel, and when a negative signal is applied at the input even though the device may be configured for unipolar mode. Overvoltage protection is active even if the device is in power-down mode or V_{DD} = 0V.

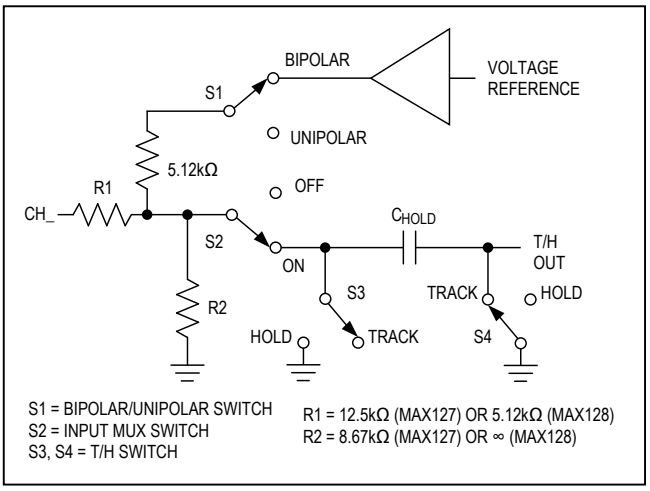


Figure 2. Equivalent Input Circuit

Digital Interface

The MAX127/MAX128 feature a 2-wire serial interface consisting of the SDA and SCL pins. SDA is the data I/O and SCL is the serial clock input, controlled by the master device. A2–A0 are used to program the MAX127/MAX128 to different slave addresses. (The MAX127/MAX128 only work as slaves.) The two bus lines (SDA and SCL) must be high when the bus is not in use. External pullup resistors (1kΩ or greater) are required on SDA and SCL to maintain I^2C compatibility. Table 1 shows the input control-byte format.

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
START	SEL2	SEL1	SEL0	RNG	BIP	PD1	PD0

BIT	NAME	DESCRIPTION
7 (MSB)	START	The logic “1” received after acknowledge of a write bit (R/$\overline{W}$ = 0) defines the beginning of the control byte.
6, 5, 4	SEL2, SEL1, SEL0	These three bits select the desired “ON” channel **(Table 2)**.
3	RNG	Selects the full-scale input voltage range **(Table 3)**.
2	BIP	Selects unipolar or bipolar conversion mode **(Table 3)**.
1, 0 (LSB)	PD1, PD0	These two bits select the power-down modes **(Table 4)**.

Table 2. Channel Selection

SEL2	SEL1	SEL0	CHANNEL
0	0	0	CH0
0	0	1	CH1
0	1	0	CH2
0	1	1	CH3
1	0	0	CH4
1	0	1	CH5
1	1	0	CH6
1	1	1	CH7

Table 4. Power-Down and Clock Selection

PD1	PD0	SEL0
0	X	Normal Operation (always on)
1	0	Standby Power-Down Mode (STBYPD)
1	1	Full Power-Down Mode (FULLPD)

Table 3. Range and Polarity Selection

INPUT RANGE (V)	RNG	BIP	NEGATIVE FULL SCALE (V)	ZERO SCALE (V)	FULL SCALE (V)
MAX127					
0 to 5	0	0	—	0	V_{REF} x 1.2207
0 to 10	1	0	—	0	V_{REF} x 2.4414
±5	0	1	-V_{REF} x 1.2207	0	V_{REF} x 1.2207
±10	1	1	-V_{REF} x 2.4414	0	V_{REF} x 2.4414
MAX128					
0 to V_{REF}/2	0	0	—	0	V_{REF}/2
0 to V_{REF}	1	0	—	0	V_{REF}
±V_{REF}/2	0	1	-V_{REF}/2	0	V_{REF}/2
±V_{REF}	1	1	-V_{REF}	0	V_{REF}

Slave Address

The MAX127/MAX128 have a 7-bit-long slave address. The first four bits (MSBs) of the slave address have been factory programmed and are always 0101. The logic state of the address input pins (A2–A0) determine the three LSBs of the device address (Figure 3). A maximum of eight MAX127/MAX128 devices can therefore be connected on the same bus at one time.

A2–A0 may be connected to V_{DD} or DGND, or they may be actively driven by TTL or CMOS logic levels.

The eighth bit of the address byte determines whether the master is writing to or reading from the MAX127/MAX128 (R/$\overline{W}$ = 0 selects a write condition. R/$\overline{W}$ = 1 selects a read condition).

Conversion Control

The master signals the beginning of a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. When the master has finished communicating with the slave, the master issues a STOP condition (P), which is a low-to-high transition on SDA while SCL is high (Figure 4). The bus is then free for another transmission. Figure 5 shows the timing diagram for signals on the 2-wire interface. The address-byte, control-byte, and data-byte are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit words. Nine clock cycles are required to transfer the data in or out of the MAX127/MAX128. (Figures 9 and 10).

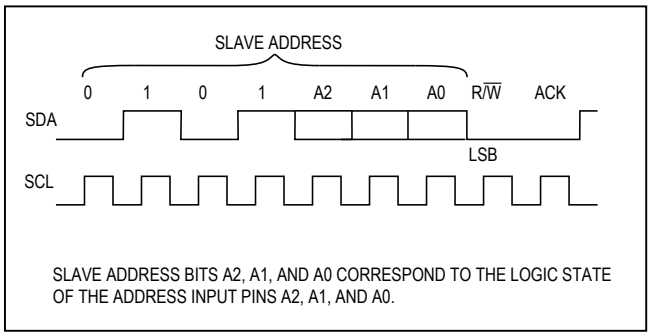


Figure 3. Address Byte

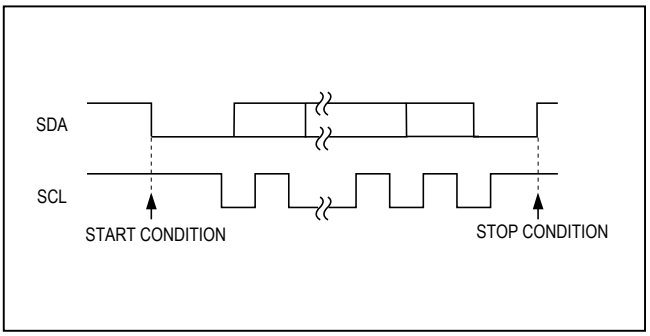


Figure 4. START and STOP Conditions

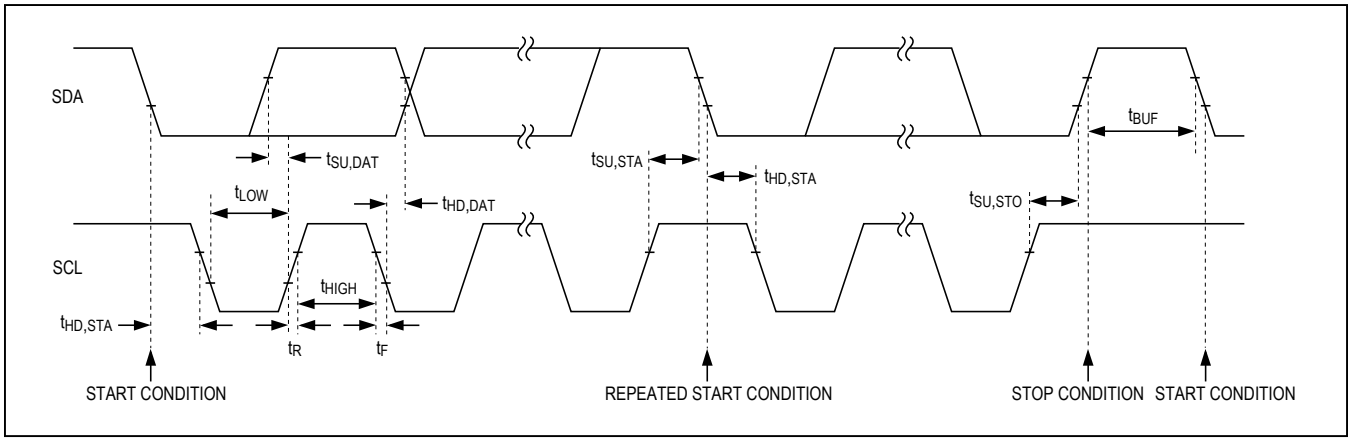


Figure 5. 2-Wire Serial-Interface Timing Diagram

Start a Conversion (Write Cycle)

A conversion cycle begins with the master issuing a START condition followed by seven address bits (Figure 3) and a write bit (R/$\overline{W}$ = 0). Once the eighth bit has been received and the address matches, the MAX127/MAX128 (the slave) issues an acknowledge by pulling SDA low for one clock cycle (A = 0). The master then writes the input control byte to the slave (Figure 8). After this byte of data, the slave issues another acknowledge, pulling SDA low for one clock cycle. The master ends the write cycle by issuing a STOP condition (Figure 6).

When the write bit is set (R/$\overline{W}$ = 0), acquisition starts as soon as Bit 2 (BIP) of the input control-byte has been latched and ends when a STOP condition has been issued. Conversion starts immediately after acquisition. The MAX127/MAX128's internal conversion clock frequency is 1.56MHz, resulting in a typical conversion time of 7.7µs. Figure 9 shows a complete write cycle.

Read a Conversion (Read Cycle)

Once a conversion starts, the master does not need to wait for the conversion to end before attempting to read the data from the slave. Data access begins with the master issuing a START condition followed by a 7-bit address (Figure 3) and a read bit (R/$\overline{W}$ = 1). Once the eighth bit has been received and the address matches, the slave issues an acknowledge by pulling low on SDA for one clock cycle (A = 0) followed by the first byte of serial data (D11–D4, MSB first). After the first byte has been issued by the slave, it releases the bus for the master to issue an acknowledge (A = 0). After receiving the acknowledge, the slave issues the second byte (D3–D0 and four zeros) followed by a NOT acknowledge ($\overline{A}$=1) from the master to indicate that the last data byte has been received. Finally, the master issues a STOP condition (P), ending the read cycle (Figure 7).

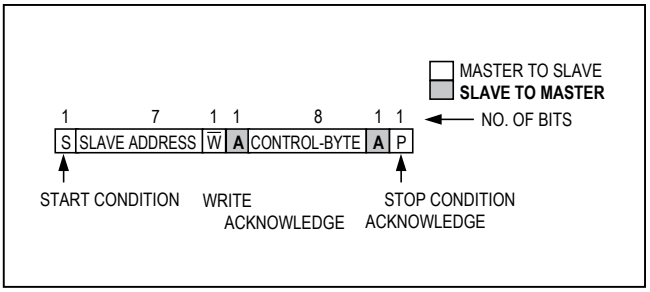


Figure 6. Write Cycle

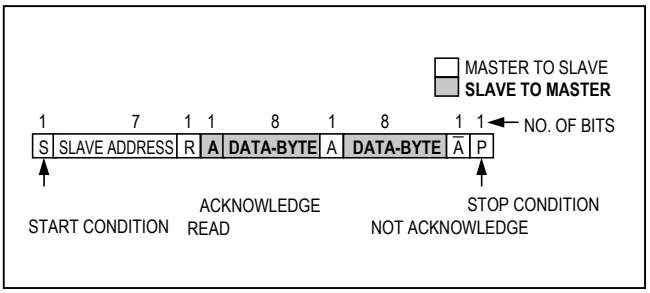


Figure 7. Read Cycle

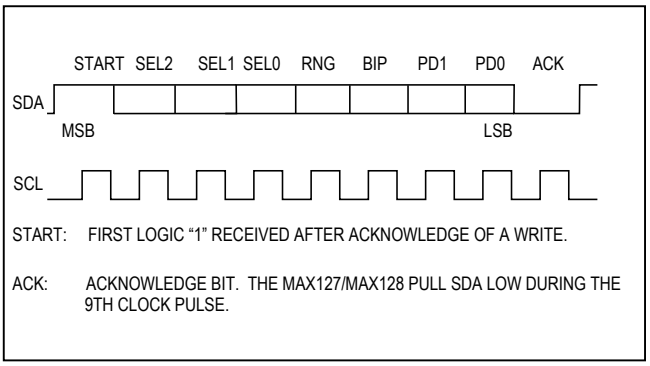


Figure 8. Command Byte

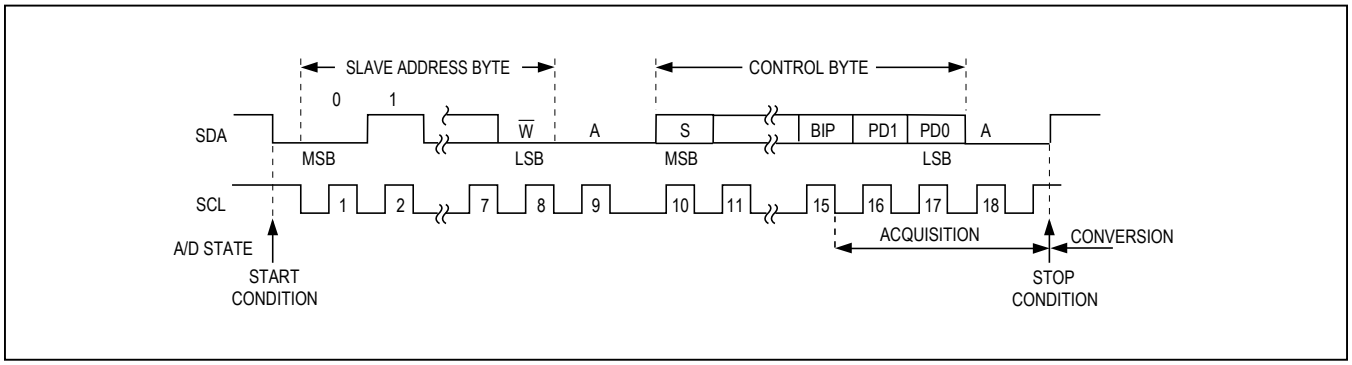


Figure 9. Complete 2-Wire Serial Write Transmission

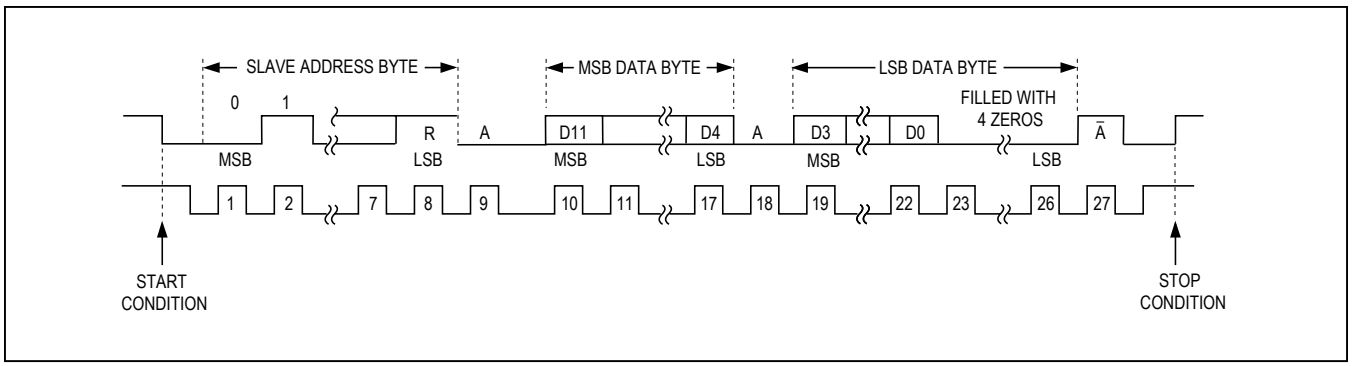


Figure 10. Complete 2-Wire Serial Read Transmission

The MAX127/MAX128 ignore acknowledge and not-acknowledge conditions issued by the master during the read cycle. The device waits for the master to read the output data or waits until a STOP condition is issued. Figure 10 shows a complete read cycle.

In unipolar input mode, the output is straight binary. For bipolar input mode, the output is two's complement. For output binary codes see the *Transfer Function* section.

Applications Information

Power-On Reset

The MAX127/MAX128 power up in normal operating mode, waiting for a START condition followed by the appropriate slave address. The contents of the input and output data registers are cleared at power-up.

Internal or External Reference

The MAX127/MAX128 operate with either an internal or an external reference (Figures 11a–11c). An external reference is connected to either REF or to REFADJ.

The REFADJ internal buffer gain is trimmed to 1.6384 to provide 4.096V at REF from a 2.5V reference.

Internal Reference

The internally trimmed 2.50V reference is amplified through the REFADJ buffer to provide 4.096V at REF. Bypass REF with a 4.7µF capacitor to AGND and bypass REFADJ with a 0.01µF capacitor to AGND (Figure 11a). The internal reference voltage is adjustable to ±1.5% (±65 LSBs) with the reference-adjust circuit of Figure 12.

External Reference

To use the REF input directly, disable the internal buffer by connecting REFADJ to V_{DD} (Figure 11b). Using the REFADJ input eliminates the need to buffer the reference externally. When the reference is applied at REFADJ, bypass REFADJ with a 0.01µF capacitor to AGND (Figure 11c).

At REF and REFADJ, the input impedance is a minimum of 10kΩ for DC currents. During conversions, an external reference at REF must be able to drive a 400µA DC load, and must have an output impedance of 10Ω or less. If the reference has higher input impedance or is noisy, bypass REF with a 4.7µF capacitor to AGND as close to the chip as possible.

With an external reference voltage of less than 4.096V at REF or less than 2.5V at REFADJ, the increase in RMS noise to the LSB value (full-scale voltage/4096) results in performance degradation and loss of effective bits.

Power-Down Mode

To save power, put the converter into low-current shutdown mode between conversions. Two programmable power-down modes are available, in addition to the hardware shutdown. Select STBYPD or FULLPD by programming PD0 and PD1 in the input control byte (Table 4). When software power-down is asserted, it becomes effective only after the end of conversion. In all power-down modes, the interface remains active and conversion results may be read. Input overvoltage protection is active in all power-down modes.

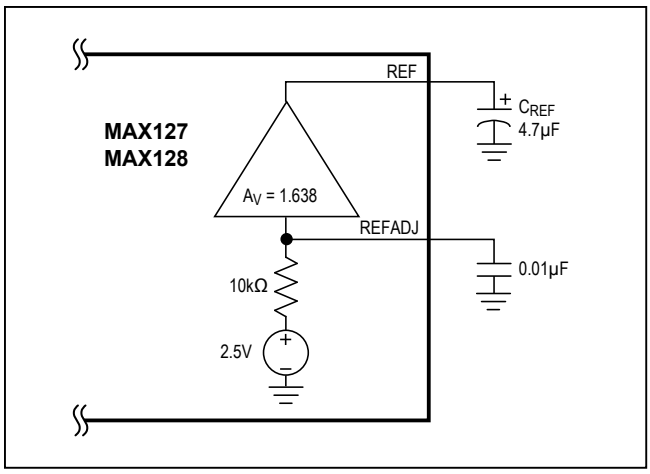


Figure 11a. Internal Reference

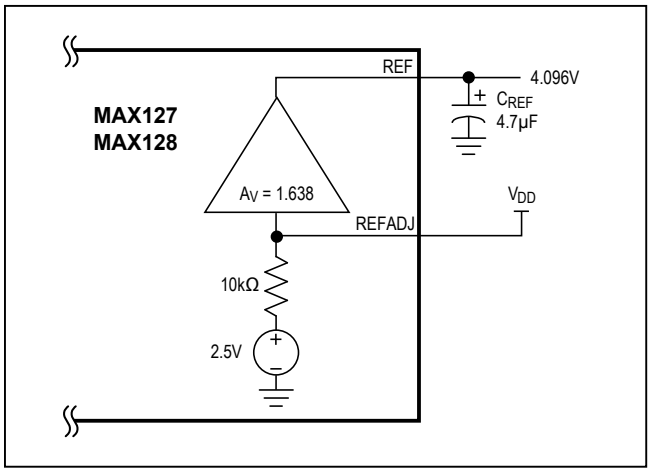


Figure 11b. External Reference, Reference at REF

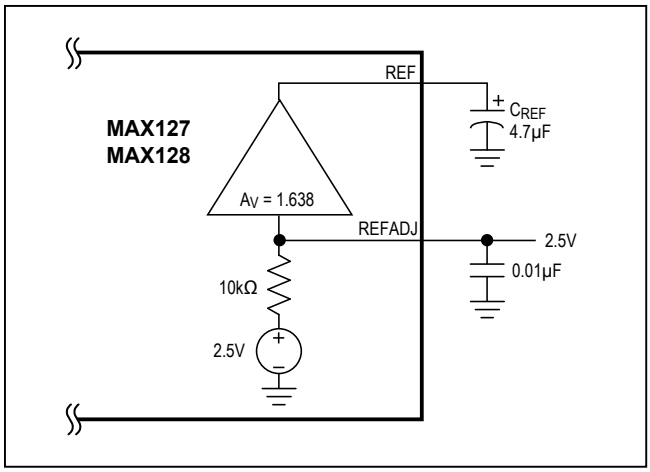


Figure 11c. External Reference, Reference at REFADJ

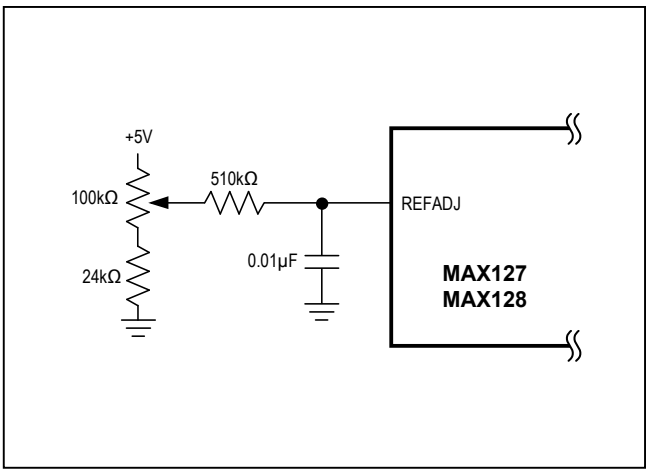


Figure 12. Reference-Adjust Circuit

To power-up from a software-initiated power-down, a START condition followed by the correct slave address must be received (with R/$\overline{W}$ = 0). The MAX127/MAX128 power-up after receiving the next bit.

For hardware-controlled power-down (FULLPD), pull $\overline{SHDN}$ low. When hardware shutdown is asserted, it becomes effective immediately and any conversion in progress is aborted.

Choosing Power-Down Modes

The bandgap reference and reference buffer remain active in STBYPD mode, maintaining the voltage on the 4.7µF capacitor at REF. This is a “DC” state that does not degrade after standby power-down of any duration.

In FULLPD mode, only the bandgap reference is active. Connect a 33µF capacitor between REF and AGND to maintain the reference voltage between conversions and to reduce transients when the buffer is enabled and disabled. Throughput rates down to 1ksps can be achieved without allotting extra acquisition time for reference recovery prior to conversion. This allows conversion to begin immediately after power-down ends. If the discharge of the REF capacitor during FULLPD exceeds the desired limits for accuracy (less than a fraction of an LSB), run a STBYPD power-down cycle prior to starting conversions. Take into account that the reference buffer recharges the bypass capacitor at an 80mV/ms slew rate, and add 50µs for settling time.

Auto-Shutdown

Selecting STBYPD on every conversion automatically shuts the MAX127/MAX128 down after each conversion without requiring any start-up time on the next conversion.

Transfer Function

Output data coding for the MAX127/MAX128 is binary in unipolar mode with 1 LSB = (FS/4096) and two's complement binary in bipolar mode with 1 LSB = [(2 x |FS|)/4096]. Code transitions occur halfway between successive-integer LSB values. Figures 13a and 13b show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively. For full-scale (FS) values, refer to Table 3.

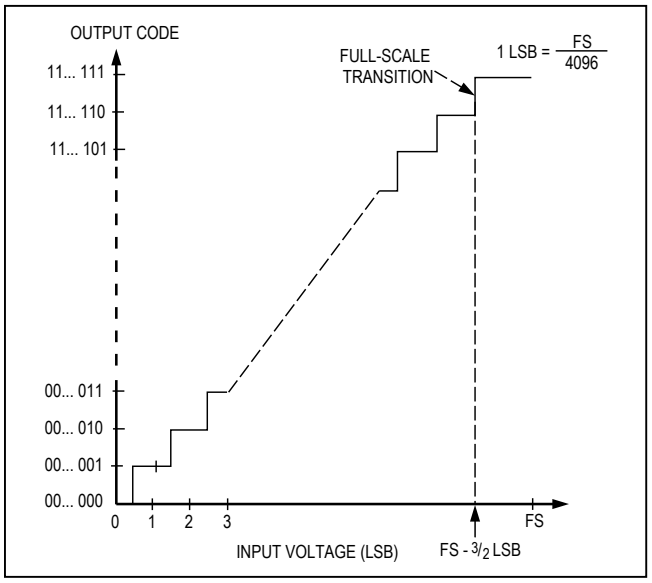


Figure 13a. Unipolar Transfer Function

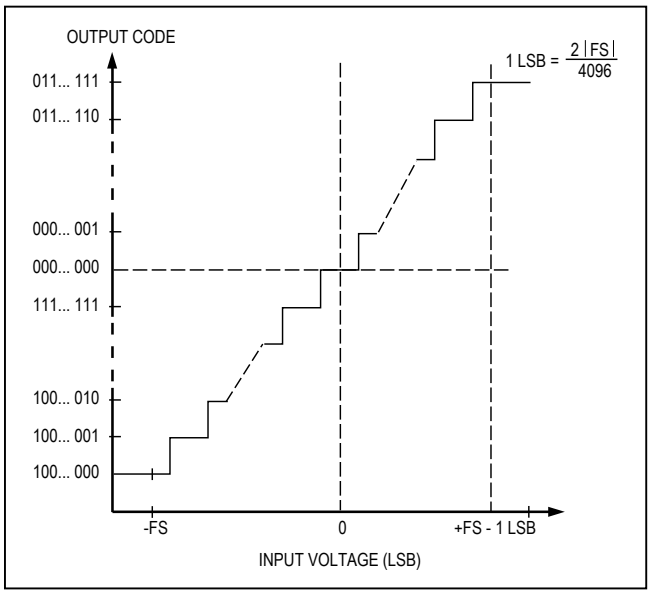


Figure 13b. Bipolar Transfer Function

Layout, Grounding, and Bypassing

Careful PCB layout is essential for best system performance. For best performance, use a ground plane. To reduce crosstalk and noise injection, keep analog and digital signals separate. Connect analog grounds and DGND in a star configuration to AGND. For noise-free operation, ensure the ground return from AGND to the supply ground is low impedance and as short as possible. Connect the logic grounds directly to the supply ground. Bypass V_{DD} with 0.1µF and 4.7µF capacitors to AGND to minimize highand low-frequency fluctuations. If the supply is excessively noisy, connect a 5Ω resistor between the supply and V_{DD}, as shown in Figure 14.

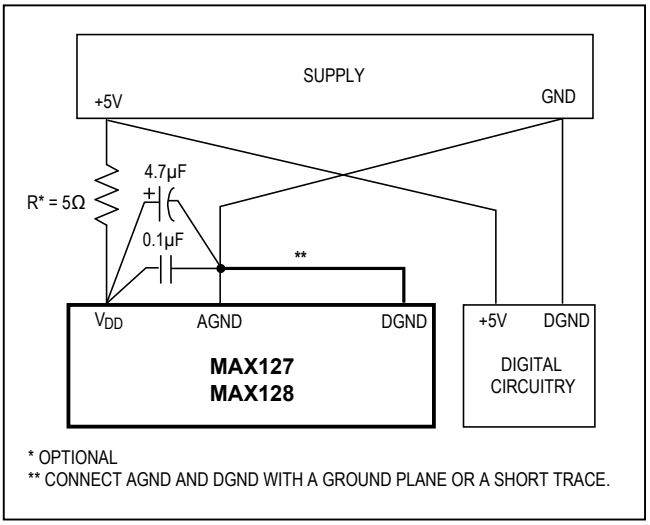


Figure 14. Power-Supply Grounding Connection

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX127ACAI+	0°C to +70°C	28 SSOP	±1/2
MAX127BCAI+	0°C to +70°C	28 SSOP	±1
MAX127AENG+	-40°C to +85°C	24 Narrow PDIP	±1/2
MAX127BENG+	-40°C to +85°C	24 Narrow PDIP	±1
MAX127AEAI+	-40°C to +85°C	28 SSOP	±1/2
MAX127BEAI+	-40°C to +85°C	28 SSOP	±1
MAX128BCNG+	0°C to +70°C	24 Narrow PDIP	±1
MAX128BCAI+	0°C to +70°C	28 SSOP	±1
MAX128BENG+	-40°C to +85°C	24 Narrow PDIP	±1
MAX128BEAI+	-40°C to +85°C	28 SSOP	±1

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

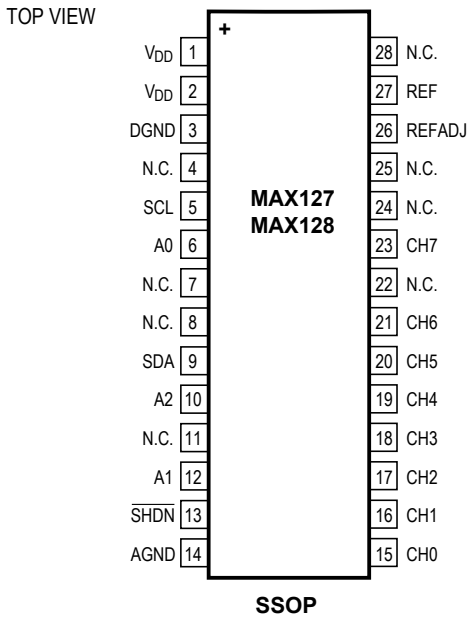
PROCESS: BiCMOS

Package Information

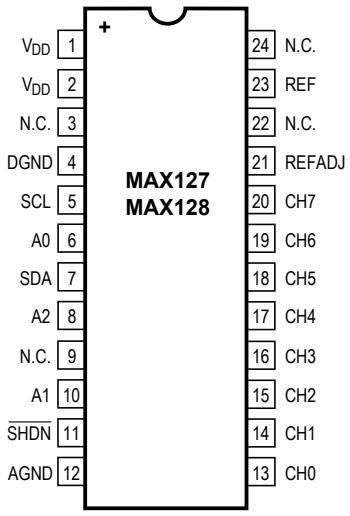
For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 PDIP	N24+8	21-0043	—
28 SSOP	A28+3	21-0056	90-0095

Pin Configurations



SSOP



NARROW PDIP

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