MAX13335E/MAX13336E

Dual Automotive Differential Audio Receivers with I²C Control and Diagnostics

General Description

The MAX13335E/MAX13336E are high-fidelity stereo audio input amplifiers designed for automotive applications requiring audio-level detection and/or jack sensing capability.

The devices feature a dual-channel, low-noise, programmable gain amplifier that accepts fully differential and quasi-differential input signals with diagnostics capability controlled through an I²C interface. The devices' audio receiver can also pair with the MAX13325/MAX13326 audio transmitter to form a complete differential audio link in automotive systems.

Each channel of the device features high common-mode rejection ratio (CMRR) (80dB), enabling the recovery of audio signals in the presence of large common-mode noise in automotive environments. An integrated programmable gain amplifier is adjustable from -14dB to +16dB (MAX13335E) and -22dB to +8dB (MAX13336E) with zero-crossing detection to provide an optimum output-signal level and limit zip noise. The external flexible diagnostic inputs can be configured to perform jack sense functions or to detect short-to-battery, short-to-ground, open load, and shorts between channels.

The audio inputs are protected against ISO 10605 ±15kV Air Gap and ±8kV Contact Discharge ESD pulses. Both devices have a -40°C to +105°C operating temperature range, and are available in a 16-pin QSOP package.

Benefits and Features

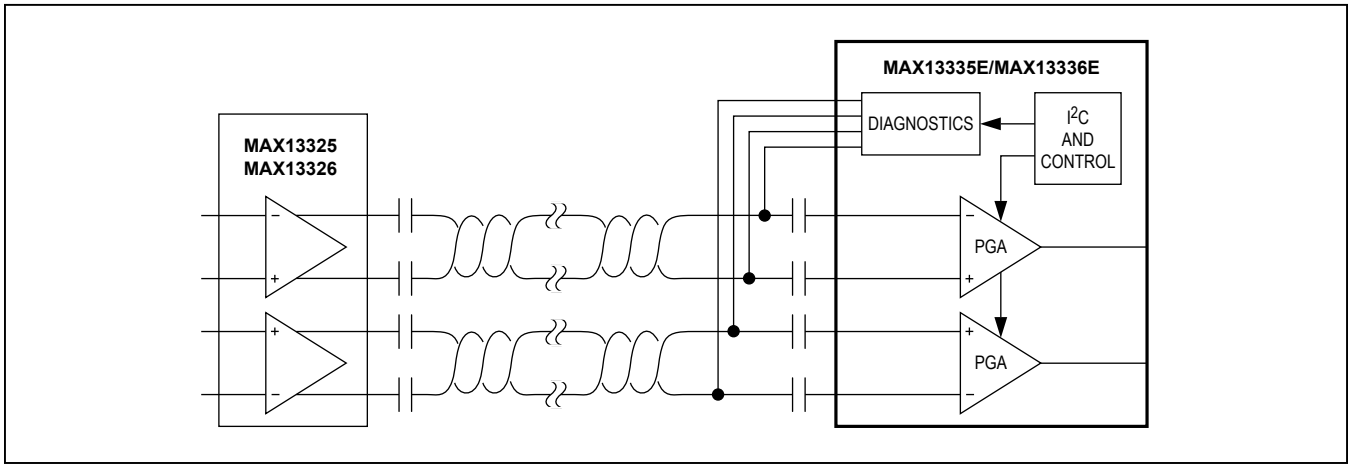
- +3.3V or +5V Operation
- +28V to -16V Tolerant Inputs
- Wide Common-Mode Input Range (-5V to +11.5V)
- Fully Differential Inputs Up to $7V_{RMS}$
- Quasi-Differential Inputs Up to $3.5V_{RMS}$
- Audio Presence Detection
- Jack Sense Detection
- Diagnostic Capability
- Programmable Gain with Zero-Crossing Detection
- I²C Control Interface
- Automotive Grade ESD Protection
  - ISO 10605 ±15kV Air Gap
  - ±8kV Contact Discharge

Applications

- Radio Head Units
- RSA/RSE
- Connectivity Modules
- Automotive Telematics

Ordering Information ***appears at end of data sheet.***

Typical Application Circuits



Typical Application Circuits ***continued at end of data sheet.***

maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND.....-0.3V to +6V
D_ to GND.....-16V to +28V
INL_, INR_ to GND.....-10V to +15V
OUTR, OUTL to GND..... -0.3V to (V_{DD} + 0.3V)
SDA, SCL, $\overline{INT}$ to GND.....-0.3V to +6V
REF to GND..... -0.3V to (V_{DD} + 0.3V)
Output Short-Circuit Duration.....Continuous

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 9.6 mW/°C above +70°C).....771.5 mW
Operating Junction Temperature Range..... -40°C to +150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

QSOP
Junction-to-Ambient Thermal Resistance(θ_{JA}).....103.7°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 5V, A_V = -6dB, R_L = 10kΩ, f = 20Hz to 20kHz, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = 25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply-Voltage Range	V_{DD}	V_{REF} = 1.68V	-5%	3.3	+5%	V
		V_{REF} = 2.5V	-5%	5.0	+5%	
Quiescent Supply Current	I_{DD}	$V_{INL_}$ = $V_{INR_}$ = V_{DD}/2		11		mA
Shutdown Supply Current	I_{SHDN}	SHDN bit = 1		6	10	µA
REF Output Voltage	V_{REF}	V_{DD} = 3.3V	-4%	1.68	+4%	V
		V_{DD} = 5V	-3%	2.5	+3%	
Thermal Shutdown	T_{SHDN}	(Note 3)		+150		°C
Thermal Shutdown Hysteresis	T_{HYS}	(Note 3)		15		°C

Electrical Characteristics (continued)

(V_{DD} = 5V, A_V = -6dB, R_L = 10kΩ, f = 20Hz to 20kHz, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = 25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AMPLIFIERS							
Programmable Gain Amp	A_V	G_[3:0] = 0000	MAX13335E		-14		dB
		G_[3:0] = 0001			-12		
		G_[3:0] = 0010			-10		
		G_[3:0] = 0011			-8		
		G_[3:0] = 0100			-6		
		G_[3:0] = 0101			-4		
		G_[3:0] = 0110			-2		
		G_[3:0] =0111			0		
		G_[3:0] =1000			2		
		G_[3:0] =1001			4		
		G_[3:0] =1010			6		
		G_[3:0] =1011			8		
		G_[3:0] =1100			10		
		G_[3:0] =1101			12		
		G_[3:0] =1110			14		
		G_[3:0] =1111			16		
		G_[3:0] = 0000	MAX13336E		-22		
		G_[3:0] = 0001			-20		
		G_[3:0] = 0010			-18		
		G_[3:0] = 0011			-16		
		G_[3:0] = 0100			-14		
		G_[3:0] = 0101			-12		
		G_[3:0] = 0110			-10		
		G_[3:0] =0111			-8		
		G_[3:0] =1000			-6		
		G_[3:0] =1001			-4		
		G_[3:0] =1010			-2		
		G_[3:0] =1011			0		
		G_[3:0] =1100			2		
		G_[3:0] =1101			4		
		G_[3:0] =1110			6		
		G_[3:0] =1111			8		
Gain Error	A_{ERR}	Within V_{CM} operating range			±0.4		dB
Gain Matching	A_{MCH}	Within V_{CM} operating range			±0.4		dB

Electrical Characteristics (continued)

(V_{DD} = 5V, A_V = -6dB, R_L = 10kΩ, f = 20Hz to 20kHz, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = 25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IOS}	A_V = 0dB		-10		+10	mV
Input Impedance	R_{IN}	Differential	MAX13335E	13.5	22	33	kΩ
			MAX13336E	19	30	42	
		Single-ended	MAX13335E	8.5	14	21	
			MAX13336E	11	17	24	
Common-Mode Rejection Ratio	A_{CMRR}	Within V_{CM} range, f = DC, A_V = -2dB (Note 4)	MAX13335E	60	80		dB
		V_{CM} = $2V_{RMS}$, f = 20Hz to 20kHz (Note 3)		60			
		Within V_{CM} range, f = DC, A_V = -10dB (Note 4)	MAX13336E	65	85		
		V_{CM} = $2V_{RMS}$, f = 20Hz to 20kHz (Note 3)		65			
Power-Supply Rejection Ratio	A_{PSRR}	f = 1kHz, V_{RIPPLE} = 200mV_{P-P} (Note 3)		-80			dB
Input Voltage Range	V_{IN}	Quasi-differential source, V_{DD} = 3.3V	MAX13335E			1.3	V_{RMS}
		Quasi-differential source, V_{DD} = 5V				2	
		Differential source, V_{DD} = 3.3V				2.6	
		Differential source, V_{DD} = 5V				4.0	
		Quasi-differential source, V_{DD} = 3.3V	MAX13336E			2.3	
		Quasi-differential source, V_{DD} = 5V				3.5	
		Differential source, V_{DD} = 3.3V				4.6	
		Differential source, V_{DD} = 5V				7.0	
Input Common-Mode Voltage Range	V_{CM}	V_{DD} = 3.3V	MAX13335E	-1.2		4.6	V
		V_{DD} = 5V		-1.8		7.0	
		V_{DD} = 3.3V	MAX13336E	-3.3		7.6	
		V_{DD} = 5V		-5.0		11.5	

Electrical Characteristics (continued)

(V_{DD} = 5V, A_V = -6dB, R_L = 10kΩ, f = 20Hz to 20kHz, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = 25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Range	V_{OUT}	R_L = 10kΩ		0.1		V_{DD} - 0.1	V
Total Harmonic Distortion Plus Noise	THD+N	f = 1kHz, $V_{OUT_}$ = 1.4V_{RMS} (Note 3)			0.01		%
Signal-to-Noise Ratio	SNR	$V_{OUT_}$ = 1.4V_{RMS} (Note 3)	MAX13335E		104.8		dB
			MAX13336E		99.4		
Output Noise	V_N	A_V = 0dB, unweighted (Note 3)	MAX13335E		8		μV_{RMS}
			MAX13336E		15		
Slew Rate	SR	C_L = 300pF (Note 3)		0.5			V/µs
Maximum Capacitive Load	C_L	No sustained oscillation (Note 3)			300		pF
Crosstalk	A_{XTALK}	V_{IN} = 2V_{RMS} (Note 3)			-80		dB
Mute Attenuation	A_{MUTE}	MUTE bit = 1, V_{IN} = 2V_{RMS} (Note 3)			-80		dB
Shutdown Attenuation	A_{SHDN}	SHDN bit = 1, V_{IN} = 2V_{RMS} (Note 3)			-80		dB
LEVEL SENSE/CLIP DETECTION							
Audio Presence Threshold	V_{TAP}	Output referred		127	200	268	mV_{RMS}
Clip-Level Warning	V_{TCP}	Positive clip warning level			90		% V_{DD}
	V_{TCN}	Negative clip warning level			10		
DIAGNOSTIC I/O							
Pullup Current Limit	I_{IDH}	$V_{D_}$ = 1.5V, CTRL0.DGAIN = 0	D_[3:0]=0001		40		µA
			D_[3:0]=0010		97		
			D_[3:0]=0011		154		
			D_[3:0]=0100		210		
			D_[3:0]=0101		265		
			D_[3:0]=0110		320		
			D_[3:0]=0111		375		
			D_[3:0]=1000		430		
			D_[3:0]=1001		485		
			D_[3:0]=1010		540		
			D_[3:0]=1011		595		
			D_[3:0]=1100		650		
			D_[3:0]=1101		705		
Pulldown Current	I_{IDL}	D_[3:0] = 1110, $V_{D_}$ < V_{CM}			32	65	µA
Trip High Threshold	V_{IDH}	$R_{D_}$ = 1kΩ to 10kΩ			1.94		V
Trip Low Threshold	V_{IDL}	$R_{D_}$ = 1kΩ to 10kΩ			0.92		V
Switch Diode	V_{DON}	D_[3:0] = 1111			0.7		V
Input Resistance	R_{DOFF}	Off-state D_[3:0] = 0000, $V_{D_}$ < V_{CM}		1			MΩ
Leakage Current	I_{DLKG}	Off-state D_[3:0] = 0000, $V_{D_}$ < V_{CM}			±10		µA

Electrical Characteristics (continued)

(V_{DD} = 5V, A_V = -6dB, R_L = 10kΩ, f = 20Hz to 20kHz, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = 25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION						
ISO 10605 Air Gap	V_{ESD}	2kΩ/150pF, INL_, INR_		±15		kV
Contact Discharge	V_{ESD}	330Ω/330pF, INL_, INR_		±8		kV
DIGITAL INTERFACE						
Input Voltage High	V_{INH}	SDA, SCL	0.7 x V_{DD}			V
Input Voltage Low	V_{INL}	SDA, SCL			0.3 x V_{DD}	V
Input Voltage Hysteresis	V_{HYS}	SDA, SCL		0.14 x V_{DD}		mV
I/O Leakage Current	I_{LKG}	SDA, SCL, $\overline{INT}$		±10		µA
Output Low Voltage	V_{OL}	SDA, $\overline{INT}$, I_{SINK} = 3mA			0.4	V
EN to Full Operation Time	t_{SON}	C_{REF} = 2.2µF (Note 3)		100		ms
I²C TIMING						
Output Fall Time	t_{OF}	C_{BUS} = 10pF to 400pF			250	ns
Pin Capacitance	C_{IN}				10	pF
Clock Frequency	f_{SCL}				400	kHz
SCL Low Time	t_{LOW}		1.3			µs
SCL High Time	t_{HIGH}		0.6			µs
START Condition Hold Time	$t_{HD:STA}$	Repeated START condition	0.6			µs
START Condition Setup Time	$t_{SU:STA}$	Repeated START condition	0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		900	ns
Data Setup Time	$t_{SU:DAT}$		100			ns
Input Rise Time	t_R	SCL, SDA			300	ns
Input Fall Time	t_F	SCL, SDA			300	ns
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Bus Free Time	t_{BUF}	Between START and STOP conditions	1.3			µs
Maximum Bus Capacitance	C_{BUS}	Per bus line			400	pF

Note 2: Specifications within minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

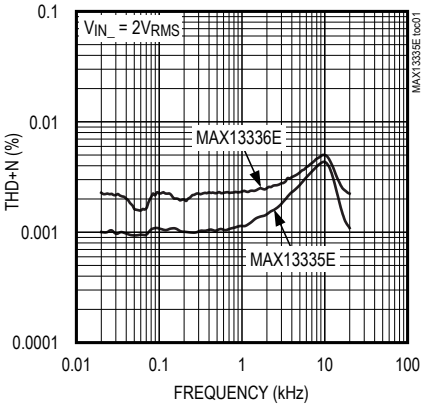
Note 3: Guaranteed by bench characterization.

Note 4: $A_{CMRR} = 20\log(\Delta V_{IOS}/\Delta V_{CM})$.

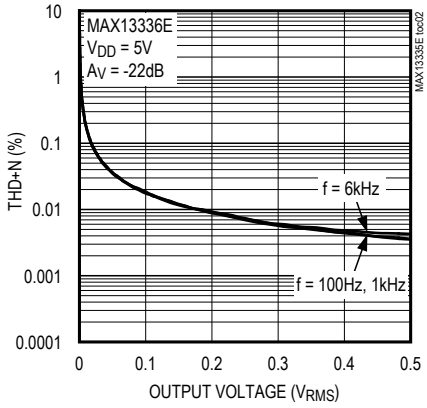
Typical Operating Characteristics

(V_{DD} = 5V, A_V = -6dB, R_L = 10kΩ, BW = 20Hz to 20kHz, T_A = +25°C, unless otherwise noted.)

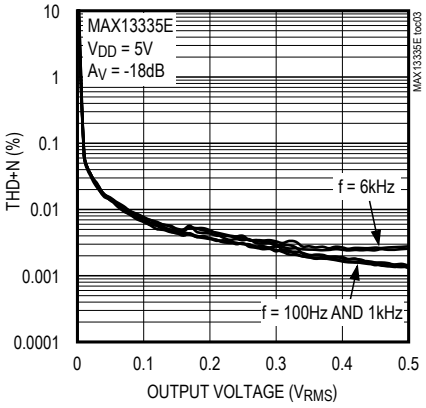
THD+N vs. FREQUENCY



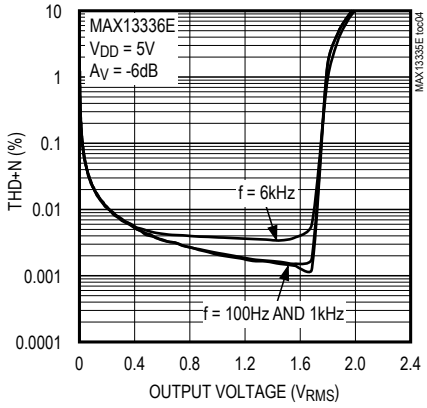
THD+N vs. OUTPUT VOLTAGE



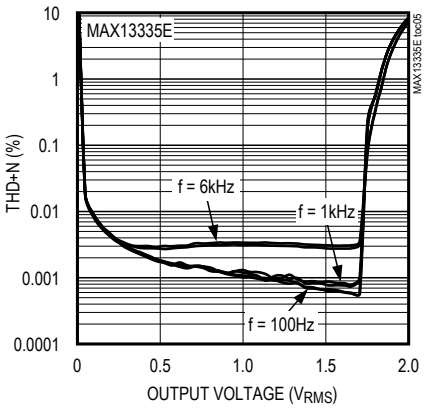
THD+N vs. OUTPUT VOLTAGE



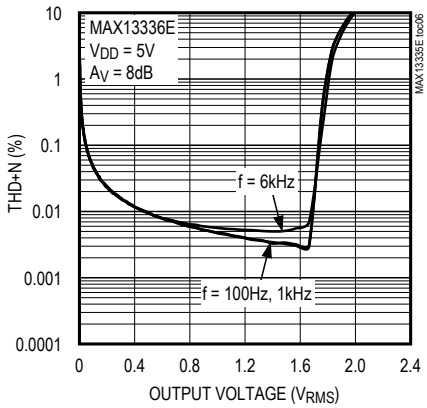
THD+N vs. OUTPUT VOLTAGE



THD+N vs. OUTPUT VOLTAGE



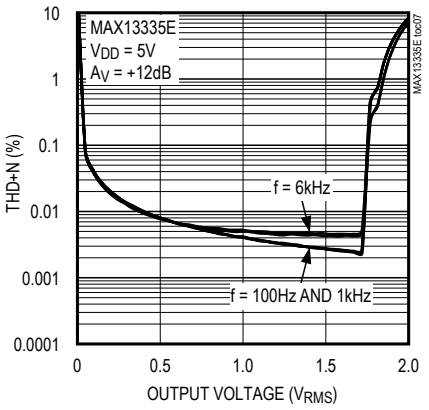
THD+N vs. OUTPUT VOLTAGE



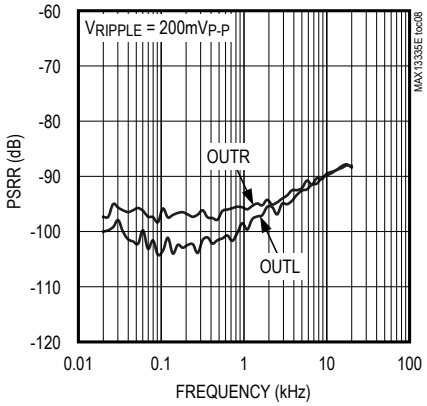
Typical Operating Characteristics (continued)

(V_{DD} = 5V, A_V = -6dB, R_L = 10kΩ, BW = 20Hz to 20kHz, T_A = +25°C, unless otherwise noted.)

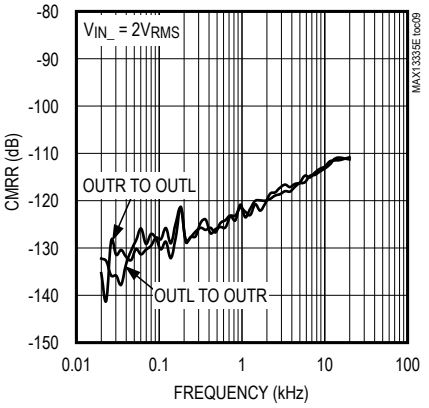
THD+N vs. OUTPUT VOLTAGE



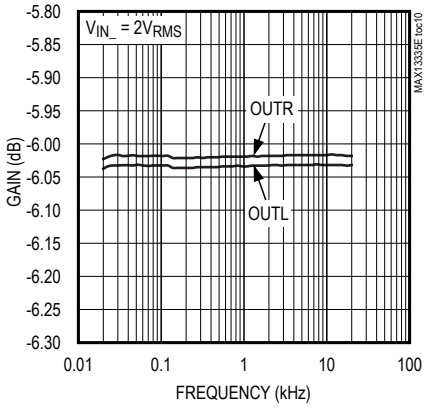
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



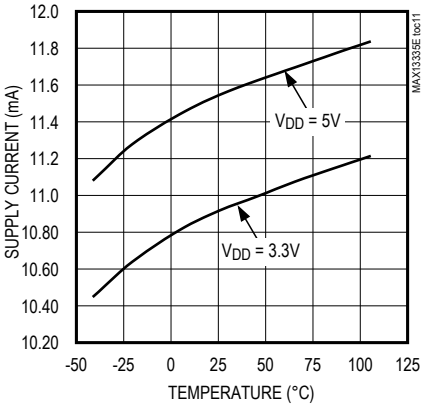
CROSSTALK vs. FREQUENCY



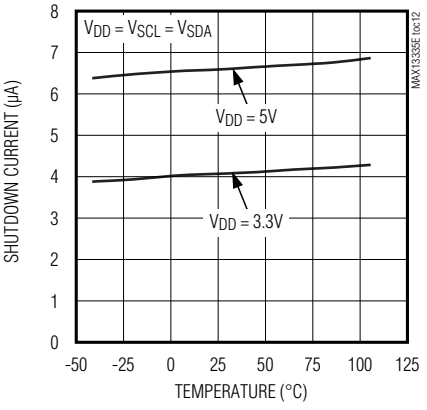
GAIN MATCHING vs. FREQUENCY



SUPPLY CURRENT vs. TEMPERATURE



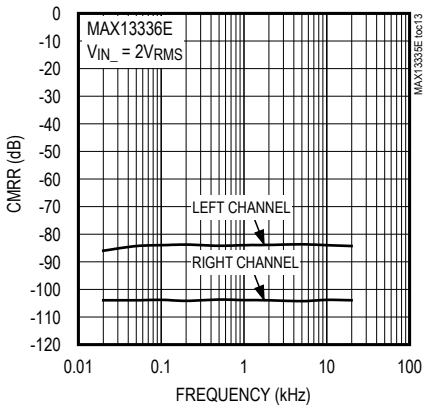
SHUTDOWN CURRENT vs. TEMPERATURE



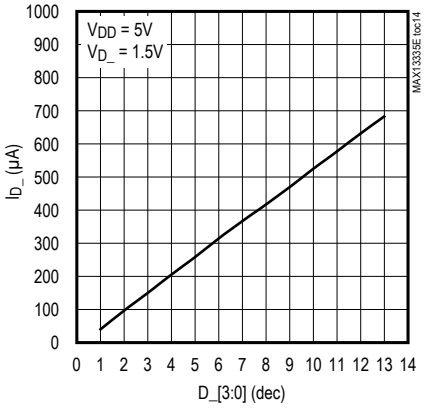
Typical Operating Characteristics (continued)

(V_{DD} = 5V, A_V = -6dB, R_L = 10kΩ, BW = 20Hz to 20kHz, T_A = +25°C, unless otherwise noted.)

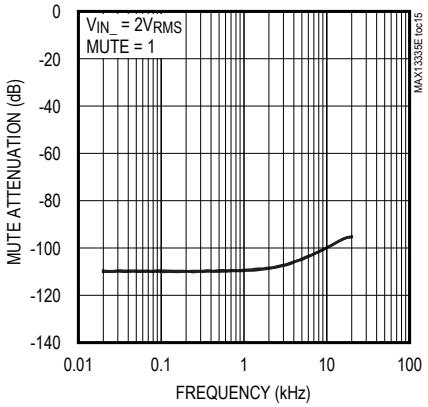
COMMON-MODE REJECTION RATIO vs. FREQUENCY



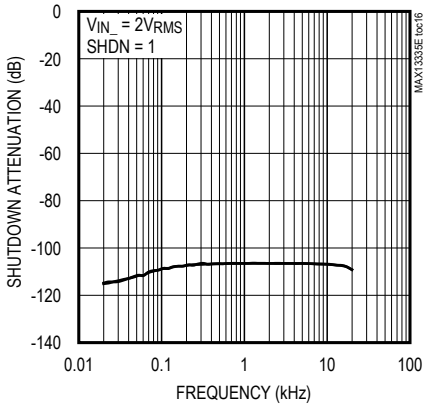
DIAGNOSTIC CURRENT SOURCE vs. D_[3:0]



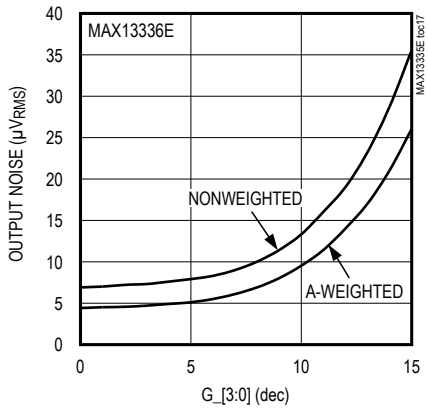
MUTE ATTENUATION vs. FREQUENCY



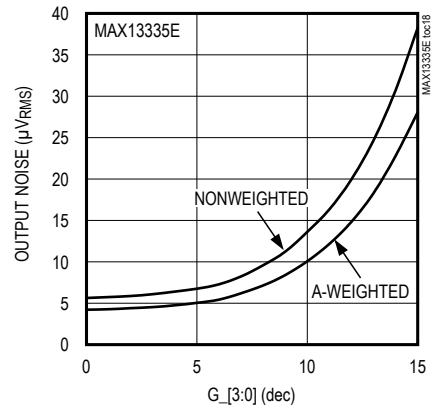
SHUTDOWN ATTENUATION vs. FREQUENCY



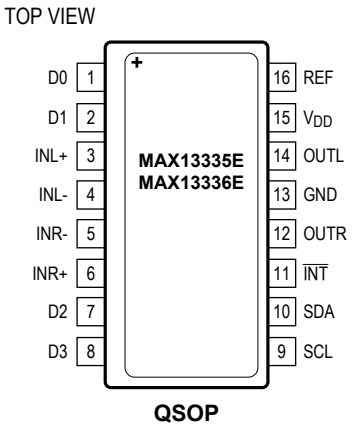
OUTPUT NOISE vs. GAIN SETTING



OUTPUT NOISE vs. GAIN SETTING



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	D0	Diagnostic I/O 0. I/O pin used for jack sense and diagnostics.
2	D1	Diagnostic I/O 1. I/O pin used for jack sense and diagnostics.
3	INL+	Noninverting Left-Channel Audio Input
4	INL-	Inverting Left-Channel Audio Input
5	INR-	Inverting Right-Channel Audio Input
6	INR+	Noninverting Right-Channel Audio Input
7	D2	Diagnostic I/O 2. I/O pin used for diagnostics.
8	D3	Diagnostic I/O 3. I/O pin used for diagnostics.
9	SCL	I²C Serial-Clock Input
10	SDA	I²C Serial-Data Input and Output
11	$\overline{INT}$	Active-Low, Open-Drain Interrupt Request Output
12	OUTR	Right-Channel Audio Output
13	GND	Ground
14	OUTL	Left-Channel Audio Output
15	V_{DD}	Supply Input
16	REF	$V_{DD}/2$ Reference Output. Bypass REF to GND with a 2.2µF capacitor.

Detailed Description

The MAX13335E/MAX13336E are designed to operate with the MAX13325/MAX13326 dual automotive audio line drivers to form a complete differential audio link in automotive systems. In addition, the MAX13335E/MAX13336E can operate as an auxiliary input audio amplifier with jack sense function.

Signal Path

The devices can be configured to operate with quasi-differential (up to $3.5V_{RMS}$) and fully differential (up to $7V_{RMS}$) input signals. Both input channels feature high 80dB CMRR (typ). An integrated programmable gain amplifier with zero-crossing detection controlled through the I²C interface provides adjustable gain from -14dB to +16dB (MAX13335E) or -22dB to +8dB (MAX13336E) in +2dB increments. Zero-crossing detection can be enabled to limit the zip noise during a gain transition by delaying the gain change until a zero-crossing event occurs on the input signal.

Interrupt Output

The devices can monitor the inputs for the presence of audio, clip detection, and change-of-state in the jack sense. An active-low, open-drain interrupt request output can be configured through the I²C interface to report the presence of audio, clip detection, and change-of-state in the jack sense. The internal status register also latches the status change of those parameters until an I²C read is performed.

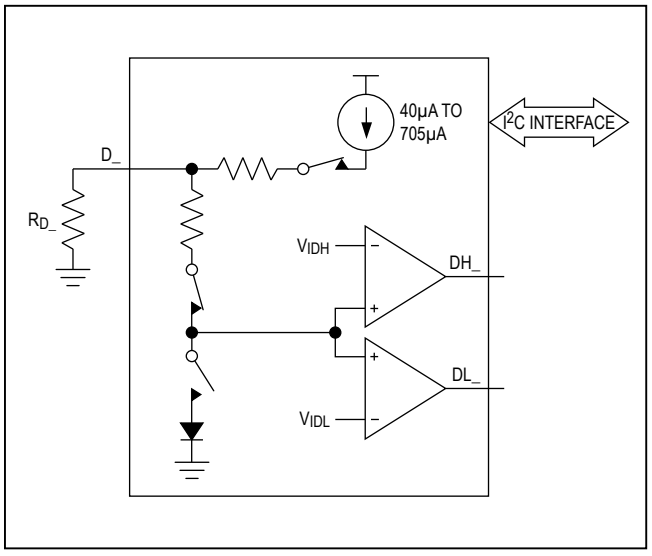


Figure 1. Diagnostic I/O Port

Thermal Shutdown

Thermal shutdown protects the device when the junction temperature exceeds +150°C (typ). The device resumes operation when the junction temperature drops below the thermal shutdown hysteresis of 15°C (typ). The internal status register latches the status change of the TSD bit until an I²C read is performed.

Diagnostics

The devices feature four similar diagnostic I/O ports. When configured correctly, they are capable of performing jack sense detection, short-to-ground, short-to-battery, open-load, and shorts between channels. Each diagnostic I/O port contains a programmable current source, a voltage sense, and a diode to ground.

The principle behind the diagnosis is simply forcing a current into the load attached to the I/O port and sensing the voltage to check if it is greater or smaller than the two predefined low/high thresholds. These can be easily accessed by a microcontroller through the I²C interface.

The procedure usually starts with stepping up the current source from the minimum to maximum range.

1) If the sensed voltage is consistently below the low threshold, a short-to-ground event is determined.
2) However, if the sensed voltage is consistently above the high threshold, there is a possibility of either a short-to-battery or an open-load event. In order to differentiate between them, the I/O port should be tested again with a voltage-sense-only configuration (i.e., with the current source switched off). If the sensed voltage remains above the high threshold, a short-to-battery event has occurred. Otherwise, an open-load event is detected.
3) In some current source range, if the sensed voltage is between the high and low thresholds, this could indicate that the load is present.

A valid readout of the status might require some amount of delays (to be inserted by the microcontroller) due to the settling time needed to charge/discharge any external capacitive load on the I/O port.

The diode is useful in the case of sensing an unconnected load or short between channels. Here, one end of the load can be forced to ground by the diode and the usual procedure described above can be applied to detect various events. It is, however, advisable to test the I/O port for a short-to-battery condition prior to turning on the diode as it could risk damaging the device.

See the *Applications Information* section for various examples on how the diagnostic can be set up to detect different events.

Applications Information

Serial Interface

Writing to the device using I²C requires that first the master send a START condition (S) followed by the device's I²C address. After the address, the master sends the address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a repeated START condition (Sr) to communicate to another I²C slave (Figure 2).

Bit Transfer

Each SCL rising edge transfers one data bit. The data on SDA must remain stable during the high portion of the SCL clock pulse (Figure 3). Changes in SDA while SCL is high are read as control signals (see the *START and STOP Conditions* section). When the serial interface is inactive, SDA and SCL idle high.

START and STOP Conditions

A master device initiates communication by issuing a START condition (S) which is a high-to-low transition on SDA with SCL high. A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission by a STOP condition (P) (see the *Acknowledge Bit* section). A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). The STOP condition frees the bus. If a repeated START condition (S_r) is generated instead of a STOP condition, the bus remains active. When a STOP condition or incorrect slave ID is detected, the device internally disconnects SCL from the serial interface until the next START or repeated START condition, minimizing digital noise and feedthrough.

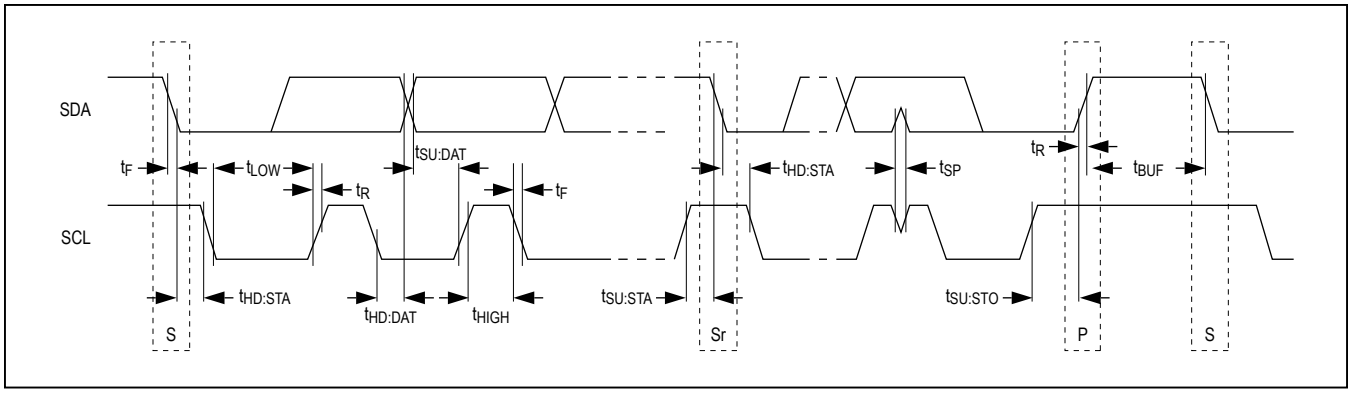


Figure 2. I²C Timing

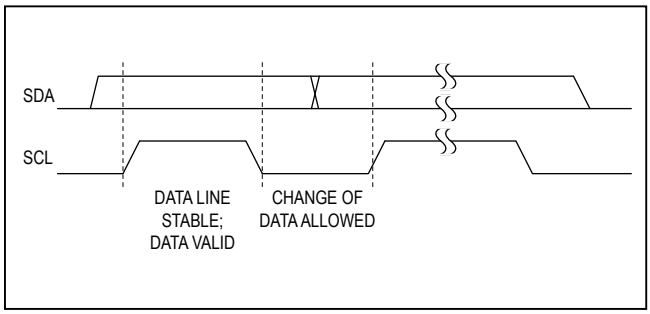


Figure 3. Bit Transfer

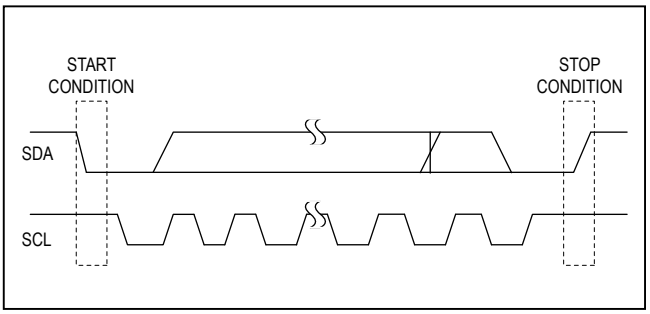


Figure 4. START/STOP Conditions

Acknowledge Bit

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake the receipt of each byte of data when in write mode. The device pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received (Figure 5). Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master could retry communication. The master must pull down SDA during the 9th clock cycle to acknowledge receipt of data when the device is in read mode. An acknowledge must be sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the device, followed by a STOP condition.

Slave Address

The device is programmable to one of the four I²C slave addresses (Table 2). The power-on default I²C slave address of the device for read/write is 0xD0/0xD1 (1101000R/$\overline{W}$). The I²C slave address of the device can be selected by writing to Control Register 1 (0x03) while $\overline{INT}$ is pulled low externally during the I²C write duration (Figure 6).

Single Byte-Write Operation

For a single byte-write operation, send the slave address as the first byte followed by the register address and then a single data byte (Figure 7).

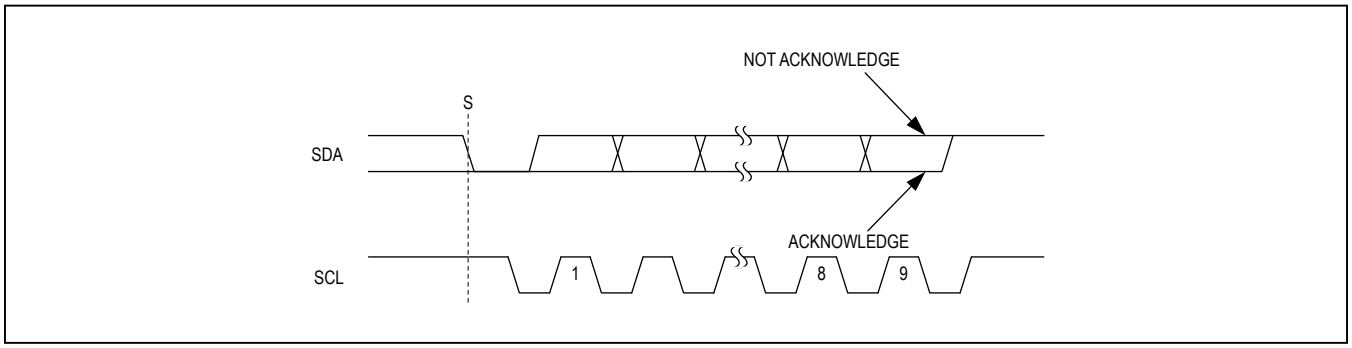


Figure 5. Acknowledge and Not-Acknowledge Bits

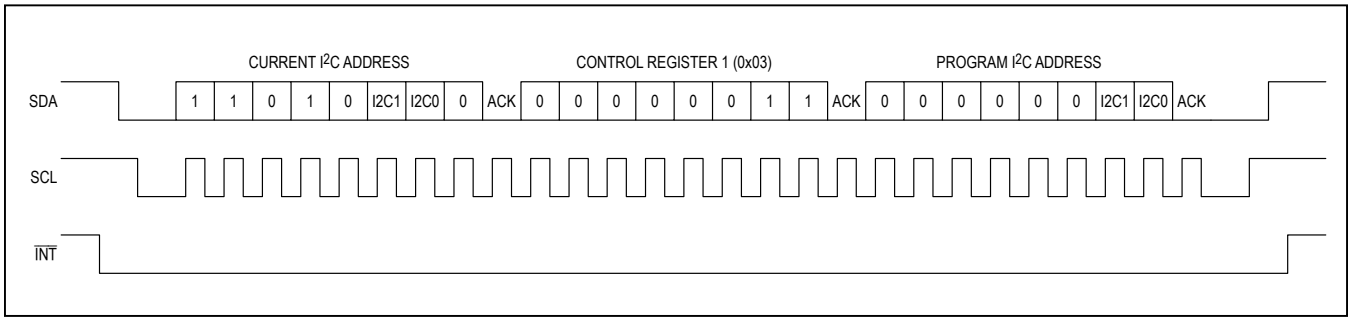


Figure 6. I²C Slave Address Programming

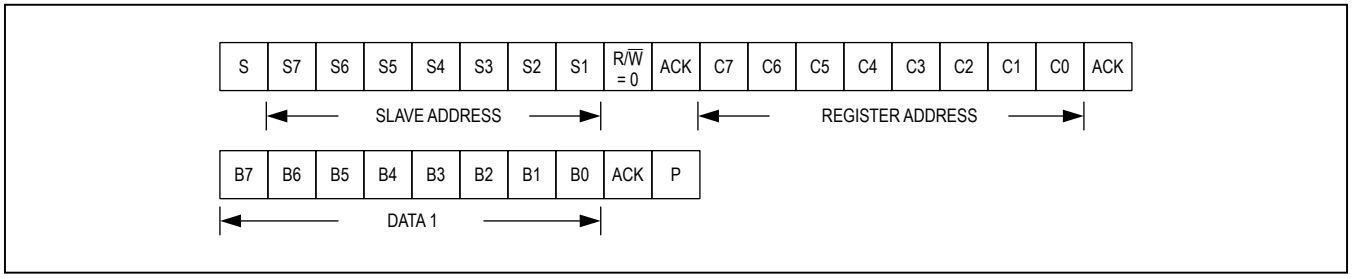


Figure 7. A Single Byte-Write Operation

Burst-Write Operation

For a burst-write operation, send the slave address as the first byte followed by the register address and then the data bytes (Figure 8).

Single Byte-Read Operation

For a single byte-read operation, send the slave address with a write as the first byte followed by the register address. Then send a repeated START condition followed by the slave address with the read bit set. After the slave sends the data byte, send a not-acknowledge followed by a STOP condition (Figure 9).

Burst-Read Operation

For a burst-read operation, send the slave address with a write as the first byte followed by the register address. Then send a repeated START condition followed by the slave address with the read bit set. The slave sends data bytes until a not-acknowledge condition is sent (Figure 10).

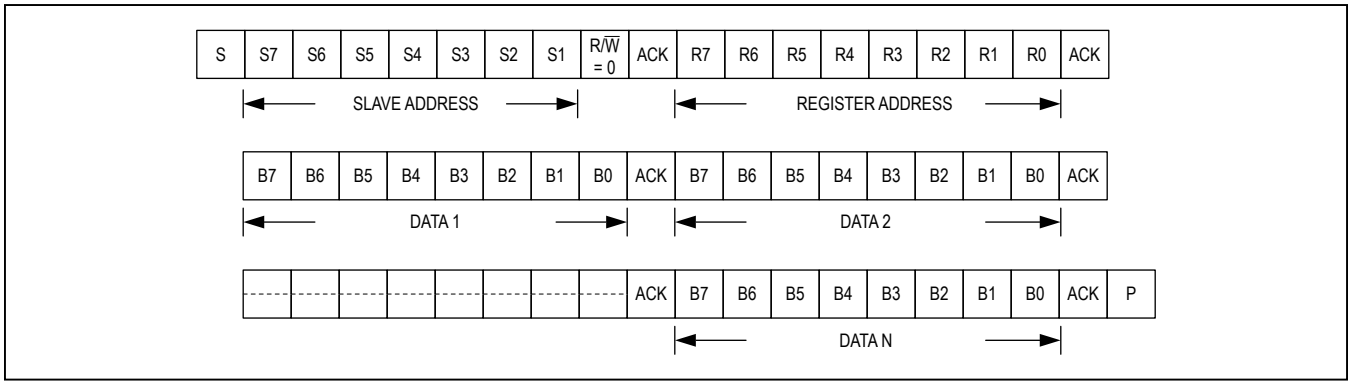


Figure 8. A Burst-Write Operation

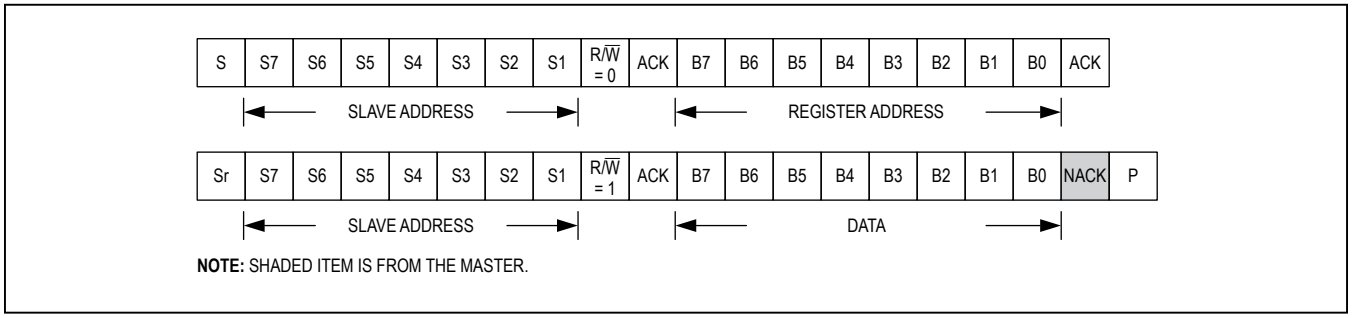


Figure 9. A Single Byte-Read Operation

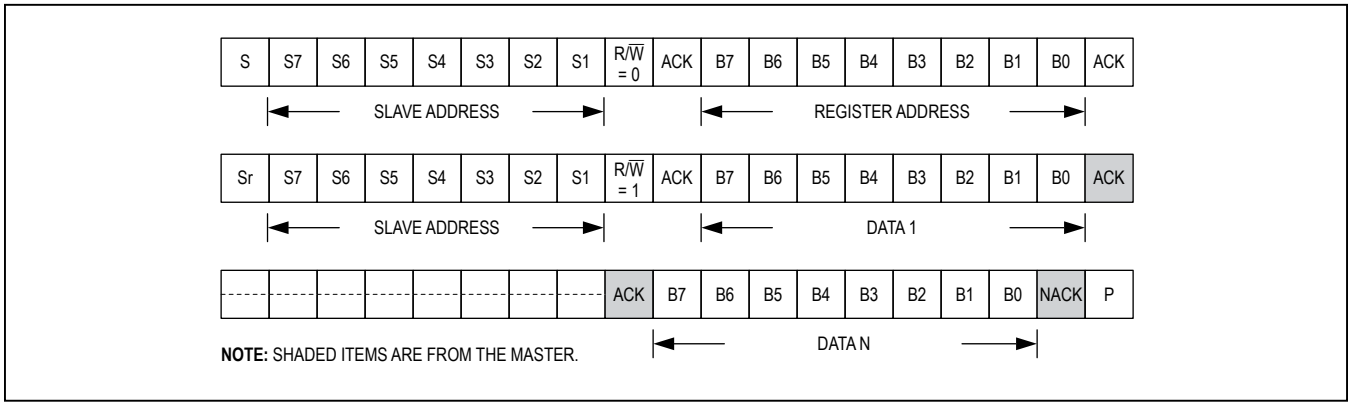


Figure 10. A Burst-Read Operation

Register Map

NAME	REG	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W	POR SETTINGS
STAT0	00	DH3	DL3	DH2	DL2	DH1	DL1	DH0	DL0	R	0x00
STAT1	01	APD	CLD	JSD	TSD	—	ID2	ID1	ID0	R	0x00
CTRL0	02	API	CLI	JSI	—	—	ZEN	MUTE	SHDN	R/$\overline{W}$	0x00
CTRL1	03	—	—	—	—	—	—	I2C1	I2C0	R/$\overline{W}$	0x00
DIAG0	04	D1[3]	D1[2]	D1[1]	D1[0]	D0[3]	D0[2]	D0[1]	D0[0]	R/$\overline{W}$	0x00
DIAG1	05	D3[3]	D3[2]	D3[1]	D3[0]	D2[3]	D2[2]	D2[1]	D2[0]	R/$\overline{W}$	0x00
GAIN	06	GL3	GL2	GL1	GL0	GR3	GR2	GR1	GR0	R/$\overline{W}$	0x00

Status Register 0 (STAT0)

ADDRESS: 0x00 MODE: R								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	DH3	DL3	DH2	DL2	DH1	DL1	DH0	DL0
POR	0	0	0	0	0	0	0	0

The bits in Status Register 0 are updated to reflect the states of the upper (DH_) and lower (DL_) comparator's threshold when voltage sensing is enabled for the corresponding diagnostic I/O. Combinations of DH_ and DL_ can be used to decode the fault on the I/O port.

Bits 7, 5, 3, 1: DH_ (Diagnostic Upper Comparator Threshold V_{IDH})

0 = Below upper threshold

1 = Above upper threshold

Bits 6, 4, 2, 0: DL_ (Diagnostic Lower Comparator Threshold V_{IDL})

0 = Below lower threshold

1 = Above lower threshold

Table 1. Interpretation of Diagnostic Status Bits

DH_	DL_	CONDITION
0	0	Short-to-ground (or disabled)
0	1	No fault
1	0	Invalid (not used)
1	1	Short-to-battery if current source is disabled (i.e., D_[3:0] = 1110)
1	1	Open-load if current source is enabled (i.e., D_[3:0] = 0001 to 1101)

Status Register 1 (STAT1)

ADDRESS: 0x01 MODE: R								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	APD	CLD	JSD	TSD	—	ID2	ID1	ID0
POR	0	0	0	0	0	—	—	—

Bit 7: APD (Audio Presence Status Bit)

0 = Audio not present.

1 = Audio presence detected. $\overline{INT}$ asserts low.

Bit 6: CLD (Clip Detection Status Bit)

0 = No clipping detected.

1 = Clip warning. $\overline{INT}$ asserts low.

Bit 5: JSD (Jack Sense Status Bit)

0 = Jack removed. $\overline{INT}$ asserts low.

1 = Jack inserted. $\overline{INT}$ asserts low.

Note: $\overline{INT}$ asserts low whenever jack sense changes state.

Bit 4: TSD (Thermal Shutdown Status Bit)

0 = Within safe operating range.

1 = Overheating detected. $\overline{INT}$ pin asserts low.

Bit 3: No Function

Bit 2 to 0: ID_ (Die ID)

001 = MAX13335E

010 = MAX13336E

Note: Reading of Status Register 1 (REG = 0x01) releases $\overline{INT}$ and resets bits APD, CLD, JSD, and TSD back to zero.

Control Register 0 (CTRL0)

ADDRESS: 0x02 MODE: R/$\overline{W}$								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	API	CLI	JSI	—	DGAIN	ZEN	MUTE	SHDN
POR	0	0	0	0	0	0	0	0

Bit 7: API (Audio Presence Interrupt Enable Bit)

0 = Disable

1 = Enable*

*Bit automatically resets to 0 when an audio presence interrupt occurs.

Bit 6: CLI (Clip Warning Interrupt Enable Bit)

0 = Disable

1 = Enable*

*Bit automatically resets to 0 when a clip warning interrupt occurs.

Bit 5: JSI (Jack Sense Interrupt Enable Bit)

The JSI bit can be set only after D1[3:0] and D0[3:0] in the Diagnostic register 0 (DIAG0) has been programmed.

0 = Disable

1 = Enable*

*Bit automatically resets to 0 when a jack sense interrupt occurs.

Bits 4: No Function (0 should be written during write access.)

Bit 3: DGAIN (Diagnostic Pullup Current Gain Bit)

Gain adjustment used to set the diagnostic pullup current value on the D0–D3 pins.

0 = Nominal; pullup current values match typical values in the *Electrical Characteristics* table.

1 = 1.5x; Increases the diagnostic current by 1.5x the nominal values listed for the Pullup Current Limit parameter in the *Electrical Characteristics* table

Bit 2: ZEN (Zero-Crossing Enable Bit)

Enabling zero-crossing detection loads the new PGA gain settings at the zero-crossing signal to avoid zip noise.

0 = Disable

1 = Enable

Bit 1: MUTE (Mute Enable Bite)

0 = Play mode

1 = Mute mode

Bit 0 : SHDN (Shutdown Enable Bit)

0 = Normal mode

1 = Shutdown mode

Control Register 1 (CTRL1)

ADDRESS: 0x03 MODE: R/$\overline{W}$								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	—	—	—	—	—	—	I2C1	I2C0
POR	0	0	0	0	0	0	0	0

Table 2. I²C Address

A7	A6	A5	A4	A3	A2 (I2C1)	A1 (I2C0)	A0 (R/$\overline{W}$)	READ	WRITE
1	1	0	1	0	0	0	—	0xD1	0xD0
1	1	0	1	0	0	1	—	0xD3	0xD2
1	1	0	1	0	1	0	—	0xD5	0xD4
1	1	0	1	0	1	1	—	0xD7	0xD6

Bits 7 to 2: No Function (0 should be written during write access.)

Bits 1 and 0: I2C_

The I2C1 and I2C0 bits determine the I²C slave address of the device. The I²C slave address is changed by writing to CTRL1 while $\overline{INT}$ is pulled low (e.g., by an external microcontroller) for the duration of the I²C write cycle.

Diagnostic Register 0 (DIAG0)

ADDRESS: 0x04 MODE: R/$\overline{W}$								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	D1[3]	D1[2]	D1[1]	D1[0]	D0[3]	D0[2]	D0[1]	D0[0]
POR	0	0	0	0	0	0	0	0

Diagnostic Register 1 (DIAG1)

ADDRESS: 0x05 MODE: R/$\overline{W}$								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	D3[3]	D3[2]	D3[1]	D3[0]	D2[3]	D2[2]	D2[1]	D2[0]
POR	0	0	0	0	0	0	0	0

The Diagnostic registers, DIAG0 and DIAG1, program the state of the four diagnostic I/O ports D_. The diagnostic ports can be programmed to operate in one of the four states:

1) Setting D_[3:0] = 0000 disables the corresponding diagnostic I/O.
2) Setting D_[3:0] = 0001 to 1101 enables the internal current source (40µA to 705µA) and voltage sensing. The voltage sensing utilizes a window comparator with an upper threshold of 1.94V and a lower threshold of 0.92V (see the *Diagnostic Configurations* section).
3) Setting D_[3:0] = 1110 enables voltage sensing only.
4) Setting D_[3:0] = 1111 enables the internal diode to ground.

Table 3. Diagnostic I/O Port States

D_[3:0]	FUNCTION
0000	Diagnostic output disabled.
0001	Enables the 40µA current source and voltage sense.
0010	Enables the 97µA current source and voltage sense.
0011	Enables the 154µA current source and voltage sense.
0100	Enables the 210µA current source and voltage sense.
0101	Enables the 265µA current source and voltage sense.
0110	Enables the 320µA current source and voltage sense.
0111	Enables the 375µA current source and voltage sense.
1000	Enables the 430µA current source and voltage sense.
1001	Enables the 485µA current source and voltage sense.
1010	Enables the 540µA current source and voltage sense.
1011	Enables the 595µA current source and voltage sense.
1100	Enables the 650µA current source and voltage sense.
1101	Enables the 705µA current source and voltage sense.
1110	Enable voltage sense. The current source is disabled.
1111	Enables the diode. The current source and voltage sense are disabled.

Gain Register (GAIN)

ADDRESS: 0x06 MODE: R/$\overline{W}$								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	GL3	GL2	GL1	GL0	GR3	GR2	GR1	GR0
POR	0	0	0	0	0	0	0	0

Bits 7 to 0: G_

The Gain register sets the gain of the internal programmable gain amplifier (A_V) for the left (GL[3:0]) and right (GR[3:0]) channels. The gain of the programmable gain amplifier (A_V) is determined by the following transfer function:

$$Gain(A_V) = -14dB + (G_[3:0] \times 2)dB \text{ (for MAX13335E)}$$

$$Gain(A_V) = -22dB + (G_[3:0] \times 2)dB \text{ (for MAX13336E)}$$

Diagnostic Configurations

The device's diagnostics can be configured for local jack sense, remote jack sense, and differential drive connections (see the *Typical Application Circuits*). Diagnostic registers DIAG0 and DIAG1 configure the diagnostic I/O ports D_ as a current-source output with voltage sensing enabled, a voltage sensing input, or a diode to GND. When voltage sensing is enabled, the current states of the internal window comparator are updated to status register STAT0. A valid readout of the STAT0 register might require some amount of delays (to be inserted by the microcontroller) between configuring the diagnostic and reading the status register due to the settling time needed to charge/discharge the external capacitive load on the D_ pins.

Local Jack Sense

The device is configured for jack sense function when the jack is localized to the same module. In this application example, the diagnostic I/O D1 is configured as a 97µA current-source output and D0 is configured for voltage sensing. When a plug is not inserted, the internal spring contact of the jack shorts D1 to D0. The 97µA current source from D1 pulls D0 to V_{DD} resulting in DH0 = 1. When a plug is inserted, the internal spring contact of the jack is forced open and disconnects D1 from D0. This results in D0 going low and hence DH0 = 0.

Remote Jack Sense Detection

When the jack is remotely located, the device can be used for additional fault detection of the wiring harness used for the connection. See the *Typical Application Circuits*.

Differential Connection

For fully differential applications, the device can be configured to detect faults in the wiring harness as shown in the *Typical Application Circuits*.

Table 4. Local Jack Sense Diagnostic Configuration

CONFIGURATION	FUNCTION	COMPARATOR OUTPUT	STATUS
D1[3:0] = 0010 D0[3:0] = 1110	Source 97µA Source off	DH0 = H	Device not plugged in
D1[3:0] = 0010 D0[3:0] = 1110	Source 97µA Source off	DH0 = L	Device plugged in

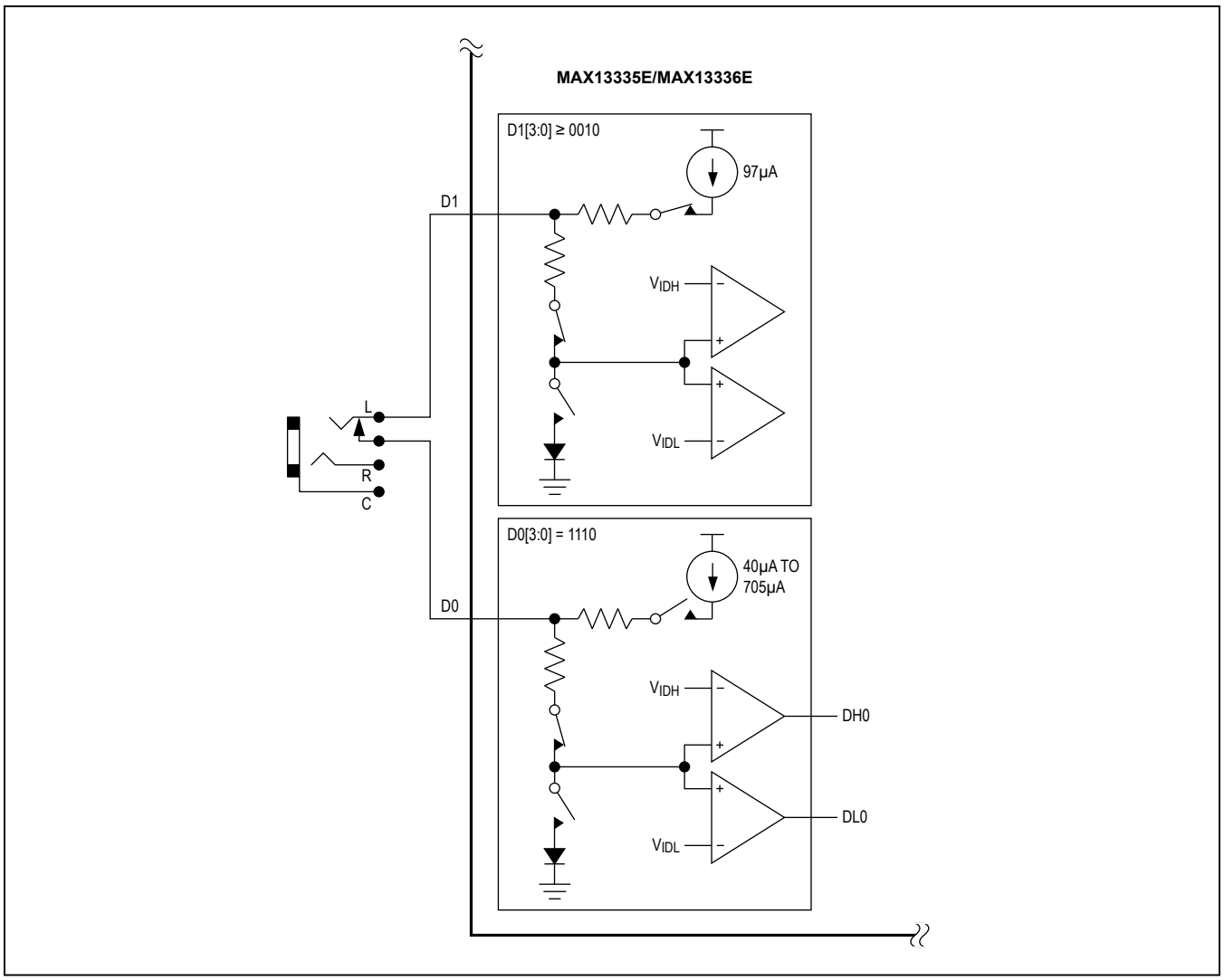


Figure 11. Diagnostic Setup for Local Jack Sense

Audio Presence Detection

When the device is used in an auxiliary input amplifier, it can detect if audio is present at the inputs so the downstream DSP does not have to continuously convert the analog signal to digital in order to monitor the audio stream. This can save two ADC inputs as the auxiliary input can be muxed with another audio stream that is mutually exclusive. To do this, perform the following steps:

1) Set the gain in the GAIN register based on the required input audio level where the APD threshold is exceeded. The threshold is set to $200mV_{RMS}/G_[3:0]$.
2) Set API bit in the CTRL0 register to enable the APD interrupt.

When the input audio level exceeds $200mV_{RMS}/G_[3:0]$ the $\overline{INT}$ pin is asserted. The microcontroller can read back the STAT0 register to check for APD = 1.

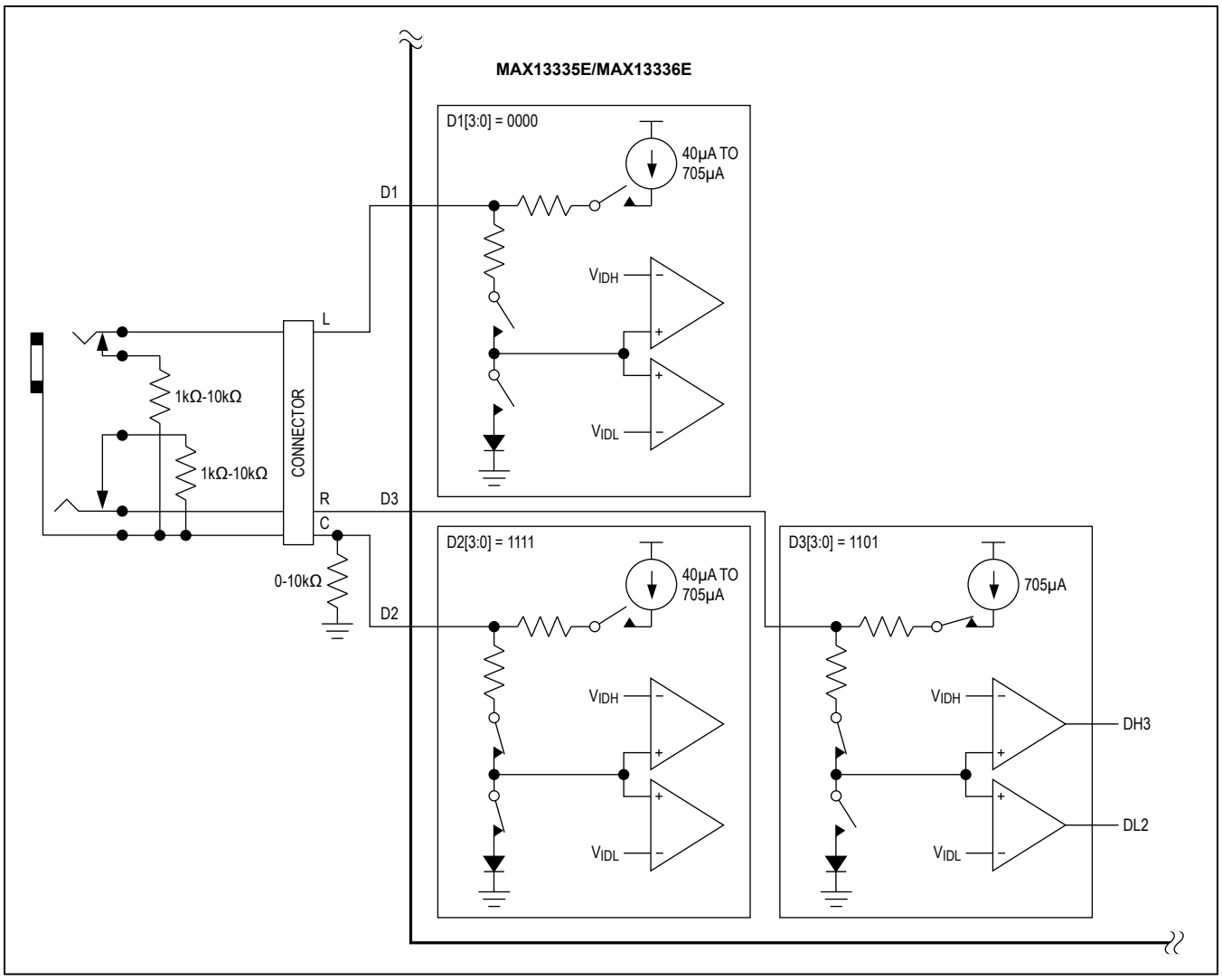


Figure 12. Diagnostic Setup for Remote Jack Sense

Low-Power Standby with Jack Sense

When the device is used as an auxiliary amplifier, there is the option to put the device into a low-power standby mode while waiting for a plug to be inserted into the jack. To do this, perform the following steps:

1) Connect D0 to the R (or L) of the jack.
2) Connect R_{SENSE} (or L_{SENSE}) of the jack with a 50Ω resistor to ground.
3) Set the SHDN bit to 1 in the CTRL0 register to power down the amplifier.
4) Set D0[3:0] = 0001 to source 40µA out of the D0 pin.
5) Enable the JSI bit in the CTRL0 register.

When a plug is inserted, the DH0 comparator trips and subsequently asserts the interrupt $\overline{INT}$ pin. The microcontroller can read back the STAT0 register to check for DH0 = 1 and follow up by setting SHDN to 0.

In the standby state, the typical current consumption is reduced to 290µA.

ESD Guide

For maximum protection against IEC 61000-4-2 and ISO 10605 ESD pulses, a 1kΩ or larger resistor is recommended on every diagnostic D_ pin before the input AC-coupling capacitor. Additionally, a suitable ESD diode must be connected from the DC-blocking ceramic capacitor to ground. The ESD diode can be connected on either side of the DC-blocking capacitor; however, depending on application requirements, the IC side may allow for a lower clamping voltage, which results in a smaller ESD device. If the input source is always DC biased to $V_{BAT}/2$, then a unidirectional ESD device can be used when clamping on the input side of the DC-blocking capacitor. See Figure 13.

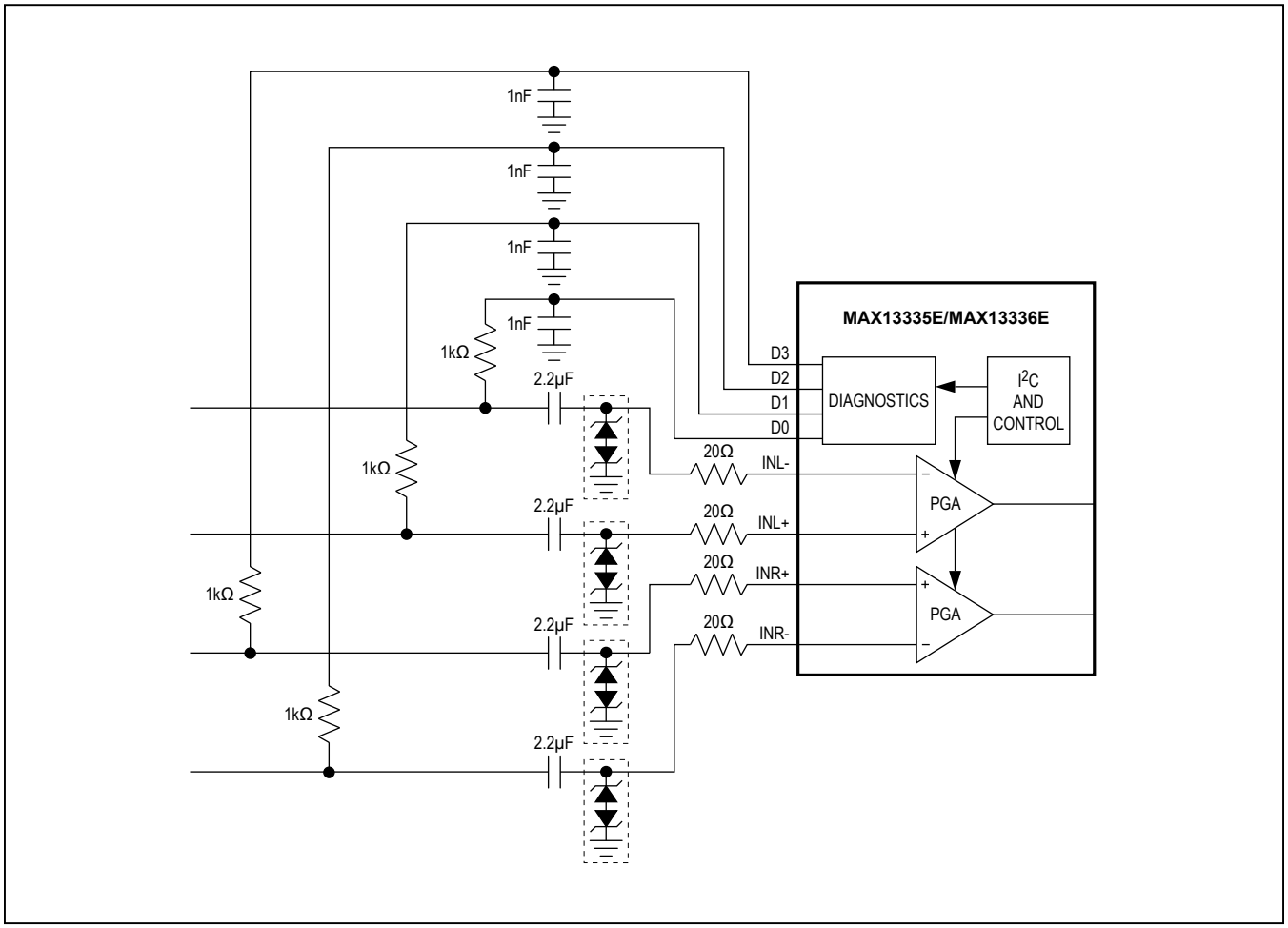
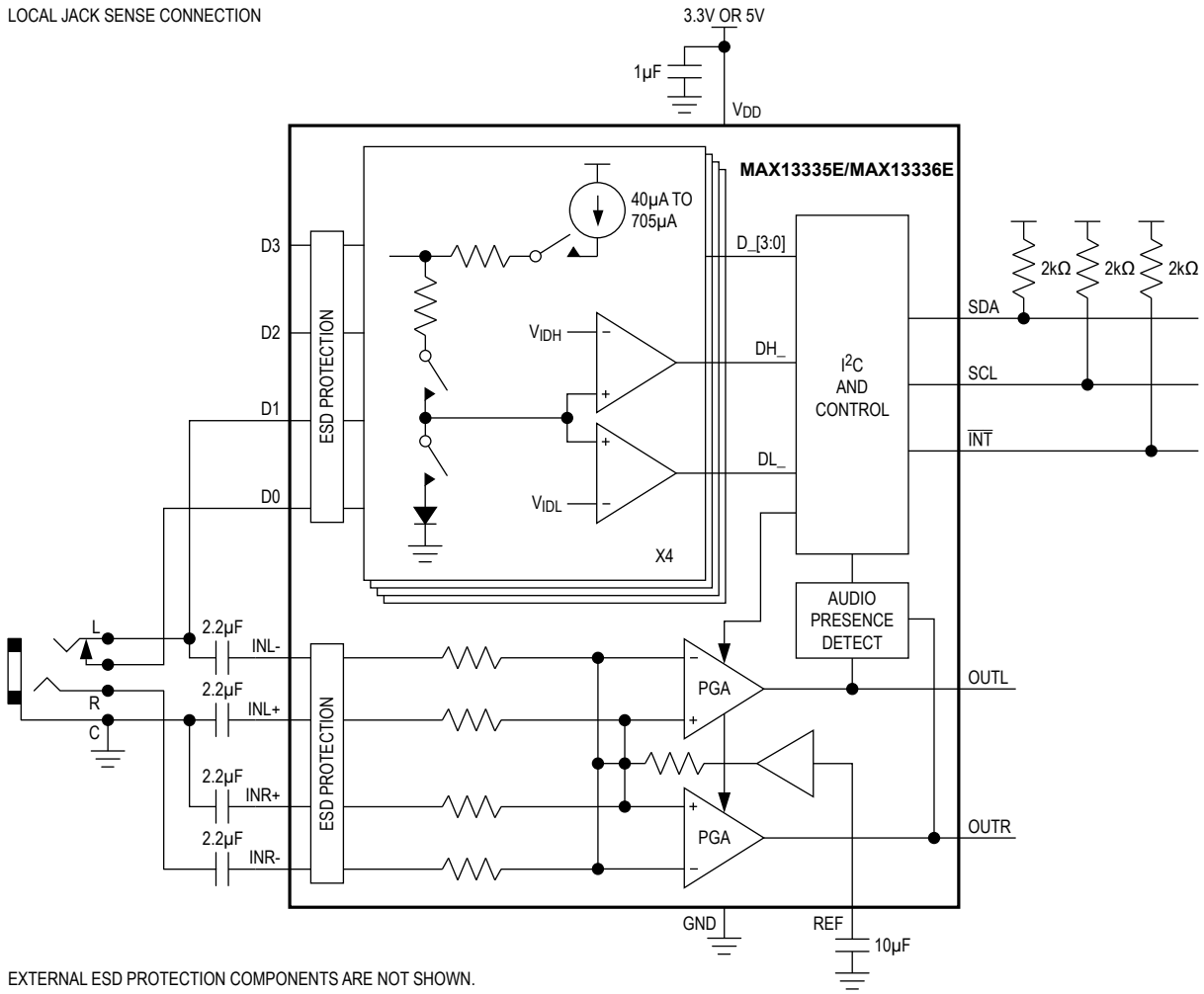
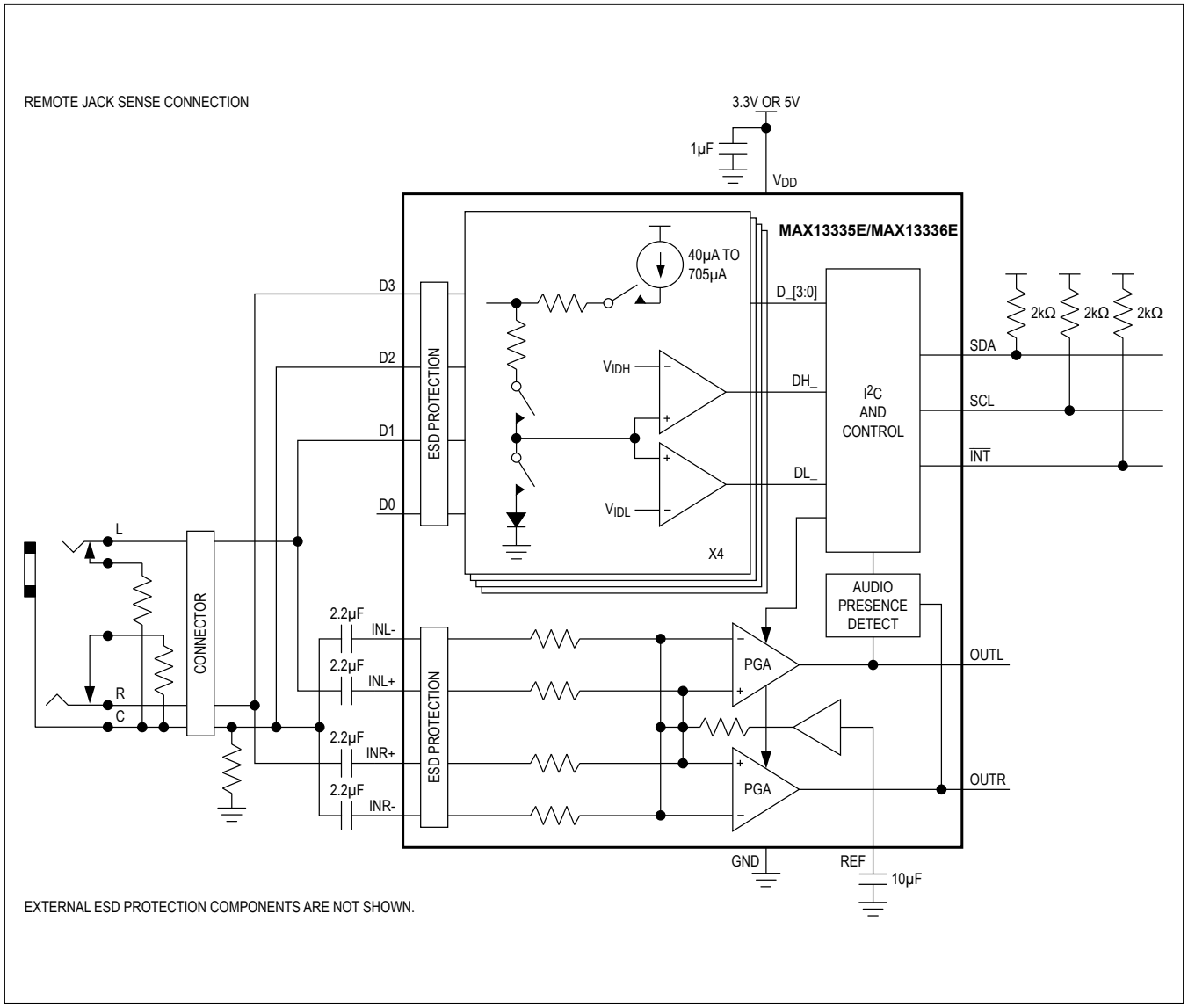


Figure 13. ESD Protection Technique Against IEC 61000-4-2 and ISO 10605 Pulses

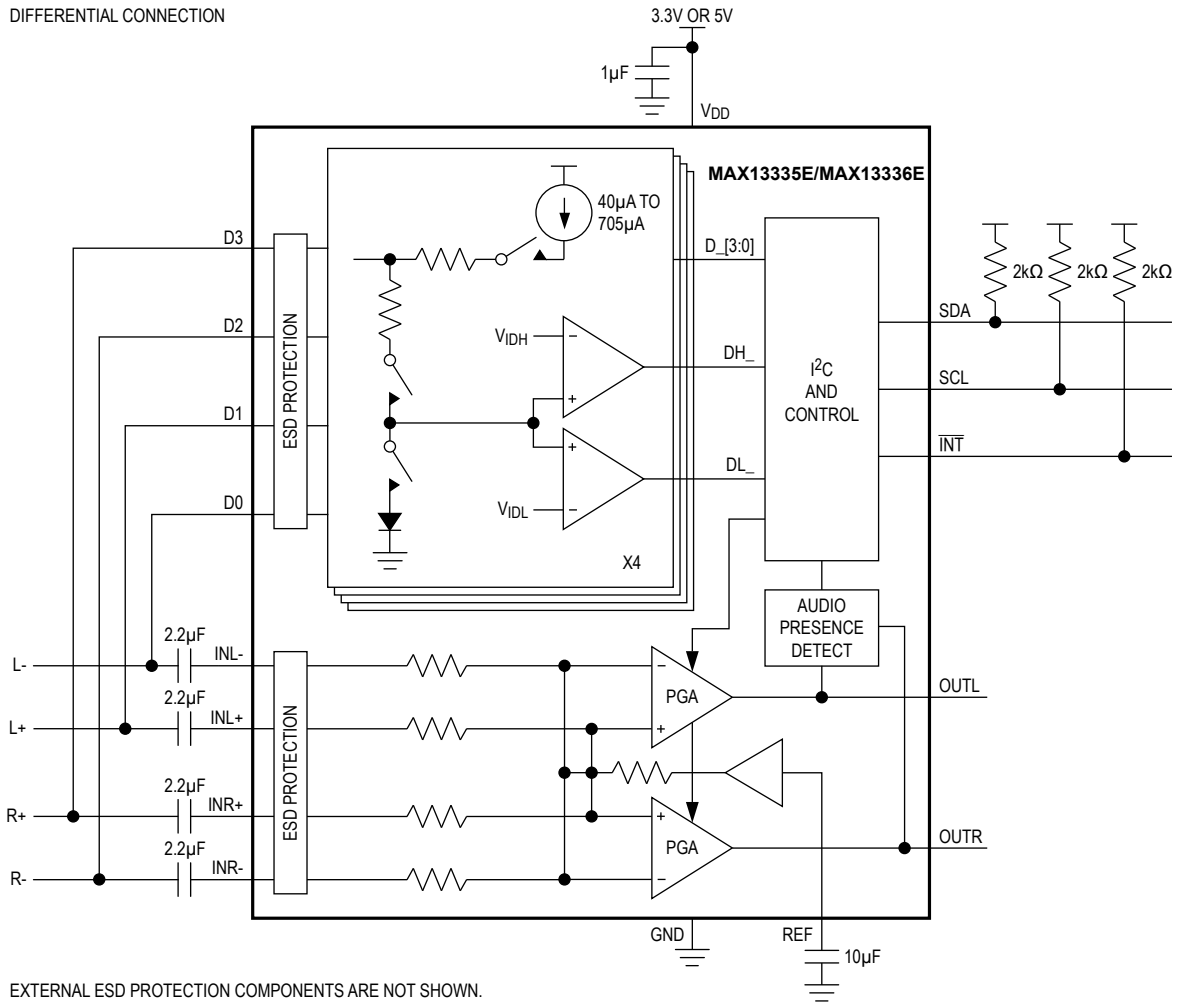
Typical Application Circuits (continued)



Typical Application Circuits (continued)



Typical Application Circuits (continued)



Ordering Information

PART	TEMP RANGE	GAIN RANGE (dB)	OPTIONS	PIN-PACKAGE
MAX13335EGEE/V+	-40°C to +105°C	-14 to +16	Differential V_{IN} up to $4V_{RMS}$; quasi-differential V_{IN} up to $2V_{RMS}$	16 QSOP
MAX13336EGEE/V+	-40°C to +105°C	-22 to +8	Differential V_{IN} up to $7V_{RMS}$; quasi-differential V_{IN} up to $3.5V_{RMS}$	16 QSOP

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BCD

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+1	**21-0055**	**90-0167**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/12	Initial release	—
1	7/12	Corrected the read operation procedure in the *Single Byte-Read Operation* and *Burst-Read Operation* sections	14
2	9/17	Added row for CTRL0.DGAIN=0 to *Diagnostic I/O* section in *Electrical Characteristics* table; added Bit 3: DGAIN reference below the *Control Register 0 (CTRL0)* table	5, 17
3	1/18	Updated Bit 3 in the *Control Register 0 (CTRL0)* section	17

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.