19-4503; Rev 0; 4/09

3-Channel, Low-Leakage ESD Protector

General Description

The MAX14541E low-capacitance ±15kV ESD-protection diode array is designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND.

The MAX14541E protects against ESD pulses up to ±15kV Human Body Model (HBM) and ±15kV Air-Gap Discharge, as specified in IEC 61000-4-2. The device has a 6pF (typ) on-capacitance per channel, making them ideal for use on high-speed data I/O interfaces.

The MAX14541E is a triple I/O protector designed for biometric connectors, portable connectors, and SVGA video connections with ultra-low leakage current.

The device is available in a 5-pin SC70 package and is specified over the -40°C to +125°C automotive operating temperature range.

Applications

Glucose Meters

MP3 Players

Digital Cameras

Handheld Equipment

Features

- **High-Speed Data Line ESD Protection**
  - **±15kV Human Body Model**
  - **±15kV IEC 61000-4-2 Air-Gap Discharge**
  - **±8kV IEC 61000-4-2 Contact Discharge**
- **6pF (typ) Low Input Capacitance**
- **1nA (max) Low-Leakage Current**
- **+0.9V to +16V Supply Voltage Range**
- **5-Pin SC70 (2.0mm x 2.2mm) Package**

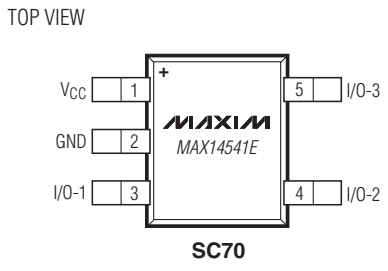
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX14541EAXK+T	-40°C to +125°C	5 SC70	ATY

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Pin Configuration



SC70

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3-Channel, Low-Leakage ESD Protector

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC} to GND.....-0.3V to +18V
I/O-1, I/O-2, I/O-3 to GND ..... -0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (derate 3.1mW/°C above +70°C) 246.9mW
Thermal Resistance (Note 1)
θ_{JA}.....324°C/W
θ_{JC} .....115°C/W
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

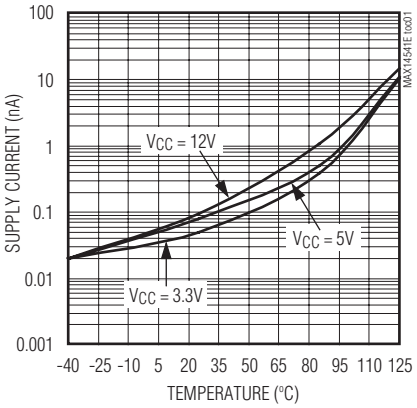
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}			0.9		16	V
Supply Current	I_{CC}				1	100	nA
Diode Forward Voltage	V_F	I_F = 10mA, T_A = +25°C		0.65		0.95	V
Channel Clamp Voltage (Note 3)	V_C	T_A = +25°C, ±15kV Human Body Model, I_F = 10A	Positive transients			V_{CC} + 25	V
			Negative transients			-25	
		T_A = +25°C, ±8kV Contact Discharge (IEC 61000-4-2), I_F = 24A	Positive transients			V_{CC} + 60	V
			Negative transients			-60	
		T_A = +25°C, ±15kV Air-Gap Discharge (IEC 61000-4-2), I_F = 45A	Positive transients			V_{CC} + 100	V
			Negative transients			-100	V
Channel Leakage Current (Note 4)		T_A = -40°C to +50°C		-1		+1	nA
		T_A = -40°C to +125°C		-1		+1	µA
I/O Capacitance		Bias of V_{CC}/2, f = 1MHz (Note 4)			6	7	pF
ESD PROTECTION							
Human Body Model					±15		kV
IEC 61000-4-2 Air-Gap Discharge					±15		kV
IEC 61000-4-2 Contact Discharge					±8		kV

Note 2: Parameters are 100% production tested at T_A = +25°C. Specifications over temperature guaranteed by design only.
Note 3: Idealized clamp voltages. See the *Applications Information* section for more information.
Note 4: Guaranteed by design, not production tested.

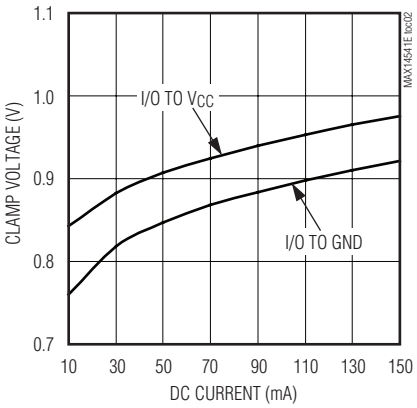
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

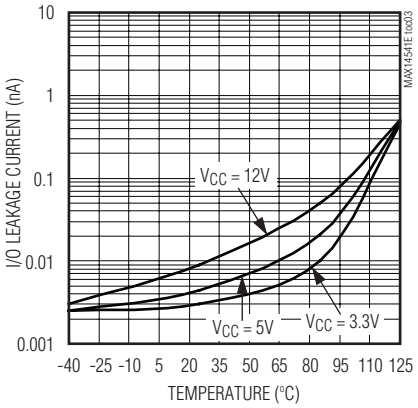
SUPPLY CURRENT vs. TEMPERATURE



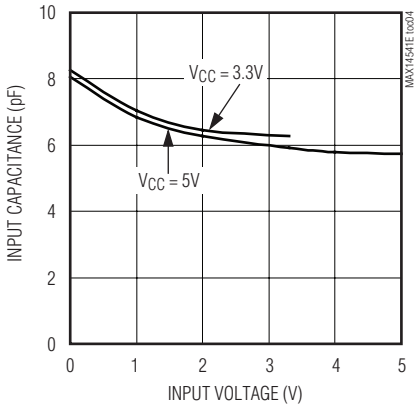
CLAMP VOLTAGE vs. DC CURRENT



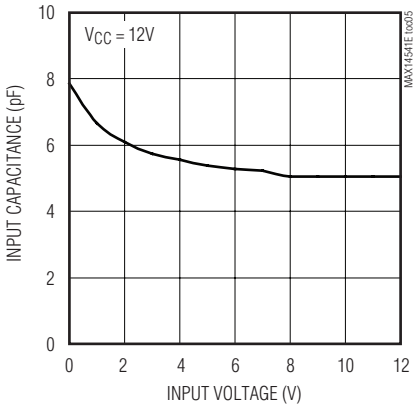
I/O LEAKAGE CURRENT vs. TEMPERATURE



INPUT CAPACITANCE vs. INPUT VOLTAGE



INPUT CAPACITANCE vs. INPUT VOLTAGE

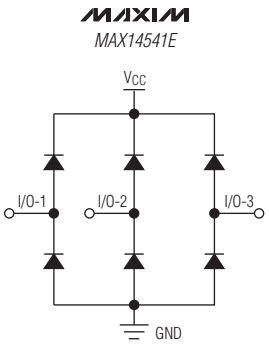


3-Channel, Low-Leakage ESD Protector

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor as close as possible to the device.
2	GND	Ground. Connect GND with a low-impedance connection to the ground plane.
3	I/O-1	ESD-Protected Channel
4	I/O-2	ESD-Protected Channel
5	I/O-3	ESD-Protected Channel

Functional Diagram



Detailed Description

The MAX14541E low-leakage, low-capacitance, ±15kV ESD-protection diode arrays are suitable for high-speed and general-signal ESD protection. Low input capacitance makes this device ideal for ESD protection of high-speed signals. Each channel consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND. The MAX14541E is a 3-channel device (see the *Functional Diagram*).

The MAX14541E is designed to work in conjunction with a device's intrinsic ESD protection. The MAX14541E limits the excursion of the ESD event to below ±25V peak voltage when subjected to the Human Body Model waveform. When subjected to the IEC 61000-4-2 Contact Discharge waveform, the peak voltage is limited to ±60V. The peak voltage is limited to ±100V when subjected to Air-Gap Discharge. The device protected by the MAX14541E must be able to withstand these peak voltages, plus any additional voltage generated by the parasitic of the board.

Applications Information

Design Considerations

Maximum protection against ESD damage results from proper board layout (see the *Layout Recommendations* section). A good layout reduces the parasitic series inductance on the ground line, supply line, and protected signal lines. The MAX14541E ESD diodes clamp the voltage on the protected lines during an ESD event and shunt the current to GND or V_{CC}. In an ideal circuit, the clamping voltage (V_C) is defined as the forward voltage drop (V_F) of the protection diode, plus any supply voltage present on the cathode.

For positive ESD pulses:

$$V_C = V_{CC} + V_F$$

For negative ESD pulses:

$$V_C = -V_F$$

The effect of the parasitic series inductance on the lines must also be considered (Figure 1).

For positive ESD pulses:

$$V_C = V_{CC} + V_{F(D1)} + \left(L1 \times \frac{d(I_{ESD})}{dt}\right) + \left(L2 \times \frac{d(I_{ESD})}{dt}\right)$$

For negative ESD pulses:

$$V_C = -\left(V_{F(D2)} + \left(L1 \times \frac{d(I_{ESD})}{dt}\right) + \left(L3 \times \frac{d(I_{ESD})}{dt}\right)\right)$$

where I_{ESD} is the ESD current pulse.

During an ESD event, the current pulse rises from zero to peak value in nanoseconds (Figure 2). For example, in a +15kV IEC 61000-4-7 Air-Gap Discharge ESD event, the pulse current rises to approximately 45A in 1ns ($di/dt = 45 \times 10^9$). An inductance of only 10nH adds an additional 450V to the clamp voltage, and represents approximately 0.5in of board trace. Regardless of the device's specified diode clamp voltage, a poor layout with parasitic inductance significantly increases the effective clamp voltage at the protected signal line. Minimize the effects of parasitic inductance by placing the MAX14541E as close as possible to the connector (or ESD contact point).

A low-ESR 0.1µF capacitor is required between V_{CC} and GND to get the maximum ESD protection possible. This bypass capacitor absorbs the charge transferred by a positive ESD event. Ideally, the supply rail (V_{CC}) would absorb the charge caused by a positive ESD strike without changing its regulated value. All power supplies have an effective output impedance on their positive rails. If a power supply's effective output impedance is 1Ω, then by using V = I x R, the clamping voltage of V_C increases by the equation $V_C = I_{ESD} \times R_{OUT}$. A +8kV IEC 61000-4-2 ESD event generates a current spike of 24A. The clamping voltage increases by $V_C = 24A \times 1\Omega$, or $V_C = 24V$. Again, a poor layout without proper bypassing increases the clamping voltage. A ceramic chip capacitor mounted as close as possible to the MAX14541E V_{CC} pin is the best choice for this application. A bypass capacitor should also be placed as close as possible to the protected device.

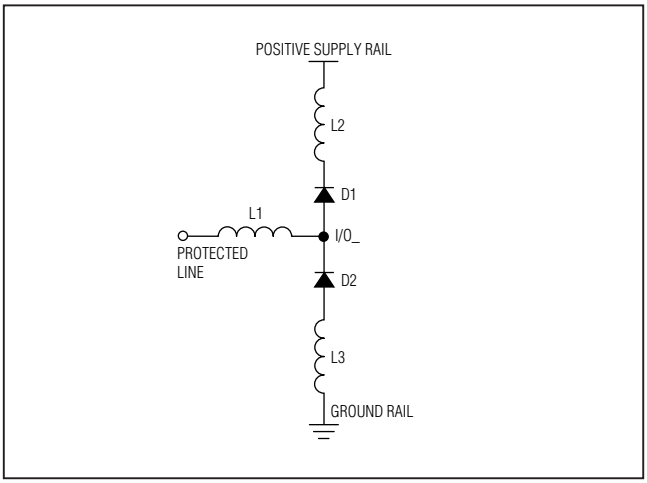


Figure 1. Parasitic Series Inductance

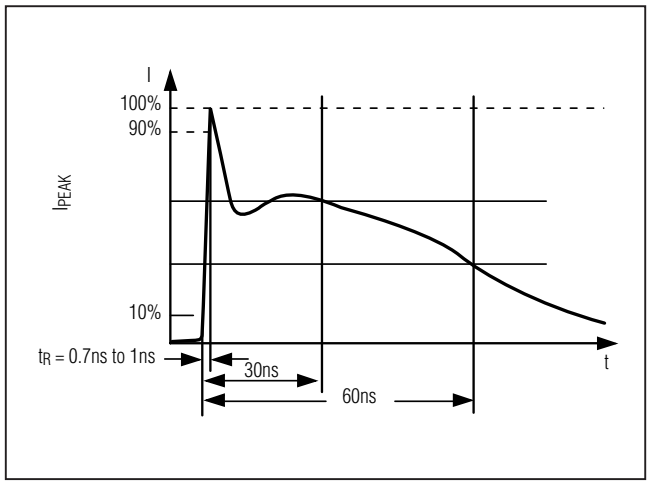


Figure 2. IEC 61000-4-2 ESD Generator Current Waveform

ESD Protection

ESD protection can be tested in various ways. The MAX14541E are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge Method specified in IEC 61000-4-2
- ±15kV using the IEC 61000-4-2 Air-Gap Discharge Method

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 3 shows the Human Body Model, and Figure 4 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX14541E helps users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 Model is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 5), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 2 shows the current waveform for the ±8kV IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

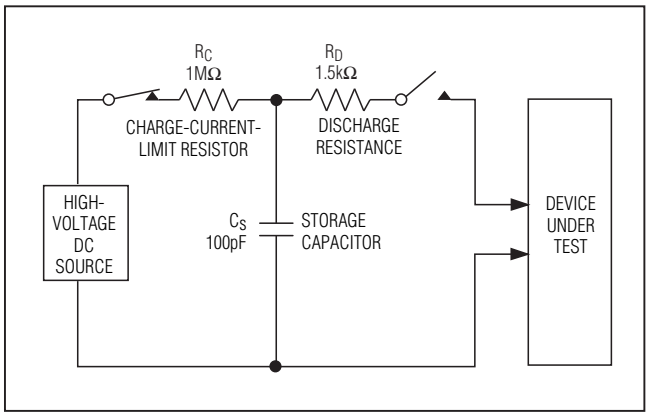


Figure 3. Human Body ESD Test Model

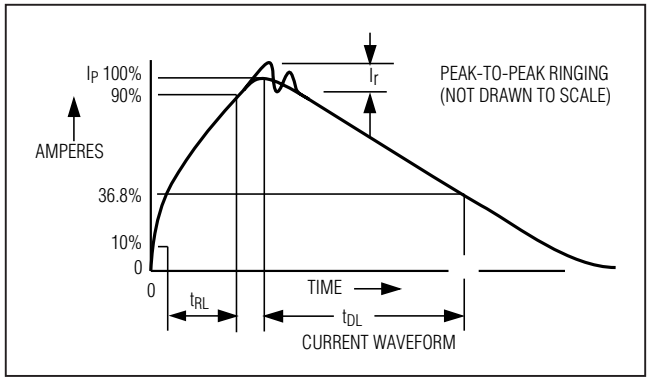


Figure 4. Human Body Model Current Waveform

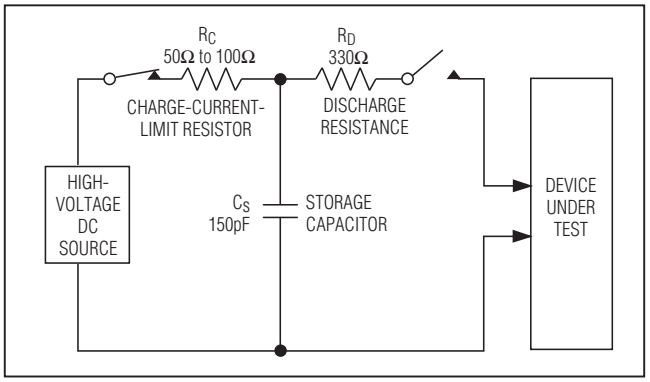


Figure 5. IEC 61000-4-2 ESD Test Model

Layout Recommendations

Proper circuit-board layout is critical to suppress ESD-induced line transients (see Figure 6). The MAX14541E clamps to 100V; however, with improper layout, the voltage spike at the device can be much higher. A lead inductance of 10nH with a 45A current spike results in an additional 450V spike on the protected line. It is essential that the layout of the PCB follows these guidelines:

1) Minimize trace length between the connector or input terminal, I/O_, and the protected signal line.
2) Use separate planes for power and ground to reduce parasitic inductance and to reduce the impedance to the power rails for shunted ESD current.
3) Ensure short low-inductance ESD transient return paths to GND and V_{CC}.
4) Minimize conductive power and ground loops.
5) Do not place critical signals near the edge of the PCB.
6) Bypass V_{CC} to GND with a low-ESR ceramic capacitor as close as possible to V_{CC}.
7) Bypass the supply of the protected device to GND with a low-ESR ceramic capacitor as close as possible to the supply pin.

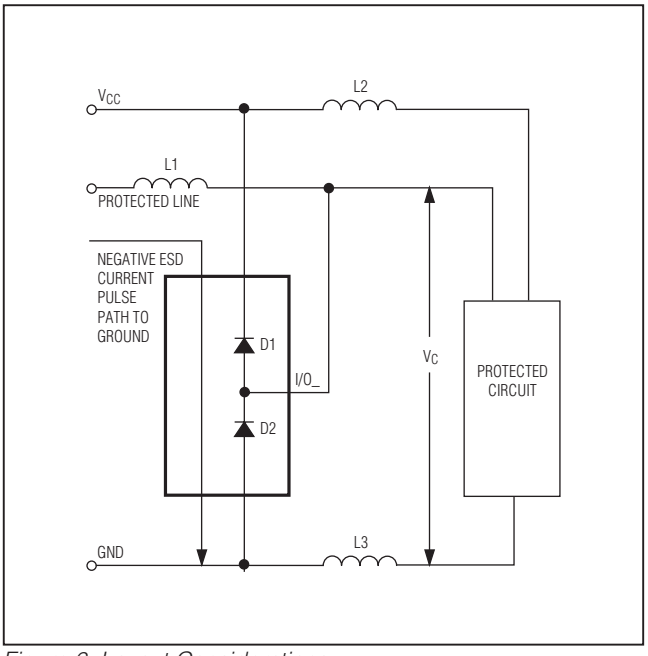
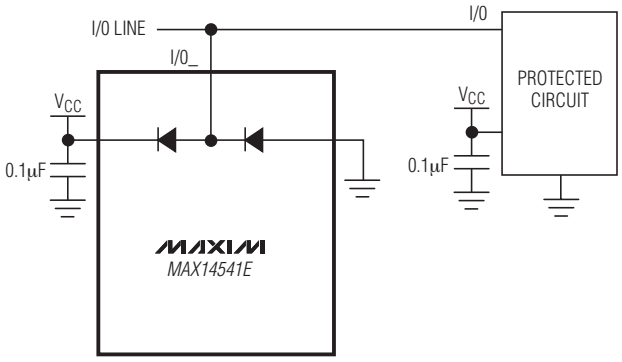


Figure 6. Layout Considerations

Typical Application Circuit



3-Channel, Low-Leakage ESD Protector

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
5 SC70	X5+1	21-0076

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