# MAX14954

# Ruggedized Quad PCIe Redriver with Equalization and Extended Temperature Operation

## General Description

The MAX14954 is a quad equalizer/redriver designed to improve PCI Express® (PCIe) signal integrity by providing programmable input equalization at its receiver and programmable redrive circuitry. The output circuitry reestablishes deemphasis lost on the board and compensates for circuit-board loss. The device permits optimal placement of key PCIe components. The device is useful with stripline, microstrip printed circuits, and balanced 100Ω cable.

The device is tailored for PCIe and features electrical idle and receiver detection on each channel. It is optimized for PCIe Gen III (8.0GT/s) and Gen II (5.0GT/s) data rates, while still handling Gen I (2.5GT/s).

The MAX14954 is available in a small, lead-free, 42-pin (3.5mm x 9.0mm) TQFN package for optimal layout and minimal space requirements. The device is specified over -40°C to +85°C extended operating temperature range.

## Applications

- Industrial/Embedded PCs
- Computer on Modules
- Carrier Boards
- Test Equipment
- Rack Server Industrial PCs
- Medical Equipment

## Benefits and Features

- Fully Integrated for Ease of Use and Design Flexibility
  - Optimized for PCIe Gen III (8.0GT/s), Gen II (5.0GT/s); Gen I (2.5 GT/s) Compatible
  - Four Levels of Input Equalization Up to 16dB
  - Eight Levels of Output Deemphasis Up to 9dB
- High Level of Performance to Overcome Noise in Lossy Channels
  - Random Jitter: 0.5ps$_{RMS}$ (typ)
  - Deterministic Jitter: 10.5ps$_{P-P}$ (typ)
  - Equalization Permits Placement Up to 30in FR4
- Robust Solution for Harsh Environments
  - Industrial Temperature Rated: -40°C to + 85°C
  - ±5kV Human Body Model (HBM) Protection on All Pins
  - Housed in a Flow-Through (3.5mm x 9.5mm) TQFN Package for Resistance to Vibration/ Shocks

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX14954.related.*

*PCI Express is a registered trademark of PCI-SIG Corp.*

*19-6531; Rev 0; 11/12*

maxim integrated™

## Absolute Maximum Ratings

(Voltages referenced to GND.)
$V_{CC}$ ..... -0.3V to +4V
All Other Pins (Note 1) ..... -0.3V to ($V_{CC}$ + 0.3V)
Continuous Current IN_P/IN_N ..... ±30mA
Peak Current IN_P/IN_N
(pulsed for 1µs, 1% duty cycle) ..... ±100mA

Continuous Power Dissipation ($T_A$ = +70°C)
TQFN (derate 34.5mW/°C above +70°C) ..... 2759mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

**Note 1:** All I/O pins are clamped by internal diodes.

## Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) ..... 29°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$) ..... 2°C/W

**Note 2:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Characteristics

($V_{CC}$ = +3.0V to +3.6V, $C_{CL}$ = 200nF coupling capacitor on each output, $R_L$ = 50Ω on each output, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DC PERFORMANCE** | | | | | | | |
| Power-Supply Range | $V_{CC}$ | | | 3.0 | | 3.6 | V |
| Supply Current | $I_{CC}$ | EN = $V_{CC}$ | OEQ2 = GND, OEQ1 = GND, OEQ0 = GND | | 205 | 260 | mA |
| | | | OEQ2 = GND, OEQ1 = GND, OEQ0 = $V_{CC}$ | | 212 | 270 | |
| | | | OEQ2 = GND, OEQ1 = $V_{CC}$, OEQ0 = GND | | 214 | 270 | |
| | | | OEQ2 = GND, OEQ1 = $V_{CC}$, OEQ0 = $V_{CC}$ | | 247 | 305 | |
| | | | OEQ2 = $V_{CC}$, OEQ1 = GND, OEQ0 = GND | | 213 | 270 | |
| | | | OEQ2 = $V_{CC}$, OEQ1 = GND, OEQ0 = $V_{CC}$ | | 263 | 330 | |
| | | | OEQ2 = $V_{CC}$, OEQ1 = $V_{CC}$, OEQ0 = GND | | 276 | 345 | |
| | | | OEQ2 = $V_{CC}$, OEQ1 = $V_{CC}$, OEQ0 = $V_{CC}$ | | 328 | 410 | |

## Electrical Characteristics (continued)

($V_{CC}$ = +3.0V to +3.6V, $C_{CL}$ = 200nF coupling capacitor on each output, $R_L$ = 50Ω on each output, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Standby Current | $I_{STBY}$ | EN = GND | OEQ2 = GND, OEQ1 = GND, OEQ0 = GND | | 113 | 150 | mA |
| | | | OEQ2 = GND, OEQ1 = GND, OEQ0 = $V_{CC}$ | | 122 | 150 | |
| | | | OEQ2 = GND, OEQ1 = $V_{CC}$, OEQ0 = GND | | 125 | 155 | |
| | | | OEQ2 = GND, OEQ1 = $V_{CC}$, OEQ0 = $V_{CC}$ | | 150 | 185 | |
| | | | OEQ2 = $V_{CC}$, OEQ1 = GND, OEQ0 = GND | | 122 | 150 | |
| | | | OEQ2 = $V_{CC}$, OEQ1 = GND, OEQ0 = $V_{CC}$ | | 172 | 210 | |
| | | | OEQ2 = $V_{CC}$, OEQ1 = $V_{CC}$, OEQ0 = GND | | 184 | 225 | |
| | | | OEQ2 = $V_{CC}$, OEQ1 = $V_{CC}$, OEQ0 = $V_{CC}$ | | 237 | 290 | |
| Differential Input Impedance | $Z_{RX-DIFF-DC}$ | DC | | 80 | 100 | 120 | Ω |
| Differential Output Impedance | $Z_{TX-DIFF-DC}$ | DC | | 80 | 100 | 120 | Ω |
| Common-Mode Resistance to GND When Input Terminations Are Not Powered | $Z_{RX-HIGH-IMP-DC}$ | -150mV < $V_{IN_CM}$ < 200mV | | 50 | | | kΩ |
| Common-Mode Resistance to GND When Input Terminations Are Powered | $Z_{RX-DC}$ | DC | | 20 | 25 | 30 | Ω |
| Output Short-Circuit Current | $I_{TX-SHORT}$ | Single-ended (Note 4) | | 90 | | | mA |
| Common-Mode Delta Between Active and Idle States | $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ | | | | | 8 | mV |
| DC Output Offset During Active State | $V_{TX-ACTIVE-DIFF-DC}$ | $\lvert(V_{OUT_P} - V_{OUT_N})\rvert$ | | | | 100 | mV |
| DC Output Offset During Electrical Idle | $V_{TX-IDLE-DIFF-DC}$ | $\lvert(V_{OUT_P} - V_{OUT_N})\rvert$ | | | | 100 | mV |

## Electrical Characteristics (continued)

($V_{CC}$ = +3.0V to +3.6V, $C_{CL}$ = 200nF coupling capacitor on each output, $R_L$ = 50Ω on each output, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Note 4)** | | | | | | |
| Differential Input Return Loss | $RL_{RX-DIFF}$ | f = 0.05GHz to 1.25GHz | 10 | | | dB |
| | | f = 1.25GHz to 2.5GHz | 8 | | | |
| | | f = 2.5GHz to 4GHz | 5 | | | |
| Common-Mode Input Return Loss | $RL_{RX-CM}$ | f = 0.05GHz to 2.5GHz | 6 | | | dB |
| | | f = 2.5GHz to 4GHz | 4 | | | |
| Differential Output Return Loss | $RL_{TX-DIFF}$ | f = 0.05GHz to 1.25GHz | 10 | | | dB |
| | | f = 1.25GHz to 2.5GHz | 8 | | | |
| | | f = 2.5GHz to 4GHz | 4 | | | |
| Common-Mode Output Return Loss | $RL_{TX-CM}$ | f = 0.05GHz to 2.5GHz | 6 | | | dB |
| | | f = 2.5GHz to 4GHz | 4 | | | |
| Redriver Operation Differential Input-Signal Range | $V_{RX-DIFF-PP}$ | | 100 | | 1200 | $mV_{P-P}$ |
| Full-Swing Differential Output Voltage (No Deemphasis) | $V_{TX-DIFF-PP}$ | $\|(V_{OUT_P} - V_{OUT_N})\|$, OEQ2 = GND, OEQ1 = GND, OEQ0 = GND | 800 | | 1350 | $mV_{P-P}$ |
| Output Deemphasis Ratio, 0dB | $V_{TX-DE-RATIO-0dB}$ | OEQ2 = GND, OEQ1 = GND, OEQ0 = GND, Figure 1 | | 0 | | dB |
| Output Deemphasis Ratio, 3.5dB | $V_{TX-DE-RATIO-3.5dB}$ | OEQ2 = GND, OEQ1 = GND, OEQ0 = $V_{CC}$, Figure 1 | | 3.5 | | dB |
| Output Deemphasis Ratio, 6dB | $V_{TX-DE-RATIO-6dB}$ | OEQ2 = GND, OEQ1 = $V_{CC}$, OEQ0 = GND, Figure 1 | | 6 | | dB |
| Output Deemphasis Ratio, 6dB with Higher Amplitude | $V_{TX-DE-HA-RATIO-6dB}$ | OEQ2 = GND, OEQ1 = $V_{CC}$, OEQ0 = $V_{CC}$, Figure 1 | | 6 | | dB |
| Output Deemphasis Ratio, 3.5dB with Preshoot | $V_{TX-DE-PS-RATIO-3.5dB}$ | OEQ2 = $V_{CC}$, OEQ1 = GND, OEQ0 = GND, Figure 1 | | 3.5 | | dB |
| Output Deemphasis Ratio, 6dB with Preshoot | $V_{TX-DE-PS-RATIO-6dB}$ | OEQ2 = $V_{CC}$, OEQ1 = GND, OEQ0 = $V_{CC}$, Figure 1 | | 6 | | dB |
| Output Deemphasis Ratio, 9dB with Preshoot | $V_{TX-DE-PS-RATIO-9dB}$ | OEQ2 = $V_{CC}$, OEQ1 = $V_{CC}$, OEQ0 = GND, Figure 1 | | 9 | | dB |
| Output Deemphasis Ratio, 9dB with Preshoot with Higher Amplitude | $V_{TX-DE-PS-HA-RATIO-9dB}$ | OEQ2 = $V_{CC}$, OEQ1 = $V_{CC}$, OEQ0 = $V_{CC}$, Figure 1 | | 9 | | dB |
| Input Equalization, 5dB | $V_{RX-EQ-5dB}$ | INEQ1 = GND, INEQ0 = GND (Note 5) | | 5 | | dB |
| Input Equalization, 8dB | $V_{RX-EQ-8dB}$ | INEQ1 = GND, INEQ0 = $V_{CC}$ (Note 5) | | 8 | | dB |
| Input Equalization, 12dB | $V_{RX-EQ-12dB}$ | INEQ1 = $V_{CC}$, INEQ0 = GND (Note 5) | | 12 | | dB |

## Electrical Characteristics (continued)

($V_{CC}$ = +3.0V to +3.6V, $C_{CL}$ = 200nF coupling capacitor on each output, $R_L$ = 50Ω on each output, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = +3.3V and $T_A$ = +25°C.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Equalization, 16dB | $V_{RX-EQ-16dB}$ | INEQ1 = $V_{CC}$, INEQ0 = $V_{CC}$ (Note 5) | | 16 | | dB |
| **AC PERFORMANCE (Note 4)** | | | | | | |
| Output Common-Mode Voltage Swing Peak-to-Peak | $V_{TX-CM-AC-PP}$ | Max($V_{OUT_P}$ + $V_{OUT_N}$)/2 - Min($V_{OUT_P}$ + $V_{OUT_N}$)/2 | | | 100 | $mV_{P-P}$ |
| Propagation Delay | $t_{PD}$ | | 120 | 160 | 240 | ps |
| Rise/Fall Time | $t_{TX-RISE-FALL}$ | (Note 6) | 20 | | | ps |
| Rise/Fall Time Mismatch | $t_{TX-RF-MISMATCH}$ | (Note 6) | | | 5 | ps |
| Deterministic Jitter | $t_{TX-DJ-DD}$ | K28.5 pattern, AC-coupled, $R_L$ = 50Ω, data rate = 8GT/s | | 10.5 | 23.5 | $ps_{P-P}$ |
| Random Jitter | $t_{TX-RJ-DD}$ | D10.2 pattern, no deemphasis, no preshoot, data rate = 8GT/s | | 0.5 | 1.5 | $ps_{RMS}$ |
| Electrical Idle Entry Delay | $t_{TX-IDLE-SET-TO-IDLE}$ | From input to output, D10.2 pattern, data rate = 1GT/s | | 5 | 8 | ns |
| Electrical Idle Exit Delay | $t_{TX-IDLE-TO-DIFF-DATA}$ | From input to output, D10.2 pattern, data rate = 1GT/s | | 5 | 8 | ns |
| Electrical Idle Detect Threshold | $V_{TX-IDLE-THRESH}$ | D10.2 pattern, data rate = 1GT/s, (Note 3) | 65 | 112 | 175 | $mV_{P-P}$ |
| | | D10.2 pattern, data rate = 1GT/s to 8GT/s | | 112 | | |
| Output Voltage During Electrical Idle (AC) | $V_{TX-IDLE-DIFF-AC-P}$ | $\lvert(V_{OUT_P} - V_{OUT_N})\rvert$ | | | 20 | $mV_{P-P}$ |
| Receiver Detection Pulse Amplitude | $V_{TX-RCV-DETECT}$ | Voltage change in positive direction | | 600 | | mV |
| Receiver Detection Pulse Width | | | | 150 | | ns |
| Receiver Detection Retry Period | | | | 300 | | ns |
| **CONTROL LOGIC** | | | | | | |
| Input Logic-Level Low | $V_{IL}$ | | | | 0.6 | V |
| Input Logic-Level High | $V_{IH}$ | | 1.4 | | | V |
| Input Logic Hysteresis | $V_{HYST}$ | | | 0.1 | | V |
| Input Pulldown Resistance | $R_{PD}$ | | 200 | 250 | | kΩ |
| **ESD PROTECTION** | | | | | | |
| ESD Voltage | | Human Body Model | | ±5 | | kV |

**Note 3:** All units are 100% production tested at $T_A$ = +85°C. Specifications for all temperature limits are guaranteed by design.
**Note 4:** Guaranteed by design, unless otherwise noted.
**Note 5:** Equivalent to same amount of deemphasis driving the input.
**Note 6:** Rise and fall times are measured using 20% and 80% levels.

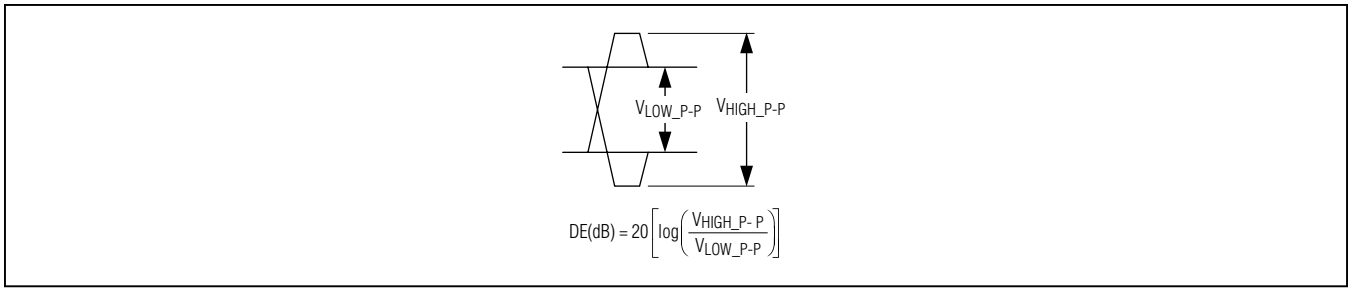
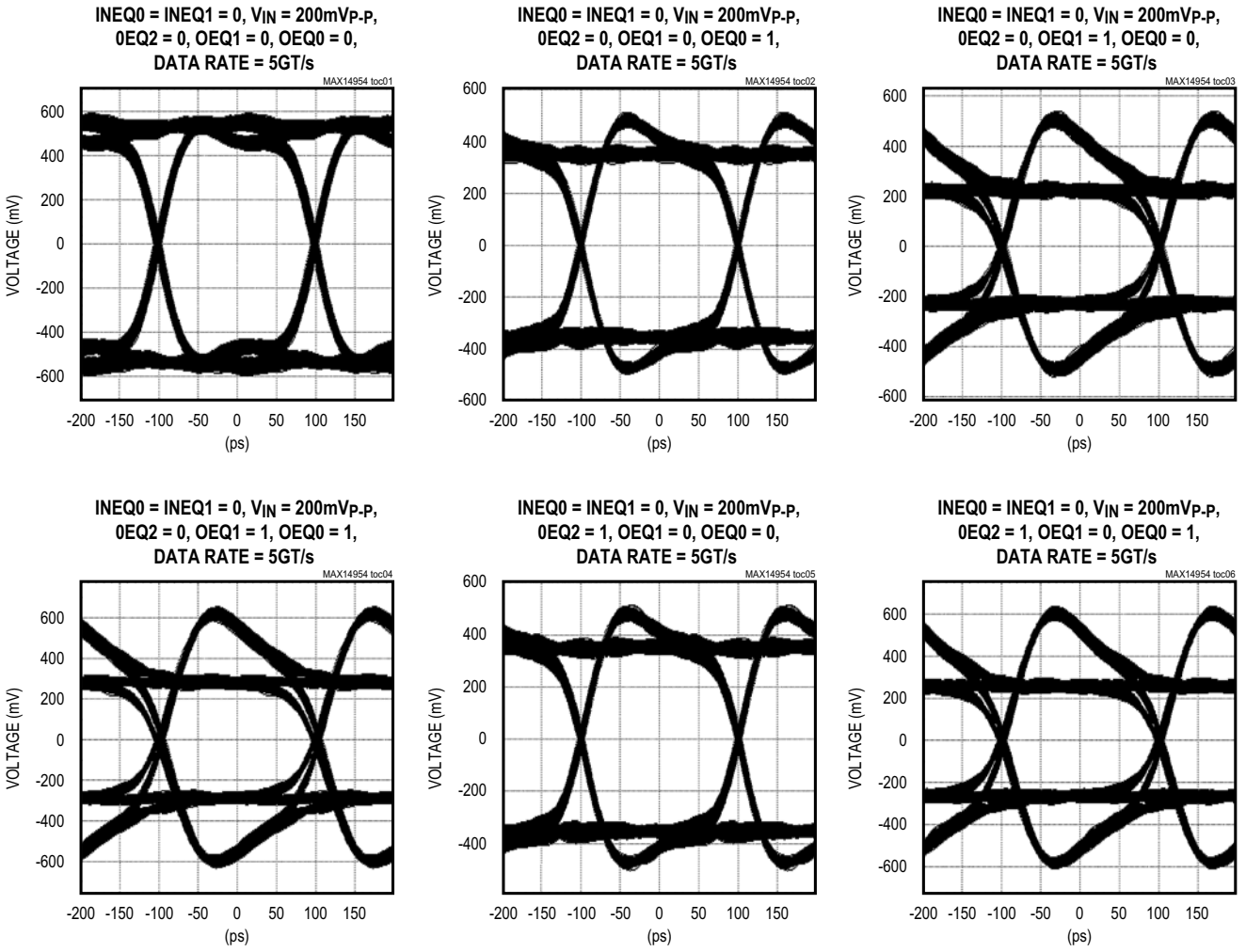



*Figure 1. Illustration of Output Deemphasis*

## Typical Operating Characteristics

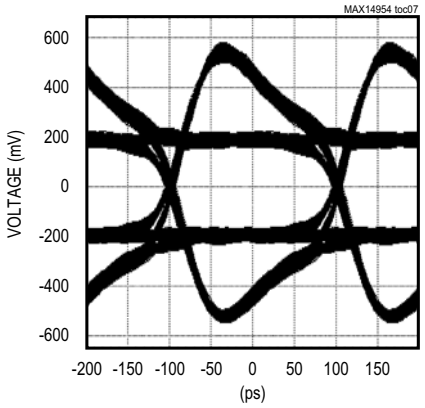
($T_A$ = +25°C, unless otherwise noted.)



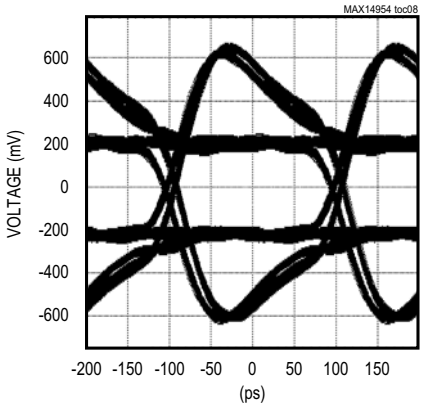
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

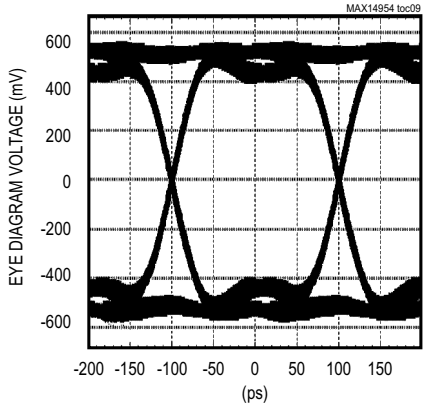
**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 0, OEQ0 = 1, DATA RATE = 5GT/s**



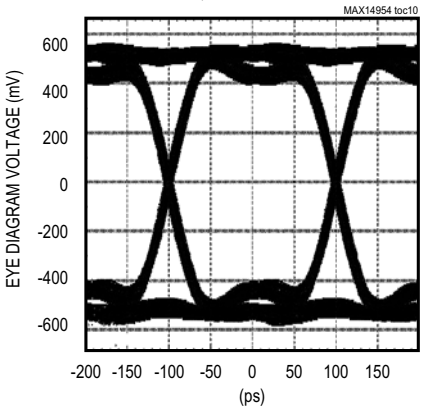

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 1, OEQ0 = 1, DATA RATE = 5GT/s**



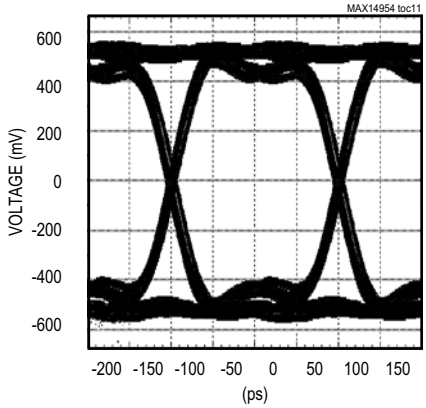

**INEQ1 = 0, INEQ0 = 1, $V_{IN}$ = 500mV$_{P-P}$, 0EQ2 = OEQ1 = OEQ0 = 0, 6in MICROSTRIP ON INPUT, DATA RATE = 5GT/s**



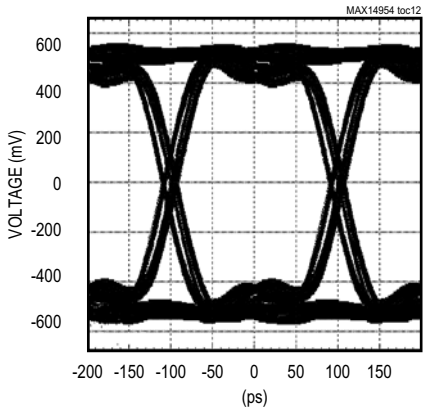

**INEQ1 = 0, INEQ0 = 1, $V_{IN}$ = 500mV$_{P-P}$, 0EQ2 = OEQ1 = OEQ0 = 0, 12in MICROSTRIP ON INPUT, DATA RATE = 5GT/s**




**INEQ0 = 1, INEQ1 = 1, $V_{IN}$ = 500mV$_{P-P}$, WITH 19in STRIPLINE, 0EQ0 = OEQ1 = OEQ2 = 0, DATA RATE = 5GT/s**



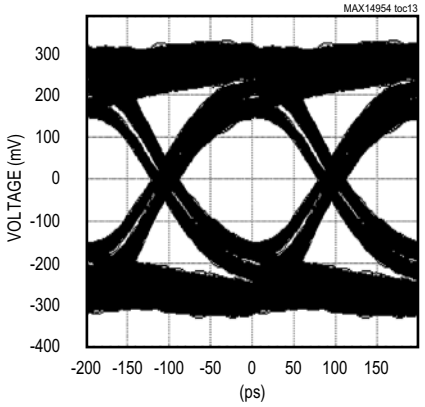

**INEQ0 = 0, INEQ1 = 0, $V_{IN}$ = 500mV$_{P-P}$, WITH 19in STRIPLINE, 0EQ0 = OEQ1 = OEQ2 = 0, DATA RATE = 5GT/s**



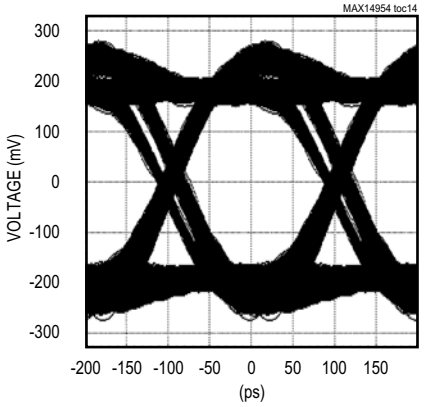
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

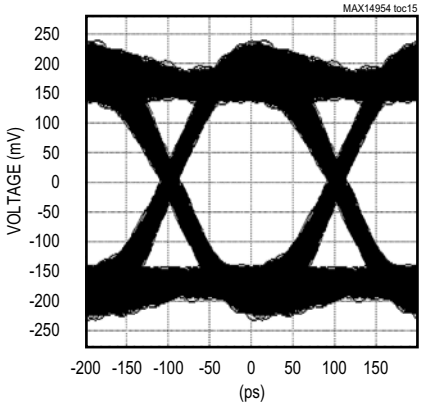
**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 0, OEQ0 = 1, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 5GT/s**



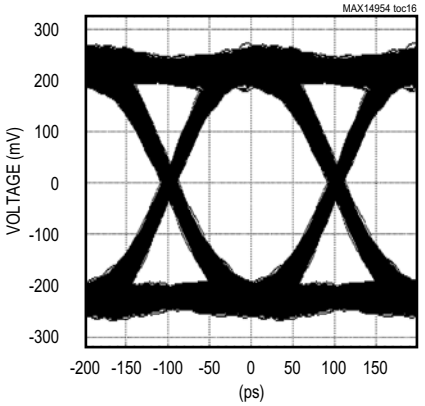

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 1, OEQ0 = 1, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 5GT/s**



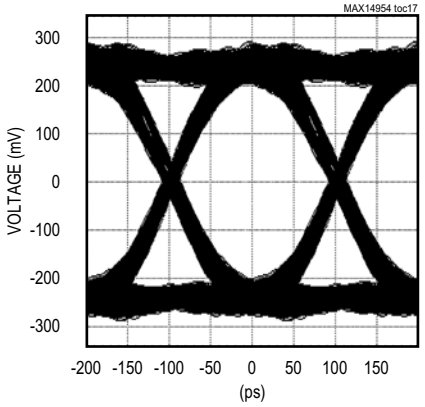

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 1, OEQ0 = 0, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 5GT/s**



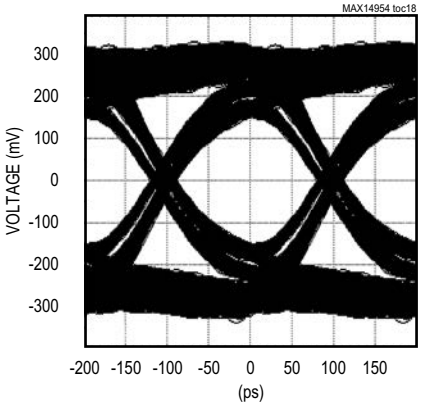

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 0, OEQ0 = 1, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 5GT/s**




**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 1, OEQ0 = 1, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 5GT/s**



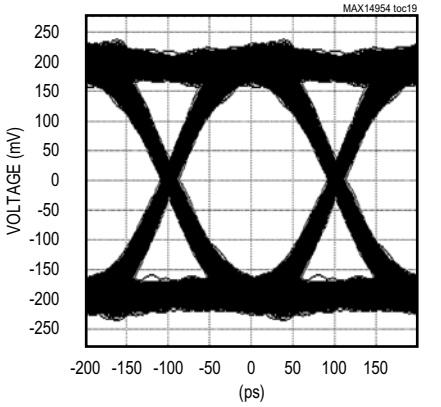

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 0, OEQ0 = 1, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 5GT/s**



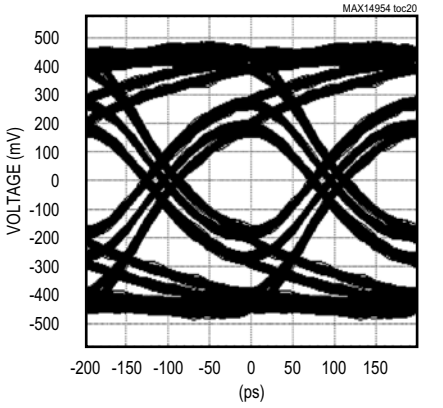
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

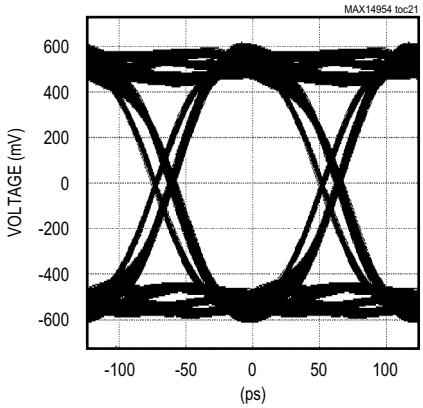
**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 1, OEQ0 = 0, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 5GT/s**



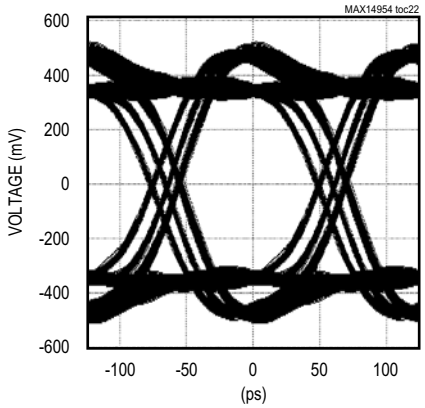

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 0, OEQ0 = 0, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 5GT/s**



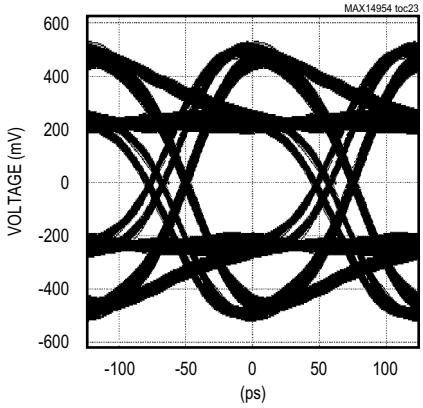

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 0, OEQ0 = 0, DATA RATE = 8GT/s**



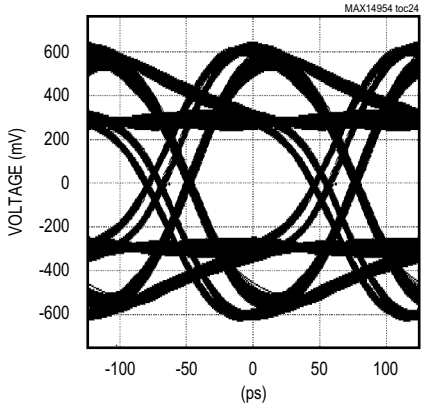

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 0, OEQ0 = 1, DATA RATE = 8GT/s**




**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 1, OEQ0 = 0, DATA RATE = 8GT/s**



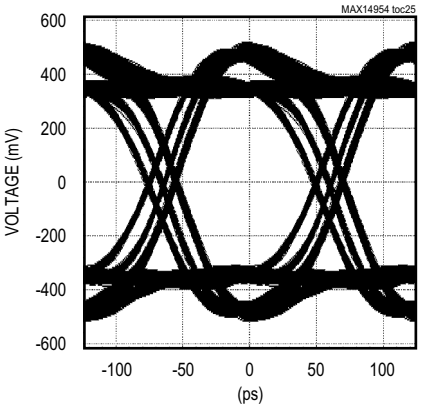

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 1, OEQ0 = 1, DATA RATE = 8GT/s**



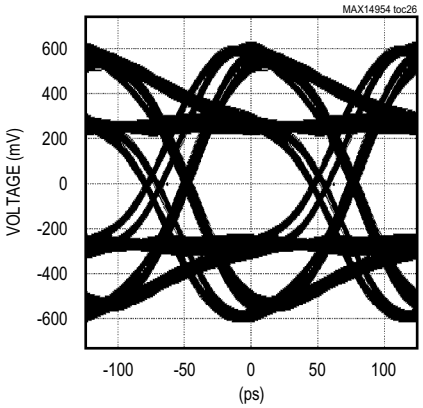
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

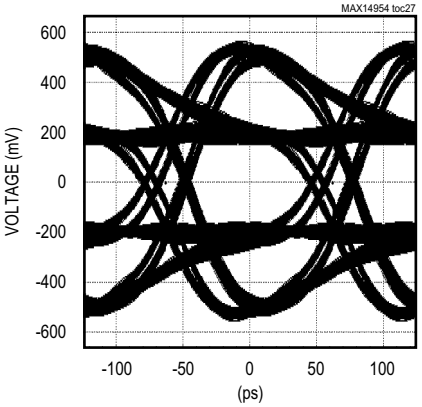
**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 0, OEQ0 = 0, DATA RATE = 8GT/s**



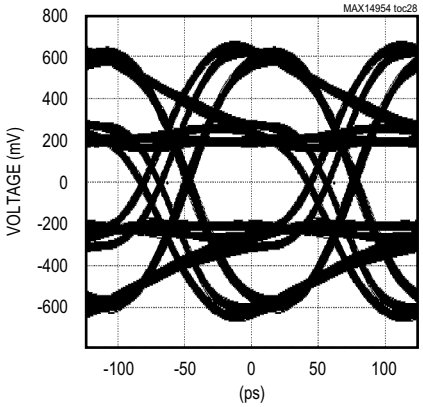

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 0, OEQ0 = 1, DATA RATE = 8GT/s**



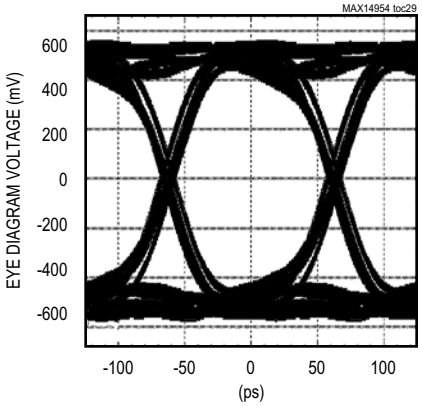

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 1, OEQ0 = 0, DATA RATE = 8GT/s**



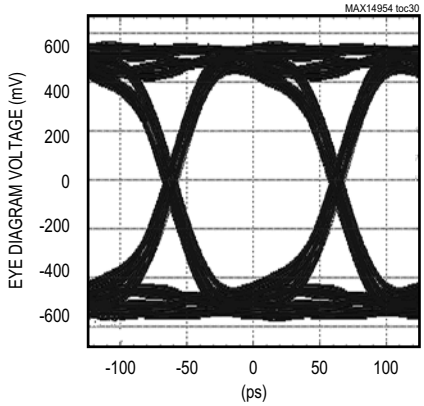

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 1, OEQ0 = 1, DATA RATE = 8GT/s**




**INEQ1 = 0, INEQ0 = 0, $V_{IN}$ = 500mV$_{P-P}$, OEQ2 = OEQ1 = OEQ0 = 0, 6in MICROSTRIP ON INPUT, DATA RATE = 8GT/s**



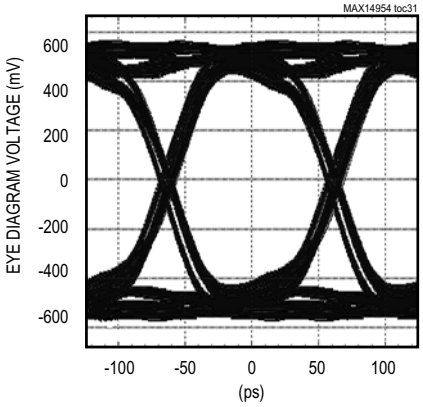

**INEQ1 = 0, INEQ0 = 1, $V_{IN}$ = 500mV$_{P-P}$, OEQ2 = OEQ1 = OEQ0 = 0, 12in MICROSTRIP ON INPUT, DATA RATE = 8GT/s**



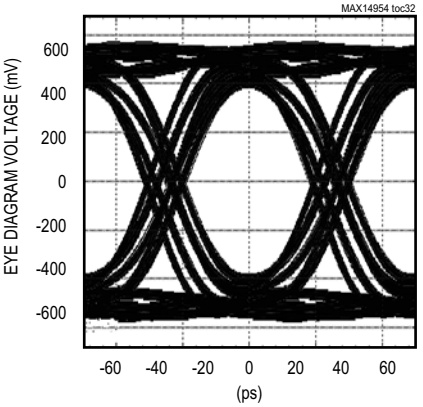
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

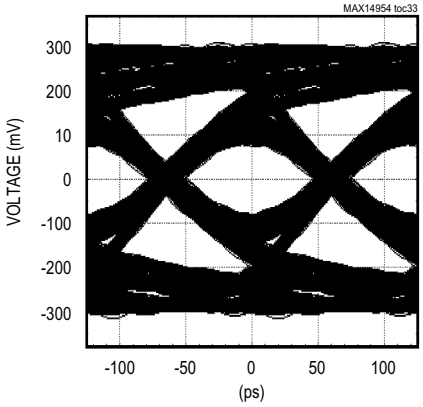
**INEQ1 = 1, INEQ0 = 0, $V_{IN}$ = 500mV$_{P-P}$, OEQ2 = OEQ1 = OEQ0 = 0, 18in MICROSTRIP ON INPUT, DATA RATE = 8GT/s**



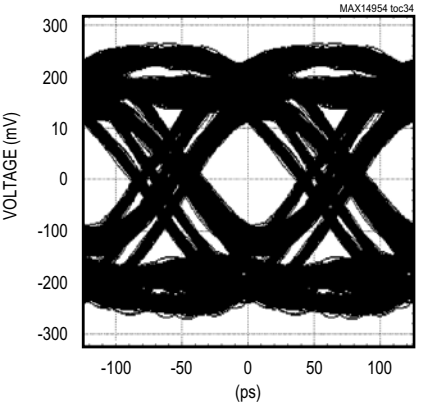

**INEQ1 = 1, INEQ0 = 1, $V_{IN}$ = 500mV$_{P-P}$, OEQ2 = OEQ1 = OEQ0 = 0, 24in MICROSTRIP ON INPUT, DATA RATE = 8GT/s**



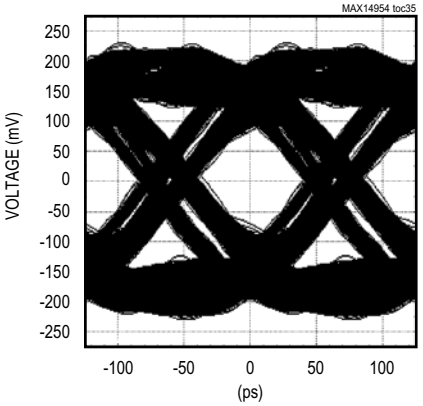

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 0, OEQ0 = 1, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 8GT/s**



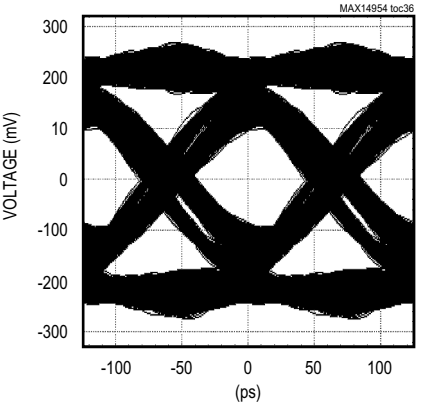

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 1, OEQ0 = 1, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 8GT/s**




**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 1, OEQ0 = 0, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 8GT/s**



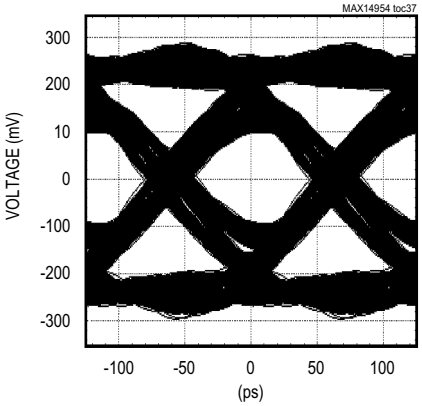

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 0, OEQ0 = 1, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 8GT/s**



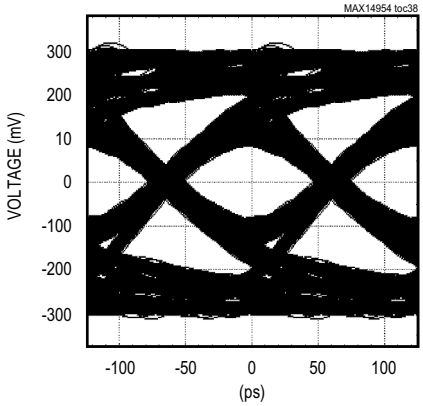
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

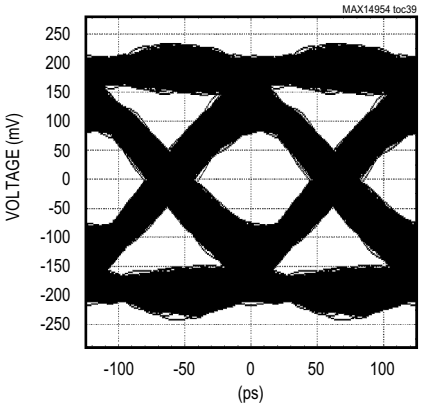
**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 1, OEQ0 = 0, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 8GT/s**



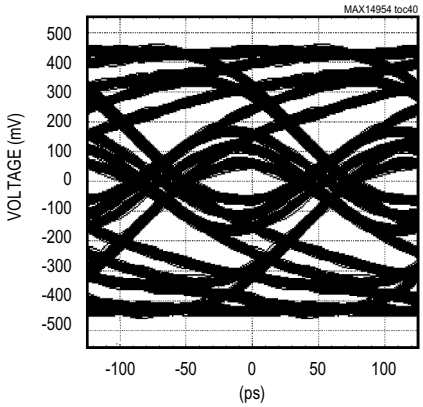

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 1, OEQ1 = 0, OEQ0 = 0, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 8GT/s**



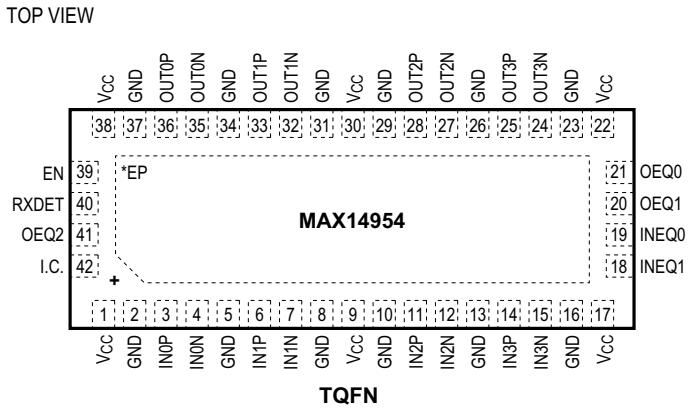

**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 1, OEQ0 = 0, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 8GT/s**




**INEQ0 = INEQ1 = 0, $V_{IN}$ = 200mV$_{P-P}$, 0EQ2 = 0, OEQ1 = 0, OEQ0 = 0, OUTPUT AFTER 19in STRIPLINE, DATA RATE = 8GT/s**



## Pin Configuration




*CONNECT EXPOSED PAD (EP) TO GND.

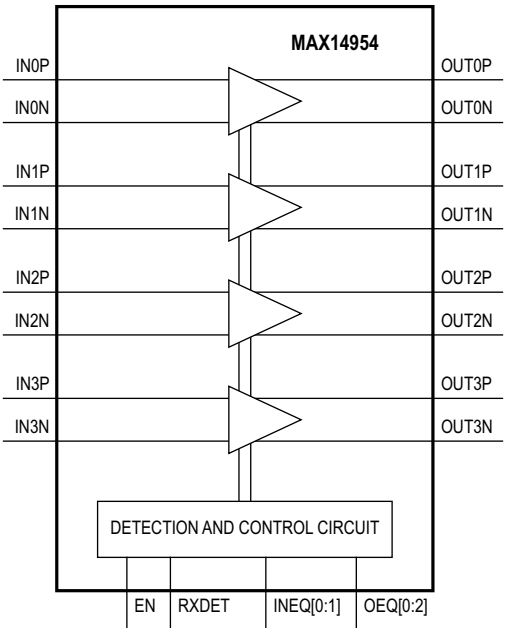
## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 9, 17, 22, 30, 38 | $V_{CC}$ | Power-Supply Input. Bypass $V_{CC}$ to GND with 1µF and 0.1µF capacitors in parallel as close as possible to the device. |
| 2, 5, 8, 10, 13, 16, 23, 26, 29, 31, 34, 37 | GND | Ground |
| 3 | IN0P | Noninverting Input, Channel 0 |
| 4 | IN0N | Inverting Input, Channel 0 |
| 6 | IN1P | Noninverting Input, Channel 1 |
| 7 | IN1N | Inverting Input, Channel 1 |
| 11 | IN2P | Noninverting Input, Channel 2 |
| 12 | IN2N | Inverting Input, Channel 2 |
| 14 | IN3P | Noninverting Input, Channel 3 |
| 15 | IN3N | Inverting Input, Channel 3 |
| 18 | INEQ1 | Input Equalization Control MSB. INEQ1 has a 250kΩ (typ) internal pulldown resistor. |
| 19 | INEQ0 | Input Equalization Control LSB. INEQ0 has a 250kΩ (typ) internal pulldown resistor. |
| 20 | OEQ1 | Output Deemphasis Control Bit 1. OEQ1 has a 250kΩ (typ) internal pulldown resistor. |
| 21 | OEQ0 | Output Deemphasis Control LSB. OEQ0 has a 250kΩ (typ) internal pulldown resistor. |
| 24 | OUT3N | Inverting Output, Channel 3 |
| 25 | OUT3P | Noninverting Output, Channel 3 |
| 27 | OUT2N | Inverting Output, Channel 2 |
| 28 | OUT2P | Noninverting Output, Channel 2 |
| 32 | OUT1N | Inverting Output, Channel 1 |
| 33 | OUT1P | Noninverting Output, Channel 1 |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 35 | OUT0N | Inverting Output, Channel 0 |
| 36 | OUT0P | Noninverting Output, Channel 0 |
| 39 | EN | Enable Input. Drive EN low for standby mode. Drive EN high for normal mode. EN has a 250kΩ (typ) internal pulldown resistor. |
| 40 | RXDET | Receiver Detection Control Bit. Drive RXDET high to initiate receiver detection. Drive RXDET low for normal mode. RXDET has a 250kΩ (typ) internal pulldown resistor. |
| 41 | OEQ2 | Output Deemphasis Control MSB. OEQ2 has a 250kΩ (typ) internal pulldown resistor. |
| 42 | I.C. | Internally Connected Pin |
| — | EP | Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance as well as good ground conductivity to the device. |

## Functional Diagram



## Detailed Description

The MAX14954 quad equalizer/redriver is designed to support Gen III (8.0GT/s), Gen II (5.0GT/s), and Gen I (2.5GT/s) PCIe data rates. The device contains four identical drivers with electrical idle/receive detect on each lane and equalization/deemphasis/preshoot to compensate for circuit-board loss. Programmable input equalization circuitry reduces deterministic jitter, improving signal integrity. The device output features a programmable output deemphasis/preshoot, permitting optimal placement of key PCIe components and longer runs of stripline, microstrip, or cable.

### Programmable Input Equalization

Programmable input equalization is controlled by two bits: INEQ1 and INEQ0 (Table 1).

### Table 1. Input Equalization

| INEQ1 | INEQ0 | INPUT EQUALIZATION (dB) |
|---|---|---|
| 0 | 0 | 5 |
| 0 | 1 | 8 |
| 1 | 0 | 12 |
| 1 | 1 | 16 |

### Programmable Output Deemphasis/Preshoot

Programmable output deemphasis is controlled by three bits: OEQ2, OEQ1, and OEQ0 for deemphasis/preshoot ratios of 0dB, 3.5dB, 6dB, and 9dB (Table 2).

### Table 2. Output Deemphasis/Preshoot

| OEQ2 | OEQ1 | OEQ0 | OUTPUT DEEMPHASIS/ PRESHOOT RATIO (dB) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 3.5 |
| 0 | 1 | 0 | 6 |
| 0 | 1 | 1 | 6 (peak-to-peak swing is 1.2V) |
| 1 | 0 | 0 | 3.5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 9 (peak-to-peak swing is 0.9V) |
| 1 | 1 | 1 | 9 (peak-to-peak swing is 1.0V) |

### Receiver Detection

The device features receiver detection on each channel. Upon initial power-up, if EN is high, receiver detection initializes. Receiver detection can also be initiated on a rising or falling edge of the RXDET input when EN is high. During this time, the device remains in low-power standby mode and the outputs are disabled, despite the logic-high state of EN. Until a channel has detected a receiver, the receiver detection repeats indefinitely on each channel. If a channel detects a receiver, the other channels are limited to retries for 100ms (typ). For each channel upon receiver detection, input common-mode termination and electrical idle detection are enabled (Table 3).

### Electrical Idle Detection

The device features electrical idle detection to prevent unwanted noise from being redriven at the output. When the device detects that the differential input has fallen below the $V_{TX\text{-}IDLE\text{-}THRESH}$ low limit, it squelches the output. For differential input signals that are above $V_{TX\text{-}IDLE\text{-}THRESH}$ high limit, the device turns on the output and redrives the signal. There is little variation in output common-mode voltage between electrical idle and redrive modes.

### Table 3. Receiver Detection Input Function

| RXDET | EN | DESCRIPTION |
|---|---|---|
| X | 0 | Receiver detection is inactive. |
| X | 1 | Following a rising edge of the EN signal, indefinite retries until receiver detects at least one channel. Retries stop after 100ms (typ) if any channel receiver is detected. |
| Rising/falling edge | 1 | Initiates receiver detection. |

*X = Don't care.*

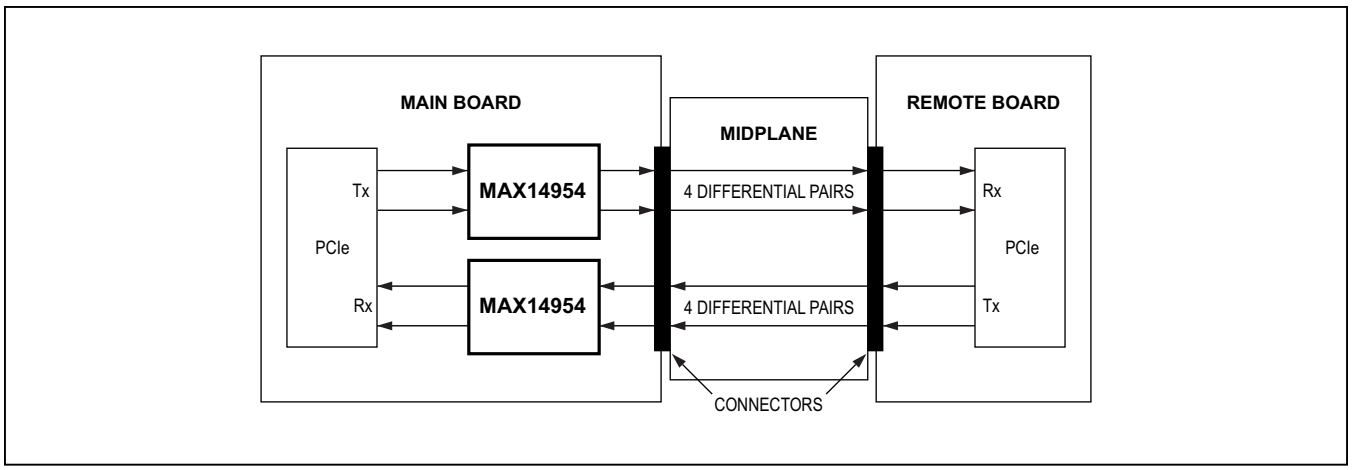



*Figure 2. Typical Application Diagram*

## Applications Information

Figure 2 shows a typical application with two MAX14954s, both residing on the main board with input and output equalization set individually for optimal performance. The MAX14954 Rx equalizer is set to receive a degraded signal coming from a remote board through two sets of connectors and a midplane stripline. The output of the Rx section has little or no output equalization. The Tx section takes a high-quality signal and provides boost to the output (deemphasis).

### Layout

Circuit-board layout and design can significantly affect the performance of the device. Use good, high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on data signals. Power-supply decoupling should also be placed as close as possible to $V_{CC}$. Always connect $V_{CC}$ to a power plane. It is recommended to run receive and transmit signals on different layers to minimize crosstalk.

### Exposed-Pad Package

The exposed-pad, 42-pin TQFN package incorporates features that provide a very low-thermal-resistance path for heat removal from the device. The exposed pad on the device must be soldered to the circuit-board ground plane for proper thermal performance and good ground connectivity. For more information on exposed-pad packages, refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

### Power-Supply Sequencing

**Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.**

Proper power-supply sequencing is recommended for all devices. Always apply GND then $V_{CC}$ before applying signals, especially if the signal is not current limited.

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX14954ETO+ | -40°C to +85°C | 42 TQFN-EP* |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

**EP = Exposed pad.*

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 42 TQFN-EP | T423590+1 | 21-0181 | 90-0078 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 11/12 | Initial release | — |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

*Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.*

Maxim Integrated and the Maxim Integrated logo are trademarks of Maxim Integrated Products, Inc. © 2012 Maxim Integrated Products, Inc. 