19-1214; Rev 1; 1/98

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

MAXIM

Digitally Adjustable LCD Bias Supplies

General Description

The MAX1620/MAX1621 convert a 1.8V to 20V battery voltage to a positive or negative LCD backplane bias voltage. Backplane bias voltage can be automatically disabled when the display logic voltage is removed, protecting the display. These devices use very little PC board area, come in ultra-small QSOP packages, and require only small, low-profile external components.

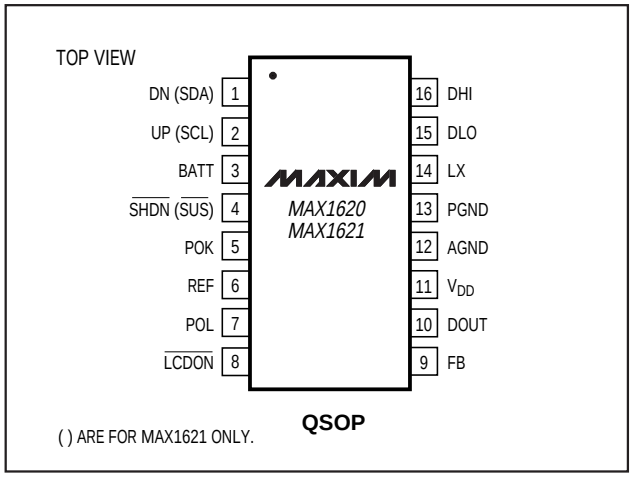
Output voltage can be set to a desired positive or negative voltage range with external resistors, and adjusted over that range with the on-board digital-to-analog converter (DAC) or with a potentiometer. The MAX1620/MAX1621 include a 5-bit DAC, allowing digital software control of the bias voltage. The MAX1620 uses up/down digital signaling to adjust the DAC, and the MAX1621 uses the System Management Bus (SMBus™) 2-wire serial interface.

These devices use a low-cost, external, N-channel MOSFET power switch or NPN transistor, and can be configured for positive or negative output voltages. Operating current is a low 150µA, typically provided from a display's logic supply of 3.0V to 5.5V. The MAX1620/MAX1621 are available in a 16-pin QSOP package.

Applications

Notebook Computers
Palmtop Computers
Personal Digital Assistants
Portable Data-Collection Terminals

Pin Configuration



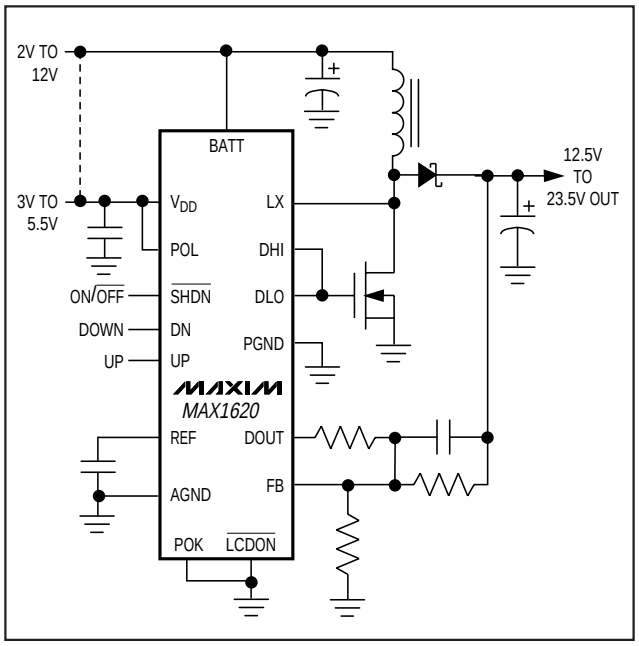
Features

- **1.8V to 20V Battery Input Voltage**
- **Automatic Disable when Display Logic is Shut Down**
- **Extremely Small QSOP Package**
- **32-Level Internal DAC**
- **SMBus Serial Interface (MAX1621)**
- **Positive or Negative Output Voltage**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1620EEE	-40°C to +85°C	16 QSOP
MAX1621EEE	-40°C to +85°C	16 QSOP

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to 6V
PGND to AGND .....±0.3V
BATT, LX, $\overline{LCDON}$ to AGND .....-0.3V to 30V
DHI, DLO to PGND .....-0.3V to (V_{DD} + 0.3V)
DOUT, FB, POL, POK, REF to AGND .....-0.3V to (V_{DD} + 0.3V)
UP, DN, $\overline{SHDN}$ to AGND .....-0.3V to 6V
SCL, SDA, $\overline{SUS}$ to AGND .....-0.3V to 6V
I_{DHI} 60mA
I_{DLO} .....-30mA
$I_{\overline{LCDON}}$ .....-10mA
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range
MAX1620EEE/MAX1621EEE .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{BATT} = 10V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING REGULATOR					
V_{DD} Operating Range		3.0		5.5	V
V_{DD} Supply Current	Operating mode, output in regulation, V_{DD} = 5.5V		150	250	µA
	Shutdown mode, $V_{\overline{SHDN}}$ = V_{DD}, V_{DD} = 5.5V		9	20	
Positive Output Voltage				27	V
Negative Output Voltage				-27	V
Undervoltage Lockout Threshold (Note 1)		1.5		2.8	V
BATT Input Current	BATT = 12V, operating mode		13	20	µA
	BATT = 12V, shutdown mode			1	
LX Input Current	LX = 12V, operating mode		13	20	µA
	LX = 12V, shutdown mode			1	
BATT Operating Range (Note 2)		1.8		20	V
Microsecond-Volt Time Constant (k-factor)	1.8V ≤ BATT ≤ 20V, T_A = +25°C		20		µs-V
	4V ≤ BATT ≤ 12V, T_A = 0°C to +85°C	16.5		23.5	
On-Resistance (DLO, DHI)	V_{DD} = 4.5V		7		Ω
	V_{DD} = 3.0V		14		
DHI Output Current (Note 3)	V_{DD} = 5V		50		mA
DLO Output Current (Note 3)	V_{DD} = 5V		-25		mA
FB Regulation Voltage	POL = V_{DD}, 3.0V ≤ V_{DD} ≤ 5.5V	1.46	1.5	1.53	V
	POL = AGND, 3.0V ≤ V_{DD} ≤ 5.5V	-8	0	8	mV
FB Input Current (Note 3)	FB = REF + 100mV	-20		10	nA
	FB = -50mV	-10		85	
$\overline{LCDON}$ Low, Sinking Current	$V_{\overline{LCDON}}$ = 0.4V, POK = 1.017V	-2	-6		mA
$\overline{LCDON}$ High, Leakage Current	$V_{\overline{LCDON}}$ = 28V, POK = 0.967V			1	µA
POK Threshold Voltage	Voltage on POK rising	0.967	0.992	1.017	V
POK Hysteresis			12		mV
REFERENCE AND DAC OUTPUT					
REF Voltage	No load	1.47	1.5	1.53	V
REF Load Regulation	0µA ≤ I_{REF} ≤ 25mA		3	10	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, V_{BATT} = 10V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DOUT Maximum Output Voltage (Note 3)	0µA ≤ I_{DOUT} ≤ 40µA	REF - 0.02		REF + 0.02	V
DOUT Minimum Output Voltage (Note 3)	-20µA ≤ I_{DOUT} ≤ 0µA	0		0.007	V
DOUT Resolution	48.39mV step size	5			Bits
DOUT Differential Nonlinearity	Guaranteed monotonic			±1	LSB
DIGITAL INPUTS AND OUTPUTS					
UP, DN, $\overline{SHDN}$, POL Input High Voltage	3.0V ≤ V_{DD} ≤ 3.6V	1.4			V
	V_{DD} = 5.5V	2.3			
UP, DN, $\overline{SHDN}$, POL Input Low Voltage				0.6	V
UP, DN, $\overline{SHDN}$, POL Input Leakage Current	V_{IN} = 0V or V_{IN} = V_{DD}			±1	µA
SCL, SDA, $\overline{SUS}$ Input High Voltage	3.0V ≤ V_{DD} ≤ 3.6V	1.4			V
	V_{DD} = 5.5V	2.3			
SCL, SDA, $\overline{SUS}$ Input Low Voltage				0.6	V
SCL, SDA, $\overline{SUS}$ Input Leakage Current	V_{IN} = 0V or V_{IN} = V_{DD}			±1	µA
SDA Output Low Voltage	I_{SDA} = -6mA			0.4	V

TIMING CHARACTERISTICS

(**T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAX1620 (Figure 1)						
Pulse Width High (UP, DN)	t_1		1			µs
Pulse Width Low (UP, DN)	t_2		1			µs
Pulse Separation (UP, DN)	t_3		1			µs
Counter Reset Time	t_4		1			µs
MAX1621 (Figures 2 and 3)						
SDA to SCL Data-Setup Time	$t_{SU:DAT}$		500			ns
SCL to SDA Data-Hold Time	$t_{HD:DAT}$	(Note 4)	0			ns
SCL/SDA Rise Time	t_R	(Note 4)			1	µs
SCL/SDA Fall Time	t_F	(Note 4)			300	ns
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
Start Condition SCL to SDA Setup Time	$t_{SU:STA}$		4.7			µs
Start Condition SDA to SCL Hold Time	$t_{HD:STA}$		4			µs
Stop Condition SCL_ to SDA_ Setup Time	$t_{SU:STO}$		4			µs
SCL Falling Edge to SDA Valid Master Clocking in Data	t_{DV}				1	µs

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{BATT} = 10V, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted. Limits over this temperature range are guaranteed by design.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING REGULATOR					
V_{DD} Operating Range		3.0		5.5	V
V_{DD} Supply Current	Operating mode, output in regulation		150	250	µA
	Shutdown mode, $V_{\overline{SHDN}} = V_{DD}$			20	
Positive Output Voltage				27	V
Negative Output Voltage				-27	V
Undervoltage Lockout Threshold (Note 1)		1.5		2.8	V
BATT Operating Range (Note 2)		1.8		20	V
Microsecond-Volt Time Constant (k-factor)	4V ≤ BATT ≤ 12V	16		24	µs-V
FB Regulation Voltage	POL = V_{DD}, 3.0V ≤ V_{DD} ≤ 5.5V	1.44	1.5	1.56	V
	POL = AGND, 3.0V ≤ V_{DD} ≤ 5.5V	-10	0	10	mV
FB Input Current (Note 3)	FB = REF + 100mV	-30		10	nA
	FB = 0V - 50mV	-10		120	
POK Threshold Voltage	Voltage on POK rising	0.957	0.992	1.027	V
REFERENCE AND OUTPUT					
REF Voltage	No load	1.44	1.5	1.56	V
REF Load Regulation	0µA ≤ I_{REF} ≤ 25µA		5	10	mV
DOUT Maximum Output Voltage (Note 3)	0µA ≤ I_{DOUT} ≤ 40µA	REF - 0.02		REF + 0.02	V
DOUT Minimum Output Voltage (Note 3)	-20µA ≤ I_{DOUT} ≤ 0µA	0		0.01	V
DOUT Differential Nonlinearity	Guaranteed monotonic			±1	LSB
DIGITAL INPUTS AND OUTPUTS					
UP, DN, $\overline{SHDN}$, POL Input High Voltage	3.0V ≤ V_{DD} ≤ 3.6V	1.4			V
	V_{DD} = 5.5V	2.3			
UP, DN, $\overline{SHDN}$, POL Input Low Voltage				0.6	V
SCL, SDA, $\overline{SUS}$ Input High Voltage	3.0V ≤ V_{DD} ≤ 3.6V	1.4			V
	V_{DD} = 5.5V	2.3			
SCL, SDA, $\overline{SUS}$ Input Low Voltage				0.6	V
SDA Output Low Voltage	I_{SDA} = -6mA			0.4	V

TIMING CHARACTERISTICS

(V_{DD} = 3.3V, V_{BATT} = 10V, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted. Limits over this temperature range are guaranteed by design.)

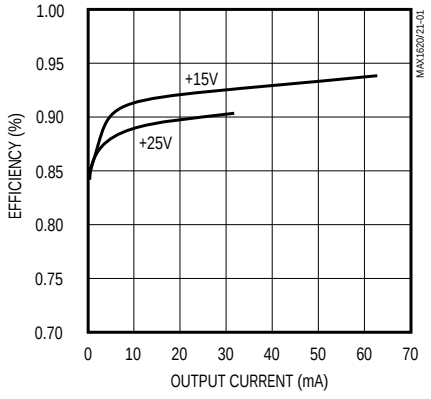
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAX1620 (Figure 1)						
Pulse Width High (UP, DN)	t_1		1			µs
Pulse Width Low (UP, DN)	t_2		1			µs
Pulse Separation (UP, DN)	t_3		1			µs
Counter Reset Time	t_4		1			µs
MAX1621 (Figures 2 and 3)						
SDA_ to SCL_ Data-Setup Time	$t_{SU:DAT}$		500			ns
SCL_ to SDA_ Data-Hold Time	$t_{HD:DAT}$		0			ns
SCL/SDA Rise Time	t_R				1	µs
SCL/SDA Fall Time	t_F				300	ns
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
Start Condition SCL_ to SDA_ Setup Time	$t_{SU:STA}$		4.7			µs
Start Condition SDA_ to SCL_ Hold Time	$t_{HD:STA}$		4			µs
Stop Condition SCL_ to SDA_ Setup Time	$t_{SU:STO}$		4			µs
SCL Falling Time to SDA Valid Master Clocking in Data	t_{DV}				1	µs

Note 1: The setting in the DAC is guaranteed to remain valid as long as V_{DD} is greater than the UVLO threshold.
Note 2: BATT Operating Range is guaranteed by the Microsecond-Volt Time Constant specification.
Note 3: Current sourced from a pin is denoted as positive current. Current sunk into a pin is denoted as negative current.
Note 4: Guaranteed by design.

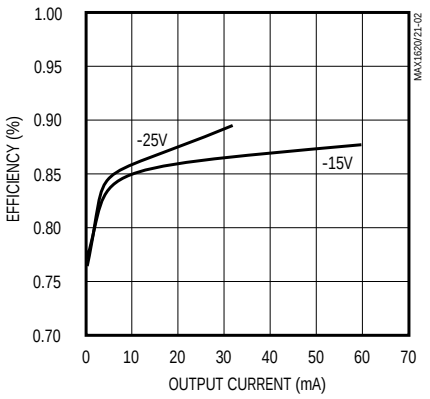
Typical Operating Characteristics

(V_{DD} = 5V, V_{BATT} = 10V, L1 = 100µH, T_A = +25°C, unless otherwise noted.)

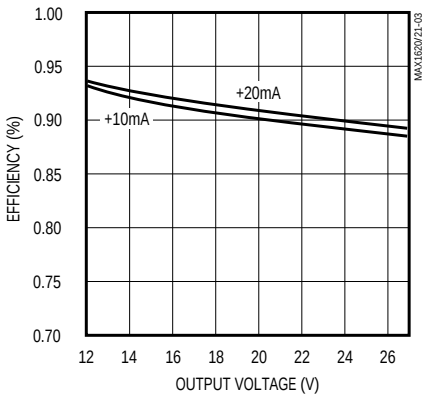
EFFICIENCY vs. OUTPUT CURRENT



EFFICIENCY vs. OUTPUT CURRENT



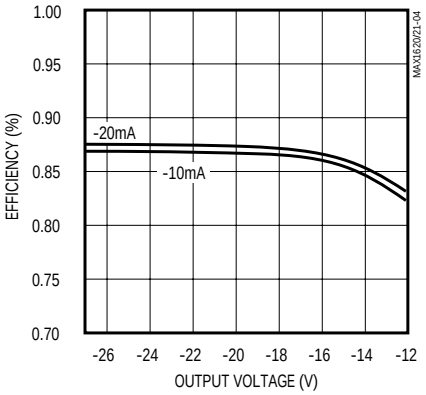
EFFICIENCY vs. OUTPUT VOLTAGE



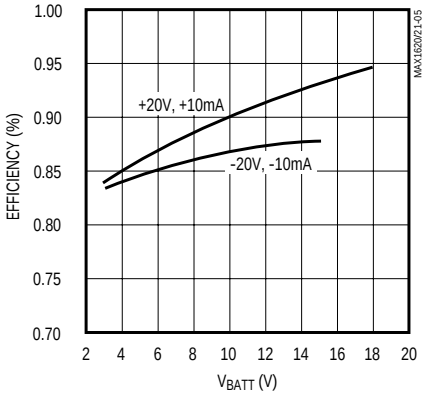
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{BATT} = 10V, L1 = 100µH, T_A = +25°C, unless otherwise noted.)

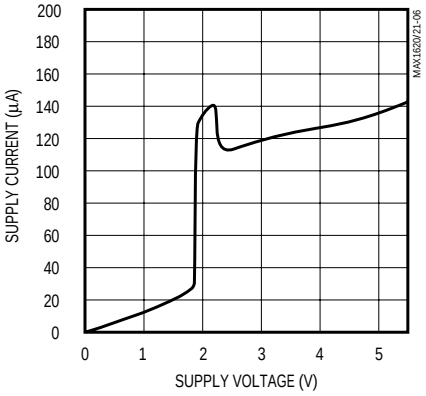
EFFICIENCY vs. OUTPUT VOLTAGE



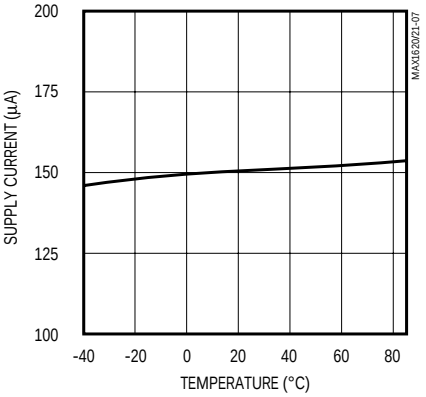
EFFICIENCY vs. V_{BATT}



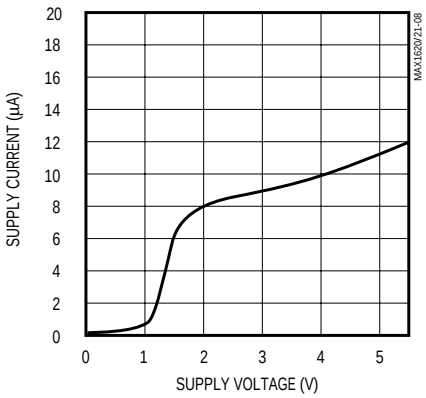
SUPPLY CURRENT vs. SUPPLY VOLTAGE



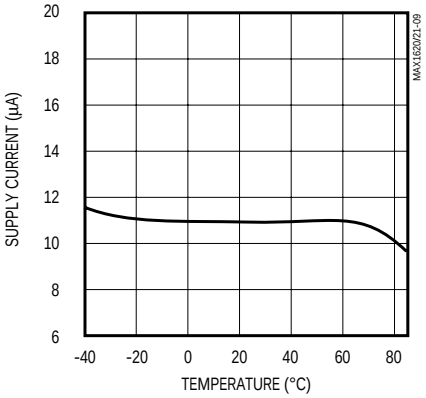
SUPPLY CURRENT vs. TEMPERATURE



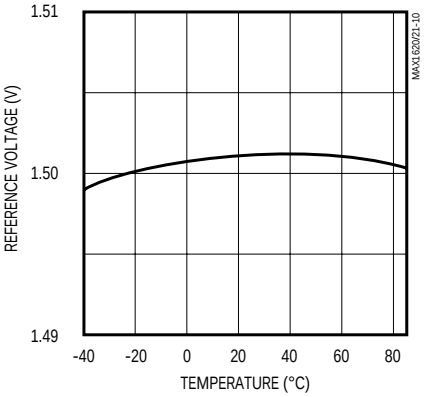
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



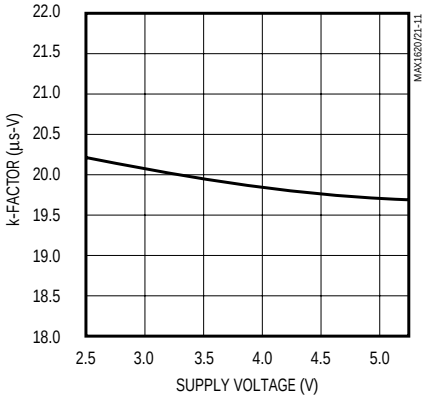
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



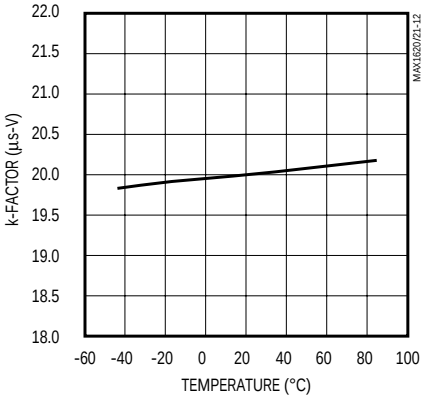
REFERENCE VOLTAGE vs. TEMPERATURE



k-FACTOR vs. SUPPLY VOLTAGE



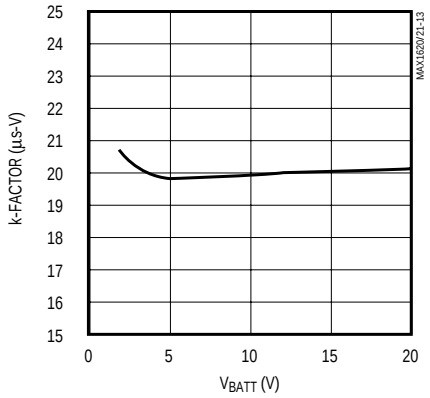
k-FACTOR vs. TEMPERATURE



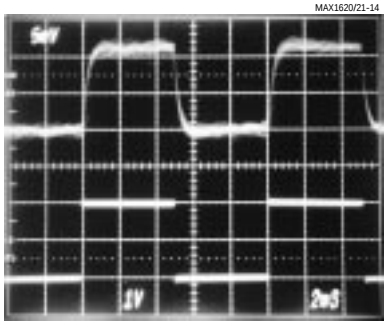
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{BATT} = 10V L1 = 100µH, V_{OUT} = 22.3V, T_A = +25°C, unless otherwise noted.)

k-FACTOR vs. V_{BATT}



LINE-TRANSIENT RESPONSE



V_{OUT}
(AC COUPLED, 5mV/div)

5.3V

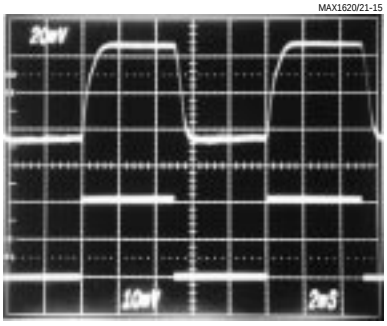
V_{DD}
(AC COUPLED, 1V/div)

3.3V

2ms/div

I_{LOAD} = 20mA

LOAD-TRANSIENT RESPONSE



V_{OUT}
(AC COUPLED, 20mV/div)

20mA

I_{OUT}
(10mA/div)

0

2ms/div

I_{LOAD} = 0mA TO 20mA

Pin Description

PIN		NAME	FUNCTION
MAX1620	MAX1621		
1	—	DN	Logic-Level Input. A rising edge on DN decreases $\lvert V_{OUT} \rvert$. UP = DN = high resets the counter to mid-scale.
—	1	SDA	System Management Bus Serial-Data Input and Open-Drain Output
2	—	UP	Logic-Level Input. A rising edge on UP increases $\lvert V_{OUT} \rvert$. UP = DN = high resets the counter to mid-scale.
—	2	SCL	System Management Bus Serial-Clock Input
3	3	BATT	Battery Voltage-Sense Input
4	—	$\overline{SHDN}$	Logic-Level Shutdown Input (active-low)
—	4	$\overline{SUS}$	System Management Bus Suspend-Mode Input (active-low)
5	5	POK	Power OK Voltage-Sense Input, 1V threshold
6	6	REF	Reference Voltage Output. Bypass REF with 0.1µF to AGND.
7	7	POL	Logic-Level Input. POL selects output voltage polarity: high = positive boost, low = negative boost.
8	8	$\overline{LCDON}$	Open-Drain Output. $\overline{LCDON}$ controls LCD with external PNP.
9	9	FB	Feedback Voltage Input
10	10	DOUT	DAC Output Voltage
11	11	V_{DD}	IC Input Supply, 3.0V to 5.5V
12	12	AGND	Analog Ground
13	13	PGND	Power Ground
14	14	LX	Switching-Voltage Sense Input
15	15	DLO	External Transistor Drive, Low
16	16	DHI	External Transistor Drive, High

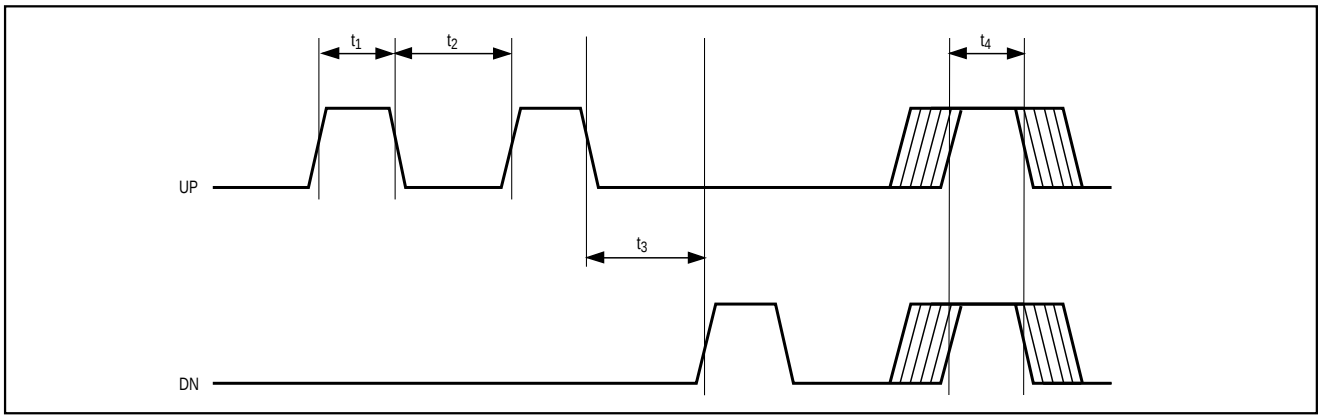


Figure 1. MAX1620 UP and DN Signal Timing

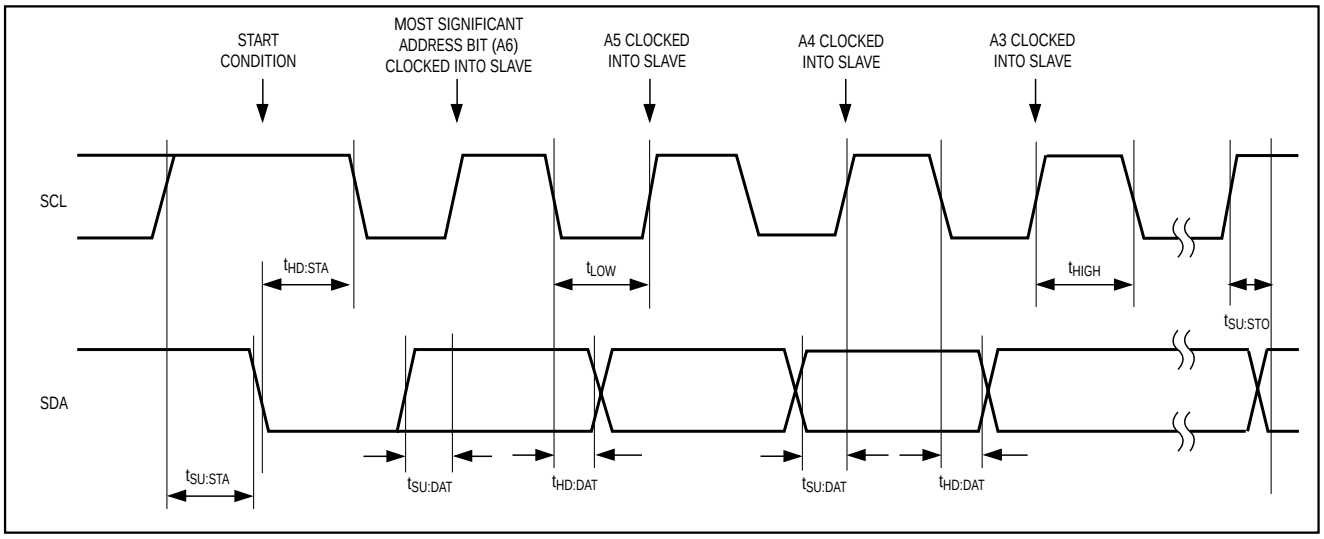


Figure 2. MAX1621 SMB Serial-Interface Timing—Address

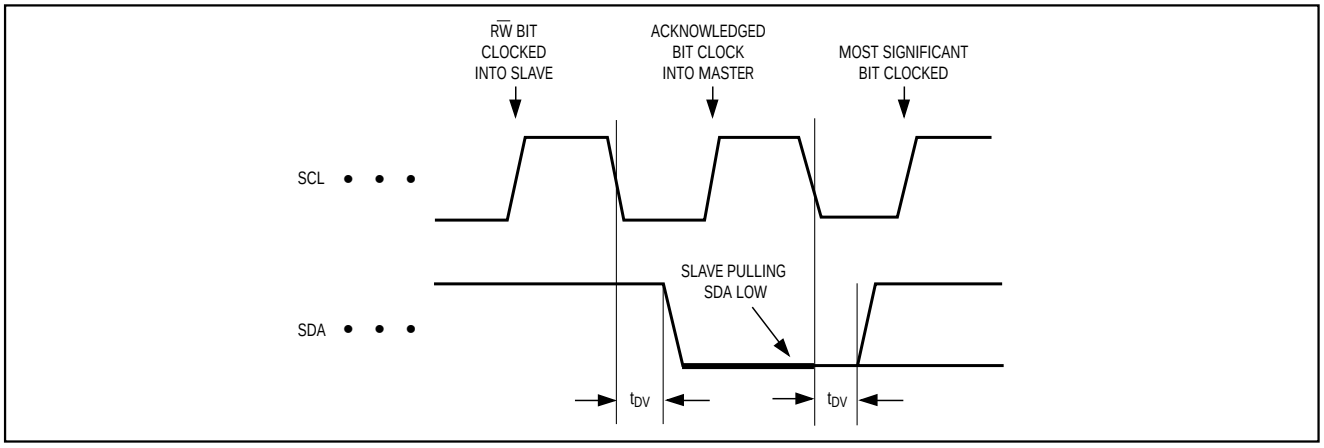


Figure 3. MAX1621 SMB Serial-Interface Timing—Acknowledge

Detailed Description

The MAX1620/MAX1621 are step-up power controllers that drive an external N-channel FET or NPN transistor to convert power from a 1.8V to 20V battery to a higher positive or negative voltage. They are configured as negative-output, inverting power controllers with one additional diode and one additional capacitor. Either configuration's output voltage can be adjusted with external resistors, or digitally adjusted with an internal digital-to-analog converter (DAC). The MAX1620 uses pin-defined controls for the DAC, while the MAX1621 communicates with the DAC via the SMBus™ interface.

Operating Principle

The MAX1620/MAX1621 operate in discontinuous-conduction mode (where the inductor current ramps to zero by the end of each switching cycle) and with a constant peak current, without requiring a current-sense resistor. Switch on-time is inversely proportional to the input voltage V_{BATT} by a microsecond-volt constant, or k-factor, of 20µs-V (e.g., for V_{BATT} = 10V, on-time = 2µs).

For an ideal boost converter operating in discontinuous-conduction mode (no power losses), output current is proportional to input voltage and peak inductor current:

$$I_{OUT} = \frac{1}{2} \times I_{PK} \times V_{BATT} / V_{OUT}$$

I_{PK} is proportional to on-time (t_{ON}), which, for these parts, is determined by the k-factor:

$$I_{PK} = \text{k-factor} / L$$

Discontinuous conduction is detected by monitoring the LX node voltage. When the inductor's energy is completely delivered, the LX node voltage snaps back to the BATT voltage. When this crossing is sensed, another pulse is issued if the output is still out of regulation.

Positive Output Voltage

To select a positive output voltage, tie the polarity pin (POL) to V_{DD} and use the typical boost topology shown in Figure 4. FB regulation voltage is 1.5V. For optimum stability, V_{OUT} should be greater than 1.1 (V_{BATT}).

Negative Output Voltage

To select a negative output voltage, tie POL to GND (Figure 5). In this configuration, the internal error amplifier's output is inverted to provide the correct feedback polarity. FB regulation voltage is 0V. D1, D2, C4, and C5 form an inverting charge pump to generate the negative voltage. This allows application of the positive boost switching topology to negative output voltages.

The negative output circuit has two possible connections. In the standard connection, D1's cathode is connected to BATT. This connection features the best output ripple performance, but $|V_{OUT}|$ must be limited to no more than 27V - 1.1(V_{BATT}). If a larger negative voltage is needed, an alternative connection allows a maximum negative output of -27V, but with the additional constraint that $|V_{OUT}| > 1.1V_{BATT}$. To use the alternative circuit, connect D1's cathode to ground rather than BATT (Figure 6). Increase C4 to 2.2µF to improve output ripple performance.

The negative charge pump limits the output current to the charge transferred each cycle multiplied by the

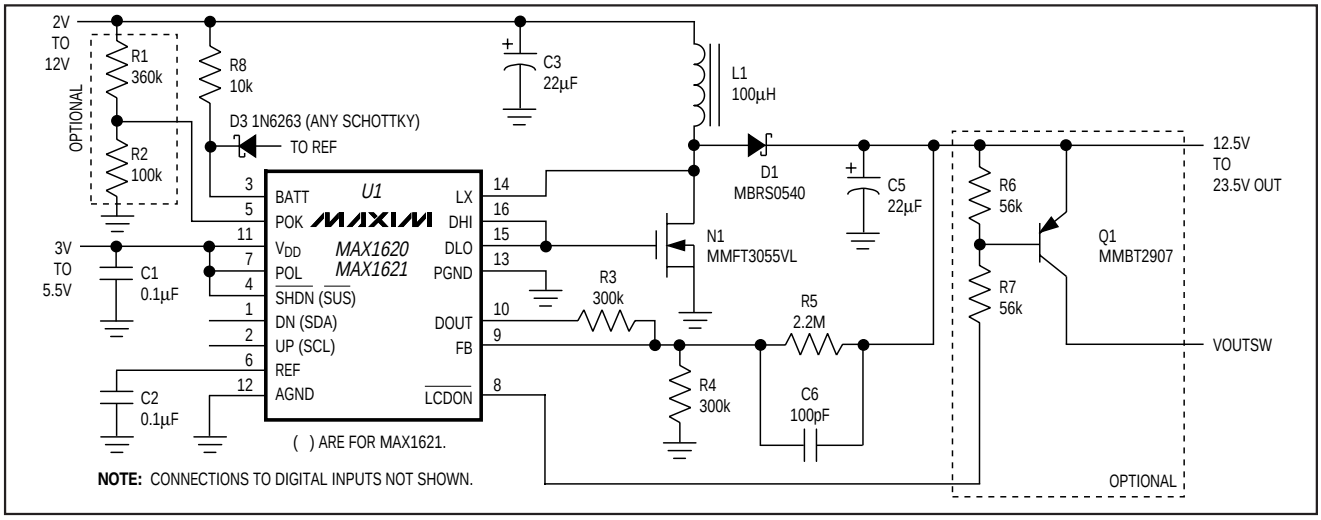


Figure 4. Typical Operating Circuit—Positive Output

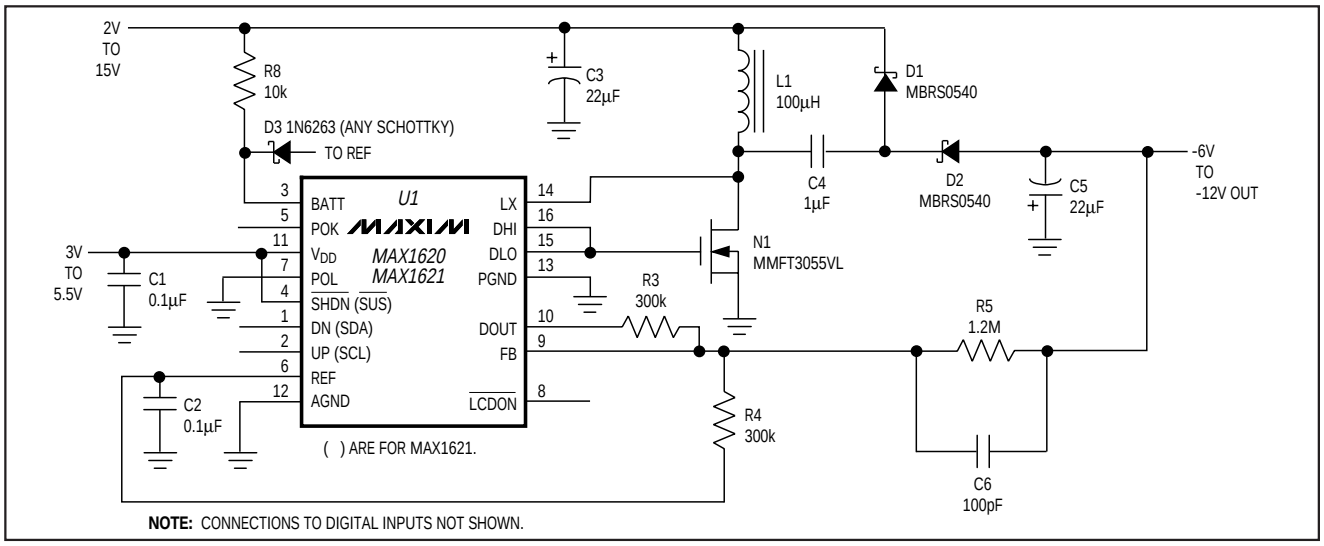


Figure 5. Typical Operating Circuit—Negative Output

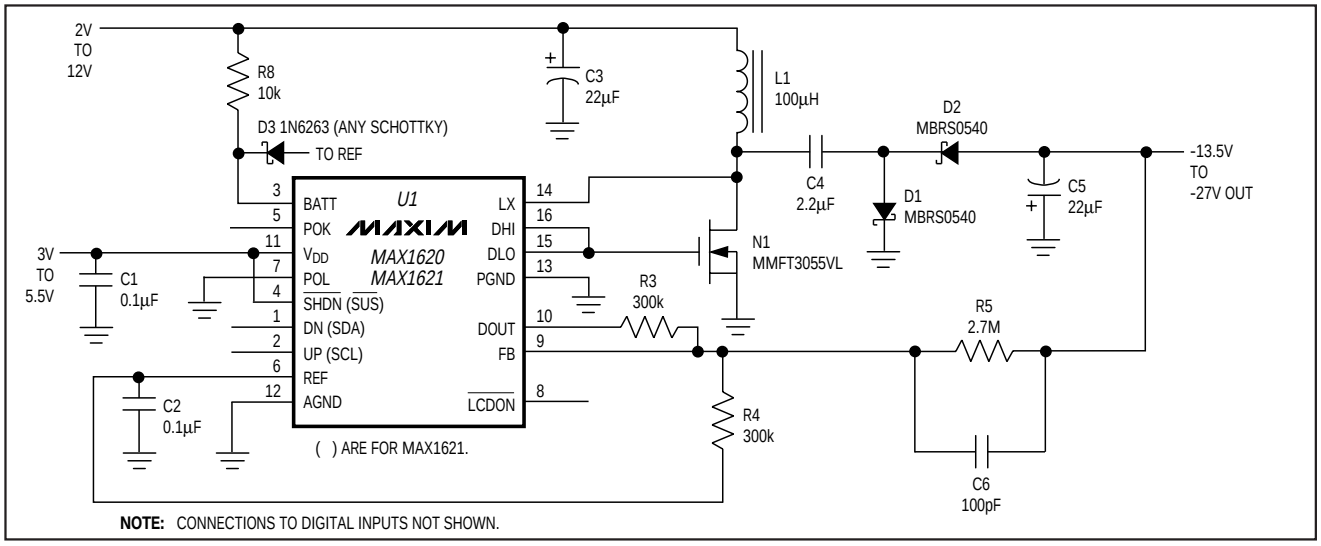


Figure 6. Alternative Negative Output—Maximum Voltage

maximum switching frequency. The following equation represents the output current for the ideal case (no power losses) of Figure 5:

$$I_{OUT} = \frac{1}{2} \times (k\text{-factor} / L) \times V_{BATT} / (V_{BATT} + V_{OUT})$$

This means that a higher peak current is required to achieve the same output current in the negative output circuit as in the positive output circuit.

The output current for Figure 6 uses the same current equation as the positive boost.

Output Voltage Control

The output voltage is set with a voltage divider to the feedback pin (FB). For a positive output, the divider is referred to GND; for a negative output, the divider is referred to REF.

Output voltage can be adjusted with an internal DAC summing current into FB through an external resistor. The 5-bit DAC is controlled with a user-programmable up/down counter. On power-up or after a reset, the counter sets the DAC output to 10000 binary, or half-scale.

The MAX1620 controls the DAC counter with the UP and DN pins. A rising edge on UP increases $|V_{OUT}|$ by decrementing the counter and decreasing the DAC output voltage one step; a rising edge on DN decreases $|V_{OUT}|$ by incrementing the counter and increasing the DAC output voltage one step. Holding both UP and DN high resets the counter to half-scale. The counter will **not** roll over at either the FS or ZERO code. The control direction of UP and DN reverses for a negative output, to maintain the same control direction of the output voltage in absolute magnitude.

The MAX1621 controls the counter to the DAC through the SMBus interface. The counter is treated as a 5-bit register and resets on power-up. The setting in the DAC is guaranteed to remain valid as long as V_{DD} is greater than the UVLO threshold (see Note 1 in the *Electrical Characteristics*).

The MAX1620/MAX1621's open-drain DMOSFET ($\overline{LCDON}$) can be used to disconnect the LCD panel from the positive bias voltage with an external transistor. The FET turns off ($\overline{LCDON}$ = float) if power-OK voltage (POK) falls below 1V. In the MAX1621, $\overline{LCDON}$ can also be controlled by the SMB command. $\overline{LCDON}$ cannot switch negative output voltages.

To prevent uncontrolled boosting when the output is disconnected, the feedback resistors must sense the boosted voltage rather than the output of the $\overline{LCDON}$ switch (Figure 4).

Shutdown Mode

The MAX1620 shuts down when the $\overline{SHDN}$ pin is low. The internal reference and biasing circuitry turn off, and the supply current drops to 9µA. In shutdown, DOUT = 0V and $\overline{LCDON}$ floats. UP/DN are ignored to preserve the DAC state for the MAX1620. Tie unused logic inputs to AGND for lowest operating current.

The MAX1621 can be shut down using the SMBus interface (Table 2).

Reset Modes

If the MAX1620 is not in shutdown mode, the DAC can be reset to mid-scale by holding UP and DN high. Mid-scale is 16 steps from the minimum DAC output and 15 steps from the maximum.

The MAX1620/MAX1621 reset the DAC counter to mid-scale at power-up or when V_{DD} is below the undervoltage lockout threshold of 2.2V (typ).

MAX1621 Digital Interface

A single byte of data written over the Intel SMBus controls the MAX1621. Figures 7 and 8 show example single-byte writes. The MAX1621 contains two 2-bit registers for storing configuration data, and one register for the 5-bit DAC data. Tables 1 and 2 describe the data format for the configuration registers. The MAX1621 responds only to its own address (0101100 binary).

The REGSEL bit addresses the configuration registers. REGSEL = 0 for the $\overline{SUS}$ register; REGSEL = 1 for the OPR register. Each configuration register consists of a $\overline{SHDN}$ bit and an LCDON bit. One of the two configuration registers is always active. The state of the $\overline{SUS}$ pin determines the active register. The OPR register is active with $\overline{SUS}$ = high. The $\overline{SUS}$ register is active with $\overline{SUS}$ = low.

Each byte written to the MAX1621 updates the DAC register. DAC data is preserved in shutdown and when toggling between configuration registers. Since there is only one DAC register, $\overline{SUS}$ cannot be used to toggle between two DAC codes.

Status information can be read from the MAX1621 using the SMBus read-byte protocol. Figure 9 shows an example status read and Table 3 describes the status-information format.

During shutdown (SUS = 1 and OPR-SHDN = 0, or SUS = 0 and SUS-SHDN = 0), the MAX1621 serial interface remains fully functional and can be used to set either the OPR-SHDN or SUS-SHDN bits to return the MAX1621 to its normal operational state.

Separate/Same Power for L1 and V_{DD}

Separate voltage sources can supply the inductor (L1) and the IC (V_{DD}). This allows operation from low-voltage batteries as well as high-voltage sources because chip bias (150µA) is provided by a logic supply (3V to 5.5V) while output power is sourced directly from the battery to L1. Conversely, L1 and V_{DD} can also be supplied from one supply if it remains with V_{DD}'s operating limits (3V to 5.5V). If L1 and V_{DD} are fed from the same voltage, D3 and R8 (Figures 4, 5, 6, and 10) can be omitted, and BATT may be connected directly to V_{DD}.

Table 1. MAX1621 Configuration Byte with REGSEL = 0 (write to $\overline{SUS}$ register)

BIT	NAME	POR STATE*	DESCRIPTION
7	REGSEL	—	Register Select. A zero in this bit writes the next two bits into the $\overline{SUS}$ register and the remaining five bits into the DAC register (Figure 7).
6	$\overline{SUS}$-$\overline{SHDN}$	0	With $\overline{SUS}$ = low, 1 = operating, and 0 = shutdown.
5	$\overline{SUS}$-LCDON	0	With $\overline{SUS}$ = low, 1 = LCD on, and 0 = LCD off.
4 3 2 1 0	D4 (MSB) D3 D2 D1 D0	1 0 0 0 0	DAC Input Data

**Initial register state after power-up.*

Table 2. MAX1621 Configuration Byte with REGSEL = 1 (write to OPR register)

BIT	NAME	POR STATE*	DESCRIPTION
7	REGSEL	—	Register Select. A one in this bit writes the next two bits into the OPR register and the remaining five bits into the DAC register (Figure 7).
6	OPR-$\overline{SHDN}$	1	With $\overline{SUS}$ = high, 1 = operating, and 0 = shutdown.
5	OPR-LCDON	1	With $\overline{SUS}$ = high, 1 = LCD on, and 0 = LCD off.
4 3 2 1 0	D4 (MSB) D3 D2 D1 D0	1 0 0 0 0	DAC Input Data

**Initial register state after power-up.*

Table 3. MAX1621 Status Bits

BIT	NAME	DESCRIPTION
7	POK	If the voltage applied to POK is greater than 0.992V and the MAX1621 is not shut down, this bit returns 1; otherwise, it returns 0.
6	—	Reserved for future use.
5	—	Reserved for future use.
4 3 2 1 0	D4 (MSB) D3 D2 D1 D0	DAC Register Data

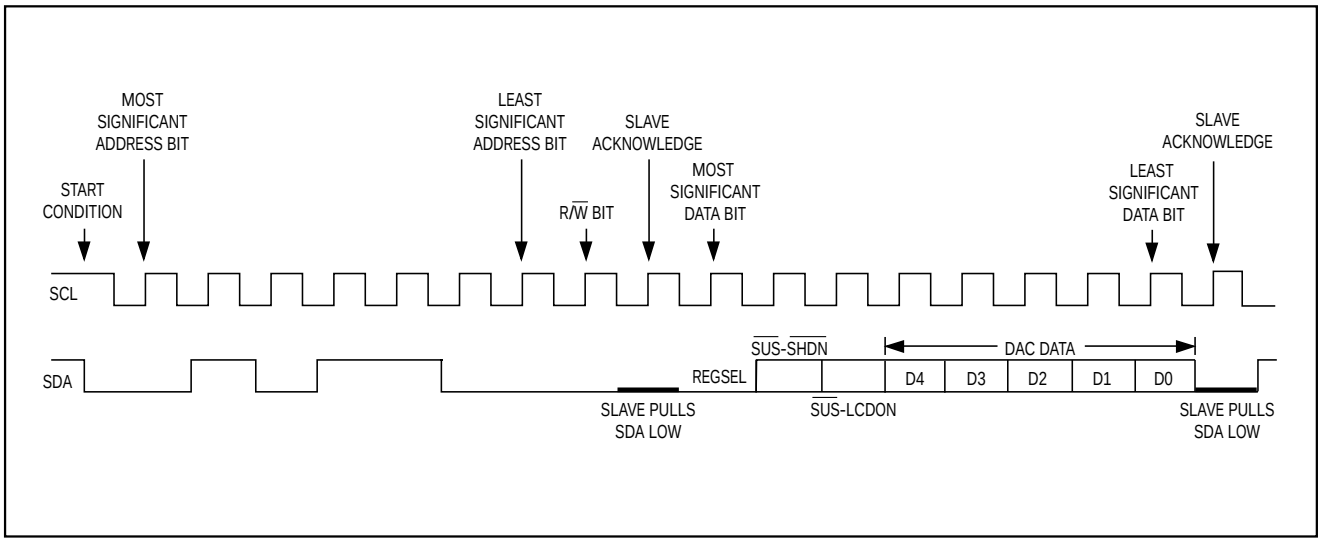


Figure 7. MAX1621 Serial-Interface Single-Byte Write Example (REGSEL = 0)

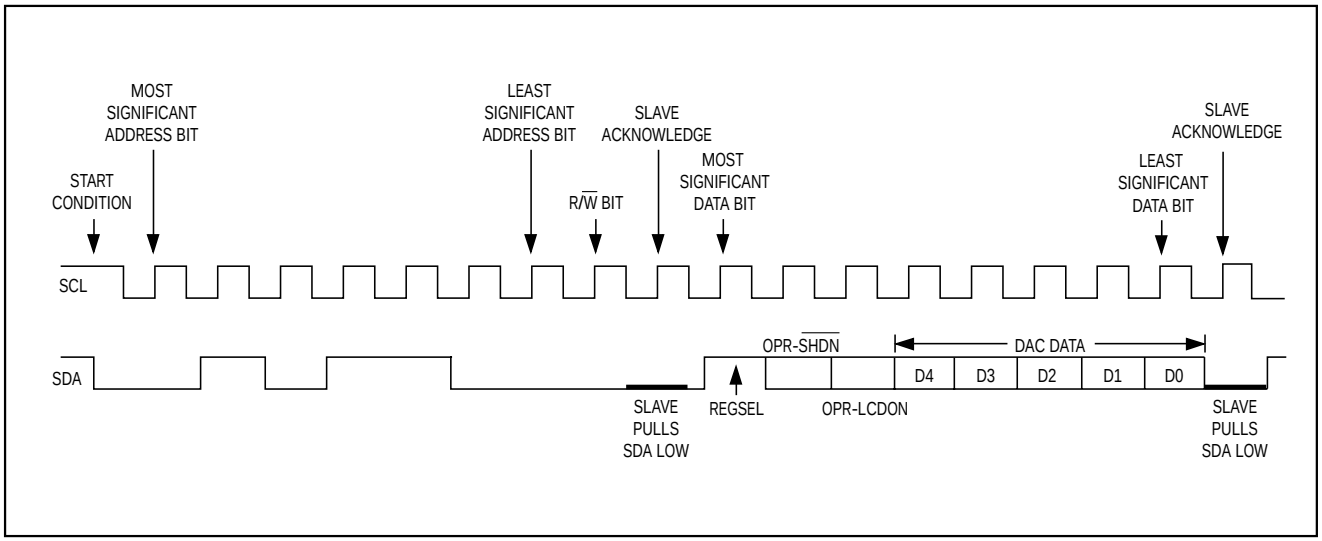


Figure 8. MAX1621 Serial-Interface Single-Byte Write Example (REGSEL = 1)

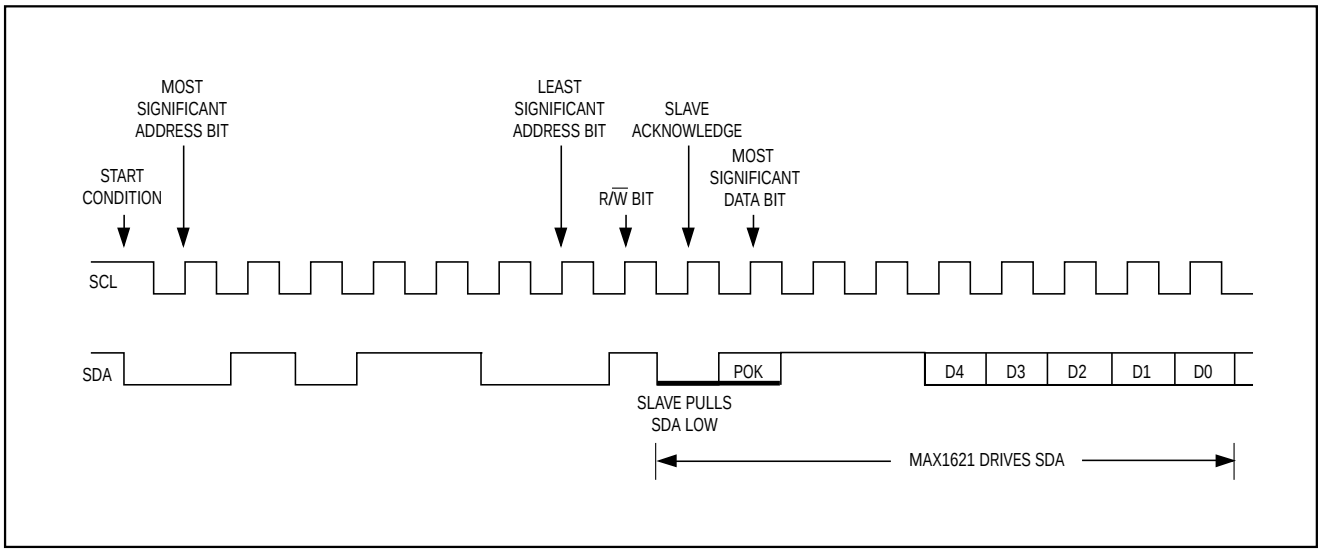


Figure 9. MAX1621 Serial-Interface Read Example

Design Procedure and Component Selection

The MAX1620/MAX1621 output voltage can be adjusted manually or via a digital interface. In addition, positive bias voltage can be switched with $\overline{LCDON}$ using an external PFET or PNP transistor.

Output Adjustment

Setting the Minimum Output Voltage

The minimum output voltage is set with a resistor-divider (R4-R5, Figure 4) from V_{OUT} to AGND. The FB threshold voltage is 1.5V. Choose R4 to be 300kΩ so that the current in the divider is about 5µA. Determine R5 as follows:

$$R5 = R4 \times (V_{OUT,MIN} - V_{FB}) / V_{FB}$$

For example, if $V_{OUT,MIN}$ = 12.5V:

$$R5 = 300k\Omega \times (12.5 - 1.5) / (1.5) = 2.2M\Omega$$

Mount R4 and R5 close to the FB pin to minimize parasitic capacitance.

For a negative output voltage, the FB threshold voltage is 0V, and R4 is placed between FB and REF (Figures 5 and 6). Again, choose R4 to be 300kΩ so that the current in the divider is about 5µA. Then determine R5 as follows:

$$R5 = R4 \times \left| V_{OUT,MIN} / V_{REF} \right|$$

For example, if $V_{OUT,MIN}$ = -12.5V:

$$R5 = 300k\Omega \times \left| (12.5) / (1.5) \right| = 2.5M\Omega$$

Setting the Maximum Output Voltage (DAC Adjustment)

The DAC is adjustable from 0V to 1.5V in 32 steps, and 1LSB = 1.5V / 31. DAC adjustment of V_{OUT} is provided by adding R3 to the divider circuit (Figure 4). Be sure that $V_{OUT,MAX}$ does not exceed the LCD panel rating.

For $V_{OUT,MAX}$ = 25V and $V_{OUT,MIN}$ = 12.5V, R3 is determined as follows:

$$R3 = R5 \times (V_{FB}) / (V_{OUT,MAX} - V_{OUT,MIN})$$
$$= 2.2M\Omega \times (1.5) / (25 - 12.5) = 264k\Omega$$

The general form for V_{OUT} as a function of the DAC output (V_{DOUT}) is:

$$V_{OUT} = V_{OUT,MIN} + (V_{FB} - V_{DOUT}) \times R5 / R3$$

At power-up the DAC resets to mid-scale (10000), which corresponds to V_{DOUT} = 0.774V; therefore, the output voltage after reset is as follows:

$$V_{OUT,RESET} = V_{OUT,MIN} + (1.5 - 0.774) \times R5 / R3$$

Note that for a positive output voltage, V_{OUT} increases as V_{DOUT} decreases. $V_{OUT,MAX}$ corresponds to V_{DOUT} = 0V, and $V_{OUT,MIN}$ corresponds to V_{DOUT} = 1.5V.

For a negative output voltage, $V_{OUT} = V_{OUT,MIN} + (V_{FB} - V_{DOUT}) \times R5 / R3$. Assume $V_{OUT,MAX}$ = -25V and $V_{OUT,MIN}$ = -12.5V; then determine R3 and $V_{OUT,RESET}$ as follows:

$$R3 = R5 \times (V_{FB} - V_{DOUT,MAX}) / (V_{OUT,MAX} - V_{OUT,MIN})$$
$$= 2.5M\Omega \times (0 - 1.5) / (-25 - -12.5) = 300k\Omega$$

$$V_{OUT,RESET} = -12.5 + (0 - 0.774) \times (2.5M) / (300k) = -18.95V$$

Note that for a negative output voltage, $|V_{OUT}|$ increases as V_{DOUT} increases. $|V_{OUT,MAX}|$ corresponds to V_{DOUT} = 1.5V, and $|V_{OUT,MIN}|$ corresponds to V_{DOUT} = 0V.

Potentiometer Adjustment

The output can be adjusted with a potentiometer instead of the DAC. Choose R_{POT} = 100kΩ, and connect it between REF and GND. Connect R3 to the potentiometer's wiper, instead of to DOUT. The same design equations as above apply.

Controlling the LCD Using POK and ***LCDON***

When voltage at POK is greater than 1V, the open-drain $\overline{LCDON}$ output pulls low. $\overline{LCDON}$ withstands 27V; therefore, it can drive a PFET or PNP transistor to switch on the MAX1620/MAX1621's positive output. The following represent three cases for using this feature:

1) As an off switch, to ensure that a positive boosted output goes to 0V during shutdown. In this case, connect POK to $\overline{SHDN}$. Without this switch, the positive output falls to one diode-drop below the input voltage (V_{BATT}) in shutdown. $\overline{LCDON}$ is not needed for negative outputs, which will fall to 0V in shutdown anyway.
2) As an output sensing cutoff for positive outputs. Connect POK to the feedback voltage divider to sense the output voltage. The output is switched on only when it reaches a set percentage of the set voltage.
3) As an input sensing output cutoff for positive outputs. Connect POK to a voltage divider to sense the input voltage. The output is switched on only when the input reaches the set level (Figure 4).

To control the open-drain output $\overline{LCDON}$ by sensing the input voltage, connect a resistor-divider (R1-R2, Figure 4) from V_{BATT} to POK. Choose R2 = 100k. For example, if the minimum battery voltage is 5.3V, determine R1 as follows:

$$R1 = R2 \times [(V_{BATT} / V_{POK}) - 1]$$
$$= 100k \times [(5.3 / 0.992) - 1] = 434k\Omega$$

$\overline{LCDON}$ can also be controlled via software (MAX1621, Table 4).

Table 4. MAX1621 $\overline{LCDON}$ Output Truth Table

POK Pin	LCDON Bit	$\overline{LCDON}$ Output
<1V	0	Floating
<1V	1	Floating
>1V	0	Floating
>1V	1	ON, pulls low

$\overline{LCDON}$ typically drives an external PNP transistor, switching a positive V_{OUT} to the LCD. R7 limits the base current in the PNP; R6 turns off the PNP when $\overline{LCDON}$ is floating. R6 and R7 can be the same value. Choose R7 such that the minimum base current is greater than 1/50 of the collector current. For example, assume $V_{OUT,MIN}$ = 12.5V and I_{LCD} = 10mA, then determine R7 as follows:

$$R7 \leq 50 \times (12.5 - 0.7) / 10mA = 59k\Omega$$

Remember that LCD voltage is the regulated output voltage minus the drop across the PNP switch. The drop across the external transistor (typically 300mV) must be accounted for.

If a PFET is preferred for the $\overline{LCDON}$ switch, R6 and R7 in Figure 4 may both be raised to 1MΩ or more to reduce operating current. Be sure to choose a P_{FET} with adequate breakdown voltage. Since load current is typically on the order of 10mA, an on-resistance of 10Ω or less is usually adequate.

Choosing an Inductor

Practical inductor values range from 33µH to 1mH; however, 100µH is a good choice for a wide range of applications. Inductors with a ferrite core or equivalent are recommended. The inductor's current rating should exceed the peak current as set by the k-factor and the coil inductance; however, for most inductor types, the coil's specified current can be exceeded by 20% with no impact on efficiency.

The peak current is set by the coil inductance as follows:

$$I_{PK} = \text{k-factor} / L$$

and

$$I_{OUT,MIN} = \frac{1}{2} \times I_{PK} \times V_{BATT,MIN} / V_{OUT,MAX}$$

If we assume that $V_{BATT,MIN}$ = 5.3V, $V_{OUT,MAX}$ = 25V, $I_{OUT,MIN}$ = 15mA, and a minimum k-factor of 16µs-V, then the required I_{PK} is:

$$I_{PK} = 2 \times 15mA \times 25 / 5.3 = 142mA$$

and

$$L \leq = 16\mu s\text{-}V / 142mA = 113\mu H$$

The next-lowest practical inductor value is 100µH. Its current rating must be:

$$24\mu s\text{-}V \text{ (maximum k-factor)} / 100\mu H = 240mA$$

Table 5 summarizes the minimum inductance value needed to provide various output currents at several minimum input voltages. Table 6 lists some suitable coil types and manufacturers, but is not intended to be a complete list.

Table 5. Maximum Inductance vs. I_{OUT} and $V_{BATT,MIN}$ (20V output)

		$V_{BATT,MIN}$					
		1.8V	**2.7V**	**3.6V**	**5.4V**	**7.2V**	**12V**
IOUT	**5mA**	100µH	150µH	220µH	330µH	390µH	680µH
	10mA	56µH	82µH	100µH	150µH	220µH	330µH
	20mA	27µH	39µH	56µH	82µH	100µH	180µH
	30mA	18µH	27µH	33µH	56µH	68µH	120µH

Table 6. Inductor List

COMPANY	PART	µH RANGE	SIZE IN mm (H x W x L)	COMMENTS
Sumida USA (847) 956-0666 Japan 81-3-3607-5111	CD43	Up to 68µH	3.2 x 4 diameter	
	CD54	Up to 220µH	4.5 x 5.2 diameter	
	CDRH62B	Up to 330µH	3 x 6.2 x 6.2	Shielded
Coilcraft (847) 639-6400	DO1608	Up to 1mH	3.18 x 4.45 x 6.6	
	DT1608	Up to 400µH	3.18 x 4.45 x 6.6	Shielded
TDK (847) 390-4373	NLC565050	Up to 1mH	5 x 5 x 5.6	
	TPF0410	Up to 1mH	4 diameter x 10 L	Leaded coil

Digitally Adjustable LCD Bias Supplies

Diode Selection

The high maximum switching frequency of 300kHz requires a high-speed rectifier. Schottky diodes, such as the MBRS0540, are recommended. To maintain high efficiency, the average current rating of the Schottky diode must be greater than the peak switching current. Choose a reverse breakdown voltage greater than the positive output voltage or greater than the negative output voltage plus V_{BATT}.

External Switching Transistor

Again, the high maximum switching frequency requires a high-speed switching transistor to maintain efficiency. Logic-level N-channel MOSFETs, such as the MMFT3055VL, are recommended (N1). Choose a V_{DS} rating greater than the positive output voltage or greater than the negative output voltage plus V_{BATT}.

To save cost in certain applications, a bipolar transistor may be substituted for the MOSFET with a decrease in efficiency. The conditions favoring substitution are limited input voltage range (V_{DD}), low maximum battery voltage (V_{BATT}), and low output current. For example, V_{DD} = 3.0V to 3.6V, $V_{BATT,MAX}$ = 12V, and I_{OUT} = 5mA favors a bipolar transistor substitution to reduce cost.

To modify the Typical Operating Circuit (Figures 4 and 5) for a bipolar switching transistor, connect the collector to the inductor, the base to DLO, and the emitter to PGND (Figure 10). Connect the base to DHI through a series resistor to limit the base current. Choose the resistor such that the minimum base current is greater than 1/20 of the peak inductor current. For example, assume $V_{DD,MIN}$ = 3V and I_{PK} = 100mA; then $R_S \leq 20 \times (3 - 0.7) / 100mA = 460\Omega$.

Output Filter Capacitor

A 22µF, 35V, low-ESR, surface-mount tantalum output capacitor is sufficient for most applications. Output ripple voltage is dominated by the peak switch current multiplied by the output capacitor's effective series resistance (ESR). 100mVp-p output ripple is a good target for the trade-off between cost and performance. Capacitors smaller than 22µF may be used for light loads and lower peak current. Surface-mount capacitors are generally preferred because they lack the inductance and resistance of their through-hole equivalents. The AVX TPS series and the Sprague 593D and 595D series are good choices for low-ESR surface-mount tantalum capacitors.

Moderate-performance aluminum-electrolytic or tantalum capacitors can be successfully substituted in cost-sensitive applications with low output current. Matsuo and Nichicon provide suitable choices.

Input Bypass Capacitor

Two inputs, V_{DD} and V_{BATT}, require bypass capacitors. Bypass V_{DD} with a 0.1µF ceramic capacitor as close to the IC as possible. The battery supplies high currents to the inductor and requires local bulk bypassing close to the inductor. A 22µF low-ESR surface-mount capacitor is sufficient for most applications. Smaller capacitors are acceptable if peak inductor current is low or the battery's internal impedance is low and the battery is close to the inductor.

Charge-Pump Capacitor (Negative Output)

Possible negative output topologies are shown in Figures 5 and 6. Overall efficiency for the negative output configuration is less than for the positive output circuit because of the extra components in the power-transfer path. For efficient charge transfer, C4 must have low ESR and should be smaller than the output capacitor (C5). C4 sees the same voltage as C5, and should have the same voltage rating. A 1µF ceramic capacitor is a practical choice for cost and performance considerations. 2.2µF is suggested for Figure 6's circuit.

Feedback-Compensation Capacitor

The high value of the feedback resistors (R3, R4, R5, Figure 4) makes the feedback loop susceptible to phase lag because of the parasitic capacitance at the FB pin. To compensate for this, connect a capacitor (C6, Figure 4) in parallel with R5. The value of C6 depends on the parallel combination of R3, R4, R5, and the individual circuit layout. Typical values range from 33pF to 220pF.

Reference-Compensation Capacitor

The internal reference uses an external capacitor for frequency compensation. Connect a ceramic capacitor with a 0.1µF minimum value between REF and ground.

PC Board Layout and Grounding

Due to high current levels and fast switching waveforms, proper PC board layout is essential. In particular, keep all traces short, especially those connected to the FB pin and those connecting N1, L1, D1, D2, C4, and C5. Place R3, R4, and R5 as close to the feedback pin as possible.

Use a star ground configuration: connect the grounds of the input bypass capacitor, the output capacitor, and the switching transistor together, close to the IC's PGND pin. Tie AGND and PGND together at the chip.

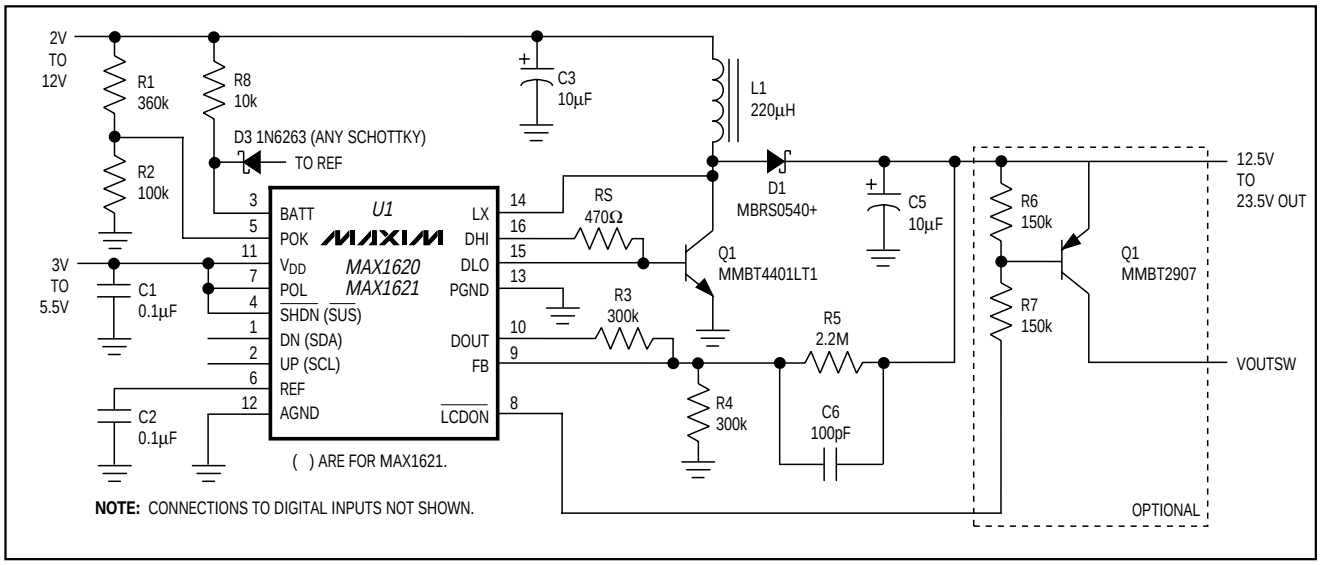
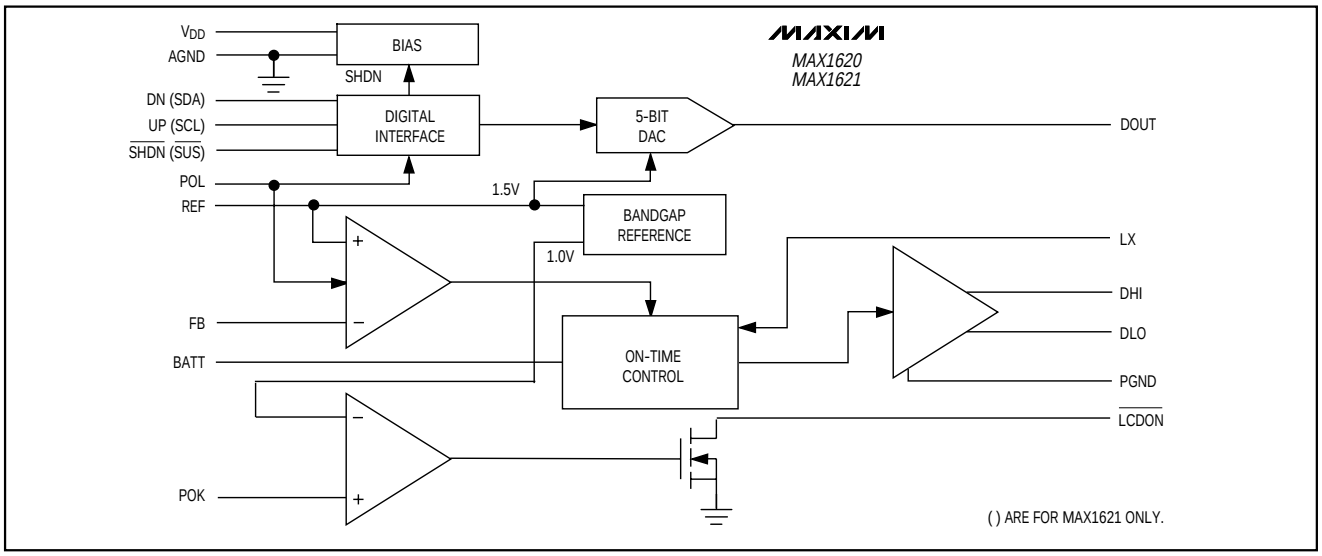


Figure 10. Positive Output with Bipolar Switching Transistor

Simplified Block Diagram



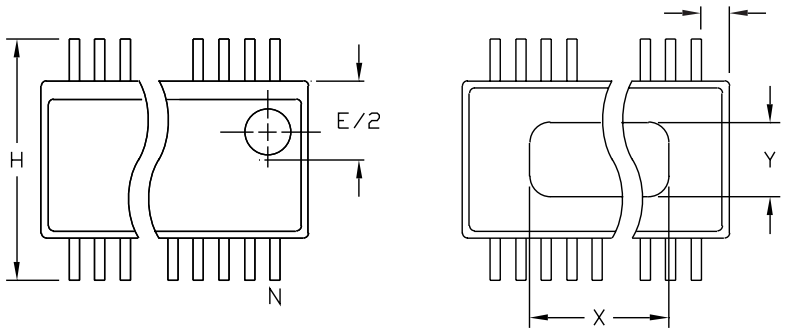
Chip Information

TRANSISTOR COUNT: 341

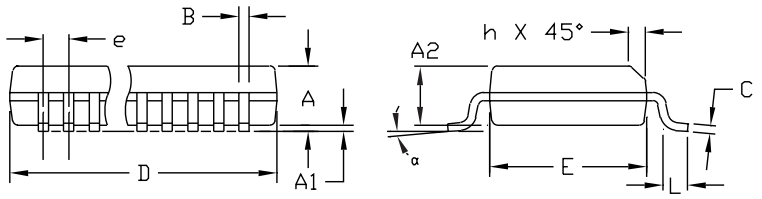
SUBSTRATE CONNECTED TO AGND

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1