MAX17600–MAX17605

4A Sink/Source Current, 12ns, Dual MOSFET Drivers

General Description

The MAX17600–MAX17605 devices are high-speed MOSFET drivers capable of sinking /sourcing 4A peak currents. The devices have various inverting and non-inverting part options that provide greater flexibility in controlling the MOSFET. The devices have internal logic circuitry that prevents shoot-through during output-state changes. The logic inputs are protected against voltage spikes up to +14V, regardless of V_{DD} voltage. Propagation delay time is minimized and matched between the dual channels. The devices have very fast switching time, combined with short propagation delays (12ns typ), making them ideal for high-frequency circuits. The devices operate from a +4V to +14V single power supply and typically consume 1mA of supply current. The MAX17600/MAX17601 have standard TTL input logic levels, while the MAX17603 /MAX17604/MAX17605 have CMOS-like high-noise margin (HNM) input logic levels. The MAX17600/MAX17603 are dual inverting input drivers, the MAX17601/MAX17604 are dual noninverting input drivers, and the MAX17602/MAX17605 devices have one noninverting and one inverting input. These devices are provided with enable pins (ENA, ENB) for better control of driver operation.

These devices are available in 8-pin (3mm x 3mm) TDFN, 8-pin (3mm x 5mm) µMAX®, and 8-pin SO packages and operate over the -40°C to +125°C temperature range.

Applications

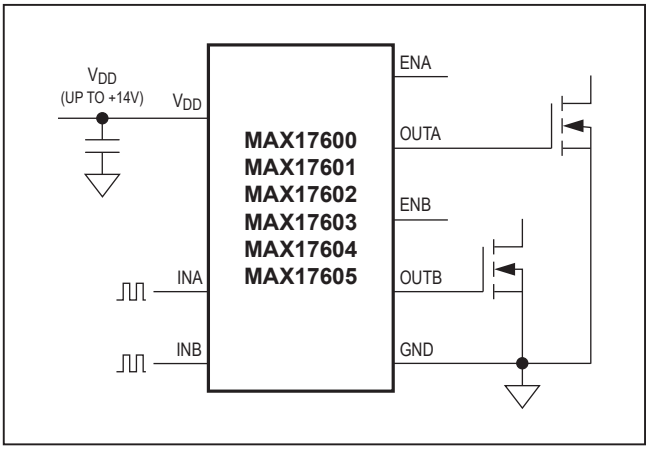
- Power MOSFET Switching
- Switch-Mode Power Supplies
- DC-DC Converters
- Motor Control
- Power-Supply Modules

***Ordering Information* appears at end of data sheet.**

Features

- Dual Drivers with Enable Inputs
- +4V to +14V Single Power-Supply Range
- 4A Peak Sink /Source Current
- Inputs Rated to +14V, Regardless of V_{DD} Voltage
- Low 12ns Propagation Delay
- 6ns Typical Rise and 5ns Typical Fall Times with 1nF Load
- Matched Delays Between Channels
- Parallel Operation of Dual Outputs for Larger Driver Output Current
- TTL or HNM Logic-Level Inputs with Hysteresis for Noise Immunity
- Low Input Capacitance: 10pF (typ)
- Thermal Shutdown Protection
- TDFN, µMAX, and SO Package Options
- -40°C to +125°C Operating Temperature Range

Typical Operating Circuit



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Absolute Maximum Ratings

V_{DD}, INA, INB, ENA, ENB to GND .....-0.3V to +16V
OUTA, OUTB to GND.....-0.3V to +16V
Junction Operating Temperature Range ..... -40°C to +125°C
Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 23.8mW/°C above +70°C) 1904mW
8-Pin SO (derate 74mW/°C above +70°C)..... 588.2mW*
8-Pin µMAX (derate 12.9mW/°C above +70°C).....1030.9mW

Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+240°C

*As per JEDEC 51 standard.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 8 TDFN	
Package Code	T833+2
Outline Number	21-0137
Land Pattern Number	90-0059
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	42°C/W
Junction to Case (θ_{JC})	8°C/W

PACKAGE TYPE: 8 SO	
Package Code	S8+2
Outline Number	21-0041
Land Pattern Number	90-0096
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	136°C/W
Junction to Case (θ_{JC})	38°C/W

PACKAGE TYPE: 8 µMAX	
Package Code	U8E+2
Outline Number	21-0107
Land Pattern Number	90-0145
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	77.6°C/W
Junction to Case (θ_{JC})	5°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 12V, C_L = 0F, at T_A = -40°C to +125°C, unless otherwise noted. Typical values are specified at T_A = +25°C. Parameters specified at V_{DD} = 4V apply to the TTL versions only.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (V_{DD})						
V_{DD} Operating Range	V_{DD}	TTL versions	4		14	V
		HNM versions	6		14	
V_{DD} Undervoltage Lockout	UVLO	V_{DD} rising	3	3.5	3.85	V
V_{DD} UVLO Hysteresis				200		mV
V_{DD} UVLO to OUT_ Delay		V_{DD} rising		120		µs
V_{DD} Supply Current	IDD_Q	Not switching, V_{DD} = 14V (Note 2)		1	2	mA
	IDD_SW	V_{DD} = 4.5V, C_L = 1nF, both channels switching at 1MHz		12	18	
DRIVER OUTPUT (SOURCE) (OUTA, OUTB)						
Peak Output Current (Sourcing)	I_{PK-P}	V_{DD} = 14V, C_L = 10nF (Note 2)		4		A
Driver Output Resistance Pulling Up (Note 3)	R_{ON-P}	V_{DD} = 14V, $I_{OUT_}$ = 100mA		0.88	1.85	Ω
		V_{DD} = 4V, $I_{OUT_}$ = 100mA		0.91	1.95	
DRIVER OUTPUT (SINK) (OUTA, OUTB)						
Peak Output Current (Sinking)	I_{PK-N}	V_{DD} = 14V, C_L = 10nF (Note 2)		4		A
Driver Output Resistance Pulling Down (Note 3)	R_{ON-N}	V_{DD} = 14V, $I_{OUT_}$ = -100mA		0.5	0.95	Ω
		V_{DD} = 4V, $I_{OUT_}$ = -100mA		0.52	1	
LOGIC INPUT (INA, INB)						
$V_{IN_}$ Logic-High Input Voltage	V_{IH}	MAX17600/1/2	2.1			V
		MAX17603/4/5	4.25			
$V_{IN_}$ Logic-Low Input Voltage	V_{IL}	MAX17600/1/2			0.8	V
		MAX17603/4/5			2.0	
Logic Input Hysteresis	V_{HYS}	MAX17600/1/2		0.34		V
		MAX17603/4/5		0.9		
Logic Input Leakage Current	I_{LKG}	V_{INA} = V_{INB} = 0V or V_{DD} (MAX17600/1/2)	-1	+0.02	+1	µA
Logic Input Bias Current	I_{BIAS}	V_{INA} = V_{INB} = 0V or V_{DD} (MAX17603/4/5)		10		µA
Logic Input Capacitance	C_{IN}	(Note 2)		10		pF

Electrical Characteristics (continued)

(V_{DD} = 12V, C_L = 0F, at T_A = -40°C to +125°C, unless otherwise noted. Typical values are specified at T_A = +25°C. Parameters specified at V_{DD} = 4V apply to the TTL versions only.) (Note 1)

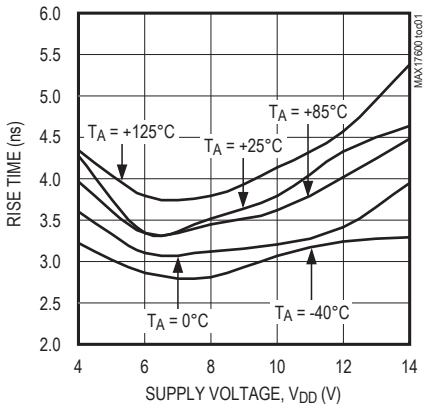
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE (ENA, ENB)						
V_{EN_H} High Level Voltage		MAX17600/1/2	2.1			V
		MAX17603/4/5	4.25			
V_{EN_L} Low Level Voltage		MAX17600/1/2			0.8	V
		MAX17603/4/5			2.0	
Enable Hysteresis	EN_{HYS}	MAX17600/1/2		0.34		V
		MAX17603/4/5		0.9		
Enable Pullup Resistor to V_{DD}	R_{pu}	MAX17600/1/2	50	100	200	kΩ
		MAX17603/4/5	100	200	400	
Propagation Delay from EN_ to OUT_ (Note 2)	t_{pd}	EN_ rising		7		ns
		EN_ falling		7		
SWITCHING CHARACTERISTICS (V_{DD} = 14V) (Note 2)						
OUT_ Rise Time	t_R	C_L = 1nF		6		ns
		C_L = 4.7nF		20		
		C_L = 10nF		40		
OUT_ Fall Time	t_F	C_L = 1nF		6		ns
		C_L = 4.7nF		16		
		C_L = 10nF		25		
Turn-On Delay Time	t_{D-ON}	C_L = 1nF		12		ns
Turn-Off Delay Time	t_{D-OFF}	C_L = 1nF		12		ns
SWITCHING CHARACTERISTICS (V_{DD} = 4.5V) (Note 2)						
OUT_ Rise Time	t_R	C_L = 1nF		5		ns
		C_L = 4.7nF		15		
		C_L = 10nF		28		
OUT_ Fall Time	t_F	C_L = 1nF		5		ns
		C_L = 4.7nF		10		
		C_L = 10nF		18		
Turn-On Delay Time	t_{D-ON}	C_L = 1nF		12		ns
Turn-Off Delay Time	t_{D-OFF}	C_L = 1nF		12		ns
MATCHING CHARACTERISTICS (Note 2)						
Matching Propagation Delays Between Channel A and Channel B		V_{DD} = 14V, C_L = 10nF		8		ns

Note 1: All devices are production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 2: Design guaranteed by bench characterization. Limits are not production tested.
Note 3: For SOIC, µMAX package options, these are only Typ parameters.

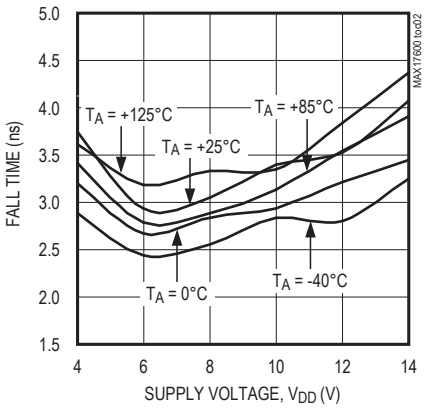
Typical Operating Characteristics

(C_L = 1nF, T_A = +25°C, unless otherwise noted.)

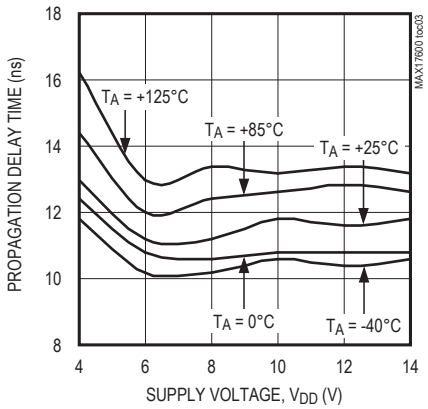
RISE TIME vs. SUPPLY VOLTAGE ($C_{OUT_}$ = 1nF)



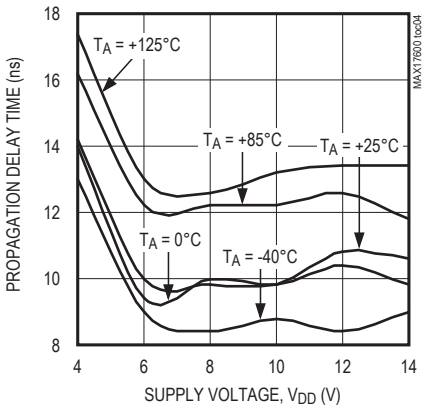
FALL TIME vs. SUPPLY VOLTAGE ($C_{OUT_}$ = 1nF)



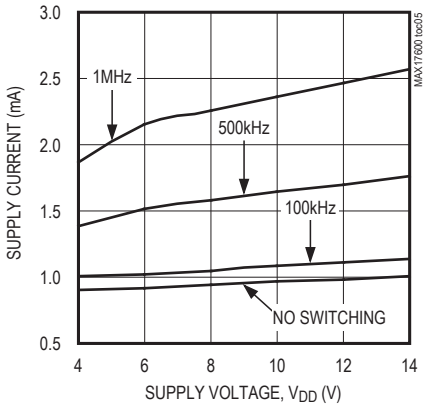
PROPAGATION DELAY TIME (LOW TO HIGH) vs. SUPPLY VOLTAGE ($C_{OUT_}$ = 1nF)



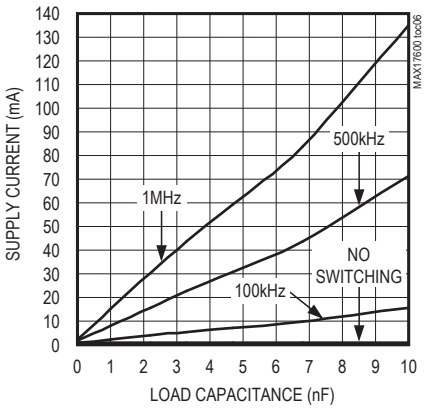
PROPAGATION DELAY TIME (HIGH TO LOW) vs. SUPPLY VOLTAGE ($C_{OUT_}$ = 1nF)



SUPPLY CURRENT vs. SUPPLY VOLTAGE ($C_{OUT_}$ = 0nF)



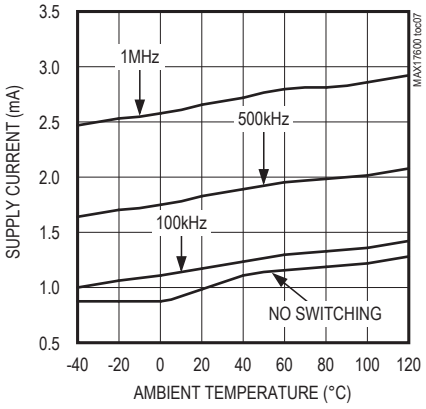
SUPPLY CURRRENT vs. LOAD CAPACITANCE (V_{DD} = 12V, C_{OUTB} = 0nF)



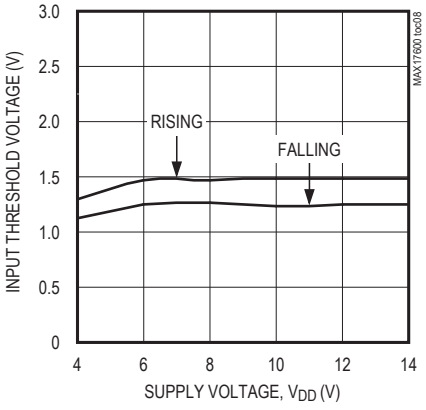
Typical Operating Characteristics (continued)

(C_L = 1nF, T_A = +25°C, unless otherwise noted.)

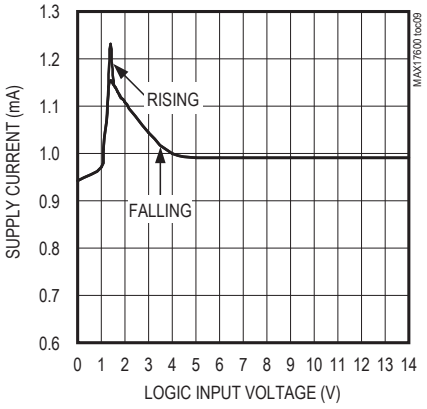
SUPPLY CURRENT vs. TEMPERATURE (V_{DD} = 12V, $C_{OUT_}$ = 0nF)



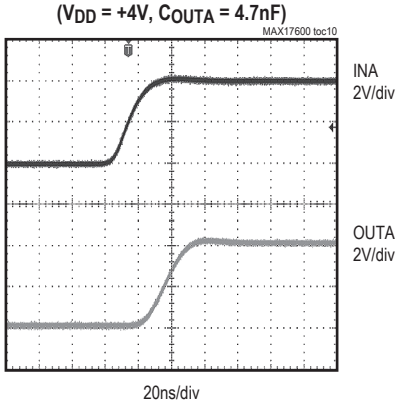
INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE ($C_{OUT_}$ = 0nF)



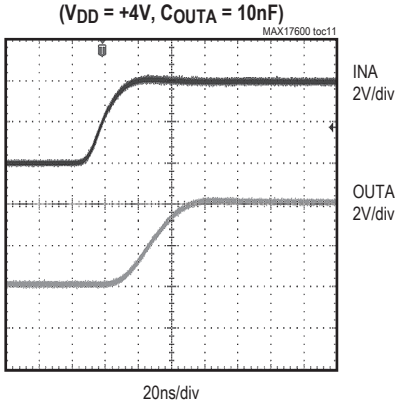
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE (V_{DD} = 12V, $C_{OUT_}$ = 0nF)



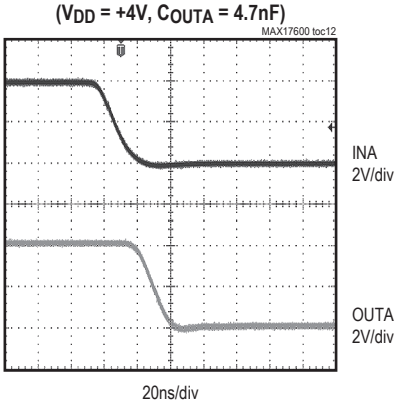
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17601) (V_{DD} = +4V, C_{OUTA} = 4.7nF)



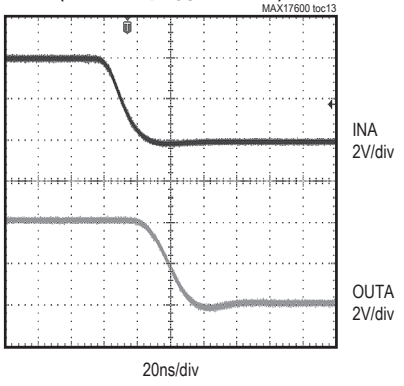
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17601) (V_{DD} = +4V, C_{OUTA} = 10nF)



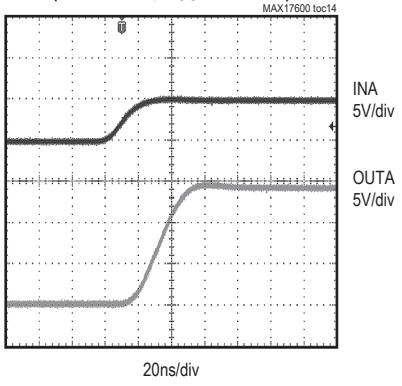
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17601) (V_{DD} = +4V, C_{OUTA} = 4.7nF)



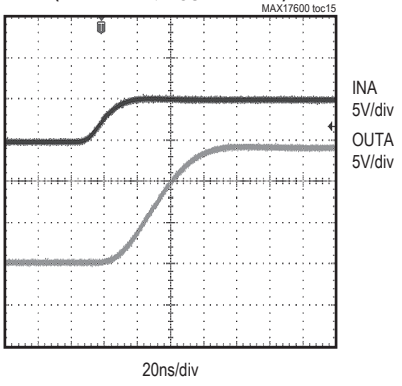
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17601) (V_{DD} = +4V, C_{OUTA} = 10nF)



LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17601) (V_{DD} = +14V, C_{OUTA} = 4.7nF)



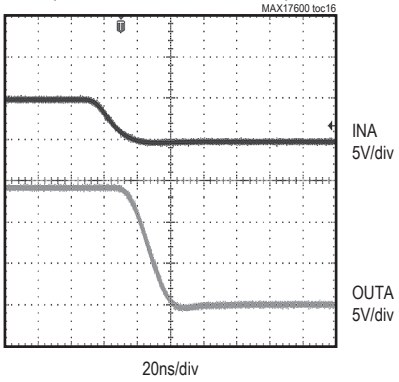
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17601) (V_{DD} = +14V, C_{OUTA} = 10nF)



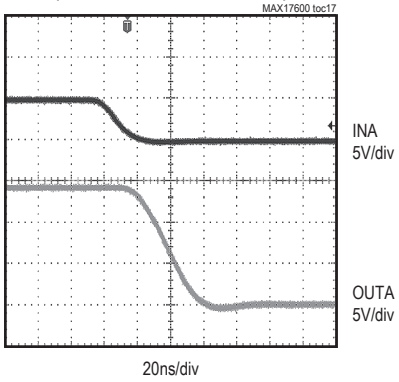
Typical Operating Characteristics (continued)

(C_L = 1nF, T_A = +25°C, unless otherwise noted.)

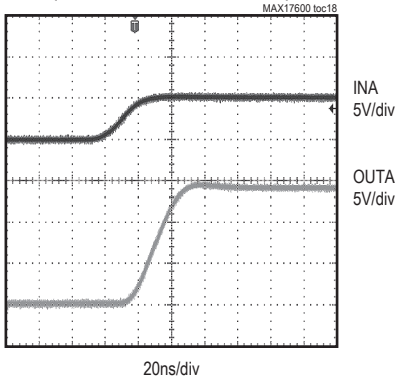
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17601) (V_{DD} = +14V, C_{OUTA} = 4.7nF)



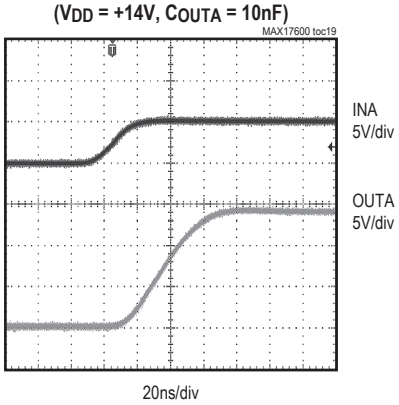
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17601) (V_{DD} = +14V, C_{OUTA} = 10nF)



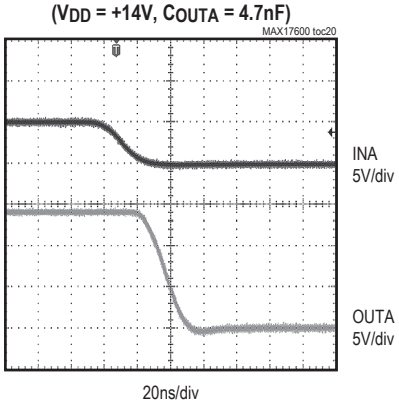
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17604) (V_{DD} = +14V, C_{OUTA} = 4.7nF)



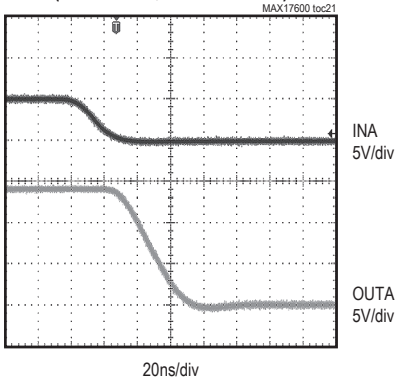
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17604) (V_{DD} = +14V, C_{OUTA} = 10nF)



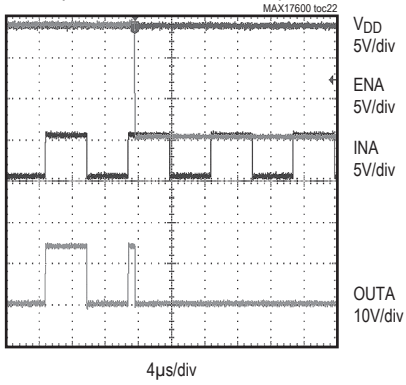
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17604) (V_{DD} = +14V, C_{OUTA} = 4.7nF)



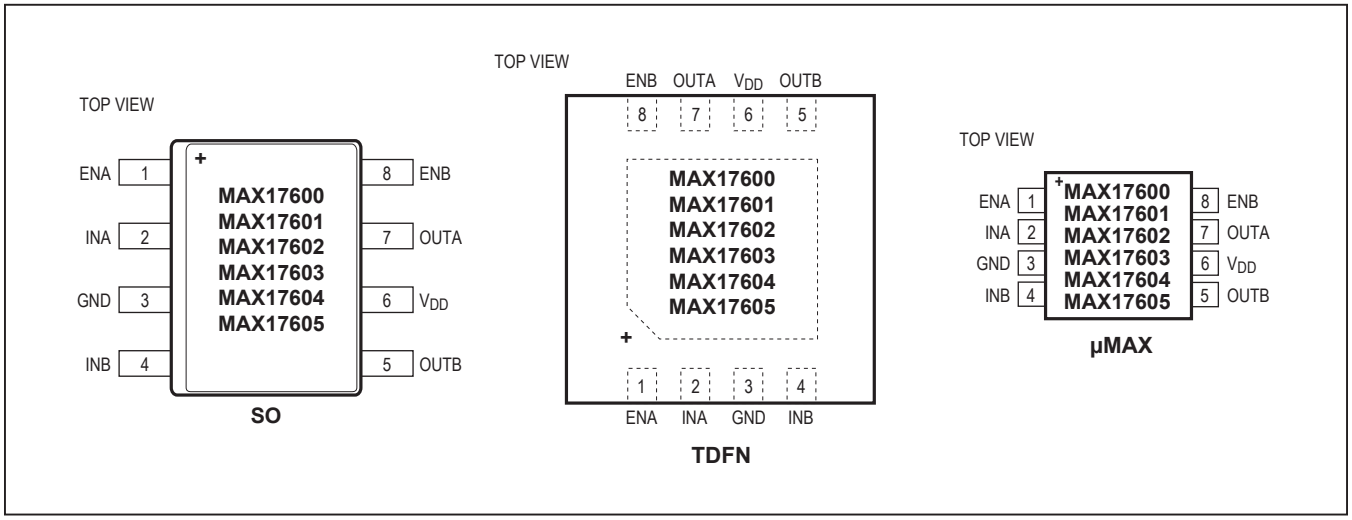
LOGIC INPUT VOLTAGE vs. OUTPUT VOLTAGE (MAX17604) (V_{DD} = +14V, C_{OUTA} = 10nF)



LOGIC OUTPUT vs. ENABLE (V_{DD} = +14V, C_{OUTA} = 0nF)



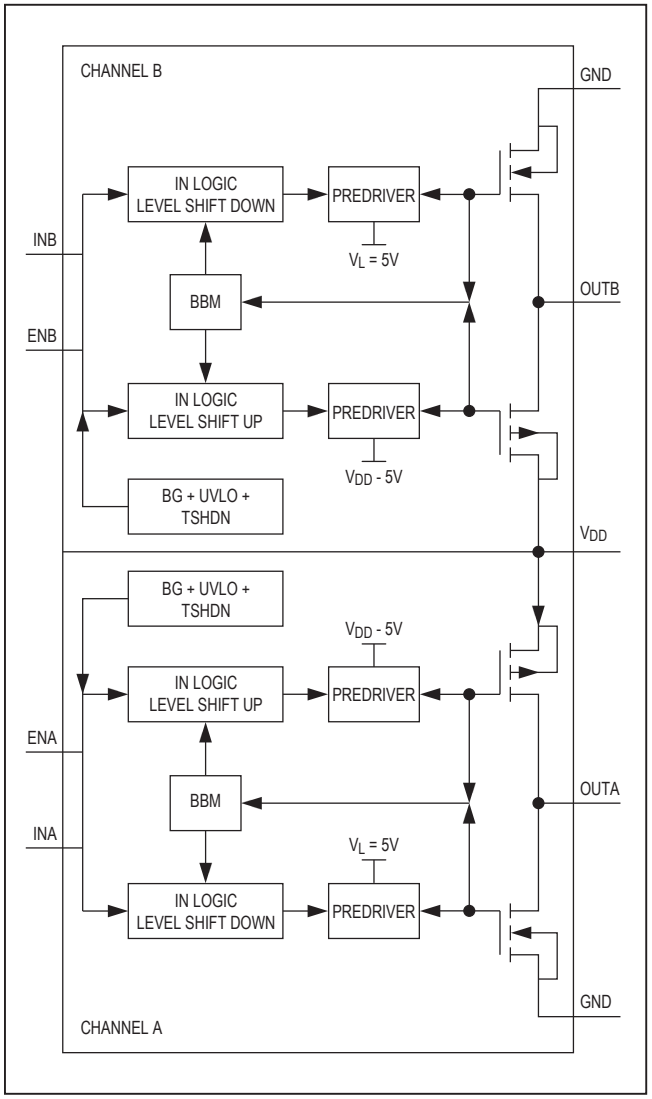
Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	ENA	Enable Input for Driver A. Internally pulled to V_{DD} through a 100kΩ resistor. Leave unconnected for always-on operation. Connect to GND for disabling the corresponding channel.
2	INA	Logic Input for Channel A
3	GND	Ground
4	INB	Logic Input for Channel B
5	OUTB	Channel B Driver Output. Sources and sinks current for channel B to turn the external MOSFET at OUTB on or off.
6	V_{DD}	Power-Supply Input. Bypass to GND with one or more low-ESR 0.1µF ceramic capacitors.
7	OUTA	Channel A Driver Output. Sources and sinks current for channel A to turn the external MOSFET at OUTA on or off.
8	ENB	Enable Input for Driver B. Internally pulled to V_{DD} through a 100kΩ resistor. Leave unconnected for always-on operation. Connect to GND for disabling the corresponding channel.
—	EP	Exposed Pad (TDFN Only). Internally connected to GND. Do not use the EP as the only ground connection.

Functional Diagram



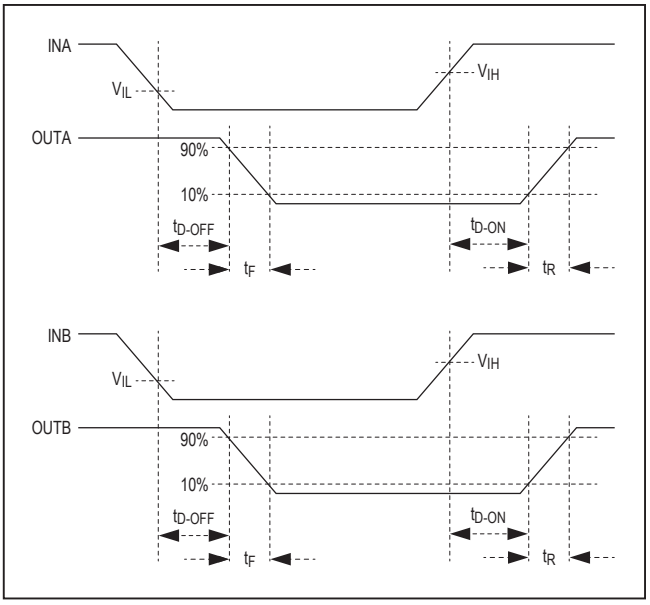


Figure 1. Timing Diagram for the MAX17601/MAX17604

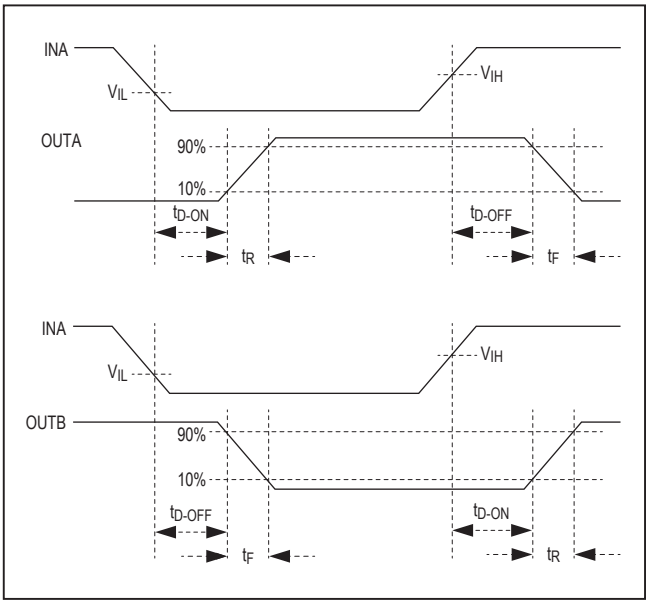


Figure 2. Timing Diagram for the MAX17602/MAX17605

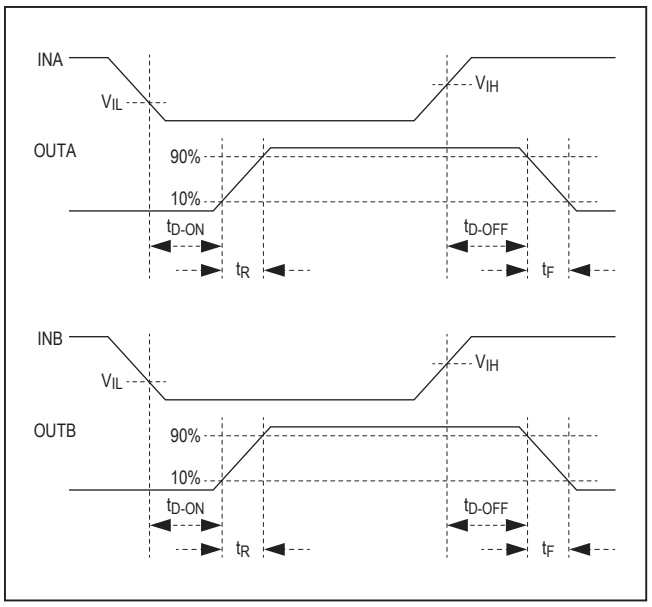


Figure 3. Timing Diagram for the MAX17600/MAX17603

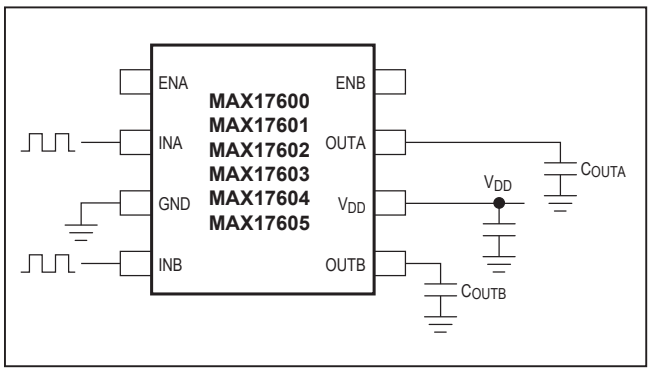


Figure 4. Test Circuit for the Timing Diagrams

Detailed Description

The MAX17600–MAX17605 are high-speed MOSFET drivers capable of sinking/sourcing 4A peak currents. The devices have various inverting and noninverting part options that provide greater flexibility in controlling the MOSFET. The devices have internal logic circuitry that prevents shoot-through during output-state changes. The logic inputs are protected against voltage spikes up to +16V, regardless of V_{DD} voltage. Propagation delay time is minimized and matched between the dual channels. The devices have very fast switching time, combined with short propagation delays (12ns typ), making them ideal for high-frequency circuits. The devices operate from a +4V to +14V single power supply and typically consume 1mA of supply current. The MAX17600/MAX17601/MAX17602 have standard TTL input logic levels, while the MAX17603/MAX17604/MAX17605 have CMOS-like high-noise margin (HNM) input logic levels. The MAX17600/MAX17603 are dual inverting input drivers, the MAX17601/MAX17604 are dual noninverting input drivers, and the MAX17602/MAX17605 have one noninverting and one inverting input. These devices are provided with enable pins (ENA and ENB) for better control of driver operation.

Logic Inputs

The MAX17600/MAX17601/MAX17602 have standard TTL input logic levels, while the MAX17603/MAX17604/MAX17605 have CMOS-like HNM input logic levels (see the *Electrical Characteristics* table). Table 1 gives the truth table for various part options.

Table 1. Truth Table

ENABLE INPUTS		LOGIC INPUTS		DUAL NONINVERTING DRIVER		DUAL INVERTING DRIVER		ONE INVERTING AND ONE NONINVERTING DRIVER	
ENA	ENB	INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
H	H	H	H	H	H	L	L	L	H
H	H	H	L	H	L	L	H	L	L
H	H	L	H	L	H	H	L	H	H
H	H	L	L	L	L	H	H	H	L
L	L	X	X	L	L	L	L	L	L

L = Logic-low, H = Logic-high.

Undervoltage Lockout (UVLO)

When V_{DD} is below the UVLO threshold, the output stage n-channel device is on and the p-channel is off, independent of the state of the inputs. This holds the outputs low. The UVLO is typically 3.6V with 200mV typical hysteresis to avoid chattering. A typical falling delay of 2µs makes the UVLO immune to narrow negative transients in noisy environments.

Driver Outputs

The devices feature 4A peak sourcing/sinking capabilities to provide fast rise and fall times of the MOSFET gate. Add a resistor in series with OUT_ to slow the corresponding rise/fall time of the MOSFET gate.

Applications Information

Supply Bypassing, Device Grounding, and Placement

Ample supply bypassing and device grounding are extremely important because when large external capacitive loads are driven, the peak current at the V_{DD} pin can approach 4A, while at the GND pin, the peak current can approach 4A. V_{DD} drops and ground shifts are forms of negative feedback for inverters and, if excessive, can cause multiple switching when the inverting input is used and the input slew rate is low. The device driving the input should be referenced to the devices' GND pin, especially when the inverting input is used. Ground shifts due to insufficient device grounding can disturb other circuits sharing the same AC ground return path. Any series inductance in the V_{DD}, OUT_, and/or GND paths can cause oscillations due to the very high di/dt that results when the devices are switched with any capacitive load. A 2.2µF or larger value ceramic capacitor is recommended, bypassing V_{DD} to GND and placed as close as possible to the pins. When driving very large loads (e.g., 10nF) at minimum rise time, 10µF or more of parallel storage capacitance is recommended. A ground plane is highly recommended to minimize ground return resistance and series inductance. Care should be taken to place the devices as close as possible to the external MOSFET being driven to further minimize board inductance and AC path resistance.

Power Dissipation

Power dissipation of the devices consists of three components, caused by the quiescent current, capacitive charge and discharge of internal nodes, and the output current (either capacitive or resistive load). The sum of these components must be kept below the maximum power-dissipation limit.

The quiescent current is 1mA typical. The current required to charge and discharge the internal nodes is frequency dependent (see the *Typical Operating Characteristics*). The devices' power dissipation when driving a ground referenced resistive load is:

$$P = D \times R_{ON}\ (MAX) \times I_{LOAD}^2 \text{ per channel}$$

where D is the fraction of the period the devices' output pulls high, R_{ON} (MAX) is the maximum pullup on-resistance of the device with the output high, and I_{LOAD} is the output load current of the devices.

For capacitive loads, the power dissipation is:

$$P = C_{LOAD} \times (V_{DD})^2 \times FREQ \text{ per channel}$$

where C_{LOAD} is the capacitive load, V_{DD} is the supply voltage, and FREQ is the switching frequency.

Layout Information

The devices' MOSFET drivers source and sink large currents to create very fast rise and fall edges at the gate of the switching MOSFET. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PCB layout guidelines are recommended when designing with the devices:

- Place at least one 2.2µF decoupling ceramic capacitor from V_{DD} to GND as close as possible to the IC. At least one storage capacitor of 10µF (min) should be located on the PCB with a low-resistance path to the V_{DD} pin of the devices. There are two AC current loops formed between the IC and the gate of the MOSFET being driven. The MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from OUT_ of the devices to the MOSFET gate to the MOSFET source and to GND of the devices. When the gate of the MOSFET is being pulled high, the active current loop is from OUT_ of the devices to the MOSFET gate to the MOSFET source to the GND terminal of the decoupling capacitor to the V_{DD} terminal of the decoupling capacitor and to the V_{DD} terminal of the devices. While the charging current loop is important, the discharging current loop is also critical. It is important to minimize the physical distance and the impedance in these AC current paths.
- In a multilayer PCB, the component surface layer surrounding the devices should consist of a ground plane containing the discharging and charging current loops.

Ordering Information/Selector Guide

PART	PIN-PACKAGE	CONFIGURATION	LOGIC LEVELS	TOP MARK
MAX17600ATA+	8 TDFN-EP* (3mm x 3mm)	Dual/Inverting	TTL	+BOJ
MAX17600ASA+	8 SO	Dual/Inverting	TTL	+
MAX17600AUA+	8 µMAX-EP*	Dual/Inverting	TTL	+AACI
MAX17601ATA+	8 TDFN-EP* (3mm x 3mm)	Dual/Noninverting	TTL	+BOK
MAX17601ASA+	8 SO	Dual/Noninverting	TTL	+
MAX17601AUA+	8 µMAX-EP*	Dual/Noninverting	TTL	+AACJ
MAX17602ATA+	8 TDFN-EP* (3mm x 3mm)	Inverting/Noninverting	TTL	+BOL
MAX17602ASA+	8 SO	Inverting/Noninverting	TTL	+
MAX17602AUA+	8 µMAX-EP*	Inverting/Noninverting	TTL	+AACK
MAX17603ATA+	8 TDFN-EP* (3mm x 3mm)	Dual/Inverting	HNM	+BOM
MAX17603ASA+	8 SO	Dual/Inverting	HNM	+
MAX17603AUA+	8 µMAX-EP*	Dual/Inverting	HNM	+AACL
MAX17604ATA+	8 TDFN-EP* (3mm x 3mm)	Dual/Noninverting	HNM	+BON
MAX17604ASA+	8 SO	Dual/Noninverting	HNM	+
MAX17604AUA+	8 µMAX-EP*	Dual/Noninverting	HNM	+AACM
MAX17605ATA+	8 TDFN-EP* (3mm x 3mm)	Inverting/Noninverting	HNM	+BOO
MAX17605ASA+	8 SO	Inverting/Noninverting	HNM	+
MAX17605AUA+	8 µMAX-EP*	Inverting/Noninverting	HNM	+AACN

Note: *All devices are specified over the -40°C to +125°C temperature range. Optional 8-pin 2mm x 3mm TDFN package is available. Contact your Maxim sales representative for more information.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/12	Initial release	—
1	5/12	Added the MAX17600	1–12
2	6/17	Updated *Electrical Characteristics* table OUT_ Rise Time for Switching Characteristics (V_{DD} = 14V and V_{DD} = 4.5V) units from pF to nF.	3–4

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