Automotive, 2V to 36V, 2.2MHz, 0.6A/1.2A Buck-Boost Converters with Integrated H-Bridge

MAX20039/MAX20040

General Description

The MAX20039/MAX20040 ICs are a small, synchronous buck-boost converter family with integrated high-side and low-side switches. The MAX20040 is designed to deliver up to 1.2A with input voltages from 2V to 36V while using only 52µA quiescent current at no load. The ICs provide an accurate output voltage of ±2%. Voltage quality can be monitored by observing the PGOOD signal.

The MAX20039/MAX20040 offer a fixed output voltage of 5V and a programmable range of 4.0V to 15V. See the *Ordering Information* table for more details. Frequency is adjustable from 220kHz to 2.2MHz, which allows for small external components, reduced output ripple, and guarantees no AM interference. Skip mode with low quiescent current of 52µA is available in the MAX20040B and MAX20040D versions of the IC. The ICs can operate with spread-spectrum frequency modulation designed to minimize EMI-radiated emissions due to the modulation frequency.

The MAX20039/MAX20040 are available in a small, 4mm x 4mm, 20-pin, side-wettable TQFN package and use very few external components.

Applications

- Infotainment Systems
- Body Electronics
- Start-Stop Systems
- Point-of-Load (PoL) Power Supply
- Power over Coax (PoC)

Benefits and Features

- Meets Stringent Automotive Quality and Reliability Requirements
  - 2V to 36V Operating V_{IN} Allows Operation in Cold-Crank Conditions
  - Tolerates Input Transients Up to 40V
  - EN Pin Compatible from 3.3V to 40V
  - 0.6A (max) Output Current (MAX20039)
  - 1.2A (max) Output Current (MAX20040)
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100
  - Increased Efficiency with Reduced BOM Cost and Board Space
  - Integrated FETs H-Bridge Architecture
  - Fixed Output Voltages
  - 20-Pin SWTQFN Package
- Low Quiescent Current Helps Designers Meet Stringent OEM Current Requirements (B and D Version only)
  - 52µA Quiescent Current when in Standby Mode
  - 10µA (max) Quiescent Current in Shutdown Mode
- High Switching Frequency Allows Use of Small External Components
  - 200kHz to 2.2MHz Operating Frequency
  - Skip Mode for Efficient Low-Power Operation (B and D version only)
  - Fixed-Frequency PWM Mode
  - External Frequency Synchronization
- Reduced EMI Emissions at the Switching Frequency
  - Spread Spectrum Can Be Enabled or Disabled

***Ordering Information* appears at end of data sheet.**

19-100271; Rev 15; 3/24

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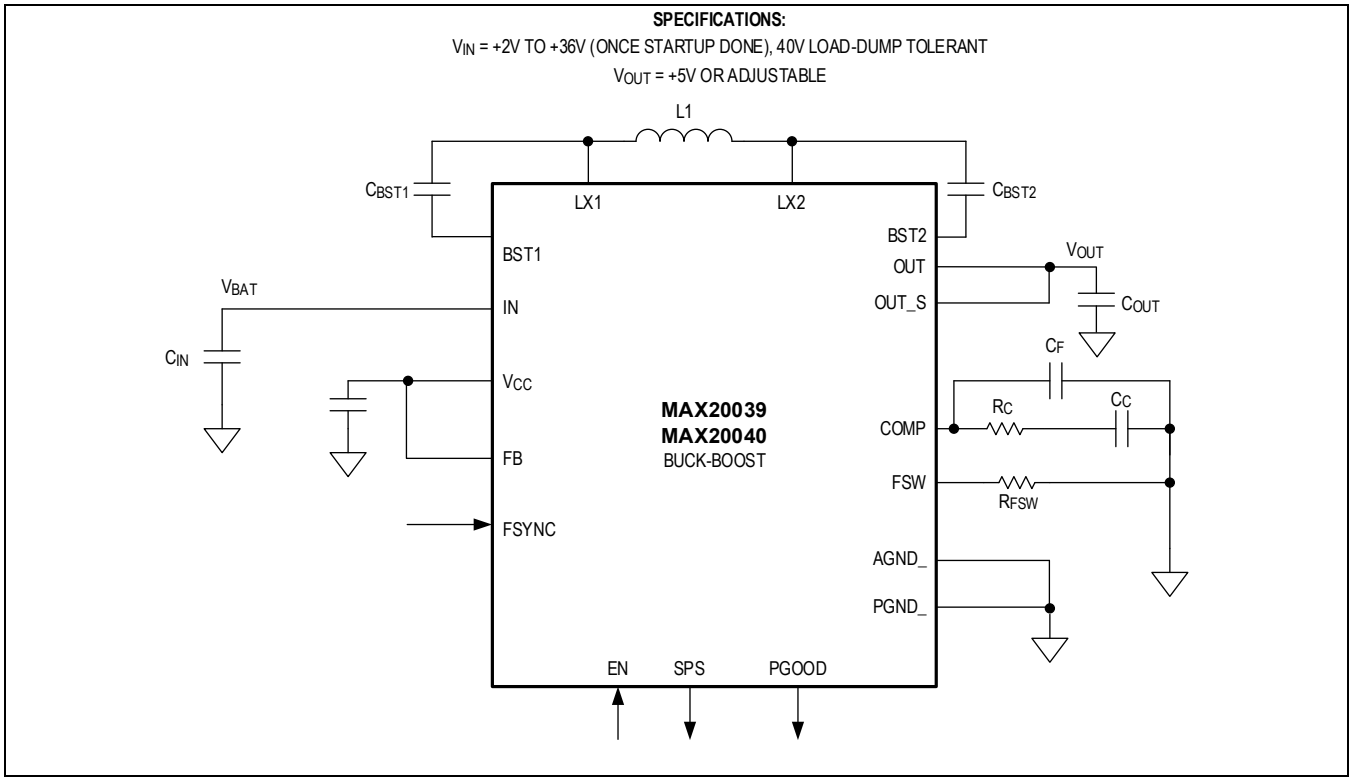
Typical Operating Circuit



Absolute Maximum Ratings

IN ..... -0.3V to +40V

EN, LX1 (Note 1) ..... -0.3V to V_{IN} + 0.3V

LX2 and OUT_S (Note 1) ..... -0.3V to V_{OUT} + 0.3V

OUT ..... -0.3V to +18V

BST1 to LX1, BST2 to LX2 (Note 2) ..... -0.3V to +5V

V_{CC}, PGOOD, SPS, FSYNC ..... -0.3V to +6V

COMP, FB, FSW ..... -0.3V to V_{CC} + 0.3V

PGND_ ..... -0.3V to +0.3V

Continuous Power Dissipation (Four-Layer Board) 20-pin SWTQFN, T_A = +70°C (derate 30.3 mW/°C above +70°C) 2424mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Soldering Temperature (reflow) ..... +260°C

Lead Temperature (soldering, 10s) ..... +300°C

Note 1: 5V is internally clamped.

Note 2: Self-protected against transient voltages exceeding these limits for ≤50ns under normal operation and loads up to the maximum rated output current.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range	T_A		-40 to +125	°C

Note: These limits are not guaranteed.

Package Information

SWTQFN-EP

Package Code	T2044Y+4C
Outline Number	*21-100068*
Land Pattern Number	*90-0409*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	33°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.*

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(V_{IN} = V_{EN} = 14V, T_A = -40°C to +125°C, T_J = -40°C to +150°C, C_{OUT} = 22µF, C_{VCC} = 2.2µF, unless otherwise noted. (*Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Normal operation (*Note 4*)	4.5		36	V
		After initial startup condition is satisfied (*Note 4*)	2			
Shutdown Supply Current	$I_{IN_SHUTDOWN}$	V_{EN} = 0V		3	10	µA
Standby Supply Current	$I_{IN_STANDBY_5V}$	V_{OUT} = 5V, no load, V_{FSYNC} = 0V, MAX20039BATPA/VY+, MAX20040BATPA/VY+, MAX20040DATPB/VY+		52	85	µA
Undervoltage Lockout	$UVLO_{IN_RISE}$	V_{IN} rising		4.2	4.45	V
	$UVLO_{IN_FALL}$	V_{IN} falling, output enabled			1.95	
V_{CC} REGULATOR						
Output Voltage	V_{CC}	V_{IN} > 6V, I_{VCC} = 1mA to 20mA	4.4	4.6	4.7	V
Dropout Voltage	V_{CCDROP}	V_{IN} = 3.5V, I_{VCC} = 20mA		0.15	0.4	V
Undervoltage Lockout	$UVLO_{VCC}$	V_{CC} rising		3.5	3.9	V
	$UVLO_{VCCFALL}$	V_{CC} voltage falling		3.2	3.65	
Short-Circuit Current Limit	I_{VCCSC}	V_{CC} shorted to AGND, after startup		50	85	mA
BUCK-BOOST CONVERTER						
Fixed Output Voltage	V_{OUT_5V}	V_{FB} = V_{CC}	4.91	5	5.08	V

(V_{IN} = V_{EN} = 14V, T_A = -40°C to +125°C, T_J = -40°C to +150°C, C_{OUT} = 22µF, C_{VCC} = 2.2µF, unless otherwise noted. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Voltage Adjustable Range	V_{OUT_ADJ}	MAX20039BATPB, MAX20040BATPB	4		15	V
		Other part numbers	4		12	
Soft-Start Ramp Time	t_{START}	V_{OUT} from 10% to 90%	4	7	10	ms
Autoretry	t_{AUTO}	Autoretry time after a fault condition has been detected		26		ms
Minimum On-Time	t_{ON_MIN}			85		ns
Minimum Off-Time	t_{OFF_MIN}	Buck mode, f_{SW} = 400kHz		300		ns
Dead Time	DT	Rising and falling edges (Note 5)		15		ns
LX1, LX2 Rise Time	t_{LX_RISE}	(Note 5)		5		ns
BST1 Switch On-Resistance	R_{ON_BST1}	V_{LX1} = 0V, I_{BST1} = 10mA		3.8	7.5	Ω
BST2 Switch On-Resistance	R_{ON_BST2}	V_{LX2} = 0V, I_{BST2} = 10mA		5	10	Ω
POWER MOSFET						
DMOS_ Resistance	$R_{DS(ON)_DMOS}$	V_{CC} = 4.5V, $I_{DS(ON)}$ = 0.2A		70	150	mΩ
LX1 Leakage Current	I_{LX1_LKG}	V_{EN} = 0V, V_{IN} = V_{LX1} = 36V, T_A = +25°C			1.0	µA
LX2 Leakage Current	I_{LX2_LKG}	V_{EN} = 0V, V_{LX2} = 12V, T_A = +25°C			1.0	µA
CURRENT SENSE (Note 6)						
Current Limit Threshold	I_{LIMIT1}	V_{FB} = V_{CC}, V_{OUT} = 5V (MAX20040)	1.9	2.15	2.5	A
		V_{FB} = V_{CC} , V_{OUT} = 5V (MAX20040D)		2.8		
	I_{LIMIT2}	V_{FB} = V_{CC}, V_{OUT} = 5V (MAX20039)	0.9	1.1	1.25	
ERROR AMPLIFIER						
Regulated Feedback Voltage	V_{FB}		1.234	1.25	1.266	V
FB Leakage Current	I_{FB_LKG}	V_{FB_LKG} = V_{CC}, T_A = +25°C			1	µA
FB Line-Regulation Error	R_{EGFB}	V_{IN} = 2V to 36V, V_{FB} = 1.25V		0.01		%/V
Transconductance (from FB to COMP)	gm	V_{FB} = 1.25V, V_{CC} = 4.5V	450	750	1000	µS
SWITCHING FREQUENCY						
FSW Voltage	V_{FSW}	I_{FSW} = 10µA	1.21		1.26	V
PWM Switching Frequency	f_{SW1}	R_{FSW} = 12kΩ	2.00	2.20	2.35	MHz
	f_{SW2}	R_{FSW} = 73.2kΩ	380	415	450	kHz
PWM Switching-Frequency Range	f_{RNG}		0.200		2.2	MHz
FSYNC External Clock Input	f_{SYNC1}	Minimum sync pulse of 100ns, R_{FOSC} = 12kΩ (Note 7)		2.2		MHz
	f_{SYNC2}	Minimum sync pulse of 100ns, R_{FOSC} = 73.2kΩ (Note 7)		440		kHz
Spread Spectrum	SPS	Spread spectrum enabled (Note 5)		$f_{SW_}$ ±3		%
OUTPUT MONITORS						
Output Overvoltage Threshold	$V_{OUT_OVP_R}$	Detected with respect to V_{FB} rising	105.5	108	110.8	%
	$V_{OUT_OVP_F}$	Detected with respect to V_{FB} falling	102.5	105	107.8	

(V_{IN} = V_{EN} = 14V, T_A = -40°C to +125°C, T_J = -40°C to +150°C, C_{OUT} = 22µF, C_{VCC} = 2.2µF, unless otherwise noted. (*Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Threshold Rising	P_{GOOD_R}	% of V_{OUT}, rising	94	96	98.3	%
PGOOD Threshold Falling	P_{GOOD_F}	% of V_{OUT}, falling	91	93	95.6	%
PGOOD Output Low Voltage	V_{PGOODL}	I_{SINK} = 1mA			0.3	V
PGOOD Leakage Current	I_{PGOOD_LEAK}	V_{PGOOD} = V_{CC}, T_A = +25°C			1	µA
PGOOD Debounce Time	t_{PGOOD}	Fault detection, rising		60		µs
		Fault detection, falling		4		
LOGIC INPUTS (EN, FSYNC, SPS)						
Input High Level		V_ rising	2.1			V
Input Low Level		V_ falling			0.8	V
EN, SPS Input Leakage Current	I_{IN_LEAK}	V_ = V_{CC}, T_A = +25°C			1	µA
FSYNC Pulldown Resistance	$R_{FSYNC-PD}$			1		MΩ
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	$T_{SHUTDOWN}$			166		°C
Thermal-Shutdown Hysteresis	T_{HYS}			18		°C

Note 3: All limits are 100% tested at +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are at T_A = +25°C.

Note 4: The input voltage range depends on the output voltage (see the *Ordering Information* table).

Note 5: Guaranteed by design; not production tested.

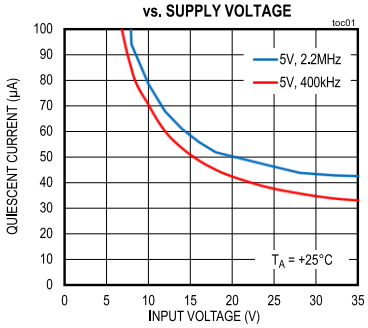
Note 6: Current measurements are performed when the part is not switching. The current-limit values measured in operation are higher due to the propagation delay of the comparators.

Note 7: The external clock frequency applied at the FSYNC pin must be within -10% to 0% of the nominal switching frequency set by the resistor connected to the FSW pin.

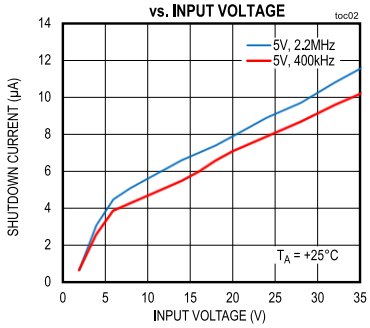
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

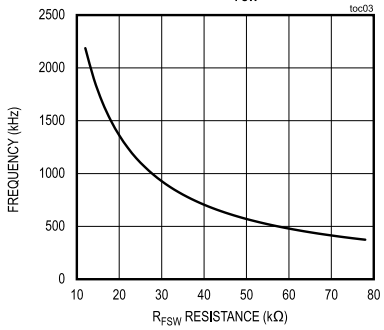
STANDBY QUIESCENT CURRENT vs. SUPPLY VOLTAGE



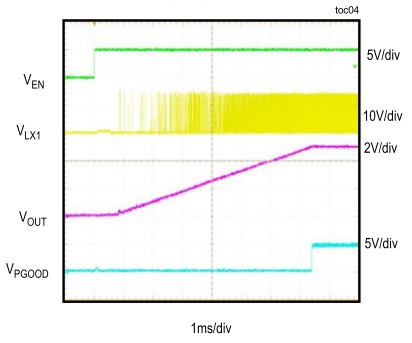
SHUTDOWN CURRENT vs. INPUT VOLTAGE



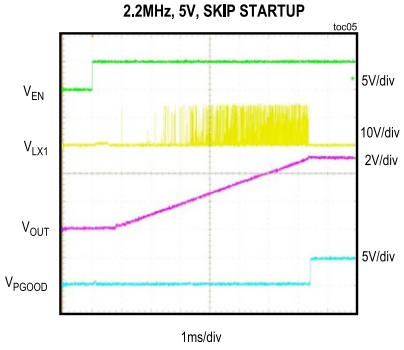
FREQUENCY vs. R_{FSW} RESISTANCE



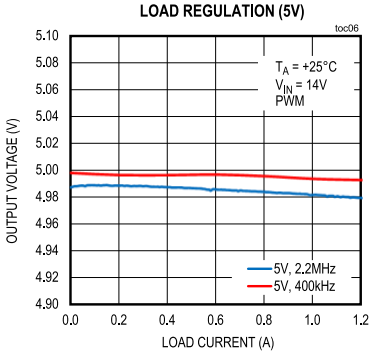
2.2MHz, 5V, PWM STARTUP



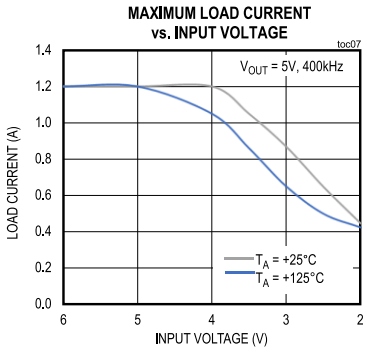
2.2MHz, 5V, SKIP STARTUP



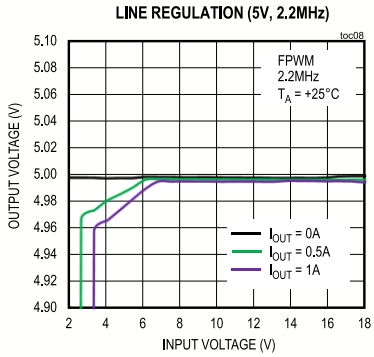
LOAD REGULATION (5V)



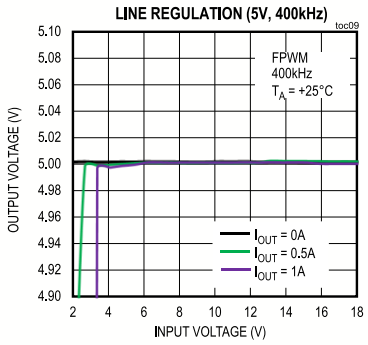
MAXIMUM LOAD CURRENT vs. INPUT VOLTAGE



LINE REGULATION (5V, 2.2MHz)

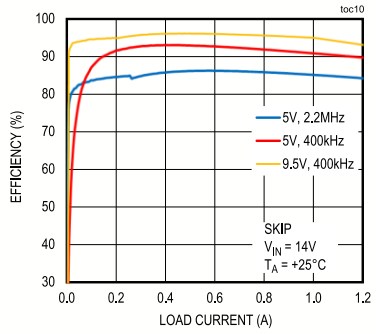


LINE REGULATION (5V, 400kHz)

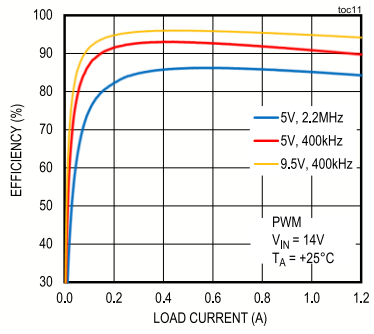


(T_A = +25°C, unless otherwise noted.)

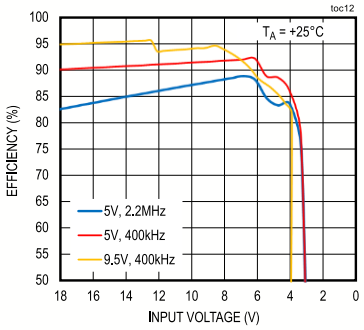
EFFICIENCY vs. LOAD CURRENT



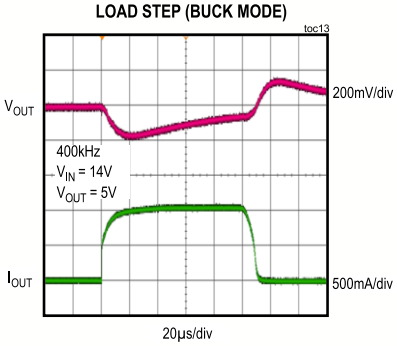
EFFICIENCY vs. LOAD CURRENT



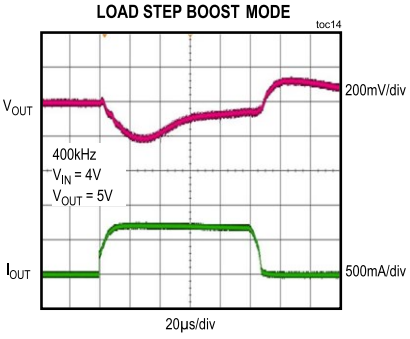
EFFICIENCY vs. INPUT VOLTAGE



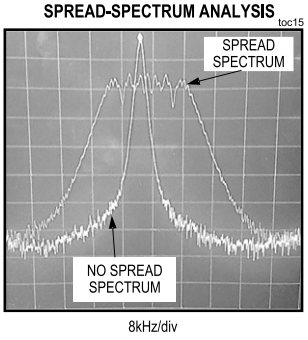
LOAD STEP (BUCK MODE)



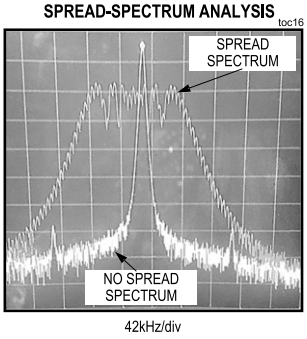
LOAD STEP BOOST MODE



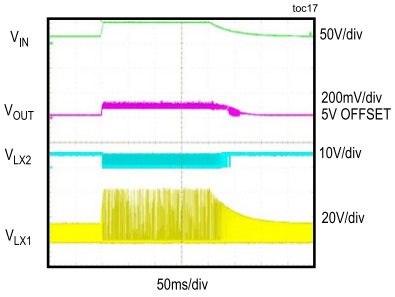
400kHz, BUCK MODE SPREAD-SPECTRUM ANALYSIS



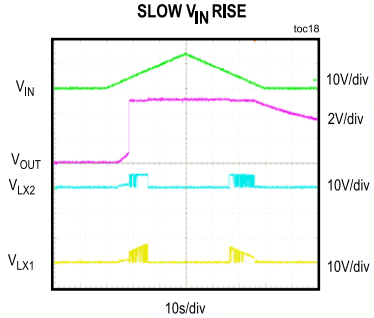
2.2MHz, BUCK MODE SPREAD-SPECTRUM ANALYSIS



2.2MHz, 5V, PWM LOAD DUMP

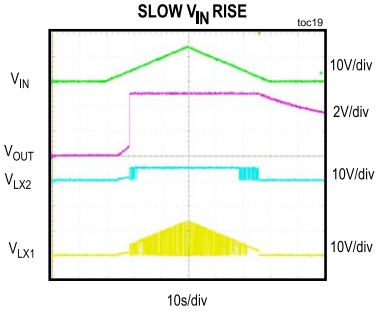


2.2MHz, 5V, SKIP SLOW V_{IN} RISE

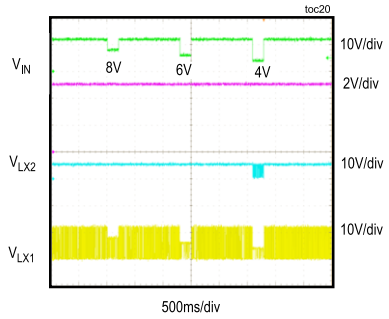


(T_A = +25°C, unless otherwise noted.)

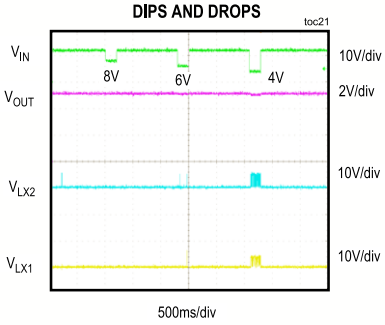
2.2MHz, 5V, PWM
SLOW V_{IN} RISE



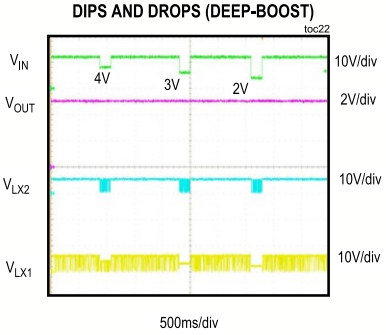
2.2MHz, 5V, PWM
DIPS AND DROPS



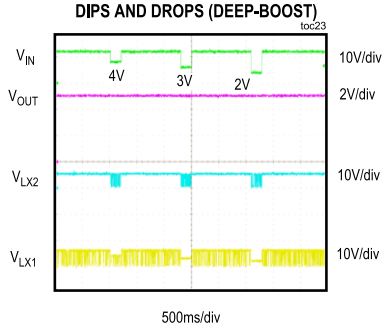
2.2MHz, 5V, SKIP
DIPS AND DROPS



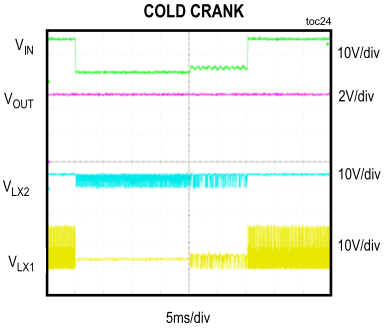
2.2MHz, 5V, PWM
DIPS AND DROPS (DEEP-BOOST)



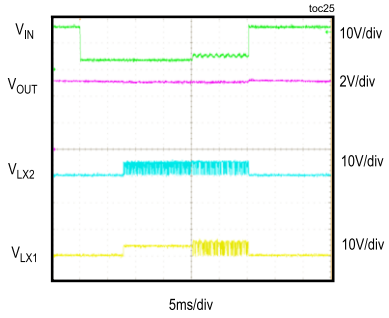
2.2MHz, 5V, SKIP
DIPS AND DROPS (DEEP-BOOST)



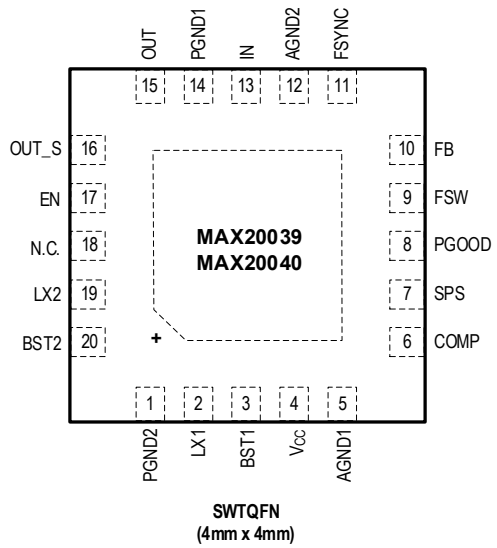
2.2MHz, 5V, PWM
COLD CRANK



2.2MHz, 5V, SKIP
COLD CRANK



Pin Configurations



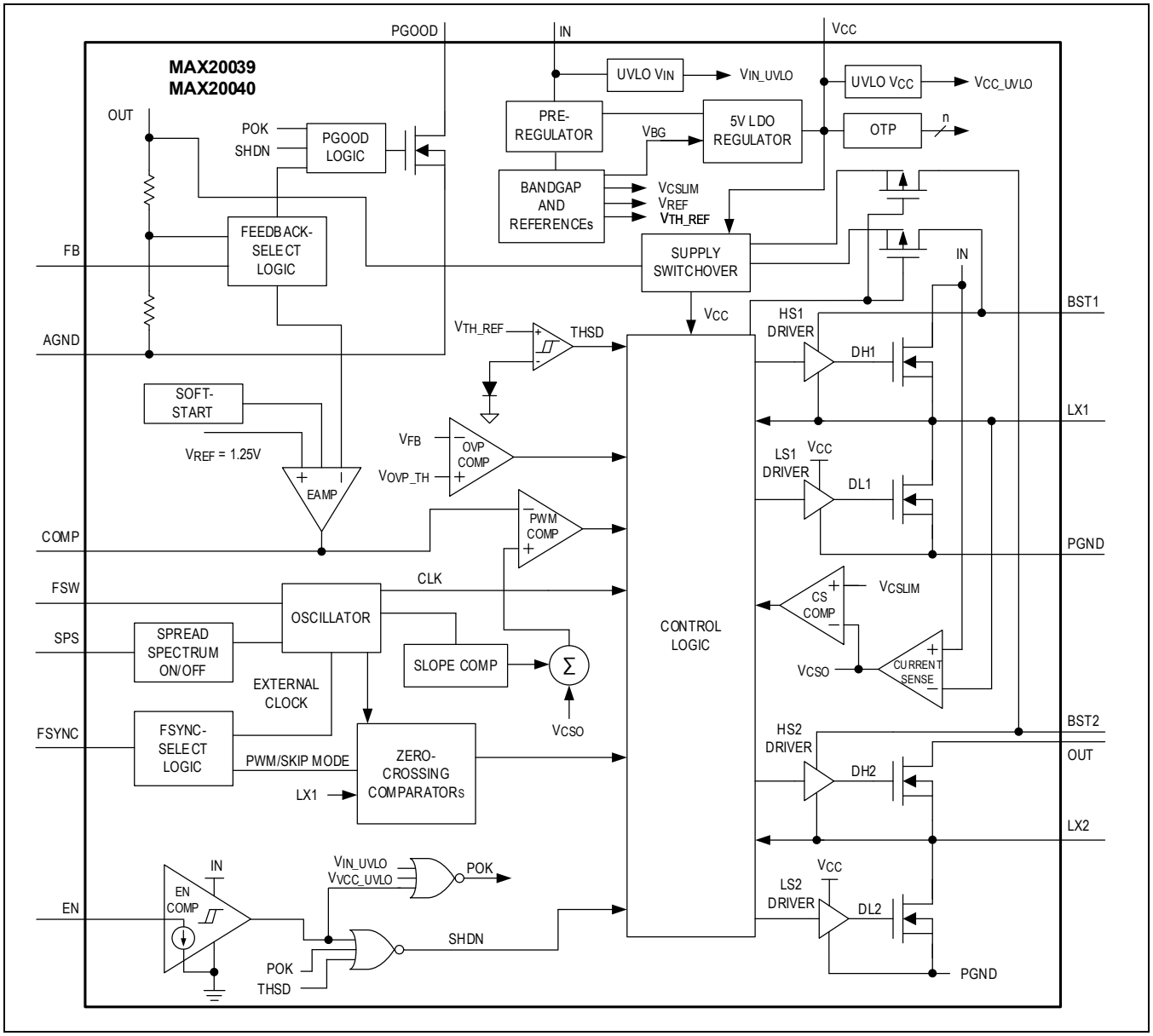
SWTQFN
(4mm x 4mm)

Pin Descriptions

PIN	NAME	FUNCTION
1	PGND2	Ground Reference for the Boost Low-Side Integrated FETs
2	LX1	IN to PGND Switching Node
3	BST1	Bootstrap Capacitor for High-Side Driver of LX1 Node. Connect a 100nF capacitor between BST1 and LX1.
4	V_{CC}	Linear Regulator Output. V_{CC} powers up the internal circuitry. Bypass with 2.2µF ceramic capacitor to AGND.
5	AGND1	Analog Ground of the IC. Connect to ground-plane reference of the PCB.
6	COMP	External Compensation. Connect the External Compensation Network of the Loop.
7	SPS	Spread-Spectrum Enable/Disable Pin. Pull high for spread spectrum on and low for spread spectrum off.
8	PGOOD	Open-Drain Output, Active-High Power-Good Indicator. PGOOD asserts when V_{OUT} is above 96% of regulation point. PGOOD goes low when V_{OUT} is below 93% of regulation point.
9	FSW	Internal-Oscillator Pin for Setting the Switching-Frequency. Connect a resistor to ground to set the desired frequency.
10	FB	Feedback Analog Input. Connect an external resistive divider from OUT to FB and AGND to set the desired output voltage. Connect to V_{CC} to set the output voltage to 5V.
11	FSYNC	Synchronization Input. Connect to AGND to enable skip mode of operation during light load. Connect to V_{CC} to force PWM mode during light-load operation. FSYNC has a 1MΩ internal pull-down.
12	AGND2	Analog Ground Reference
13	IN	Voltage-Supply Input. IN powers the internal voltage regulator. Bypass IN to PGND with a 4.7µF (min) ceramic capacitor.
14	PGND1	Ground Reference for the Buck Low-Side Integrated FETs
15	OUT	Switching-Regulator Voltage Output
16	OUT_S	Regulator Voltage-Sense Input
17	EN	High Voltage-Enable Input
18	N.C.	No Connection. Not internally connected to any circuitry.
19	LX2	OUT to PGND Switching Output Node

20	BST2	Bootstrap Capacitor for High-Side Driver of the LX2 Node. Connect a 100nF from BST2 to LX2.
—	EP	Exposed Pad

Functional Diagrams



Detailed Description

The MAX20039/MAX20040 are 0.6A/1.2A current-mode buck-boost converters, with integrated H-bridge architecture. The devices operate with input voltages from 3.5V to 36V while using only 52µA quiescent current at no load. Once the startup conditions are satisfied, the devices can operate over an extended input voltage range of 2V to 36V. The switching frequency is resistor programmable from 200kHz to 2.2MHz and can be synchronized to an external clock. The devices' output voltage is available as 5V fixed, or adjustable from 4V to 15V. The wide input voltage range, along with its ability to maintain constant output voltage during battery transients, make the devices ideal for automotive applications. In light-load applications, a logic input (FSYNC) allows the devices to operate either in skip mode for reduced current consumption, or fixed-frequency, forced-PWM mode to eliminate frequency variation and help minimize EMI. Protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery.

Linear Regulator Output (V_{CC})

The converters include a 4.6V linear regulator (V_{CC}) that provides power to the internal circuit blocks. Connect a 2.2µF ceramic capacitor from V_{CC} to AGND. Once the startup sequence is complete, V_{CC} is powered from the OUT pin to enable operation for IN down to 2V.

Wide Input Voltage Range

The converters include one supply input (IN) specified for a wide 3.5V to 36V input voltage range. Once the initial startup condition is satisfied (BIAS > UVLO and IN > 3.5V), the device operates from an extended 2V to 36V input range. The IN pin provides power to the internal BIAS supply, as well as to the four H-bridge MOSFETs. Once the output voltage is above 3.2V and the startup of the switching regulator is complete, the BIAS voltage is powered from the OUT pin. Due to the H-bridge buck-boost architecture, this enables the IC to operate from a 2V input after initial power-up is complete.

Synchronization Input (FSYNC)

FSYNC is a logic-level input useful for operating-mode selection and frequency control. Connecting FSYNC to BIAS or an external clock enables fixed-frequency, forced-PWM operation. Connecting FSYNC to AGND enables skip-mode operation. The external clock frequency at FSYNC can be lower than the internal clock by 10%. The device synchronizes to the external clock in two cycles. When the external clock signal at FSYNC is absent for more than two clock cycles, the device uses the internal clock.

Power-Good Output (PGOOD)

The converters feature an open-drain power-good output (PGOOD). PGOOD asserts when V_{OUT} rises above 96% of its regulation voltage, and deasserts when V_{OUT} drops below 93% of its regulation voltage. Connect PGOOD to BIAS with a 10kΩ resistor.

Spread-Spectrum Option

Spread spectrum can be enabled on the converters using the SPS pin. When SPS is pulled high, spread spectrum is enabled and the operating frequency is varied ±3% centered on f_{OSC}. The modulation signal is a triangular wave with a period of 110µs at 2.1MHz; therefore, f_{OSC} ramps down 3% and back to 2.2MHz in 110µs and also ramps up 3% and back to 2.1MHz in 110µs. This cycle continues to repeat. For operations at f_{OSC} values other than 2.1MHz, the modulation signal scales proportionally (e.g., at 400kHz, the 110µs modulation period increases to 110µs x 2.2MHz / 0.4MHz = 550µs). The internal spread spectrum is disabled if the device is synchronized to an external clock; however, the device does not filter the input clock on the FSYNC pin and passes any modulation (including spread spectrum) present on the driving external clock.

Internal Oscillator (FSW)

The switching frequency is set by a resistor (R_{FSW}) connected from the FSW pin to AGND (e.g., a 400kHz switching frequency is set with R_{FSW} = 73.2kΩ). Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the converters. When the junction temperature exceeds +166°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down converter, allowing the device to cool. The thermal sensor turns on the device again after the junction temperature cools by 18°C.

Light-Load Operation

Under light loads, when FSYNC is connected to AGND and the converters are in buck region, the device starts skipping cycles to maintain high efficiency. After the device detects 32 consecutive zero crossings of the inductor current, it enters PFM mode. During this mode, the peak inductor current limit is changed to ~480mA (~240mA for the 0.6A MAX20039) and inductor current is prevented from going negative. This causes the output voltage to rise. Once the output voltage rises above 103% of the regulation value, the device stops switching. The switching resumes once the output voltage falls below 101% of the regulation value. The load current at which the device enters PFM mode depends on the inductor current and inductor used.

Soft-Start

A fixed-frequency auxiliary oscillator determines the soft-start time for the converters; hence, all output voltages and frequency have a 7ms (typ) soft-start time.

Overvoltage Protection

The converters come with a cycle-by-cycle overvoltage protection. A dedicated internal comparator monitors the output voltage with fixed thresholds. If the output voltage goes higher than 108% (typ) of the regulated value, the buck high-side switch (DH1) and boost low-side switch (DL2) are turned off. The switching is turned off until the output voltage falls below 105% (typ) of the regulated value.

Short-Circuit Protection

The converters continuously monitors the DH1 current for a quick and robust short-circuit protection. If the input current consecutively hits the peak current limit 16 times and the output voltage is less than 60% of the regulation value, the device stops switching and enters hiccup mode. The autoretry time in hiccup mode is 26ms (typ).

Applications Information

Inductor Selection

Design of the inductor is a compromise between the size, efficiency, control, bandwidth, and stability of the converter. For a buck-boost application, selecting the right value of inductor becomes even more critical due to the presence of right-half-plane (RHP) zero in boost and buck-boost mode. A bigger inductance value would reduce RMS current loss in MOSFETs, core, and winding losses in the inductor. On the other hand, it slows the control loop and reduces the frequency of the RHP zero, which can cause stability concerns.

Start the selection of the inductor based on the inductor current ripple as a percentage of the maximum inductor current in buck and boost modes using Equations 1 and 2. Typically, 40% ripple of the maximum inductor current is a good compromise between speed and efficiency.

Equation 1:

$$L_{BUCK} > \frac{(V_{IN_{MAX}} - V_{OUT}) \times V_{OUT}}{f_{SW} \times I_{LMAX} \times \%\Delta I_{RIPPLE} \times V_{IN_{MAX}}}$$

Select the final value of inductance considering the ripple in both regions of operation, including RHP zero. Once the final value of inductance is selected, calculate the peak inductor current and choose an inductor with saturation current ≈20% more than the peak inductor current and the low DCR.

Peak Inductor Current

Inductors are rated for maximum saturation current. The maximum inductor current equals maximum load current, in addition to half of the peak-to-peak ripple current. For the selected inductance value, the actual peak is calculated as shown in Equation 2.

Equation 2:

$$I_{LPEAK} = \frac{V_{OUT} \times I_{OUT}}{V_{IN_{MIN}}} + \frac{V_{IN_{MIN}} \times \left(1 - \frac{V_{IN_{MIN}}}{V_{OUT}}\right)}{L \times f_{SW} \times 2}$$

Input Capacitor Design

The input capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit switching. For operation in buck mode, the input capacitor sees discontinuous input current and should be designed to handle the input RMS current given by Equation 3.

Equation 3:

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

The maximum input RMS current occurs at V_{IN} = 2 x V_{OUT} given by Equation 4.

Equation 4:

$$I_{RMS} = \frac{I_{LOAD}}{2}$$

Output Capacitor Design

To calculate the worst-case minimum output capacitance in “deep” boost mode (V_{IN-MIN} and heavy load current), see Equation 5.

Equation 5:

$$C_{OUT-MIN} \geq \frac{I_{OUT_{MAX}} \times D_{MAX}}{f_{SW} \times \Delta V_{OUT}}$$

where D_{MAX} = 0.98 A lower output capacitance can be used if not operating in a deep-boost-mode state.

The output-filter capacitor must have low enough equivalent series resistance (ESR) to meet output-ripple and load-transient requirements. The allowable output-voltage ripple, and the maximum deviation of the output voltage during load-

step currents, determines the output capacitance and its ESR. The output ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions, without tripping the overvoltage-fault protection. Use low-ESR ceramic or aluminum electrolytic capacitors at the output. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple, so the size of the output capacitor depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications.

Equation 6:

$$V_{RIPPLE(P-P)} = ESR \times I_{OUT_{MAX}} \times LIR$$

where: LIR = 0.4 (LIR is the ratio of peak-to-peak (P-P) ripple current with maximum inductor current; 40% or 0.4 is a good assumption for this parameter) The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge to be equal. When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent voltage droop and voltage rise from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem. However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability.

Output-Voltage Setting

Connect FB to V_{CC} to enable the fixed output voltage (5V) set by a preset internal resistive voltage-divider connected between the feedback pin (FB) and AGND. To externally adjust the output voltage between 4V and 15V, connect a resistive divider from the output (OUT) to FB to AGND. Calculate R_{FB1} and R_{FB2} using Equation 7.

Equation 7:

$$R_{FB1} = R_{FB2}\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where V_{FB} = 1.25V (typ) and R_{FB2} is < 50kΩ and can be typically set to 10kΩ. See *Figure 1*.

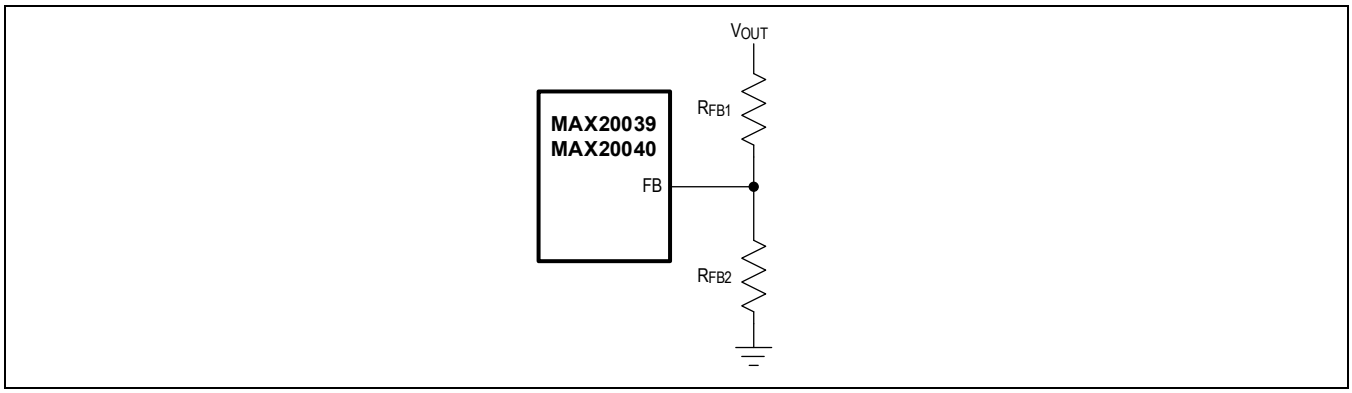


Figure 1. Setting the Output Voltage

Error-Amplifier Compensation Design for the MAX20040

The MAX20040 converter uses an internal transconductance amplifier, with its inverting input and output terminals available to the user for external frequency compensation (see *Figure 2*).

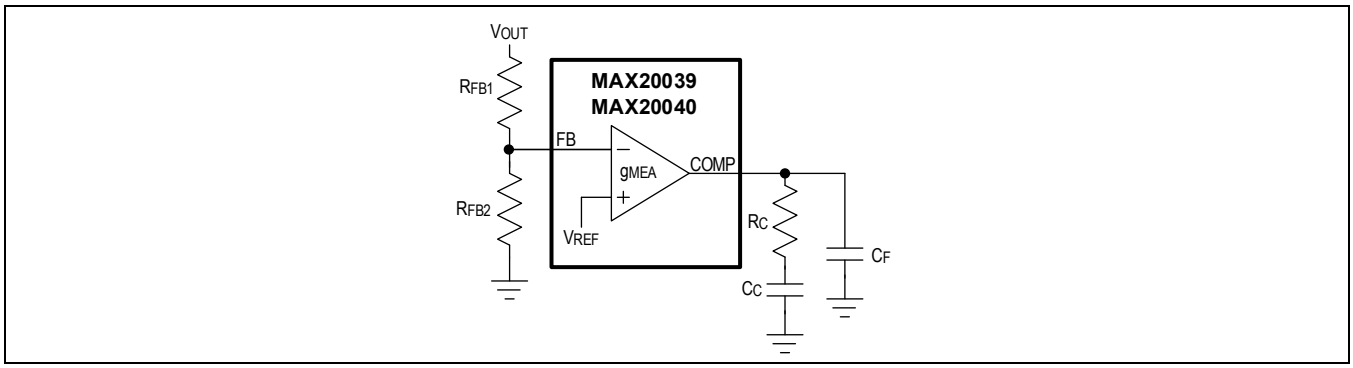


Figure 2. Compensation Network

The controller uses a peak current-mode-controlled architecture that regulates the output voltage by forcing the required current through the external inductor. Current-mode control splits the double pole in the feedback loop caused by the inductor and output capacitor into two single poles. One of the poles is moved to a high frequency outside the typical bandwidth of the converter, making it a single-pole system. This makes compensation easy with just Type II required to compensate the loop. In boost-mode, an extra right half-plane (RHP) zero is introduced by the power stage that adds extra phase delay in the control loop. To avoid any significant effect of the RHP zero on the converter stability, the compensation is designed such that the bandwidth is approximately 1/4th of the worst-case RHP zero frequency.

The design of external compensation requires some iterations to reach an optimized design. Care must be taken while designing the compensation for working in deep-boost mode and heavy load (VIN-MIN), as RHP zero frequency reduces.

A convenient way to design compensation for both buck and boost modes is to design the compensation at minimum input voltage and heavy load (deep-boost mode). At this operating point, RHP zero is at its lowest frequency. Design the compensation to achieve a bandwidth of 1/5th or lower of the RHP zero frequency. The closed-loop gain of the converter would be a combination of the power-stage gain of the converter and error-amplifier gain, where the converter's frequencies are shown below.

Equation 8:

$$f_{pBOOST} = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}}$$

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{zRHP} = \frac{R_{LOAD} \times (1 - D)^2}{2\pi \times L}$$

where the error-amplifier's frequencies are:

Equation 9:

$$f_{pdEA} = \frac{1}{2\pi \times (R_{O_EA} // R_C) \times C_C}$$

where:

R_{O_EA} is the output impedance of the error amplifier and is 18MΩ (typ). The parallel resistance of the R_{O_EA} and R_C leaves R_C as the dominating factor. A simplified equation can be:

$$f_{pdEA} = \frac{1}{(2\pi \times R_C \times C_C)}$$

Equation 10:

$$f_{zEA} = \frac{1}{2\pi \times R_C \times C_C}$$

$$f_{pEA} \cong \frac{1}{2\pi \times R_C \times C_F}$$

if $C_F << C_C$

To properly design for stability, use the following list of instructions (see *Table 1* for a design example):

1. Calculate the minimum inductance needed (L).
2. Calculate the right-half-place zero (f_{zRHP}) inherent to the boost converter.
3. Place the crossover frequency (f_C) such that it is 1/5th or lower of f_{zRHP}.
4. Calculate the remaining power-stage factors (f_{pBOOST} and f_{zMOD}).
5. Set the bandwidth to 1/5th or lower of the RHP: $f_{BW} = f_{zRHP}/5$.
6. Select the error-amplifier compensation such that:
   - f_{zEA} is 1/3rd of f_C.
   - Once the error-amplifier zero is known, calculate f_{pdEA}.
   - f_{pEA} is placed high enough to not interfere with the buck-mode frequency response. In boost-only mode, f_{pEA} can be placed at f_{zMOD} or f_{zRHP}, which is the lower frequency.

Start the design by setting the output voltage and switching frequency for the controller. Selecting R_{FB2} = 10kΩ gives R_{FB1} = 54.2kΩ, using Equation 7, to set the output voltage to 8V. Connect a 73.2kΩ between pin R_{FSW} and AGND to set the switching frequency to 400kHz.

Table 1. Design Example

PARAMETERS	VALUE
V_{OUT}	8V
f_{SW}	400kHz
V_{SUP}	3V to 18V
I_{OUT}	1.2A (max)

Inductor Design

Start the inductor selection by assuming 40% current ripple in buck mode. Use Equations 11 and 12 for the minimum inductance.

Equation 11:

$$L_{BUCK} > \frac{(V_{IN_{MAX}} - V_{OUT}) \times V_{OUT}}{f_{SW} \times I_{L_{MAX}} \times \%\Delta I_{RIPPLE} \times V_{IN_{MAX}}} = 23\mu H$$

Using the above calculation, select the closest standard value of 22µH.

Equation 12:

$$I_{L_{PEAK}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN_{MIN}}} + \frac{V_{IN_{MIN}} \times \left(1 - \frac{V_{IN_{MIN}}}{V_{OUT}}\right)}{L \times f_{SW} \times 2} = 3.31A$$

Select an inductor where saturation (I_{SAT}) current is at least 20% higher than the peak inductor current.

For a converter operating in boost mode, the inductor selection determines the right half-plane frequency and hence the stability of the converter in deep-boost mode. Calculate the RHP zero frequency in deep-boost mode using the calculated inductor value shown in Equation 13.

Equation 13:

$$f_{zRHP} = \frac{R_{LOAD} \times (1 - D)^2}{2\pi \times L} = 6.6kHz$$

With RHP zero at 6.6kHz, the loop crossover frequency (f_C) must be less than 1/5th or lower of the RHP zero frequency in deep-boost mode for stable operation.

Output Capacitor Design

With a maximum duty cycle of 0.98 and under the worst-case condition (low V_{IN}, heavy load current), calculate the minimum output capacitance following Equation 14.

Equation 14:

$$C_{OUT_{MIN}} = \frac{I_{OUT_{MAX}} \times D_{MAX}}{f_{SW} \times \Delta V_{OUT}} = 118\mu F$$

Error-Amplifier Compensation Design

Start the compensator design by calculating the critical frequencies for boost power stage at minimum input voltage and maximum load (see Equation 15).

Equation 15:

$$f_{pBOOST} = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}} = 415Hz$$

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}} = 337kHz$$

With RHP zero at 6.6kHz, the target bandwidth (f_C) for the closed-loop converter should be ≤ 1.32kHz (1/5th of the RHP) for stable operation. The zero of the error amplifier must be placed well below the bandwidth to give enough phase boost at the crossover frequency. Typically, the zero is placed close to the low-frequency pole. In such a case, resistor R_C of the compensation can be calculated using Equation 16.

Equation 16:

$$R_C = 2\pi \times f_C \times \frac{R_{CB} \times C_{OUT}}{g_m \times (1 - D_{BOOST})} \times \frac{(R_{FB2} + R_{FB1})}{R_{FB2}} = 13.92k\Omega$$

where: R_{CS} = 0.6Ω and g_m = 712µS (typ) (or 750µS (typ) from the *Electrical Characteristics* table can be used).

Choosing f_C = 1.32kHz and placing the f_{zEA} at 440Hz (1/3rd the f_C), the result is shown in Equation 17.

Equation 17:

$$C_C = \frac{1}{2\pi \times R_C \times f_{zEA}} = 26nF$$

C_F decides the location of the high-frequency pole. Select the high-frequency-pole location higher than the bandwidth in buck mode so it does not affect the phase margin and helps attenuate any high-frequency noises. Setting f_{pEA} to 100kHz is typically sufficient.

Equation 17:

$$C_F = \frac{1}{2\pi \times R_C \times f_{pEA}} = 114pF$$

For this particular application, select the error amplifier's compensation as (approximating to closest standard values):

R_C = 15kΩ, C_C = 22nF, and C_F = 100pF

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1. Use a large contiguous copper plane under the device package. Ensure that all heat-dissipating components have adequate cooling. The bottom pad of the device must be soldered down to this copper plane for effective heat dissipation and to achieve full power out of the device. Use multiple vias or a single large via in this plane for heat dissipation.
2. Isolate the power components and high-current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
3. Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path comprising input capacitor, high-side FET, inductor, and output capacitor should be as short as possible.
4. Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
5. The analog signal lines should be routed away from the high-frequency planes. This ensures integrity of sensitive signals feeding back into the device.
6. The ground connection for the analog and power section should be close to the device. This keeps the ground-current loops to a minimum. In cases where only one ground is used, adequate isolation between analog return signals and high-power signals must be maintained.

Ordering Information

PART	PIN-PACKAGE	V_{OUT} (ADJUSTABLE)	f_{SW}	V_{IN} (V)	V_{OUT} (DEFAULT)	CURRENT (A)	I_{LIM} (A) (min)	MODE
MAX20039ATPA/VY+	20 SWTQFN-EP*	4 to 9	200kHz to 2.2MHz	2 to 36	5	0.6	0.9	FPWM only
		9 to 12	< 500kHz	8 to 36				
MAX20039BATPA/VY+	20 SWTQFN-EP*	4 to 12	200kHz to 2.2MHz	2 to 36	5	0.6	0.9	SKIP or FPWM
MAX20039BATPB/VY+	20 SWTQFN-EP*	4 to 15	200kHz to 2.2MHz	2 to 36	5	0.6	0.9	SKIP or FPWM
MAX20040ATPA/VY+	20 SWTQFN-EP*	4 to 9	200kHz to 2.2MHz	2 to 36	5	1.2	1.9	FPWM only
		9 to 12	< 500kHz	8 to 36				
MAX20040BATPA/VY+	20 SWTQFN-EP*	4 to 12	200kHz to 2.2MHz	2 to 36	5	1.2	1.9	SKIP or FPWM
MAX20040BATPB/VY+	20 SWTQFN-EP*	4 to 15	200kHz to 2.2MHz	2 to 36	5	1.2	1.9	SKIP or FPWM
MAX20040DATPA/VY+	20 SWTQFN-EP*	4 to 12	200kHz to 2.2MHz	2 to 36	5	1.2	2.5	SKIP or FPWM
MAX20040FATPA/VY+ ♦	20 SWTQFN-EP*	4 to 12	200kHz to 2.2MHz	2 to 36	5	1.2	1.9	SKIP or FPWM

Note: All devices operate over the -40°C to +125°C automotive temperature range.

V Denotes an AEC-Q100 automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

SW = Side-wettable package.

**EP = Exposed pad.*

♦ *Supports input transients below UVLO (1.95V).*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	09/21	Initial release	—
1	3/18	Updated MAX20040ATPB/VY+ in Ordering Information	19
2	5/18	Updated data sheet title (changed 2.1MHz to 2.2MHz), Typical Operating Circuit, Current Sense section in the Electrical Characteristics, Note 5, TOCs 21–34 in Typical Operating Characteristics, Pin Description, Light-Load Operation, Error-Amplifier Compensation Design for the MAX20040, Inductor Design, Error-Amplifier Compensation Design, and Ordering Information sections	1–20
3	7/18	Removed future product status from the MAX20040CATPA/VY+ variant in Ordering Information	19
4	10/18	Added Notes 1 and 2, changed BST1 to LX1, BST2 to LX2 (from -03V to +6V to -03V to +5V), and deleted the BST1 and BST2 rows in the Absolute Maximum Ratings section, renumbering the remaining notes through end of Electrical Characteristics; replaced diodes going from Supply Switchover block to Control Logic block in Functional Block Diagram with pMOS symbols; changed f_{SW} (from 500MHz to 500kHz) for the MAX20040CATPA/VY+ variant in Ordering Information	3–5, 13, 19
5	3/19	Updated General Description, Benefits and Features, Electrical Characteristics, Typical Operating Characteristics, Detailed Description, and Ordering Information	1, 3–10, 12–17
6	4/19	Removed future-part designation from MAX20040BATPA/VY+ and MAX-20040DATPA/VY+ in Ordering Information	17
7	5/19	Added adjustable V_{OUT} column to Ordering Information	17
8	5/19	Removed future-part designation from MAX20039BATPA/VY+ in Ordering Information	17
9	8/19	Updated General Description, Electrical Characteristics, Detailed Description, and Applications Information; added future-parts MAX20039BATPB/VY+ and MAX20040BATPB/VY+ to Ordering Information	1, 5,12,14, 17
10	12/19	Removed all remaining future-part notation from Ordering Information	17
11	9/20	Updated Equation 9 in Applications Information and V_{OUT} (ADJUSTABLE) column in Ordering Information	16, 19
12	10/21	Updated Electrical Characteristics and Ordering Information	4, 6, 19
13	2/22	Updated Ordering Information	19
14	9/22	Updated Ordering Information	19
15	3/24	Updated Electrical Characteristics and Ordering Information	4, 19

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