Click here for production status of specific part numbers-

MAX20457

High-Efficiency, 36V, Dual Synchronous Buck Converters (3.5A/2A) for Automotive Applications

General Description

The MAX20457 offers two automotive grade synchronous buck converters with fixed frequency of either 2.1MHz or 400kHz. The two high-voltage synchronous step-down converters operate 180° out-of-phase. The IC operates with an input voltage supply from 3.5V to 36V and can operate in dropout conditions by running at 95% duty cycle. It is intended for applications with mid- to high-power requirements that operate at a wide input voltage range such as during automotive cold-crank or engine stop-start conditions.

High switching frequency up to 2.1MHz allows small external components, reduced output ripple, and guarantees no AM band interference. The switching frequency is fixed at 400kHz or 2.1MHz. FSYNC input programmability enables three modes for optimized performance: forced fixed-frequency operation, skip mode with ultra-low quiescent current, and phase-locked synchronization to an external clock. The spread spectrum option minimizes EMI interference.

The IC features the power-OK indicators and undervoltage lockout for the buck converters. Protection features include cycle-by-cycle current limit and thermal shutdown. The MAX20457 is specified for operation over the -40°C to +125°C automotive temperature range.

Applications

- Automotive Start-Stop System
- Instrument Cluster
- Distributed DC Power Systems
- Navigation and Radio Head Units

Benefits and Features

- Meets Stringent OEM Module Power Consumption and Performance Specifications
  - 10µA Supply Current with 5V Buck On
  - 8µA Supply Current with 3.3V Buck On
  - 10µA Supply Current with Both Bucks On
- Enables Crank-Ready Designs
  - Wide Input Supply Range from 3.5V to 36V
- EMI Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range
  - 20ns (typ) Minimum On-Time Guarantees Skip-Free Operation for 3.3V Output at 2.1MHz
  - Spread-Spectrum Option
  - Phase-Locked Loop (PLL) Frequency Synchronization
- Integration and Thermally Enhanced Packages Save Board Space and Cost
  - Two 2.1MHz Current-Mode Converters with Forced Fixed Frequency and Skip Modes
  - Thermally Enhanced 5mm x 5mm, 28-Pin TQFN-EP Package
- Protection Features Improve System Reliability
  - Supply Undervoltage Lockout
  - Overtemperature and Short-Circuit Protection

Ordering Information *appears at end of data sheet.*

19-100476; Rev 3; 11/19

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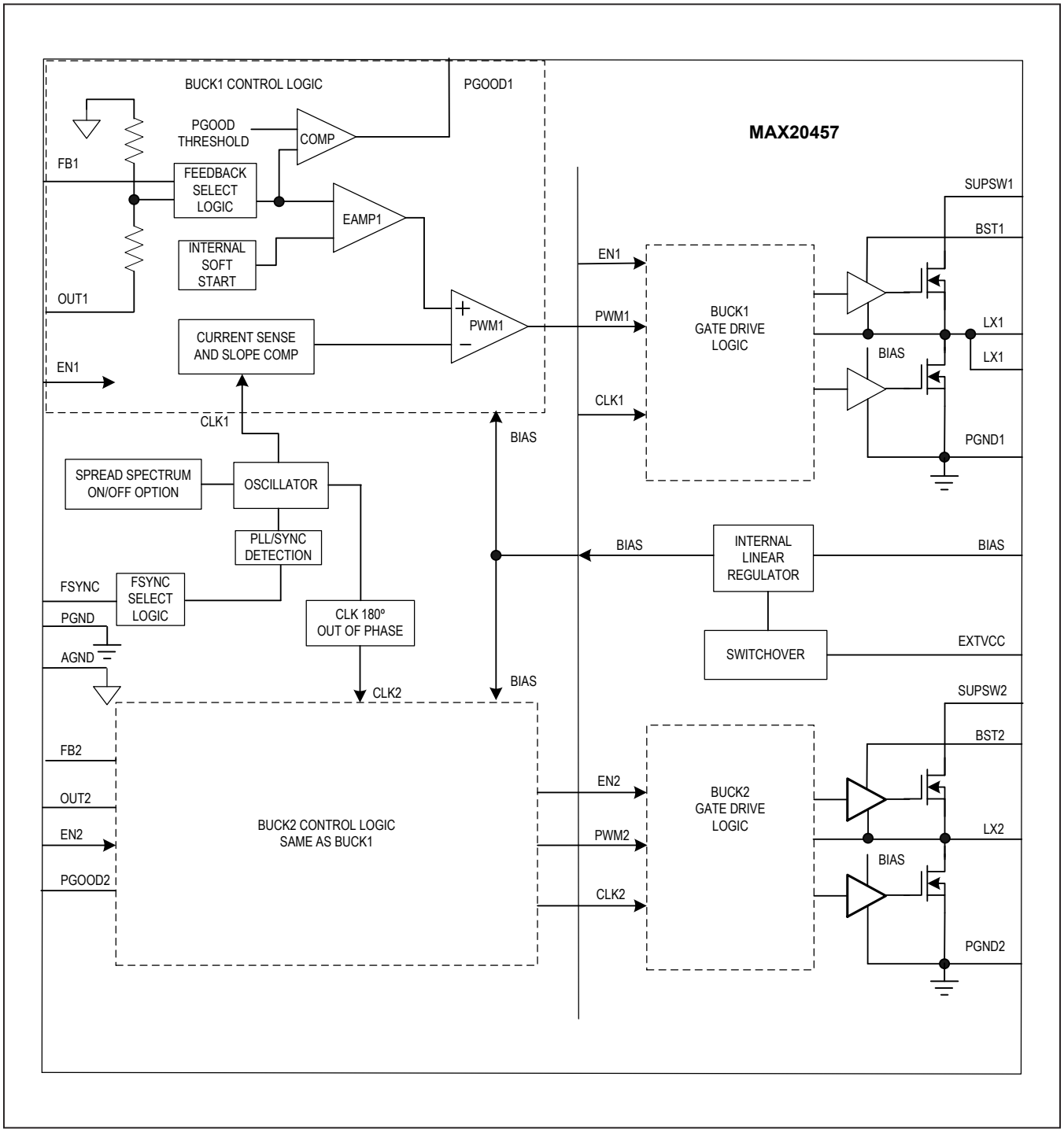
Simplified Block Diagram



Absolute Maximum Ratings

SUPSW1, SUPSW2, EN1, EN2 to AGND .....-0.3V to 40V
OUT1, OUT2 to AGND.....-0.4V to 15V
BIAS, FSYNC, PGOOD1, PGOOD2,
FB1, FB2 to AGND.....-0.3V to 6V
EXTVCC to AGND.....-0.3V to (BIAS + 0.3V)
LX_ to PGND_ .....-0.3V to (SUPSW_ + 0.3V)
BST_ to LX_ (Note 1).....-0.3V to 6V
PGND_ to AGND.....-0.3V to 0.3V

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 28.6mW/°C above +70°C).....2286mW
Operating Temperature Range.....-40°C to 125°C
Junction Temperature .....+150°C
Soldering Temperature (reflow).....+260°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature(soldering,10s) .....300°C

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Type	28 TQFN
Package Code	T2855Y+5C
Outline Number	**21-100130**
Land Pattern Number	**90-0027**
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)	
Junction to Ambient (θ_{JA})	27°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 2: Package thermal resistances were obtained using the Evaluation Kit. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

$V_{SUPSW_}$ = 14V, $V_{EN_}$ = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C) (Notes 3 and 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS STEP-DOWN CONVERTERS						
Supply Voltage Range	V_{SUP}	Normal operation	3.5		36	V
Supply Current	I_{IN}	V_{EN1} = V_{EN2} = 0V		1	5	µA
		V_{EN1} = V_{SUP}, V_{OUT1} =5V, V_{EN2} = 0V, V_{EXTVCC} = 5V, No Switching		10	18	
		V_{EN2} = V_{SUP}, V_{OUT2} = 3.3V, V_{EN1} = 0V, V_{EXTVCC} = 3.3V, no switching		8	12	
		V_{EN1} = V_{EN2} = V_{SUP}, V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{EXTVCC} = 3.3V, no switching		10		
BUCK1 Fixed Output Voltage	V_{OUT1}	V_{FB1} = V_{BIAS}, V_{OUT1} = 5V, PWM mode	4.9	5	5.1	V
		V_{FB1} = V_{BIAS}, V_{OUT1} = 5V, skip mode	4.85	5	5.15	
BUCK2 Fixed Output Voltage	V_{OUT2}	V_{FB2} = V_{BIAS}, V_{OUT2} = 3.3V, PWM mode	3.234	3.3	3.366	V
		V_{FB2} = V_{BIAS}, V_{OUT2} = 3.3V, skip mode	3.2	3.3	3.4	
Output Voltage Adjustable Range		BUCK1, BUCK2 (Note 5)	1		14	V
Regulated Feedback Voltage	V_{FB1}, V_{FB2}		0.985	1	1.015	V
Feedback Leakage Current	I_{FB1}, I_{FB2}	T_A = +25°C		0.01	1	µA
Feedback Line Regulation Error		V_{SUP} = 3.5V to 36V, $V_{FB_}$ = 1V		0.01		%/V
Dead time		BUCK1, BUCK2 (Note 5)		3		ns
Maximum Duty Cycle		BUCK1, BUCK2	95			%
Minimum On-Time	t_{ON_MIN}	BUCK1, BUCK2 (Note 5)		20		ns
Switching Frequency Accuracy		2.1MHz	1.9	2.1	2.32	MHz
		400kHz	350	400	470	kHz
Current-Limit		BUCK1	4.5	6	7.5	A
		BUCK2	2.5	3.5	4.5	
Soft-Start Ramp Time		BUCK1 and BUCK2, fixed soft-start time regardless of frequency.	3	5.5	7	ms
Phase Shift Between BUCK1 and BUCK2		PWM operation (Note 5)		180		deg
LX1, LX2 Leakage Current		V_{SUP} = 6V, $V_{LX_}$ = $V_{PGND_}$ or V_{SUP}, T_A = +25°C		0.001	5	µA
High-Side Switch On Resistance	$R_{ON_H_BUCK1}$	I_{LX1} = 1A, V_{BIAS} = 5V		50		mΩ
	$R_{ON_H_BUCK2}$	I_{LX2} = 1A , V_{BIAS} = 5V		100		

Electrical Characteristics (continued)

$V_{SUPSW_}$ = 14V, $V_{EN_}$ = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C) (Notes 3 and 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Side Switch On Resistance	$R_{ON_L_BUCK1}$	I_{LX1} = 1A, V_{BIAS} = 5V		45		mΩ
	$R_{ON_L_BUCK2}$	I_{LX2} = 1A, V_{BIAS} = 5V		90		
PGOOD1, PGOOD2 Threshold	V_{PGOOD_H}	% of $V_{OUT_}$, rising	93	95	97	%
	V_{PGOOD_F}	% of $V_{OUT_}$, falling	91.5	93.5	95.5	
PGOOD1, PGOOD2 Leakage Current		V_{PGOOD1} = V_{PGOOD2} = 5V, T_A = +25°C		0.01	1	µA
PGOOD1, PGOOD2 Output Low Voltage		I_{SINK} = 1mA			0.2	V
PGOOD1, PGOOD2 Debounce Time		Fault detection, rising and falling		20		µs
PGOOD1, PGOOD2 Assertion Time		PGOOD1, PGOOD2 low to high (Note 5)		0		ms
FSYNC INPUT						
FSYNC frequency Range		Minimum sync pulse of 100ns, f_{OSC} = 2.1MHz	1.8		2.6	MHz
		Minimum sync pulse of 1.5µs, f_{OSC} = 400kHz	250		550	kHz
FSYNC Switching Thresholds		High Threshold	1.4			V
		Low Threshold			0.4	
INTERNAL LDO BIAS AND EXTVCC						
Internal BIAS Voltage		V_{SUPSW1} > 6V		5		V
BIAS UVLO Threshold		V_{BIAS} rising		3.1	3.3	V
		V_{BIAS} falling	2.4	2.6		
EXTVCC Operating Range			3.25		5.5	V
EXTVCC Threshold	V_{TH_EXTVCC}	EXTVCC rising, hysteresis = 110mV		3	3.25	V
THERMAL OVERLOAD						
Thermal Shutdown Temperature		(Note 5)		170		°C
Thermal Shutdown Hysteresis		(Note 5)		20		°C
EN Logic Input						
High Threshold		EN_	1.8			V
Low Threshold		EN_			0.8	V
EN Input Bias Current		EN_ Logic Inputs Only, T_A = +25°C		0.01	1	µA
SPREAD SPECTRUM						
Spread Spectrum		Spread spectrum enabled		f_{OSC} ±6%		

Note 3: Limits are 100% tested at +25°C. Limits over operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at +25°C.

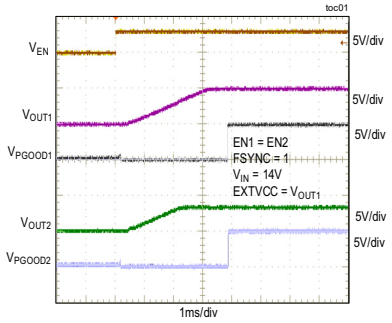
Note 4: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours

Note 5: Guaranteed by design, not production tested.

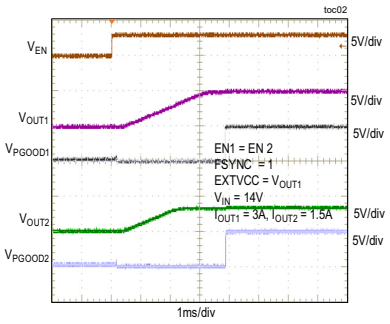
Typical Operating Characteristics

(T_A = +25ºC, unless otherwise noted.)

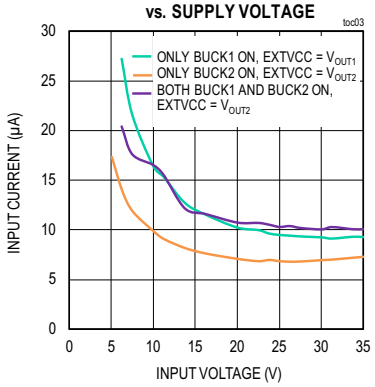
STARTUP INTO NO-LOAD



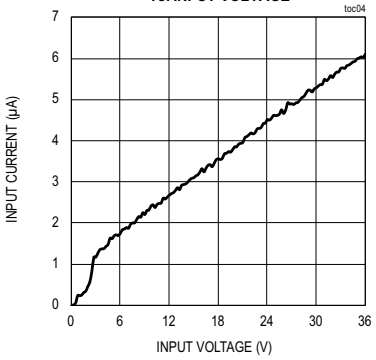
STARTUP INTO LOAD



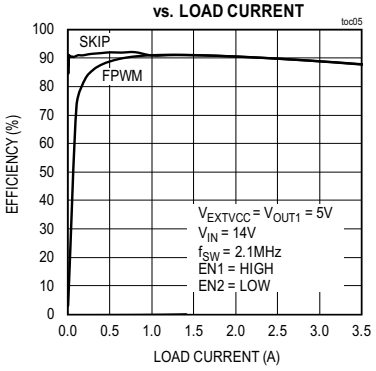
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



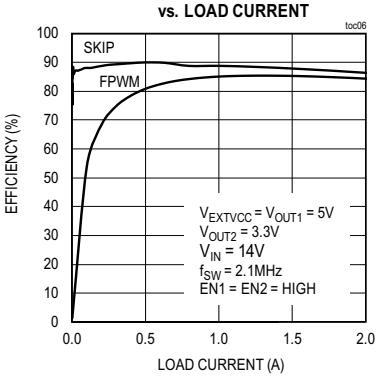
SHUTDOWN CURRENT vs. INPUT VOLTAGE



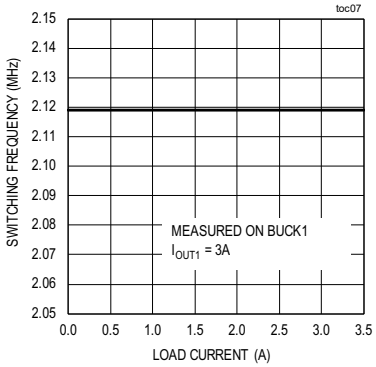
BUCK1 EFFICIENCY vs. LOAD CURRENT



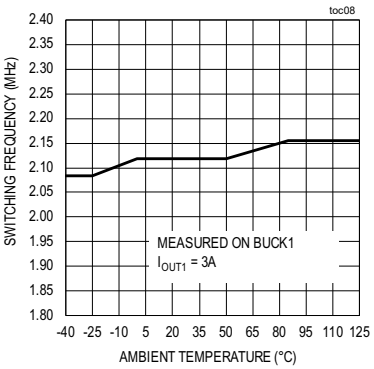
BUCK2 EFFICIENCY vs. LOAD CURRENT



SWITCHING FREQUENCY vs. LOAD CURRENT



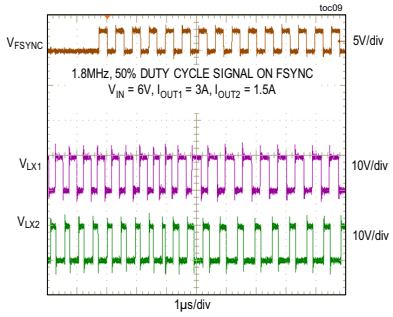
SWITCHING FREQUENCY vs. AMBIENT TEMPERATURE



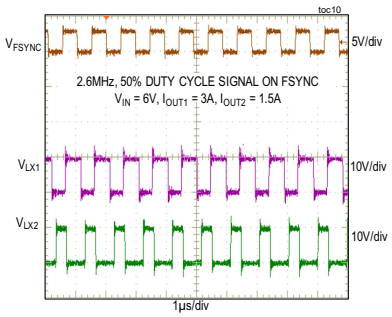
Typical Operating Characteristics (continued)

(T_A = +25ºC, unless otherwise noted.)

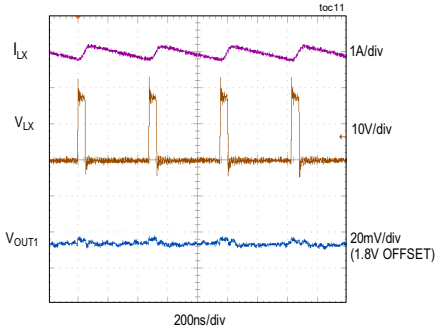
FSYNC SYNCHRONIZATION



OUT OF PHASE OPERATION

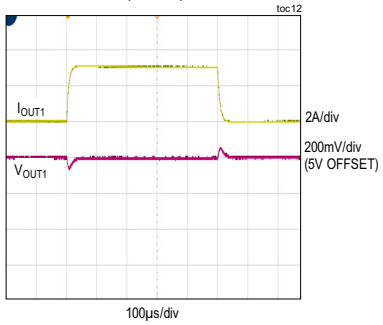


SWITCHING WAVEFORM



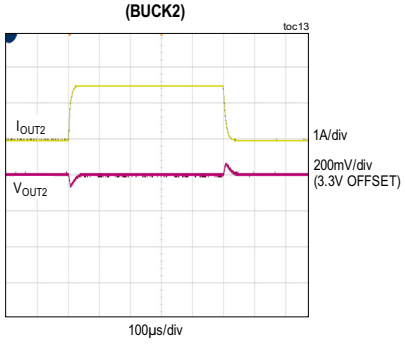
CONDITIONS: V_{IN} = 18V, V_{OUT2} = 1.8V, f_{SW} = 2.1MHz, I_{OUT2} = 1A

LOAD TRANSIENT RESPONSE (BUCK1)



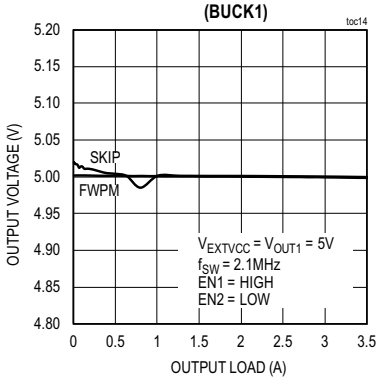
CONDITIONS: V_{OUT1} = 5V, f_{SW} = 2.1MHz, FSYNC = HIGH, EN1 ONLY

LOAD TRANSIENT RESPONSE (BUCK2)

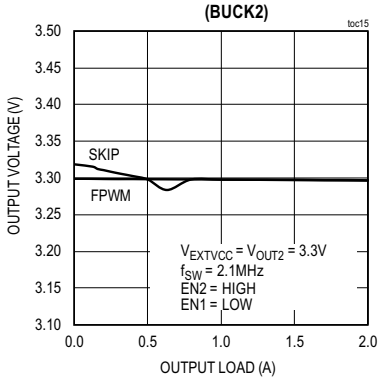


CONDITIONS: V_{OUT1} = 3.3V, f_{SW} = 2.1MHz, FSYNC = HIGH, EN1 ONLY

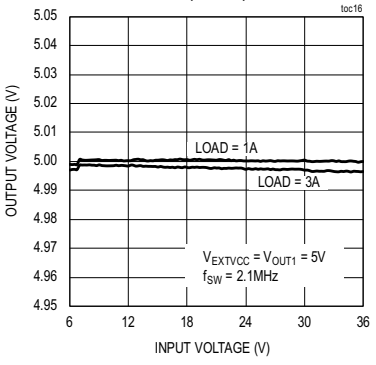
OUTPUT LOAD REGULATION (BUCK1)



OUTPUT LOAD REGULATION (BUCK2)



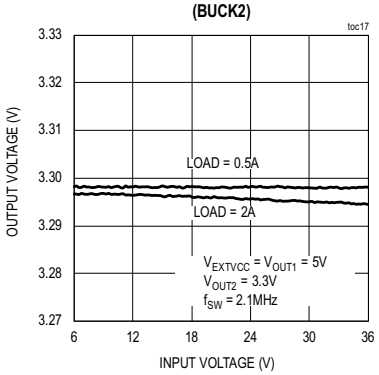
OUTPUT LINE REGULATION (BUCK1)



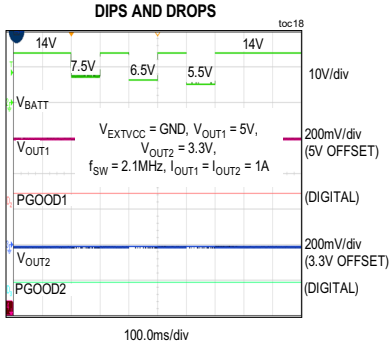
Typical Operating Characteristics (continued)

(T_A = +25ºC, unless otherwise noted.)

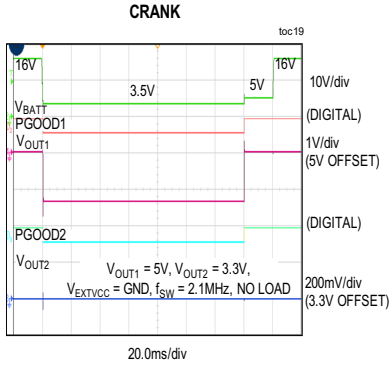
OUTPUT LINE REGULATION (BUCK2)



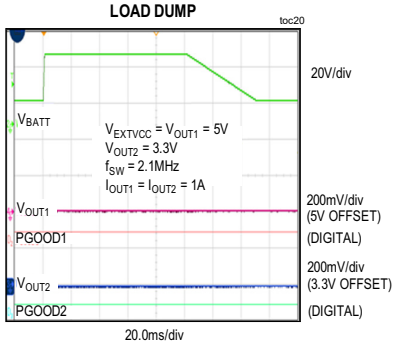
DIPS AND DROPS



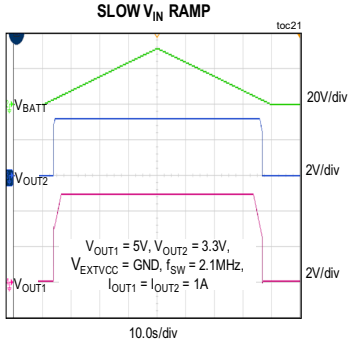
CRANK



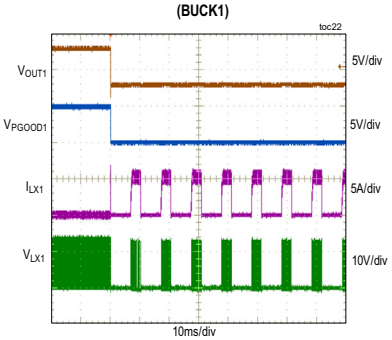
LOAD DUMP



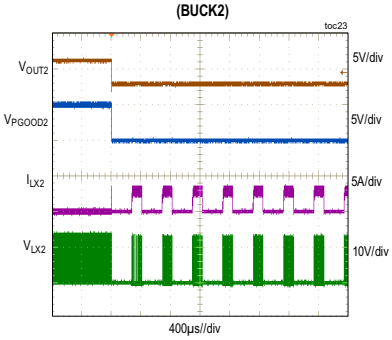
SLOW V_{IN} RAMP



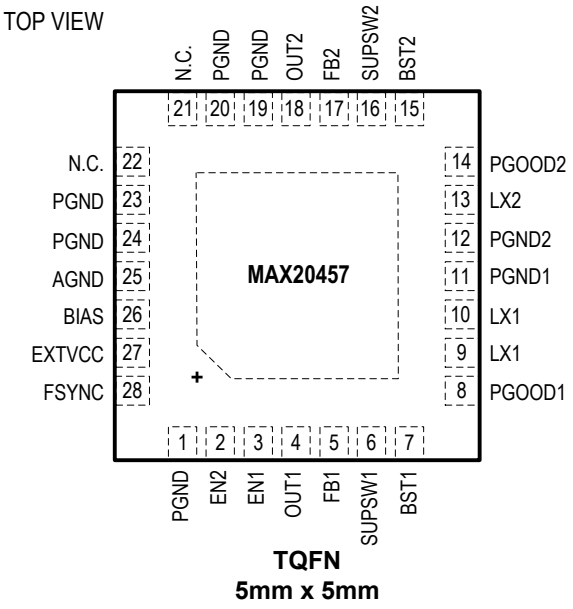
SHORT-CIRCUIT AFTER REGULATION (BUCK1)



SHORT CIRCUIT AFTER REGULATION (BUCK2)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground
2	EN2	High-Voltage Tolerant, Active High Digital Enable Input for BUCK2. Drive EN2 high to enable BUCK2.
3	EN1	High-Voltage Tolerant, Active High Digital Enable Input for BUCK1. Drive EN1 high to enable BUCK1.
4	OUT1	Output Sense Input for BUCK1. When using the internal preset 5V feedback divider, FB1 is connected to BIAS, and BUCK1 uses OUT1 to sense the output voltage.
5	FB1	Feedback Input for BUCK1. Connect FB1 to BIAS for fixed output or to a resistor divider between OUT1 and AGND to adjust the output voltage between 1V and 14V. FB1 is regulated to 1V (typ) in adjustable version.
6	SUPSW1	BUCK1 Internal High-Side Switch Supply Input and BIAS LDO Input. Bypass SUPSW1 to PGND1 with a 4.7µF ceramic capacitor.
7	BST1	Boost Flying Capacitor Connection for High-Side Gate Voltage of BUCK1. Connect a ceramic capacitor between BST1 and LX1.
8	PGOOD1	Open Drain Power-Good Output for BUCK1. PGOOD1 is low if OUT1 falls below 93.5% (typ) of output regulation voltage. PGOOD1 becomes high impedance when OUT1 rises above 95% (typ) of its regulation voltage. PGOOD1 asserts low during soft-start and in shutdown. To obtain a logic signal, pull up PGOOD1 with an external resistor connected to a positive voltage lower than 5.5V.
9, 10	LX1	BUCK1 Inductor Connection. Connect an inductor from LX1 to the BUCK1 output.
11	PGND1	Power Ground for BUCK1
12	PGND2	Power Ground for BUCK2
13	LX2	BUCK2 Inductor Connection. Connect an inductor from LX2 to the BUCK2 output.

Pin Description (continued)

PIN	NAME	FUNCTION
14	PGOOD2	Open Drain Power-Good Output for BUCK2. PGOOD2 is low if OUT2 falls below 93.5% (typ) of output regulation voltage. PGOOD2 becomes high impedance when OUT2 rises above 95% (typ) of its regulation voltage. PGOOD2 asserts low during soft-start and in shutdown. To obtain a logic signal, pull up PGOOD2 with an external resistor connected to a positive voltage lower than 5.5V.
15	BST2	Boost Flying Capacitor Connection for High-Side Gate Voltage of BUCK2. Connect a ceramic capacitor between BST2 and LX2.
16	SUPSW2	BUCK2 Internal High-Side Switch Supply Input. Bypass SUPSW2 to PGND2 with a 4.7µF ceramic capacitor.
17	FB2	Feedback Input for BUCK2. Connect FB2 to BIAS for fixed output or to a resistive divider between OUT2 and AGND to adjust the output voltage between 1V and 14V. FB2 is regulated to 1V (typ) in the adjustable version.
18	OUT2	Output Sense Input for BUCK2. When using the internal preset feedback divider, FB2 is connected to BIAS and BUCK2 uses OUT2 to sense the output voltage.
19, 20, 23, 24	PGND	Power Ground
20	PGND3	Power Ground for Boost Controller. All the high current paths for the boost controller terminates to PGND3.
21, 22	N.C.	Not Connected
25	AGND	Quiet Analog Ground for the IC
26	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to ground with a low ESR minimum 2.2µF ceramic capacitor. BIAS provides the power to the internal gate drive circuitry.
27	EXTVCC	Switchover Comparator Input. Connect a voltage between 3.25V and 5.5V to EXTVCC to power the IC and bypass the internal bias LDO. Connect EXTVCC to ground if EXTVCC is not used.
28	FSYNC	External Clock Synchronization Input. Synchronization operating frequency ratio is 1. The duty-cycle of the signal on SYNC determines the phase shift between BUCK1 and BUCK2. Use 50% duty cycle for the external clock to get a 180° phase shift between BUCK1 and BUCK2.
—	EP	Exposed Pad. Connect EP to ground. Connecting EP to ground does not remove the requirement for proper ground connections to PGND and AGND. EP is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX20457 IC is an automotive-grade switching power supply that integrates two synchronous buck converters.

1) The BUCK1 converter provides a fixed 5V/3.3V output voltage, or an adjustable 1V to 14V output voltage option, and up to 3.5A continuous current capability.
2) The BUCK2 converter provides a fixed 5V/3.3V output voltage, or an adjustable 1V to 14V output voltage option, and up to 2A continuous current capability.

Each power supply has its individual enable pin. Connect EN1 or EN2 directly to battery voltage, or to power supply sequencing logic to control each power supply on/off.

In standby mode, the total supply current is reduced to 10µA (typ). When both converters are disabled, the total current drawn is further reduced to 1µA.

Internal 5V BIAS LDO

An internal 5V BIAS LDO supplies the IC internal circuitry. SUPSW1 supplies the internal BIAS LDO. Bypass BIAS with a minimum 2.2µF ceramic capacitor. To minimize the internal power dissipation, bypass BIAS to an external 5V rail using the EXTVCC pin.

EXTVCC Switchover

The internal linear regulator can be bypassed by connecting an external 3.25V to 5.5V supply, or one of the buck converter outputs to EXTVCC. With valid supply applied to EXTVCC, BIAS is internally switched to EXTVCC and the internal linear regulator turns off. This configuration has two main advantages:

1) Reduces IC internal power dissipation
2) Improves light-load efficiency as the internal supply current is scaled down proportionally to the duty cycle if connecting any buck output to EXTVCC

If V_{EXTVCC} drops below 3V (typ), the internal regulator is enabled and BIAS is switched back to 5V.

Switching Frequency/External Synchronization

The MAX20457 provides an internal oscillator with 400kHz and 2.1MHz options. 2.1MHz frequency operation optimizes the application for the smallest component size, at the cost of lower efficiency. 400kHz frequency operation offers best overall efficiency at the expense of component size and board space.

Apply an external clock to FSYNC to enable frequency synchronization. The MAX20457 uses a phase-locked loop (PLL) to synchronize the internal oscillator to the external clock signal. The BUCK1 converter synchronizes its LX1 falling edge to the FSYNC rising edge, and the BUCK2 converter synchronizes its LX2 falling edge to the FSYNC falling edge. The FSYNC signal should have a minimum 100ns high pulse width for 2.1MHz and minimum 1.5µs high pulse width for 400kHz.

Spread-Spectrum Option

The ICs feature enhanced EMI performance with spread spectrum option. The spread spectrum is available as a factory option. When the spread spectrum is enabled, the operating frequency is varied ±6% centered at switching frequency. The modulation signal is a triangular wave with a period of 110µs at 2.1MHz. Therefore, switching frequency ramps down 6% and back to 2.1MHz in 110µs and also ramps up 6% and back to 2.1MHz in 110µs after which the cycle repeats.

For operations at 400kHz, the modulation signal scales proportionally (the 110µs modulation period for 2.1MHz increases to 110µs x 2.1MHz/0.4MHz = 577.5µs).

The internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on the FSYNC pin and pass any modulation (including spread spectrum) present on the driving external clock.

Overcurrent Protection

The MAX20457 has a cycle-by-cycle current limit and includes hiccup mode to prevent any damage from overcurrent or short-circuit on three power channels. When the inductor current continuously hits the current limit at overcurrent on any channels, the output voltage starts decreasing. If the IC detects the output voltage drops below 0.7V, it turns off that channel. After waiting for about 10ms (2x soft-start time) of hiccup time, the IC restarts that channel in case the overcurrent or short-circuit condition is removed.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ICs. When the junction temperature exceeds +170°C, an internal thermal sensor shuts down the ICs, allowing them to cool. The thermal sensor turns on the ICs again after the junction temperature cools by 20°C.

Buck Converters

The ICs provide two synchronous buck converters. The buck converters use PWM, valley current mode control scheme, making it ideal for applications with high input voltages and low output voltages. BUCK1 and BUCK2 operate 180 degrees out of phase with each other to minimize input current ripple from the minimum to the maximum input voltages.

Undervoltage Lockout (UVLO)

The internal 5V BIAS LDO undervoltage-lockout (UVLO) circuitry inhibits switching if the BIAS voltage drops below its 2.6V (typ) UVLO falling threshold. Once the BIAS voltage rises above its UVLO rising threshold, 3.1V (typ), and EN1 and EN2 enable the buck converters, BUCK1 and BUCK2 start switching and their output voltages begin soft-start.

Soft-Start

Drive EN1 and EN2 high to enable BUCK1 and BUCK2. The soft-start circuitry gradually ramps up the reference voltage during soft-start time (5ms typ) to reduce the input surge currents during startup. BIAS voltage must exceed its UVLO threshold (3.1V typ) before soft-start can be enabled.

FSYNC Mode Selection

Drive FSYNC low to enable skip mode. In skip mode, the high-side FET turns for fixed adaptable on-time (depending on V_{OUT}, V_{SUP} and f_{SW}). The high-side FET then turns off and the low-side FET turns on until the inductor current falls to the zero cross threshold. Once the low-side FET turns off by hitting the zero-crossing threshold, LX becomes high impedance and the output voltage keeps decreasing. When output voltage or FB voltage is detected below the set point, the new cycle starts by turning on the high-side FET again. In this way, the regulator switches only as needed to service load to improve system efficiency.

Drive FSYNC high to enable forced PWM (FPWM) mode. FPWM mode prevents the regulator from entering skip mode, by disabling the zero-cross detection of the inductor current. The benefit of FPWM mode is to keep the switching frequency constant under all load conditions; however, FPWM operation diverts a considerable amount of the output current to PGND, reducing the efficiency under light-load conditions. FPWM mode is useful for improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands.

Frequency Foldback

Frequency Foldback is implemented in buck converters when operating only at 2.1MHz and when the internal fixed output voltage option is selected. This is useful in case the boost controller is not used to protect its input voltage during V_{SUP} transient drops. When the input voltage of buck converter drops close to the output voltage, the converter runs at the maximum duty cycle and the high-side switch off period approaches minimum off time 100ns (typ). To prevent output voltage drifting out of regulation, frequency foldback is used to automatically reduce the switching frequency from 2.1MHz to 350kHz and maintain a high duty cycle of > 95% with 100ns (typ) off time. The frequency foldback occurs when the input voltage drops below a certain threshold calculated by formula of $V_{SUPSW_} = 1.4 \times V_{OUT_}$ (falling).

Maximum Duty-Cycle Operation

When the buck input drops close to its output regulation voltage, it enters maximum duty-cycle operation with minimum 95% duty cycle, while switching at regular switching frequency in the case of no frequency foldback, or at 350kHz after frequency foldback. The input voltage at which the buck enters dropout can be approximated as follows:

$$V_{IN_} = [V_{OUT_} + (I_{OUT_} \times RON_H_BUCK_)]/0.95$$

where RON_H_BUCK_ is listed in the EC table specification.

High-Side Gate Driver Supply (BST1/BST2)

The buck converter high-side MOSFET is turned on by closing an internal switch between BST1/BST2 and the gate of the high-side MOSFET and transferring the bootstrap capacitor's charge at BST1/BST2 to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX1/LX2 voltage drops down to ground, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor to BIAS voltage.

The selected n-channel high-side MOSFET determines the appropriate boost capacitance values ($C_{BST_}$ in the Typical Operating Circuit) according to the following equation:

$$C_{BST_} = Q_G/\Delta V_{BST_}$$

where Q_G is the total gate charge of the high-side MOSFET and $\Delta V_{BST_}$ is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose $\Delta V_{BST_}$ such that the available gate-drive voltage is not significantly degraded (e.g., $\Delta V_{BST_}$ = 100mV to 300mV) when determining $C_{BST_}$. The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF works in most cases.

Power Good Indicator (PGOOD1/PGOOD2)

Each buck converter include a power good indicator to indicate the buck output voltage status. The PGOOD_ indicator can be used to enable circuits that are supplied by the corresponding voltage rail, or to turn-on subsequent supplies.

Each PGOOD_ goes from low to high impedance when the corresponding regulator output voltage rises above 95% (typ) of its nominal regulation voltage. Each PGOOD_ goes low when the corresponding regulator output voltage drops below 93.5% (typ) of its nominal regulation voltage. Connect a 10kΩ (typ) pullup resistor from PGOOD_ to the relevant logic rail to level-shift the signal. PGOOD_ asserts low during soft-start, and when the buck converter is disabled.

Applications Information

Setting Output Voltage

Connect FB1 and FB2 to BIAS to enable fixed buck output voltages (5V or 3.3V) set by a preset internal resistive divider connected between OUT1/OUT2 and AGND. To externally adjust the output voltage between 1V and 14V, connect a resistive voltage-divider from the converter output (OUT_) to the corresponding FB_ input and then to AGND. Select the bottom-side resistors (R_{BOTTOM} from FB_ from FB_-to-AGND) less than or equal to 100kΩ. Calculate the top-side resistors (R_{TOP} from FB_ from output-to-FB_) with the following equation:

$$R_{TOP} = R_{BOTTOM} (V_{OUT_}/V_{FB_}-1)$$

where $V_{FB1} = V_{FB2} = 1V$ R_{BOTTOM} can be 50kΩ to 100kΩ.

When an external resistive divider is used to program the buck output voltage, a feed-forward capacitor in parallel with R_{TOP} with a low-pF capacitance can be used to improve control-loop phase margin.

Input Capacitor

A 4.7µF ceramic input capacitor is recommended for proper buck operation. This value can be adjusted based on application input-voltage-ripple requirements.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{SUPSW_} - V_{OUT})}}{V_{SUPSW_}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

Therefore,

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR} that peaks at the end of an on-cycle. Calculate the input capacitance and ESR required for a specific ripple using the following equation:

$$ESR\ [\Omega] = \frac{\Delta V_{ESR}}{(I_{LOAD(MAX)} + \frac{\Delta I_{P-P}}{2})}$$

$$C_{IN}\ [\mu F] = \frac{I_{LOAD(MAX)} \times (\frac{V_{OUT}}{V_{IN}})}{(\Delta V_Q \times f_{SW})}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and,

$I_{LOAD(MAX)}$ = Maximum output current in A,

ΔI_{P-P} = Peak-to-peak inductor current in A,

f_{SW} = Switching frequency in MHz,

L = Inductor value in µH.

Inductor Selection

The MAX20457 operates with two switching frequency options: 2.2MHz and 400kHz. The key parameters on inductor selection are: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The minimum required inductance is calculated as:

$$L_{MIN} = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times I_{OUT} \times LIR}$$

Table 1. Buck Converter Inductor and Output Capacitor Selection

SWITCHING FREQUENCY	BUCK1 INDUCTOR (µH)	BUCK1 OUTPUT CAPACITOR (µF)	BUCK2 INDUCTOR (µH)	BUCK2 OUTPUT CAPACITANCE (µF)
2.1MHz	2.2	2 x 22	2.2	22
400kHz	10	2 x 47	10	47 + 22

where LIR is the ratio of the inductor peak-to-peak AC current to DC average current, and 0.3 is a typical value to use.

See Table 1 for the recommended buck inductors. The inductor's saturation current rating must meet or exceed the LX current limit. For optimum transient response and highest efficiency, use inductors with a low DC resistance.

Output Capacitor

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. The capacitor is usually selected by ESR and the voltage rating rather than by capacitance value.

When using low capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot is no longer a problem.

The total voltage sag (V_{SAG}) can be calculated as follows:

$$V_{SAG} = \frac{L \times (\triangle I_{LOAD(MAX)})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})} + \frac{\triangle I_{LOAD(MAX)} \times (t - \triangle t)}{C_{OUT}}$$

The amount of overshoot (V_{SOAR}) during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} = \frac{(\triangle I_{LOAD(MAX)})^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

See Table 1 for recommended output capacitance.

ESR Considerations

The output capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load transient requirements. When using high-capacitance, low-ESR capacitors, the ESR of the filter capacitor dominates the output voltage ripple:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses, low EMI, and clean, stable operation. If possible, mount all power components on the top side of the board, and minimize the high frequency current loop as small as possible. Refer to the MAX20457 EV kit for an example layout. Follow these guidelines for good PCB layout.

Place the input bypass capacitors as close to SUPSW1 and SUPSW2 as possible. The buck input capacitors deliver high di/dt current pulses when its high-side MOSFET turns on. Minimize the parasitic inductance in the power input traces to improve efficiency and reliability.

Minimize the connection from the buck output capacitor's ground terminal to the input capacitor's ground terminal for each buck regulator. This minimizes the area of current loop when the high-side MOSFET is conducting.

Keep buck high-current paths, and power traces wide and short. Minimize the traces from each buck LX node to each inductor and from each inductor to the output capacitors. This minimizes the buck current loop area and minimizes LX trace resistance and stray capacitance to achieve optimal efficiency. Using thick copper PCBs (2 ounces vs. 1 ounce) can improve full load efficiency by 1% or more.

Keep all sensitive analog signals (FB1 and FB2) away from noisy switching nodes (LX_ and BST_) and high current loops.

Place the BIAS capacitor as close to the BIAS node as possible. Noise coupling into BIAS can disturb the reference and bias circuitry if this capacitor is installed away from the device.

Ground is the return path for the full load currents flowing into and out of the MAX20457. It is also the common reference voltage for all the analog circuits. Improper ground routing can bring extra resistance and inductance into the current loop, causing different voltage reference and worsening voltage ringing or spikes. Place a solid ground plane layer under the power loop components layer to shield the switching noise from other sensitive traces. Connect all the analog ground (AGND) and power grounds (PGND1, PGND2 and PGND) together at a single point in a star ground connection. The IC exposed pad can be the point for ground connection.

The exposed pad under the bottom of the package is attached with epoxy to the substrate of the IC, making it an excellent path to remove heat from the IC. Connect the exposed pad to large ground plane areas through external or internal layers. Place multiple small vias under the exposed pad to effectively transfer heat down to the internal ground plane and the back side of the PCB to further improve the thermal resistance from the IC package to the ambient.

Typical Application Circuits

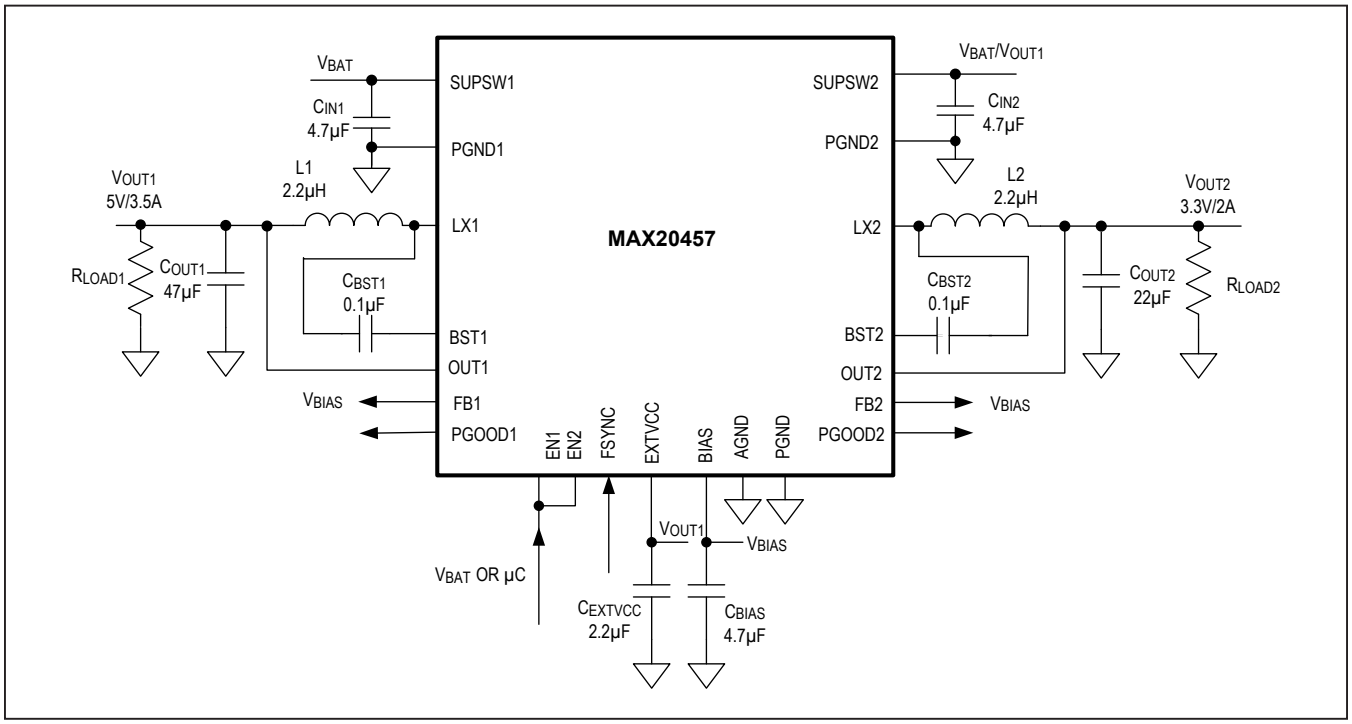


Figure 1. MAX20457ATIE/VY+ Configuration: 2.1MHz, 5V/3.3V Outputs

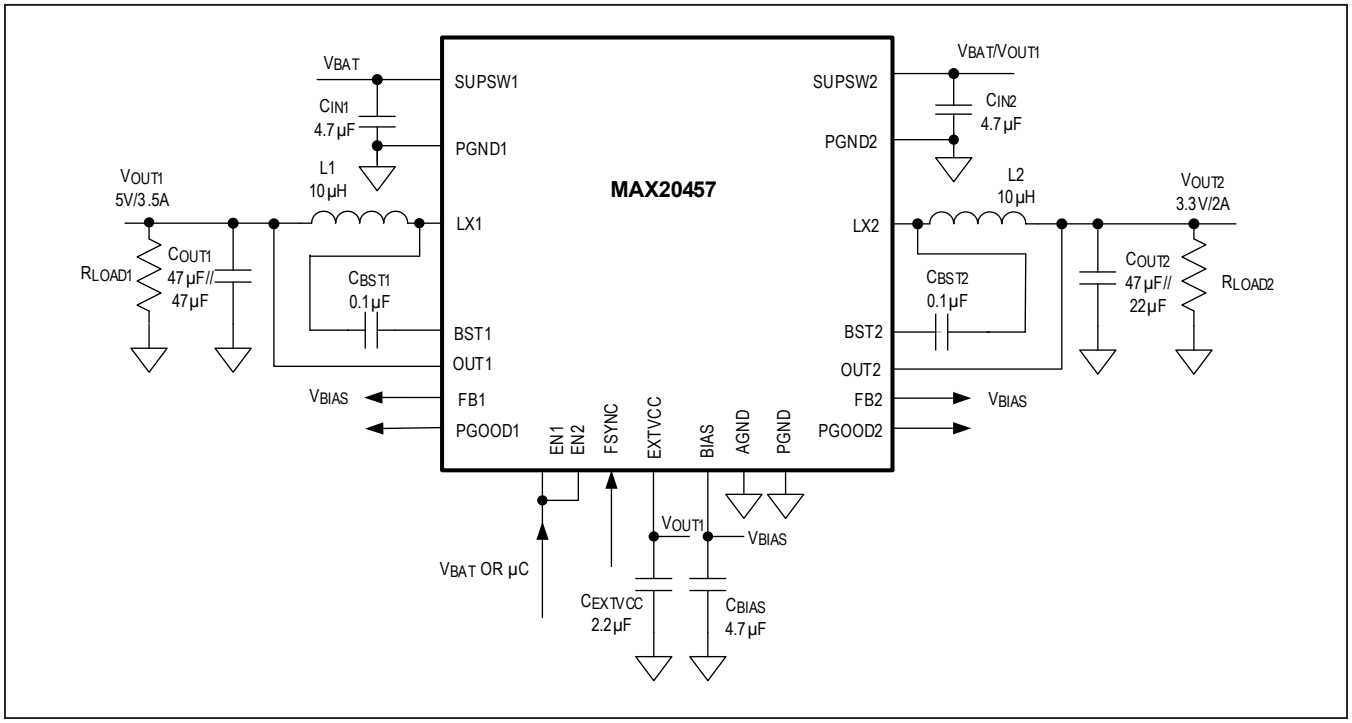


Figure 2. MAX20457ATIC/VY+ Configuration: 400kHz, 5V/3.3V Outputs

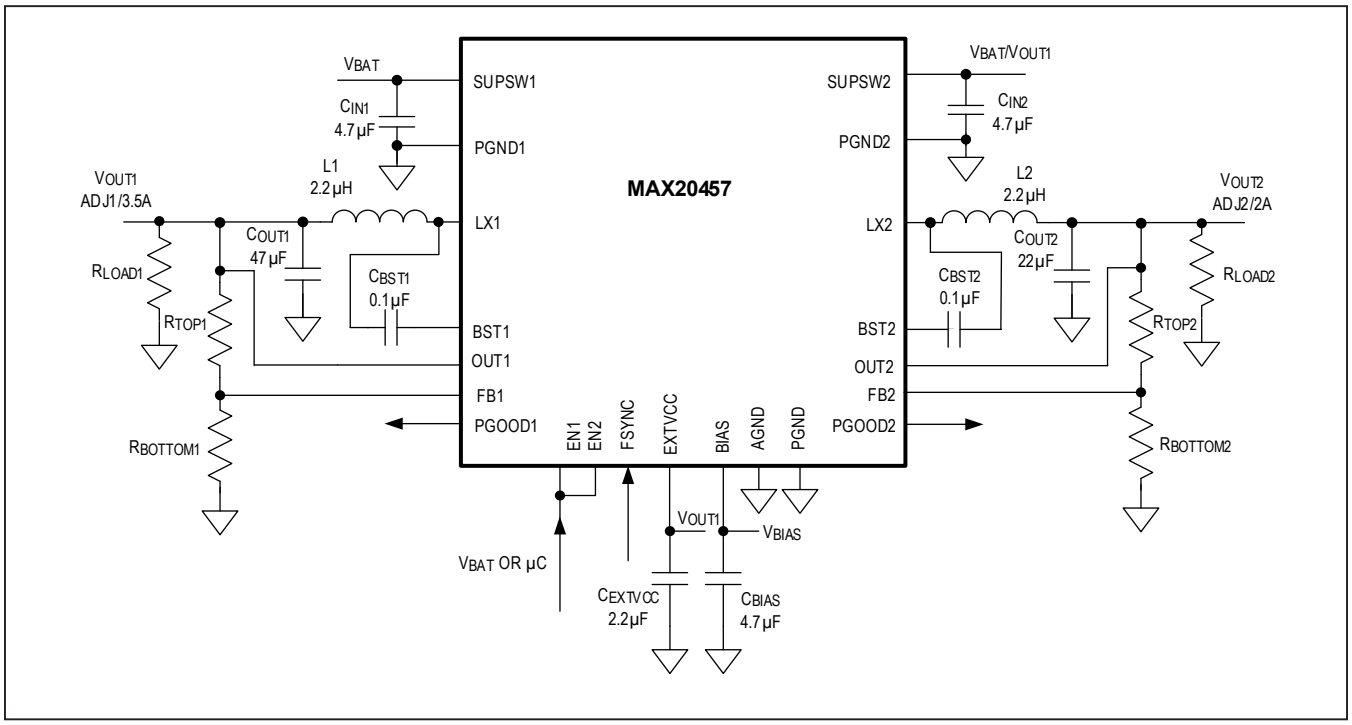


Figure 3. MAX20457ATIE/VY+ Configuration: 2.1MHz ADJ/ADJ Outputs

Ordering Information

PART NUMBER	V_{OUT} OPTIONS (V_{OUT1}/V_{OUT2}) (V)	SWITCHING FREQUENCY	SPREAD SPECTRUM
MAX20457ATIA/VY+	3.3/5	2.1MHz	Off
MAX20457ATIB/VY+	3.3/5	2.1MHz	On
MAX20457ATIC/VY+	5/3.3	400kHz	Off
MAX20457ATID/VY+	5/3.3	400kHz	On
MAX20457ATIE/VY+	5/3.3	2.1MHz	Off
MAX20457ATIF/VY+	5/3.3	2.1MHz	On
MAX20457ATIG/VY+	3.3/3.3	2.1MHz	On
MAX20457ATIH/VY+**	3.3/3.5	2.1MHz	On
MAX20457ATII/VY+**	3.3/5	400MHz	On

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape-and-reel.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/19	Initial release	—
1	4/19	Updated *Typical Operating Characteristics*, *Setting Output Voltage*, and *Ordering Information* sections	6–7,13, 16
2	7/19	Removed all future-part designations from *Ordering Information*	16
3	11/19	Updated *General Description, Electrical Characteristics, Detailed Description, Applications Information, and Ordering Information*	1, 4, 12, 13, 15, 16

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