*Click **here** for production status of specific part numbers.*

MAX2078

Octal-Channel Ultrasound Front-End with CW Doppler Mixers

General Description

The MAX2078 octal-channel ultrasound front-end is a fully integrated bipolar, high-density octal-channel ultrasound receiver optimized for low cost, high-channel count, high-performance portable and cart-based ultrasound systems. The easy-to-use IC allows the user to achieve high-end 2D, PW, and CW Doppler (CWD) imaging capability using substantially less space and power. The highly compact imaging receiver lineup, including low-noise amplifier (LNA), variable-gain amplifier (VGA), and anti-alias filter (AAF), achieves an ultra-low 2.4dB noise figure at $R_S = R_{IN} = 200\Omega$ at a very low 64.8mW per channel power dissipation. The full imaging receiver channel has been optimized for second-harmonic imaging with -64dBFS second-harmonic distortion performance with a $1V_{P-P}$ 5MHz output signal. The bipolar front-end has also been optimized for excellent low-velocity PW and color-flow Doppler sensitivity with an exceptional near-carrier SNR of 140dBc/Hz at 1kHz offset from a 5MHz $1V_{P-P}$ output clutter signal.

A fully integrated high-performance, programmable CWD beamformer is also included. Separate I/Q mixers for each channel are available for optimal CWD sensitivity in high-clutter environments, yielding an impressive near-carrier SNR of 154dBc/Hz at 1kHz offset from a 1.25MHz $200mV_{P-P}$ input clutter signal.

The MAX2078 octal-channel ultrasound front-end is available in a small 10mm x 10mm, 68-pin thin QFN package with an exposed pad and is specified over a 0°C to +70°C temperature range.

Applications

- Medical Ultrasound Imaging
- Sonar

Benefits and Features

- 8 Full Channels of LNA, VGA, AAF, and CWD Mixers in a Small, 10mm x 10mm TQFN Package
- Pin Compatible with MAX2077 with LNA, VGA, and AAF in 10mm x 10mm TQFN Variant
- Ultra-Low Full-Channel Noise Figure of 2.4dB at $R_{IN} = R_S = 200\Omega$
- Low Output-Referred Noise of $23nV/\sqrt{Hz}$ at 5MHz, 20dB Gain, Yielding a Broadband SNR of 68dB** for Excellent Second-Harmonic Imaging
- High Near-Carrier SNR of 140dBc/Hz at 1kHz Offset from a 5MHz, $1V_{P-P}$ Output Signal, and 20dB of Gain for Excellent Low-Velocity PW and Color-Flow Doppler Sensitivity in a High-Clutter Environment
- Ultra-Low-Power 64.8mW per Full-Channel (LNA, VGA, and AAF) Normal Imaging Mode (234mW per Channel in CWD Mode)
- Selectable Active Input-Impedance Matching of 50Ω, 100Ω, 200Ω, and 1kΩ
- Wide Input-Voltage Range of $330mV_{P-P}$ in High LNA Gain Mode and $550mV_{P-P}$ in Low LNA Gain Mode
- Integrated Selectable 3-Pole 9MHz, 10MHz, 15MHz, and 18MHz Butterworth AAF
- Fast-Recovery, Low-Power Modes (< 2µs)
- Fully Integrated, High Dynamic Range CWD Beamformer with Near-Carrier SNR of 154dBc/Hz at 1kHz Offset from a 1.25MHz, $200mV_{P-P}$ Input Clutter Signal

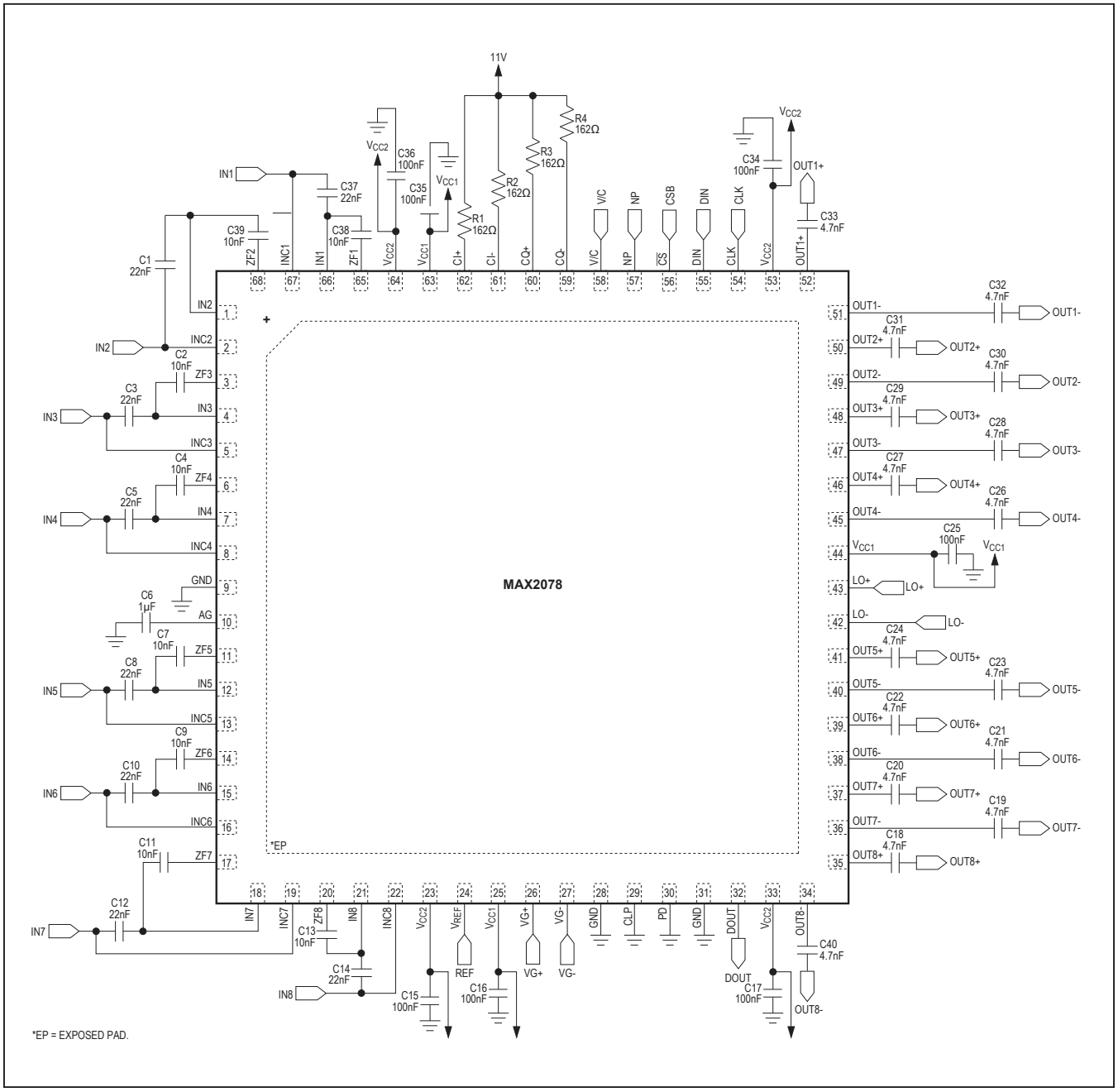
***When coupled with the MAX1437B ADC.*

***Ordering Information** appears at end of data sheet.*

19-4570; Rev 4; 6/19

maxim integrated™

Typical Application Circuit



Absolute Maximum Ratings

$V_{CC_}$ to GND .....-0.3V to +5.5V
V_{CC2} - V_{CC1} ..... > -0.3V
CI_, CQ_ to GND .....-0.3V to +13V
ZF_, IN_, AG to GND ..... -0.3V to ($V_{CC_}$ + 0.3V)
INC_ .....20mA DC
V_{REF} to GND.....-0.3V to +3V
IN_ to AG.....-0.6V to +0.6V
OUT_, LO_, DIN, DOUT, VG_, NP, $\overline{CS}$, CLK, PD, CLP, V/C to GND.....-0.3V to V_{CC1} + 0.3V
CI_, CQ_, $V_{CC_}$, V_{REF} analog and digital control signals must be applied in this order
Input Differential Voltage .....2.0V_{P-P} differential
Continuous Power Dissipation (T_A = +70°C)
68-Pin TQFN (derated 40mW/°C above +70°C).....4W
Operating Temperature Range (Note 1).....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 64 TQFN	
Package Code	T6800+2
Outline Number	**21-0142**
Land Pattern Number	**90-0099**
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2, Note 3)	
Junction to Ambient (θ_{JA})	20°C/W
Junction to Case (θ_{JC})	0.5°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a fourlayer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial.**

Note 2: Junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can only be used if the component is soldered down to a printed circuit board pad containing multiple ground vias to remove the heat. The junction temperature must not exceed 150°C.

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$, assuming there is no heat removal from the exposed pad. The junction temperature must not exceed 150°C.

DC Electrical Characteristics

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, CLP = 0, PD = 0, no RF signals applied. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage	V_{CC1}		3.13	3.3	3.47	V
4.75V/5V Supply Voltage	V_{CC2}		4.5	4.75	5.25	V
External Reference Voltage Range	V_{REF}	(Note 5)	2.475		2.525	V
CMOS Input High Voltage	V_{IH}	Applies to CMOS control inputs	2.5			V
CMOS Input Low Voltage	V_{IL}	Applies to CMOS control inputs			0.8	V
CMOS Input Leakage Current	I_{IN}	T_A = +25°C, applies to CMOS control inputs; 0V to 3.47V			10	µA
DATA Output High Voltage	DOUT_HI	10MΩ load		V_{CC1}		V
DATA Output Low Voltage	DOUT_LO	10MΩ load		0		V

DC Electrical Characteristics—VGA Mode

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, V/C = 1, CLP = 0, PD = 0, no RF signals applied. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
4.75V/5V Supply Standby Current	I_NP_5V_TOT	NP = 1, all channels		3.9	6	mA
3V Supply Standby Current	I_NP_3V_TOT	NP = 1, all channels		1.7	3	mA
4.75V/5V Power-Down Current	I_PD_5V_TOT	PD = 1, all channels		0.4	10	µA
3V Power-Down Current	I_PD_3V_TOT	PD = V_{CC1}, all channels		0.3	10	µA
3V Supply Current per Channel	I_3V_NM	Total I divided by 8, VG+ - VG- = -2V		11	16	mA
4.75V/5V Supply Current per Channel	I_5V_NM	Total I divided by 8		6.0	8.3	mA
DC Power per Channel	P_NM			64.8	92.3	mW
Differential Analog Control Voltage Range	VGAIN_RANG	VG+ - VG-		±3		V
Common-Mode Voltage for Difference Analog Control	VGAIN_COMM	(VG+ + VG-)/2		1.65 ±5%		V
Source/Sink Current for Gain Control Pins	I_ACONTROL	Per pin		±1.6	±3.5	µA
Reference Voltage Input	V_{REF}		2.475		2.525	V
Reference Current	I_{REF}	All channels		9.7	13	µA
Output Common-Mode Level	V_{CMO}			1.73		V

DC Electrical Characteristics—CW Mode

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, CLP = 0, V/C = 0, no RF signals applied. CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Current	I_{REF}			82.7		µA
Mixer LVDS LO Input Common-Mode Voltage	V_LVDS_CM	LO+ and LO-		1.25 ±0.2		V
LVDS LO Differential Input Voltage	V_LVDS_DM	Common-mode input voltage = 1.25V (Note 6)	200	700		mV_{P-P}
LVDS LO Input Common-Mode Current	I_LVDS_CM	Current out of each pin, V_LVDS_CM = 1.25V		130		µA
LVDS LO Differential Input Resistance	R_DM_LVDS	(Note 7)	4			kΩ
POWER-DOWN MODE						
4.75V/5V Supply Current per Channel	I_C_5V_P	PD = 1		0.6	10	µA
3.3V Supply Current per Channel	I_C_3_3V_P	PD = 1		0.1	10	µA
LOW-POWER MODE						
4.75V/5V Supply Current per Channel	I_C_5V_L	CLP = 1		27	30	mA
3.3V Supply Current per Channel	I_C_3_3V_L	CLP = 1		0.4	0.95	mA
11V Supply Current per Channel	I_C_11V_L	CLP = 1		6.8	8.4	mA
On-Chip Power Dissipation (All 8 Channels)	PDIS_FP_TOT_L	CLP = 1		1.44	1.7	W
NORMAL POWER MODE						
4.75V/5V Supply Current per Channel	I_C_5V_N			31	34	mA
3.3V Supply Current per Channel	I_C_3_3V_N			0.4	0.95	mA
11V Supply Current per Channel	I_C_11V_N			11.3	13	mA
On-Chip Power Dissipation (All 8 Channels)	PDIS_FP_TOT_N	(Note 8)		1.87	2.2	W

AC Electrical Characteristics

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB, D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Mode Select Response Time (Note 9)	V/C stepped from 0 to 1, DC stable within 10%		1		µs
	V/C stepped from 1 to 0, DC stable within 10%		1		
High Gain Maximum Input-Voltage Range	High LNA gain D43/D42/D41/D40 = 1/0/1/0		0.33		V_{P-P} differential
Low Gain Maximum Input-Voltage Range	Low LNA gain D43/D42/D41/D40 = 0/0/0/1		0.6		V_{P-P} differential

AC Electrical Characteristics—VGA Mode

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, V/C = 1, NP = 0, PD = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	D42/D41/D40 = 0/0/0, R_{IN} = 50Ω	47.5	50	60	Ω
	D42/D41/D40 = 0/0/1, R_{IN} = 100Ω	90	100	110	
	D42/D41/D40 = 0/1/0, R_{IN} = 200Ω	180	200	220	
	D42/D41/D40 = 0/1/1, R_{IN} = 1000Ω, f_{RF} = 2MHz	700	830	1000	
Noise Figure	R_S = R_{IN} = 50Ω, VG+ - VG- = +3V		4.5		dB
	R_S = R_{IN} =100Ω, VG+ - VG- = +3V		3.4		
	R_S = R_{IN} = 200Ω, VG+ - VG- = +3V		2.4		
	R_S = R_{IN} = 1000Ω, VG+ - VG- = +3V		2.1		
Low-Gain Noise Figure	D43/D42/D41/D40 = 0/0/0/1, LNA gain = 12.5dB, R_S = R_{IN} = 200Ω, VG+ - VG- = +3V		3.9		dB
Input-Referred Noise Voltage	D43/D42/D41/D40 = 1/1/1/0		0.9		nV/√Hz
Input-Referred Noise Current	D43/D42/D41/D40 = 1/1/1/0		2.1		pA/√Hz
Maximum Gain, High Gain Setting	VG+ - VG- = +3V	41	42.8	45	dB
Minimum Gain, High Gain Setting	VG+ - VG- = -3V	8.5	10	11	dB
Maximum Gain, Low Gain Setting	D43/D42/D41/D40 = 0/0/0/1, VG+ - VG- = +3V	34.4	36.8	38	dB
Minimum Gain, Low Gain Setting	D43/D42/D41/D40 = 0/0/0/1, VG+ - VG- = -3V	2.5	4	6	dB
Anti-Aliasing Filter 3dB Corner Frequency	D45/D44 = 0/0, f_C = 9MHz		9		MHz
	D45/D44 = 0/1, f_C = 10MHz		10		
	D45/D44 = 1/0, f_C = 15MHz		15		
	D45/D44 = 1/1, f_C = 18MHz		18		
Gain Range	VG+ - VG- = -3V to +3V		33		dB
Absolute Gain Error	Measured at T_A = +25°C, V_{VG}+ - V_{VG}- = -2V		±0.4		dB
	Measured at T_A = +25°C, V_{VG}+ - V_{VG}- = 0V		±0.4		
	Measured at T_A = +25°C, V_{VG}+ - V_{VG}- = +2V		±0.4		
Input Gain Compression	V_{VG}+ - V_{VG}- = -3V (VGA minimum gain), gain ratio with 330mV_{P-P}/50mV_{P-P} input tones		1.4		dB
	LNA low gain = 12.5dB, V_{VG}+ - V_{VG}- = -3V (VGA minimum gain), gain ratio with 600mV_{P-P}/50mV_{P-P}		0.8		
VGA Gain Response Time	Gain step up (V_{IN} = 5mV_{P-P}, gain changed from 10dB to 44dB, settling time is measured within 1dB final value)		1.4		µs
	Gain step down (V_{IN} = 5mV_{P-P}, gain changed from 44dB to 10dB, settling time is measured within 1dB final value)		1.6		

AC Electrical Characteristics—VGA Mode (continued)

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, V/C = 1, NP = 0, PD = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VGA Output Offset Under Pulsed Overload	Overdrive is ±10mA in clamping diodes, gain at 30dB, 16 pulses at 5MHz, repetition rate 20kHz; offset is measured at output when RF duty cycle is off		180		mV
Small-Signal Output Noise	20dB of gain, V_{VG}+ - V_{VG}- = -0.85V, no input signal		23		nV/√Hz
Large-Signal Output Noise	20dB of gain, V_{VG}+ - V_{VG}- = -0.85V, f_{RF} = 5MHz, f_{NOISE} = f_{RF} + 1kHz, V_{OUT} = $1V_{P-P}$ differential		35		nV/√Hz
Second Harmonic (HD2)	V_{IN} = $50mV_{P-P}$, f_{RF} = 2MHz, V_{OUT} = $1V_{P-P}$		-67		dBc
	V_{IN} = $50mV_{P-P}$, f_{RF} = 5MHz, V_{OUT} = $1V_{P-P}$		-64.2		
High-Gain IM3 Distortion	V_{IN} = $50mV_{P-P}$, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, V_{OUT} = $1V_{P-P}$ (Note 10)	-52	-61		dBc
Low-Gain IM3 Distortion	D43/D42/D41/D40 = 0/0/0/1 (R_{IN} = 200Ω, LNA gain = 12.5dB),V_{IN} = $100mV_{P-P}$, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, V_{OUT} = $1V_{P-P}$ (Note 10)	-50	-60		dBc
Standby Mode Power-Up Response Time	Gain set for 26dB, f_{RF} = 5MHz, V_{OUT} = $1V_{P-P}$, settled with in 1dB from transition on NP pin		2.1		µs
Standby Mode Power-Down Response Time	To reach DC current target ±10%		2.0		µs
Power-Up Response Time	Gain set for 28dB, f_{RF} = 5MHz, V_{OUT} = $1V_{P-P}$, settled within 1dB from transition on PD		2.7		ms
Power-Down Response Time	Gain set for 28dB, f_{RF} = 5MHz, DC power reaches 6mW/channel, from transition on PD		5		ns
Adjacent Channel Crosstalk	V_{OUT} = $1V_{P-P}$ differential, f_{RF} = 10MHz, 28dB of gain		-58		dBc
Nonadjacent Channel Crosstalk	V_{OUT} = $1V_{P-P}$ differential, f_{RF} = 10MHz, 28dB of gain		-71		dBc
Phase Matching Between Channels	Gain = 28dB, V_{VG}+ - V_{VG}- = 0.4V, V_{OUT} = $1V_{P-P}$, f_{RF} = 10MHz		±1.2		Degrees
3V Supply Modulation Ratio	Gain = 28dB, V_{VG+} - V_{VG}- = 0.4V, V_{OUT} = $1V_{P-P}$, f_{RF} = 5MHz, f_{MOD} = 1kHz, V_{MOD} = $50mV_{P-P}$, ratio of output sideband at 5.001MHz, $1V_{P-P}$		-73		dBc
4.75V/5V Supply Modulation Ratio	Gain = 28dB, V_{VG+} - V_{VG}- = 0.4V, V_{OUT} = $1V_{P-P}$, f_{RF} = 5MHz, f_{MOD} = 1kHz, V_{MOD} = $50mV_{P-P}$, ratio of output sideband at 5.001MHz, $1V_{P-P}$		-82		dBc
Gain Control Lines Common-Mode Rejection Ratio	Gain = 28dB, V_{VG+} - V_{VG}- = 0.4V, f_{MOD} = 5MHz, V_{MOD} = $50mV_{P-P}$, V_{OUT} = $1.0V_{P-P}$		-74		dBc
Overdrive Phase Delay	V_{VG+} - V_{VG}- = -3V, delay between V_{IN} = $300mV_{P-P}$ and V_{IN} = $30mV_{P-P}$ differential		5		ns
Output Impedance	Differential		100		Ω

AC Electrical Characteristics—CW Mode

(*Typical Application Circuit*, V/C = 0, PD = 0, NP = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), f_{RF} = f_{LO}/16 = 5MHz, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 4, Note 11)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CW DOPPLER MIXER						
Mixer RF Frequency Range			0.9		7.6	MHz
LO Frequency Range	LO+ and LO-		16		120	MHz
Mixer Output Frequency Range			DC		100	kHz
FULL-POWER MODE						
Noise Figure	No carrier			3.4		dB
Noise Figure at 100mV$_{P-P}$ Input	100mV$_{P-P}$ at input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			3.6		dB
Noise Figure at 200mV$_{P-P}$ Input	200mV$_{P-P}$ at input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			4.1		dB
SNR at 100mV$_{P-P}$ Input	100mV$_{P-P}$ at input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			-148.3		dBc/Hz
SNR at 200mV$_{P-P}$ Input	200mV$_{P-P}$ at input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			-153.8		dBc/Hz
Two-Tone Intermodulation IMD3 at 100mV	f_{RF1} = 5MHz, 0.1V$_{P-P}$, f_{RF2} = 5.01MHz at -25dBc, f_{LO} = 80MHz (Note 10)		-50	-55		dBc
Two-Tone Intermodulation IMD3 at 200mV	f_{RF1} = 5MHz, 0.2V$_{P-P}$, f_{RF2} = 5.01MHz at -25dBc, f_{LO} = 80MHz (Note 10)			-48.5		dBc
Mixer Output-Voltage Compliance	Valid voltage range (AC + DC) on summed mixer output pins		4.5		12	V
Channel-to-Channel Phase Matching	Measured under zero beat conditions, V_{RF} = 100mV$_{P-P}$, f_{RF} = 5MHz, f_{LO} = 80MHz (Note 12)			±0.4		Degrees
Channel-to-Channel Gain Matching	Measured under zero beat conditions, V_{RF} = 100mV$_{P-P}$, f_{RF} = 5MHz, f_{LO} = 80MHz (Notes 12, 13)			±0.2		dB
Transconductance	Calculated from LNA input voltage and twice the I or Q current	f_{RF} = 0.9MHz, f_{LO}/16 = 1MHz	19	23	26	mS
		f_{RF} = 7.6MHz, f_{LO}/16 = 7.5MHz	19	22.5	26	
LOW-POWER MODE (CLP = 1)						
Noise Figure	No carrier			3.2		dB
Noise Figure at 100mV$_{P-P}$ Input	100mV$_{P-P}$ on input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			3.5		dB
Noise Figure at 200mV$_{P-P}$ Input	200mV$_{P-P}$ on input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			4.3		dB
SNR at 100mV$_{P-P}$ Input	100mV$_{P-P}$ on input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			-148.2		dBc/Hz
SNR at 200mV$_{P-P}$ Input	200mV$_{P-P}$ on input, f_{RF} = f_{LO}/16 = 1.25MHz, measured at 1kHz offset			-153.6		dBc/Hz
Two-Tone Intermodulation IMD3	f_{RF1} = 5MHz, 0.1V$_{P-P}$, f_{RF2} = 5.01MHz at -25dBc, f_{LO} = 80MHz (Note 10)			-44		dBc

AC Electrical Characteristics—CW Mode (continued)

(*Typical Application Circuit*, V/C = 0, PD = 0, NP = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), f_{RF} = f_{LO}/16 = 5MHz, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 4, Note 11)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Mixer Output-Voltage Compliance	Valid voltage range on summed mixer output pins (Note 11)		4.5		12	V
Transconductance (Note 15)	Calculated from LNA input voltage and twice the I or Q current	f_{RF} = 1.1MHz, f_{LO}/16 = 1MHz	19	21.5	26	mS
		f_{RF} = 7.6MHz, f_{LO}/16 = 7.5MHz	19	21.5	26	

AC Electrical Characteristics—Serial Peripheral Interface

(DOUT loaded with 60pF and 10MΩ, 2ns rise and fall edges on CLK.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Speed					10	MHz
Mininimum Data-to-Clock Setup Time	t_{CS}			5		ns
Mininimum Data-to-Clock Hold Time	t_{CH}			0		ns
Mininimum Clock-to-$\overline{CS}$ Setup Time	t_{ES}			5		ns
$\overline{CS}$ Positive Mininimum Pulse Width	t_{EW}			1		ns
Mininimum Clock Pulse Width	t_{CW}			2		ns
Mininimum $\overline{CS}$ High to Mixer Clock on	$t_{MIX\overline{CS}}$			2		ns

Note 4: Minimum and maximum limits at T_A = +25°C and +70°C are guaranteed by design, characterization, and/or production test.

Note 5: Noise performance of the device is dependent on the noise contribution from V_{REF}. Use a low-noise supply for V_{REF}.

Note 6: Note that the LVDS CWD LO clocks are DC-coupled. This is to ensure immediate synchronization when the clock is first turned on. An AC-coupled LO is problematic in that the RC time constant associated with the coupling capacitors and the input impedance of the pin causes a period of time (related to the RC time constant) when the DC level on the chip side of the capacitor is outside the acceptable common-mode range and the LO swing does not excede both of the logic thresholds required for proper operation. This problem associated with AC-coupling causes an inability to ensure synchronization among beamforming channels. The LVDS signal is terminated differentially with an external 100Ω resistor on the board.

Note 7: An external 100Ω resistor terminates the LVDS differential signal path.

Note 8: Total on-chip power dissipation is calculated as $P_{DISS} = V_{CC1} \times I_{CC1} + V_{CC2} \times I_{CC2} + V_{REF} \times I_{REF} + [11V - (I_{11V}/4) \times 162] \times I_{11V}$.

Note 9: This response time does not include the CW output highpass filter. When switching to VGA mode, the CW outputs stop drawing current and the output voltage goes to the rail. If a highpass filter is used, the recovery time can be excessive and a switching network is recommended, as shown in the *Applications Information* section.

Note 10: See the *Ultrasound-Specific IMD3 Specification* section.

Note 11: The reference input noise is given for 8 channels, knowing that the reference-noise contributions are correlated in all 8 channels. If more channels are used, the reference noise must be reduced to get the best noise performance.

Note 12: Channel-to-channel gain and phase matching measured on 30 pieces during engineering characterization at room temperature. Each mixer is used as a phase detector and produces a DC voltage in the IQ plane. The phase is given by the angle of the vector drawn on that plane. Multiple channels from multiple parts are compared to each other to produce the phase variation.

Note 13: Voltage gain is measured by subtracting the output-voltage signal from the input-voltage signal. The output-voltage signal is obtained by taking the differential CW I output and summing it in quadrature with the differential CW Q output. The input voltage is defined as the differential voltage applied to the CW input pins.

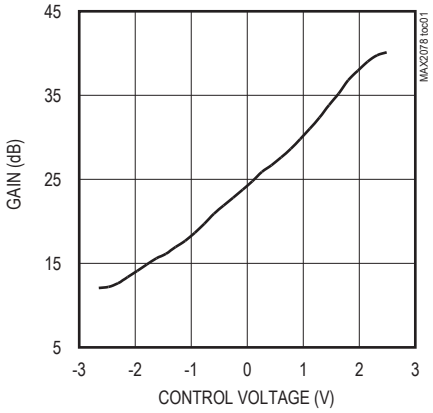
Note 14: Mixer output-voltage compliance is the range of acceptable voltages allowed on the CW mixer outputs.

Note 15: Transconductance is defined as the quadrature-combined CW differential output current at baseband divided by the mixer's input voltage.

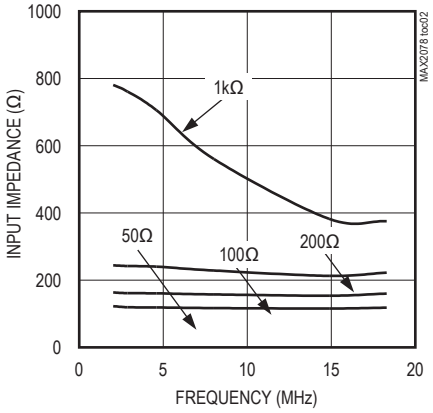
Typical Operating Characteristics

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

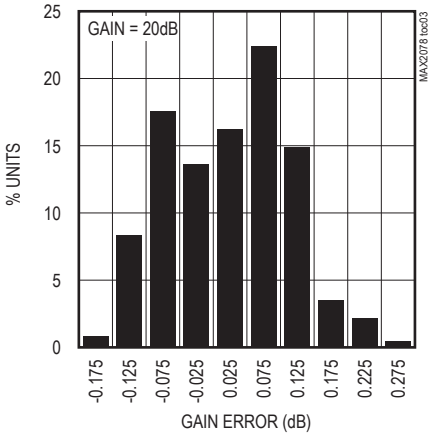
GAIN vs. DIFFERENTIAL ANALOG CONTROL VOLTAGE



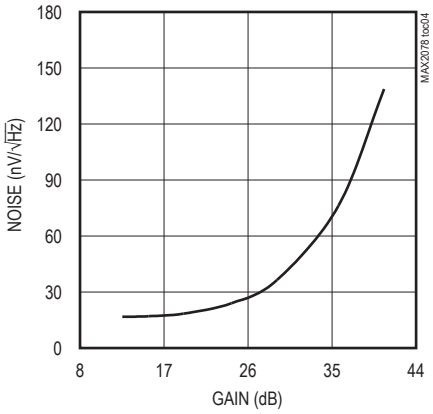
COMPLEX INPUT IMPEDANCE MAGNITUDE vs. FREQUENCY



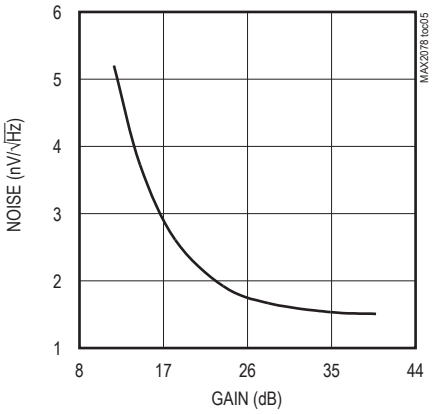
GAIN ERROR HISTOGRAM



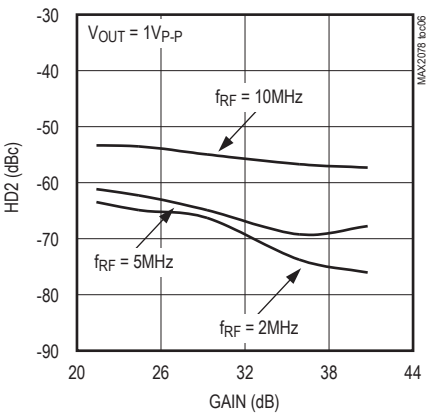
OUTPUT-REFERRED NOISE vs. GAIN



INPUT-REFERRED NOISE vs. GAIN



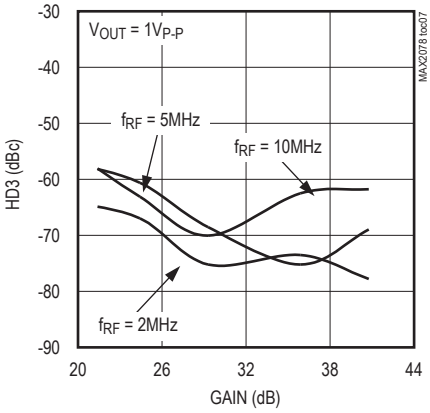
SECOND-HARMONIC DISTORTION vs. GAIN



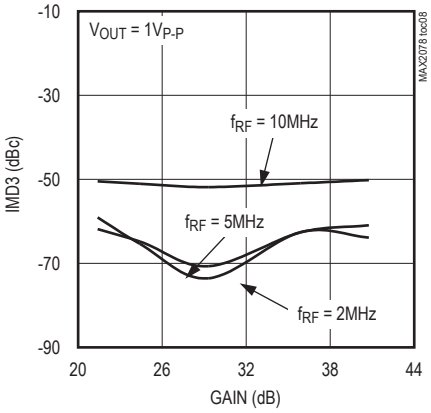
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

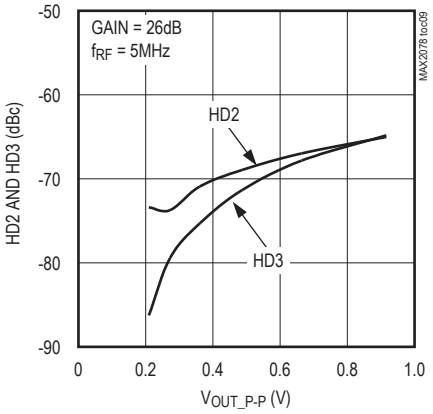
THIRD-HARMONIC DISTORTION vs. GAIN



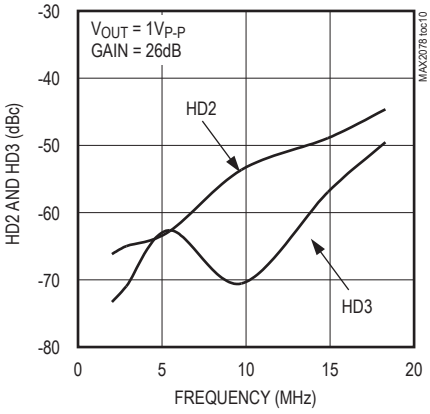
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. GAIN



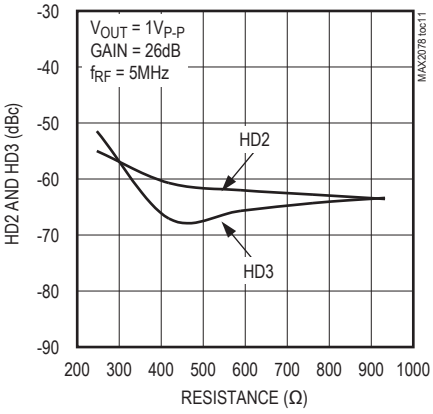
SECOND- AND THIRD-HARMONIC DISTORTION vs. V_{OUT_P-P}



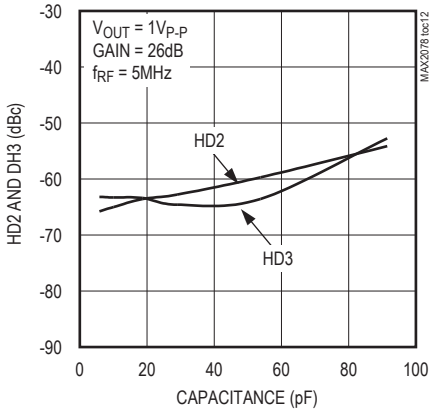
SECOND- AND THIRD-HARMONIC DISTORTION vs. FREQUENCY



SECOND- AND THIRD-HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT RESISTANCE



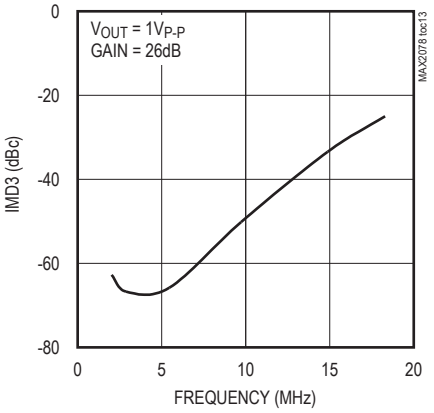
SECOND- AND THIRD-HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT LOAD CAPACITANCE



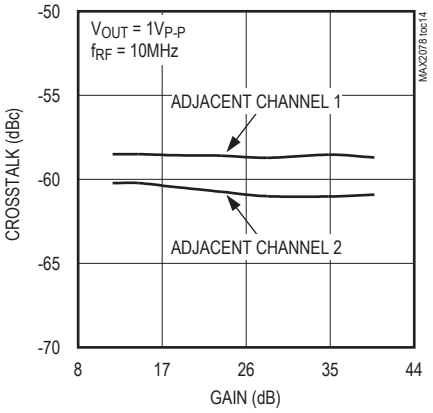
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

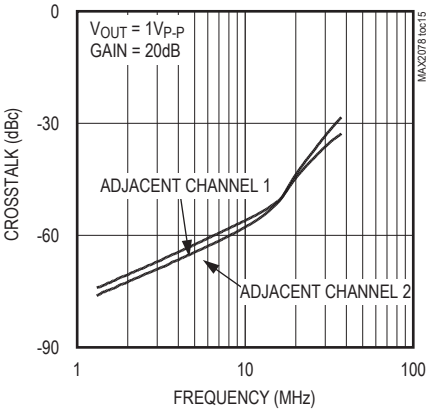
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. FREQUENCY



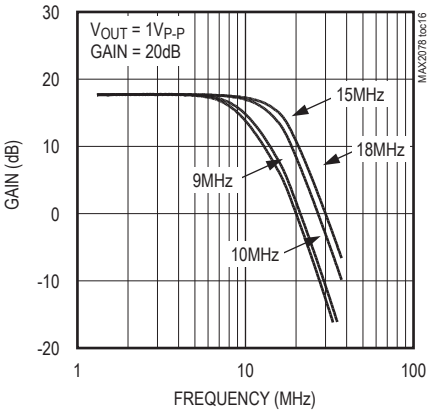
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN



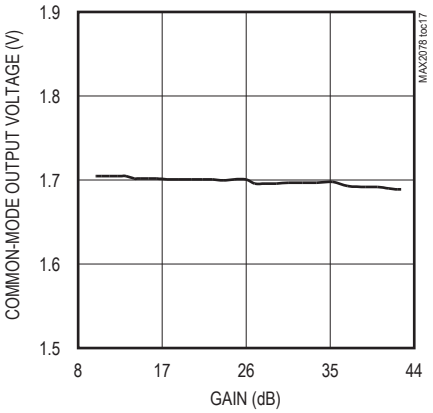
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



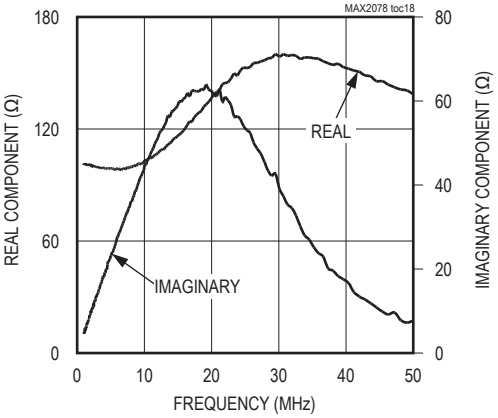
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



COMMON-MODE OUTPUT VOLTAGE vs. GAIN



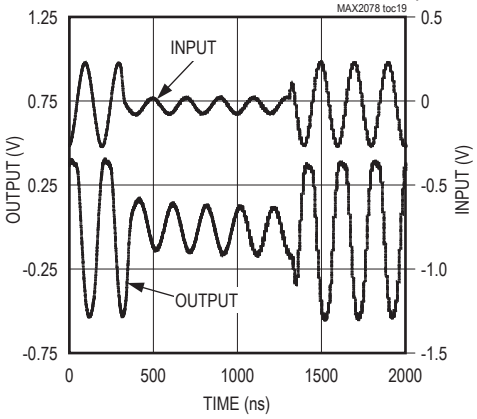
DIFFERENTIAL OUTPUT IMPEDANCE vs. FREQUENCY



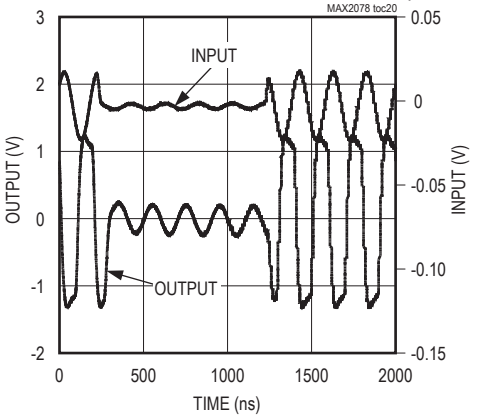
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, CLP = 0, D43/D42/D41/D40 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D45/D44 = 1/1 (f_C = 18MHz), f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, R_S = 200Ω, CI_, CQ_ pulled up to 11V through four separate 0.1% 162Ω resistors, the rise/fall time of the LVDS clock driving the LO_ is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

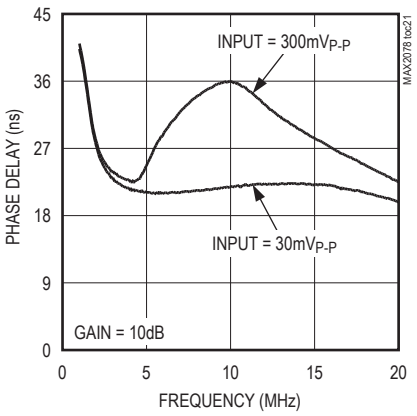
LNA OVERLOAD RECOVERY TIME
(V_{IN} = 500mV$_{P-P}$ for 1µs TO 100mV$_{P-P}$ for 1µs AND BACK TO 500mV$_{P-P}$ for 1s, GAIN = 10dB)



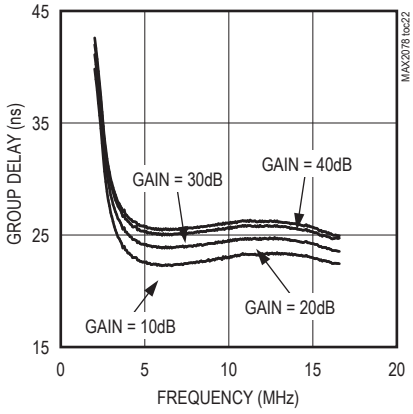
VGA OVERLOAD RECOVERY TIME
(V_{IN} = 40mV$_{P-P}$ for 1µs TO 4mV$_{P-P}$ for 1µs AND BACK TO 40mV$_{P-P}$ for 1s, GAIN = 42.5dB)



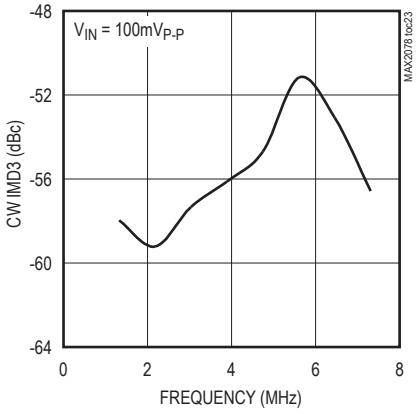
OVERDRIVE PHASE DELAY vs. FREQUENCY



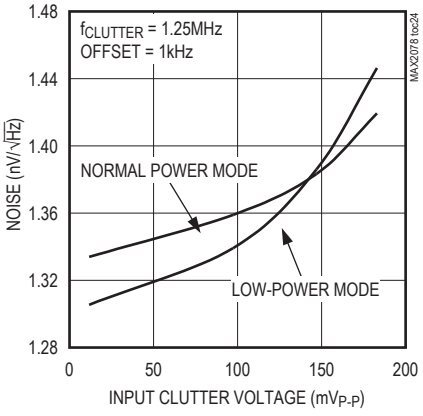
GROUP DELAY vs. FREQUENCY



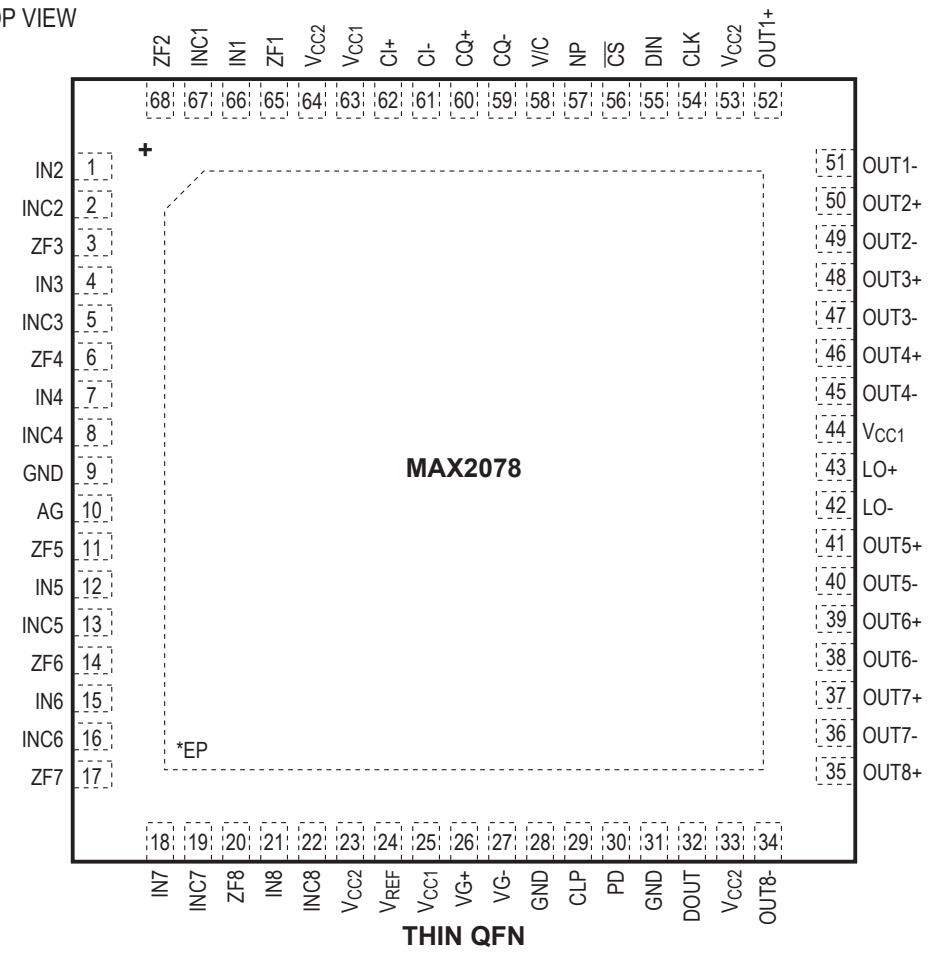
CW IMD3 vs. FREQUENCY



INPUT-REFERRED NOISE vs. INPUT CLUTTER VOLTAGE



Pin Configuration



*EP = EXPOSED PAD.

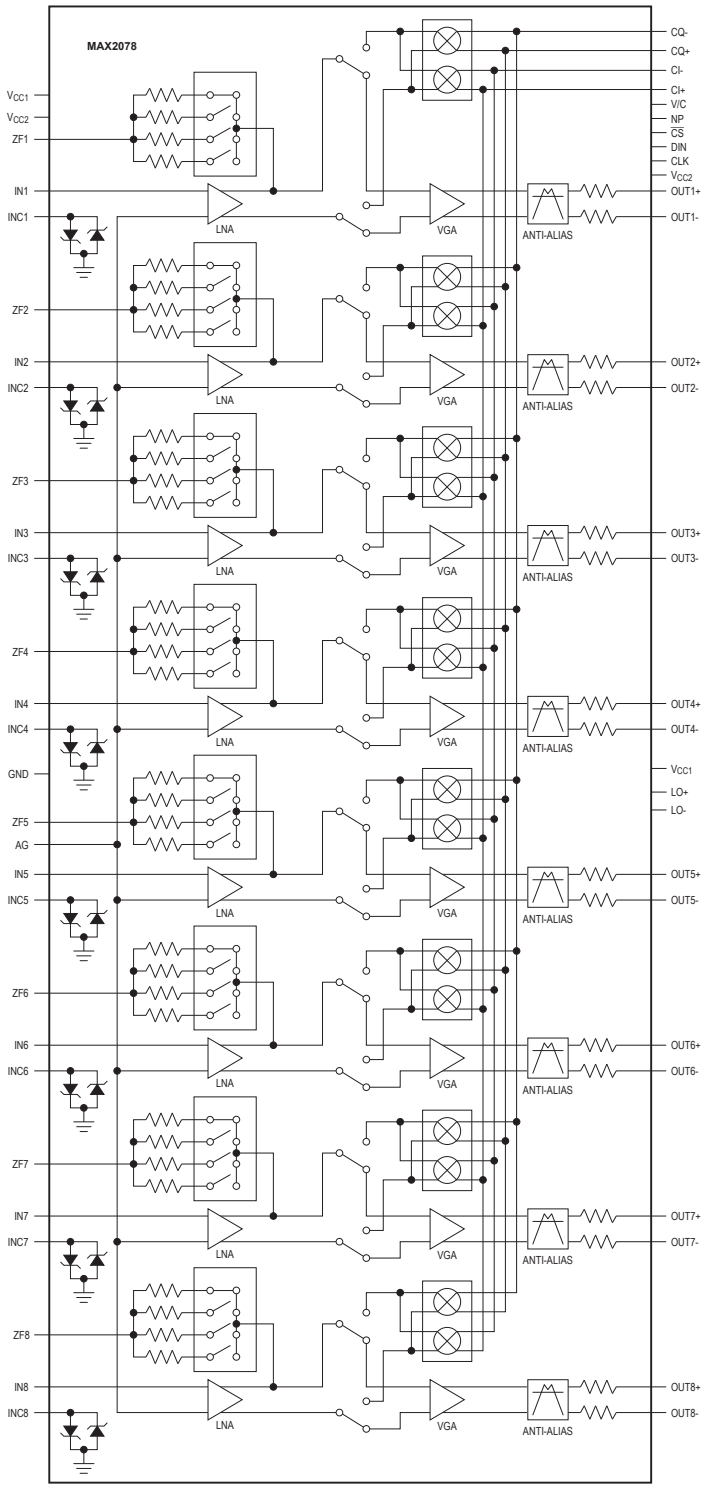
Pin Description

PIN	NAME	FUNCTION
1	IN2	Channel 2 Input
2	INC2	Channel 2 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuit* for details.
3	ZF3	Channel 3 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
4	IN3	Channel 3 Input
5	INC3	Channel 3 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuit* for details.
6	ZF4	Channel 4 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
7	IN4	Channel 4 Input
8	INC4	Channel 4 Clamp Input. Connect to the input coupling capacitor. See the *Typical Application Circuit* for details.
9, 28, 31	GND	Ground
10	AG	AC Ground. Connect a low-ESR 1µF capacitor to ground.
11	ZF5	Channel 5 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
12	IN5	Channel 5 Input
13	INC5	Channel 5 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuit* for details.
14	ZF6	Channel 6 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
15	IN6	Channel 6 Input
16	INC6	Channel 6 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuit* for details.
17	ZF7	Channel 7 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
18	IN7	Channel 7 Input
19	INC7	Channel 7 Clamp Input. Connect to the input coupling capacitor. See the *Typical Application Circuit* for details.
20	ZF8	Channel 8 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
21	IN8	Channel 8 Input
22	INC8	Channel 8 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuit* for details.
23, 33, 53, 64	V_{CC2}	4.75V Power Supply. Connect to an external 4.75V power supply. Connect all 4.75V supply pins together externally and bypass with 100nF capacitors as close as possible to the pin.
24	V_{REF}	External 2.5V Reference Supply. Connect to a low-noise power supply. Bypass to GND with a 0.1µF capacitor as close as possible to the pins. Note that noise performance of the device is dependent on the noise contribution from V_{REF}. Use a low-noise supply for V_{REF}.
25, 44, 63	V_{CC1}	3.3V Power Supply. Connect to an external 3.3V power supply. Connect all 3.3V supply pins together externally and bypass with 100nF capacitors as close as possible to the pin.
26	VG+	VGA Analog Gain Control Differential Input. Set the differential voltage to -3V for minimum gain and to +3V for maximum gain.
27	VG-	
29	CLP	CW Low-Power Mode Select Input. Drive CLP high to place CW mixers in low-power mode.
30	PD	Power-Down Mode Select Input. Set PD to V_{CC1} to place the entire device in power-down mode. Drive PD low for normal operation. This mode overrides the standby mode.
32	DOUT	Serial Port Data Output. Data output for ease of daisy-chain programming. The level is 3.3V CMOS.
34	OUT8-	Channel 8 Negative Differential Output
35	OUT8+	Channel 8 Positive Differential Output
36	OUT7-	Channel 7 Negative Differential Output

Pin Description (continued)

PIN	NAME	FUNCTION
37	OUT7+	Channel 7 Positive Differential Output
38	OUT6-	Channel 6 Negative Differential Output
39	OUT6+	Channel 6 Positive Differential Output
40	OUT5-	Channel 5 Negative Differential Output
41	OUT5+	Channel 5 Positive Differential Output
42	LO-	Differential Local Oscillator Input. LO is divided in the beamformer.
43	LO+	
45	OUT4-	Channel 4 Negative Differential Output
46	OUT4+	Channel 4 Positive Differential Output
47	OUT3-	Channel 3 Negative Differential Output
48	OUT3+	Channel 3 Positive Differential Output
49	OUT2-	Channel 2 Negative Differential Output
50	OUT2+	Channel 2 Positive Differential Output
51	OUT1-	Channel 1 Negative Differential Output
52	OUT1+	Channel 1 Positive Differential Output
54	CLK	Serial Port Clock Input (Positive Edge Triggered). 3.3V CMOS. Clock input for programming the serial shift registers.
55	DIN	Serial Port Data Input. 3.3V CMOS. Data input to program the serial shift registers.
56	CS	Serial Port Chip Select Input. 3.3V CMOS. Used to store programming bits in registers, as well as in CW mode, synchronizing all channel phases (on a rising edge).
57	NP	VGA Standby Mode Select Input. Set NP to 1 to place the entire device in standby mode. Overrides soft channel shutdown in serial shift register, but not general power-down (PD).
58	V/C	VGA/CW Mode Select Input. Set V/C to a logic-high to enable the VGAs and disable CW mode. Set V/C to a logic-low to enable the CW mixers and disable the VGA mode.
59	CQ-	8-Channel CW Negative Quadrature Output. Connect to an external 11V power supply with a 162Ω external pullup resistor.
60	CQ+	8-Channel CW Positive Quadrature Output. Connect to an external 11V power supply with a 162Ω external pullup resistor.
61	CI-	8-Channel CW Negative In-Phase Output. Connect to an external 11V power supply with a 162Ω external pullup resistor.
62	CI+	8-Channel CW Positive In-Phase Output. Connect to an external 11V power supply with a 162Ω external pullup resistor.
65	ZF1	Channel 1 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
66	IN1	Channel 1 Input
67	INC1	Channel 1 Clamp Input. Connect to the input coupling capacitor. See the *Typical Application Circuit* for details.
68	ZF2	Channel 2 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
—	EP	Exposed Pad. Internally connected to ground. Connect to a large ground plane using multiple vias to maximize thermal and electrical performance. Not intended as an electrical connection point.

Block Diagram



Detailed Description

The MAX2078 is a high-density, octal-channel ultrasound receiver optimized for low cost, high-channel count, high-performance portable and cart-based ultrasound applications. The integrated octal LNA, VGA, AAF, and programmable CWD beamformer offer a complete multi-specialty, ultrasound receiver solution.

Imaging path dynamic range has been optimized for exceptional second-harmonic performance. The complete imaging receive channel exhibits an exceptional 68dBFS** SNR at 5MHz. The bipolar front-end has also been optimized for exceptionally low near-carrier modulation noise for exceptional low-velocity pulsed and color-flow Doppler sensitivity under high-clutter conditions, achieving an impressive near-carrier SNR of 140dBc/Hz at 1kHz offset from a V_{OUT} = $1V_{P-P}$, 5MHz clutter signal.

***When coupled with the MAX1437B ADC.*

The MAX2078 also integrates an octal quadrature mixer array and programmable LO phase generators for a complete continuous-wave Doppler (CWD) beamforming solution. Separate mixers for each channel are available for optimal CWD sensitivity, yielding an impressive SNR of 154dBc/Hz at 1kHz offset from a $200mV_{P-P}$, 1.25MHz input signal. The LO phase selection for each channel is programmed using a digital serial interface and a single high-frequency clock. The serial interface is designed to allow multiple devices to be easily daisy-chained to minimize program interface wiring. The outputs of the mixers are summed into single I and Q differential current outputs.

Modes of Operation

The MAX2078 requires programming before it can be used. The operating modes are controlled by 47 programming bits. Table 1 and 2 show the functions of these programming bits.

Table 1. Summary of Programming Bits

BIT NAME	DESCRIPTION
D40, D41, D42	Input impedance programming
D43	LNA gain (D43 = 0 is low gain)
D44, D45	Anti-alias filter f_C programming
D46	Don't care
D0–D39	Beamformer programming, from channel 1 to 8

Table 2. Logic Functions of Programming Bits

D46	D45	D44	D43	D42	D41	D40	MODE
X	X	X	1	0	0	0	R_{IN} = 50Ω, LNA gain = 18.5dB
X	X	X	1	0	0	1	R_{IN} = 100Ω
X	X	X	1	0	1	0	R_{IN} = 200Ω
X	X	X	1	0	1	1	R_{IN} = 1000Ω
X	X	X	0	0	0	0	R_{IN} = 100Ω, LNA gain = 12.5dB
X	X	X	0	0	0	1	R_{IN} = 200Ω
X	X	X	0	0	1	0	R_{IN} = 400Ω
X	X	X	0	0	1	1	R_{IN} = 2000Ω
X	X	X	1	1	X	X	Open feedback
X	0	0	X	X	X	X	f_C = 9MHz
X	0	1	X	X	X	X	f_C = 10MHz
X	1	0	X	X	X	X	f_C = 15MHz
X	1	1	X	X	X	X	f_C = 18MHz

X: Don't care

Low-Noise Amplifier (LNA)

The MAX2078's LNA is optimized for excellent dynamic range and linearity performance characteristics, making it ideal for ultrasound imaging applications. When the LNA is placed in low-gain mode, the input resistance (R_{IN}), being a function of the gain A ($R_{IN} = R_F/(1 + A)$), increases by a factor of approximately 2. Consequently, the switches that control the feedback resistance (R_F) have to be changed. For instance, the 100Ω mode in high gain becomes the 200Ω mode in low gain (see Table 2).

Variable-Gain Amplifier (VGA)

The MAX2078's VGAs are optimized for high linearity, high dynamic range, and low output-noise performance, all of which are critical parameters for ultrasound imaging applications. Each VGA path includes circuitry for adjusting analog gain, as well as an output buffer with differential output ports (OUT_+, OUT_-) for driving ADCs. See the *High-Level CW Mixer and Programmable Beamformer Functional Diagram* for details.

The VGA gain can be adjusted through the differential gain control input VG+ and VG-. Set the differential gain control input voltage at -3V for minimum gain and +3V for maximum gain. The differential analog control common-mode voltage is 1.65V (typ).

Overload Recovery

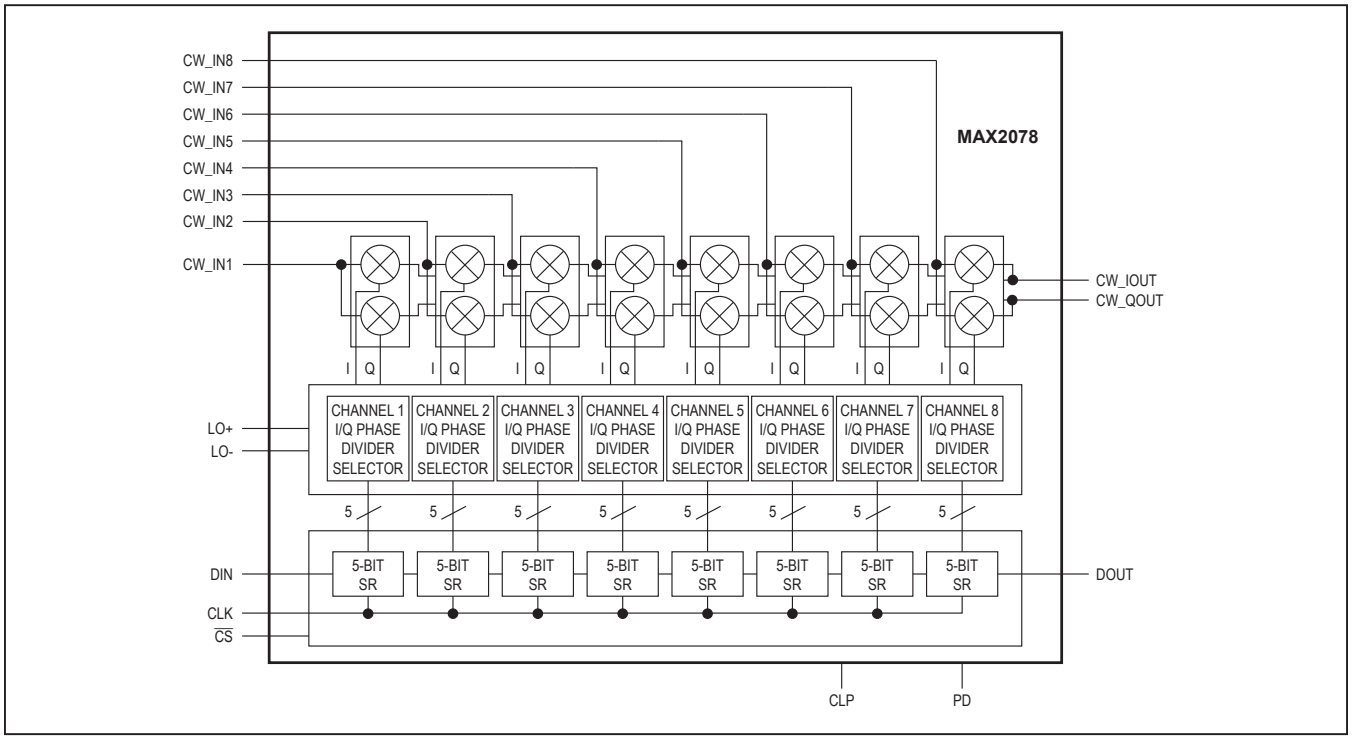
The device is also optimized for quick overload recovery for operation under the large input signal conditions that are typically found in ultrasound input buffer imaging applications. See the *Typical Operating Characteristics* for an illustration of the rapid recovery time from a transmit-related overload.

Octal Continuous-Wave (CW) Mixer

The MAX2078 CW mixers are designed using an active double-balanced topology. The mixers achieve high dynamic range and high linearity performance, with exceptionally low thermal and jitter noise, ideal for ultrasound CWD signal reception. The octal quadrature mixer array provides noise performance of 154dBc/Hz at 1kHz offset from a 1.25MHz, 200mV_{P-P} input clutter signal and a two-tone third-order ultrasound-specific intermodulation product of -48.5dBc (typ). See the *Ultrasound-Specific IMD3 Specification* section.

The octal array exhibits quadrature and in-phase differential current outputs (CQ+, CQ-, CI+, CI-) to produce the total CWD beamformed signal. The maximum differential current output is typically 3mA_{P-P} and the mixer-output compliance voltage ranges from 4.5V to 12V.

High-Level CW Mixer and Programmable Beamformer Functional Diagram



Each mixer can be programmed to 1 of 16 phases; therefore, 4 bits are required for each channel for programming. Each CW channel can be programmed to an off state by setting bit Di to 1. The power-down mode (PD) line overrides this soft shutdown.

After the serial shift registers have been programmed, the $\overline{CS}$ signal, when going high, loads the phase information in the form of 5 bits per channel into the I/Q phase divider/selectors. This presets the dividers, selecting the appropriate mixer phasing. See Table 3 for mixer phase configurations.

CW Mixer Output Summation

The outputs from the octal-channel mixer array are summed internally to produce the total CWD summed beamformed signal. The octal array produces eight differential quadrature (Q) outputs and eight differential in-phase (I) outputs. All quadrature and in-phase outputs are summed into single I and Q differential current outputs (CQ+, CQ-, CI+, CI-).

LO Phase Select

The LO phase dividers can be programmed through the shift registers to allow for 16 quadrature phases for a complete CW beamforming solution.

Synchronization

Figure 1 illustrates the serial programming of the eight individual channels through the serial data port. Note that the serial data can be daisy-chained from one part to another, allowing a single data line to be used to program multiple chips in the system.

Table 3. Mixer Phase Configurations

PER CHANNEL	MSB				LSB	SHUTDOWN
PHASE (DEGREE)	Di + 4	Di + 3	Di + 2	Di + 1		Di
0	0	0	0	0		0/1
22.5	1	0	0	0		0/1
45	0	1	0	0		0/1
67.5	1	1	0	0		0/1
90	0	0	1	0		0/1
112.5	1	0	1	0		0/1
135	0	1	1	0		0/1
157.5	1	1	1	0		0/1
180	0	0	0	1		0/1
202.5	1	0	0	1		0/1
225	0	1	0	1		0/1
247.5	1	1	0	1		0/1
270	0	0	1	1		0/1
292.5	1	0	1	1		0/1
315	0	1	1	1		0/1
337.5	1	1	1	1		0/1

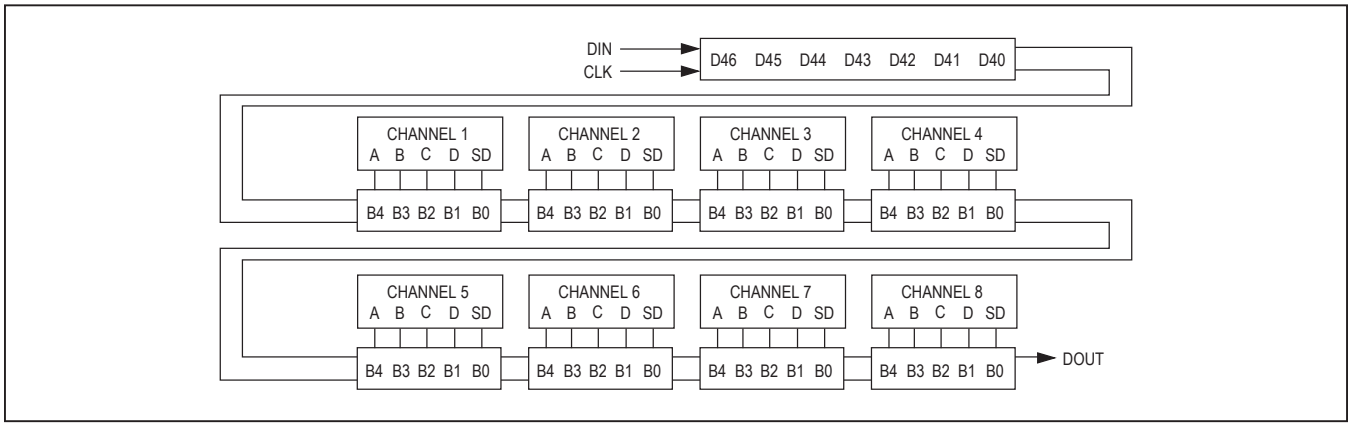


Figure 1. Data Flow of Serial Shift Register

VGA and CW Mixer Operation

During normal operation, the MAX2078 is configured so that either the VGA path is enabled while the mixer array is powered down (VGA mode), or the quadrature mixer array is enabled while the VGA path is powered down (CW mode). For VGA mode, set V/C to a logic-high and for CW mode, set V/C to a logic-low.

Power-Down and Low-Power Mode

The MAX2078 can also be powered down with PD. Set PD to V_{CC1} for power-down mode. In power-down mode, the device draws a total supply current less than 1µA. Set PD to logic-low for normal operation.

A low-power mode is available to lower the required power for CWD operation. When selected, the complex mixers operate at lower quiescent currents and the total per-channel current is lowered to 34.2mA. Note that operation in this mode slightly reduces the dynamic performance of the device. Table 4 shows the logic function of the standard operating modes.

Applications Information

Mode Select Response Time

The mode select response time is the time that the device takes to switch between CW and VGA modes. Figure 2 depicts one possible approach to interfacing the CW outputs to an instrumentation amplifier, which is used to drive an ADC. In this implementation, there are four large-value (in the range of 470nF to 1µF) capacitors between each

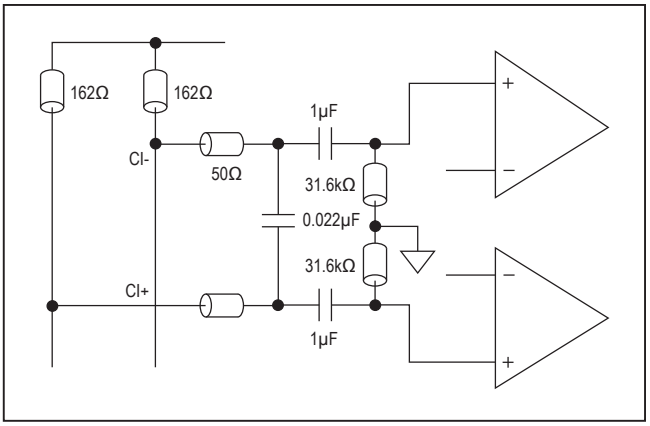


Figure 2. Typical Example of a CW Mixer's Output Circuit

of the CQ+, CQ-, CI+, CI- outputs and the circuitry they are driving. The output of the CW mixer usually drives the input of an instrumentation amplifier made up of op amps whose input impedance is set by common-mode setting resistors.

There are clearly both a highpass corner and a lowpass corner present in this output network. The lowpass corner is set primarily by the 162Ω mixer pullup resistors, the series 50Ω resistors, and the shunt 0.022µF capacitor. This lowpass corner is used to filter a combination of LO leakage and upper sideband. The highpass corner, however, is of a larger concern since it is dominated by the combination of a 1µF DC-blocking capacitor and the pair of shunt 31.6kΩ resistors.

Table 4. Logic Function of Standard Operating Modes

PD INPUT	V/C	CLP	VGA	CW MIXER	INTERNAL SWITCH TO VGA	INTERNAL SWITCH TO CW MIXER	3.3V V_{CC} CURRENT CONSUMPTION	5V V_{CC} CURRENT CONSUMPTION	11V V_{MIX} CURRENT CONSUMPTION
1	1	N/A	Off	Off	Off	Off	0.3µA	0.4µA	0
1	0	N/A	Off	Off	Off	Off	0.1µA	0.6µA	0
0	0	0	Off	On	Off	On	3.2mA	248mA	90.4mA
0	0	1	Off	On	Off	On	3.2mA	216mA	54.4mA
0	1	N/A	On	Off	On	Off	88mA	48mA	0

N/A = Not applicable.

If drawn, the simplified dominant highpass network would look like Figure 3.

The highpass pole in this case is at f_P = 1/(2 x pi x RC) ~ 5Hz. Note that this low highpass corner frequency is required to filter the downconverted clutter tone, which appears at DC, but not interfere with CWD imaging at frequencies as low as 400Hz. For example, if one wanted to use CWD down to 400Hz, then a good choice for the highpass pole would be at least a decade below this (< 40Hz) as not to incur rolloff due to the pole. Remember, if the highpass pole is set to 400Hz, the response is 3dB down at that corner frequency. The placement of the high-pass pole at 5Hz in the above example is between the DC and 40Hz limitations just discussed.

The bottom line is that any reasonably sized DC block between the output of the mixer and the instrumentation amplifier poses a significant time constant that slows the mode select switching speed.

An alternative solution to the approach in Figure 2, which enables faster mode select response time, is shown in Figure 4.

In Figure 4, the outputs of the CWD mixers are DC-coupled into the inputs of the instrumentation amplifiers. Therefore, the op amps must be able to accommodate the full compliance range of the mixer outputs, which is a maximum of 11V when the mixers are disabled, down to the 5V supply of the MAX2078 when the mixers are enabled. The op amps can be powered from 11V for the high rail and 5V for the low rail, requiring a 6V op amp.

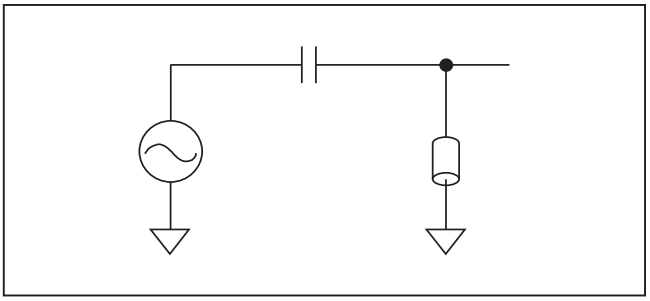


Figure 3. Simplified Circuit of Highpass Pole

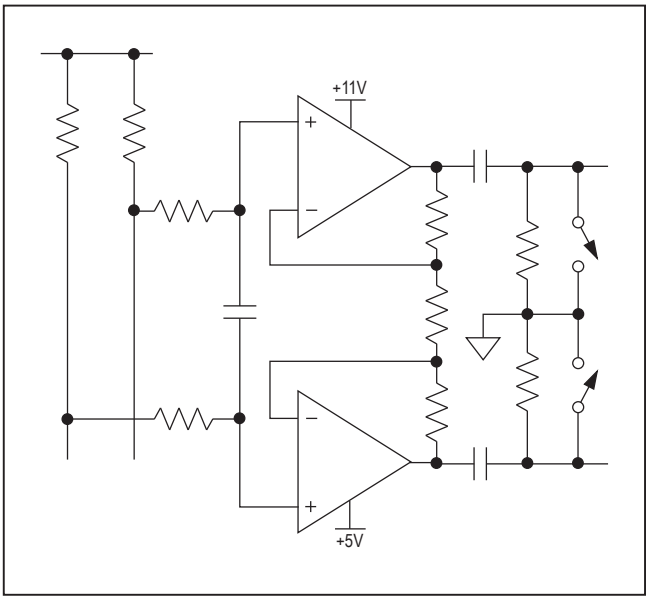


Figure 4. Improved Mode Select Response Time Achieved with DC-Coupled Input to Instrumentation Amplifier

Serial Interface

The MAX2078 is programmed using a serial shift register arrangement. This greatly simplifies the complexity of the program circuitry, reduces the number of IC pins necessary for programming, and reduces the PCB layout complexity. See Table 5 for the programming bit order. The data in (DIN) and data out (DOUT) can be daisy-chained from device to device and all front-ends can run off a single programming clock.

The data can be entered after $\overline{CS}$ goes low. Once a whole word is entered, $\overline{CS}$ needs to rise. When programming the part, enter LSB first and MSB last.

Programming the Beamformer

During the normal CWD mode, the mixer clock (LO+, LO-) is on and the programming signals (DIN, CLK, $\overline{CS}$) are off ($\overline{CS}$ = high, CLK = low, and DIN = don't care, but fixed to a high or a low). To start the programming sequence, turn off the mixer clock. Data is shifted into the shift register at a recommended 10MHz programming rate or 100ns minimum data clock period/time. Assuming a 64-channel CWD receiver, this takes about 30ms for 5 bits per channel. See Figure 5 for timing details. After the shift registers are programmed, pulling $\overline{CS}$ high loads the internal counters into I/Q phase divider/selectors with the proper values. The mixer clock needs to be off when this occurs or there might be timing issues between the load line timing and the mixer clock timing. The user turns on the mixer clock to start beamforming. The clock must turn on so that it starts at the beginning of a mixer clock cycle. A narrow glitch on the mixer clock is not acceptable and could cause metastability in the I/Q phase dividers.

Table 5. Programming Bit Order

47 REGISTER BITS																	
MSB																**LSB**	
								CHANNEL 1 (i = 1)				…	**CHANNEL 8 (i = 8)**				
D46	D45	D44	D43	D42	D41	D40	D39	D38	D37	D36	D35	…	D4	D3	D2	D1	D0
D46	D45	D44	D43	D42	D41	D40	Di + 4	Di + 3	Di + 2	Di + 1	Di	…	Di + 4	Di + 3	Di + 2	Di + 1	Di

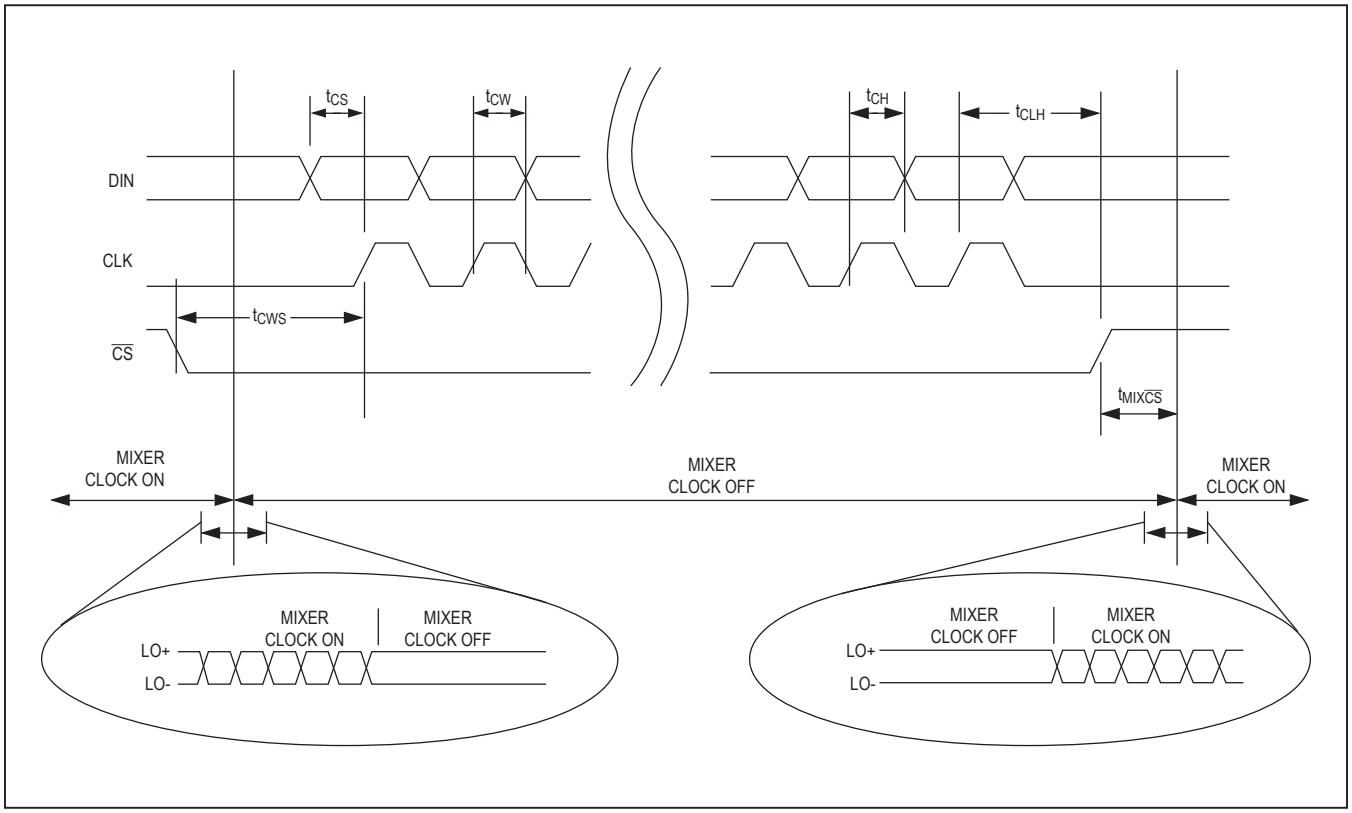


Figure 5. Shift Register Timing Diagram

Ultrasound Front-End CWD Beamformer

The user provides an LO frequency of 16MHz to 120MHz. This high clock frequency requires a differential LVDS input. Note that the LVDS CWD LO clocks are DC-coupled. This is to ensure immediate synchronization when the clock is first turned on. An AC-coupled LO is problematic in that the RC time constant associated with the coupling capacitors and the input impedance of the pin results in a period of time (related to the RC time constant) when the DC level on the chip side of the capacitor is outside the acceptable common-mode range and the LO swing cannot overcome both of the logic thresholds required for proper operation. This problem associated with AC coupling would cause an inability to ensure synchronization among beamforming channels.

The LVDS signal is terminated differentially with an external 100Ω resistor on the board. The LO input is divided internally by 16 to produce 16 phases at a frequency of 1MHz to 7.5MHz. There is one divider per channel. Each channel has a corresponding 5-bit shift register (4 bits for phase programming and 1 bit for channel enable) that is used to program the output phase of the divide-by-16 circuit. The first 4 bits of the shift register are for programming the 16 phases, and the fifth bit can be used to turn on/off each channel individually through the serial bus.

CW Mixer Output Summation

The maximum differential current output is typically $3mA_{P-P}$ and the mixer output-compliance voltage ranges from 4.5V to 12V per mixer channel. The mixer common-mode current in each of the differential mixer outputs is typically 2.83mA. The total summed current would equal N x 2.83mA in each of the 162Ω load resistors (where N = number of channels). In this case, the quiescent output voltage at $+V_{SUM}$ and $-V_{SUM}$ outputs would be 11V - (N x 2.83mA x 162Ω) = 11V - (8 x 2.83mA x 162Ω) = 7.34V. The voltage swing at each output, with one channel driven at maximum output current (differential $2.8mA_{P-P}$) while the other channels are not driven, would be $1.4mA_{P-P}$ x 162Ω or $226mV_{P-P}$ and the differential voltage would be $452mV_{P-P}$. The voltage compliance range is defined as the valid range for $+V_{SUM}$ and $-V_{SUM}$ in this example.

Active Impedance Matching

To provide exceptional noise-figure characteristics, the input impedance of each amplifier uses a feedback topology for active impedance matching. A feedback resistor of the value (1 + (A/2)) x R_S is added between the inverting input of the amplifier to the output. The input impedance is the feedback resistor (Z_F) divided by 1 + (A/2). The factor of two is due to the gain of the amplifier (A) being defined with a differential output. For common input impedances, the internal digitally programmed impedances can be used (see Table 1 and 2). For other input impedances, program the impedance for external resistor operation, and then use an externally supplied resistor to set the input impedance according to the above formula.

Table 6. Noise Figure vs. Source and Input Impedances

R_S (Ω)	R_{IN} (Ω)	NF (dB)
50	50	4.5
100	100	3.4
200	200	2.4
1000	1000	2.1

Noise Figure

The MAX2078 is designed to provide maximum input sensitivity with exceptionally low noise figure. The input active devices are selected for very-low-equivalent input noise voltage and current, optimized for source impedances from 50Ω to 1000Ω. Additionally, the noise contribution of the matching resistor is effectively divided by 1 + (A/2). Using this scheme, typical noise figure of the amplifier is approximately 2.4dB for R_{IN} = R_S = 200Ω. Table 6 illustrates the noise figure for other input impedances.

Input Clamp

The MAX2078 includes configurable integrated input-clamping diodes. The diodes are clamped to ground at ±0.8V. The input-clamping diodes can be used to prevent large transmit signals from overdriving the inputs of the amplifiers. Overdriving the inputs could possibly place charge on the input-coupling capacitor, causing longer transmit overload recovery times. Input signals are AC-coupled to the single-ended inputs IN1–IN8, but are clamped with the INC1–INC8 inputs. See the *Typical Application Circuit*. If external clamping devices are preferred, simply leave INC1–INC8 unconnected.

Analog Output Coupling

The differential outputs of the VGA are capable of driving a differential load capacitance to GND at each of the differential outputs of 25pF, and the differential capacitance across the VGA outputs is 15pF, R_L = 1kΩ. The differential outputs have a common-mode bias of approximately 1.73V. AC-couple these differential outputs if the next stage has a different common-mode input range.

Ultrasound-Specific IMD3 Specification

Unlike typical communications applications, the two input tones are not equal in magnitude for the ultrasound-specific IMD3 two-tone specification. In this measurement, f_1 represents reflections from tissue and f_2 represents reflections from blood. The latter reflections are typically 25dB lower in magnitude, and hence the measurement is defined with one input tone 25dB lower than the other. The IMD3 product of interest (f_1 - (f_2 - f_1)) presents itself as an undesired Doppler error signal in ultrasound applications (see Figure 6).

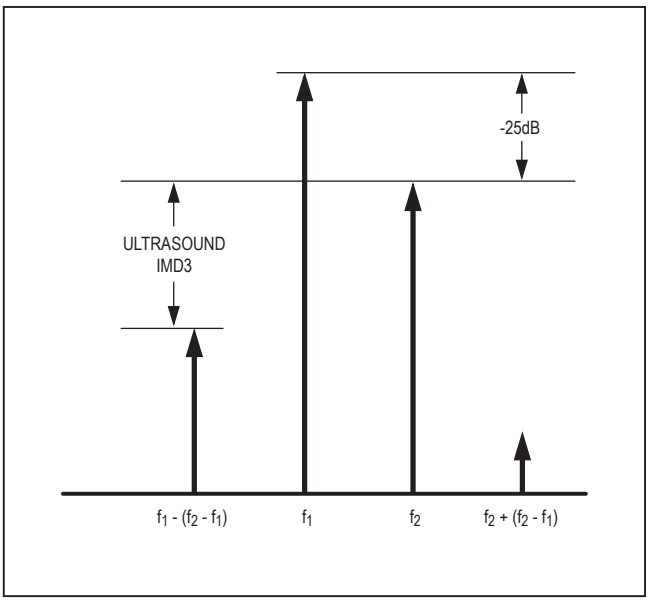


Figure 6. Ultrasound IMD3 Measurement Technique

PCB Layout

The pin configuration of the MAX2078 is optimized to facilitate a very compact physical layout of the device and its associated discrete components. A typical application for this device might incorporate several devices in close proximity to handle multiple channels of signal processing.

The exposed pad (EP) of the MAX2078's TQFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the MAX2078 is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2078CTK+	0°C to +70°C	68 Thin QFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: Complementary BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/09	Initial release	—
1	10/09	Corrected two minor errors	16, 24
2	9/11	Updated input impedance value in *AC Electrical Characteristics—VGA Mode* table	4
3	8/18	Updated Maximum Gain, Low Gain Setting (min) in the *AC Electrical Characteristics—VGA Mode* table	5
4	6/19	Updated the *DC Electrical Characteristics—VGA Mode* table	4

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