Automotive, 100W, USB PD, PPS, Buck-Boost Port Controller and Protector

MAX25432

General Description

The MAX25432 combines an automotive-grade buck-boost controller capable of full-range 3.3V to 21V programmable power supply (PPS) at up to 6.35A, USB Power Delivery (USB PD) analog front-end (AFE), legacy USB charging support, and USB Type-C® protection switches for automotive USB host or downstream-facing (DFP) applications. The USB Type-C protection switches provide automotive system-level ESD protection and 24V short-circuit protection for D+, D-, CC1, CC2, and V_{CONN}. The device can optionally support legacy charging modes for older passenger phones including BC1.2, Apple® Charge, Apple CarPlay®, Apple MFi, and USB On-The-Go (OTG).

The MAX25432B integrates a USB PD AFE, which supports the USB-IF Type-C Port Controller Interface (TCPCI) specification and can interface with any I^2C controller in the application. The MAX25432A provides configuration channel (CC) signal pass-through protection for an external USB PD controller.

P-suffix and G-suffix devices include intelligent detection and protection to avoid high short-circuit currents flowing from the car battery through the cable shield to ground during fault events, thus preventing car module damage.

The MAX25432 is available in a small, 6mm x 6mm, 40-pin TQFN-EP package and requires very few external components. The MAX25432 evaluation (EV) kit and collateral provide a convenient platform to the design engineer for rapid evaluation with reduced test and firmware development time.

Applications

- USB Hubs, Breakout Boxes, and Multimedia Hubs
- Dedicated Charging Modules
- Rear-Seat Entertainment Modules
- Head Unit, Radio, Navigation

Benefits and Features

- Integrated I^2C Buck-Boost Controller with PPS
  - 4.5V to 36V Input Operating Range
  - 3.3V to 21V Constant Voltage, 10mV LSB
  - 1A to 6.35A Current Limit, 25mA LSB
  - 220kHz, 300kHz, and 400kHz Switching Frequency
  - V_{BUS} Cable Compensation up to 516mΩ
  - External Frequency Synchronization and Spread Spectrum for Reduced EMI
- USB PD 3.1 Type-C Port Controller
  - USB-IF Compliant - TID 9154
  - Up to 800mV Ground Offset
  - Pairs with ADI TCPM for Turn-Key Solution
- MAX25432BATLP Enables:
  - ADI TCPM Alternate Mode and Dual-Role Port
  - Improved CC Detection
  - Advanced Monitoring Algorithms (V, T)
  - Dynamic Loop Control
- Highest Performance, Safest, and Lowest Cost Passenger Cable-Shield Short-to-Battery Protection
  - Minimizes Short-Circuit Currents with a Small, Single-FET Solution
- Integrated Current-Sense Amplifiers, ADC and DAC
  - Integrated 3.3V to 5.0V, 1.5W, Smart, Reliable V_{CONN} Switches and Protection, 50mA to 500mA OCP
- Integrated 24V DC Protection on Protected HVD+, HVD-, HVCC1, HVCC2 Outputs
- Integrated Legacy USB 2.0 Charging Including BC1.2, Apple CarPlay, OTG, and Apple MFi Rev 3x
- Integrated ±15kV Air-Gap/±8kV Contact-Discharge ISO 10605 and IEC 61000-4-2 ESD Protection
- -40°C to +125°C Operating Temperature Range
- 40-Pin, 6mm x 6mm, TQFN Package with EP
- AEC-Q100 and AEC-Q006 Qualified

***Ordering Information* appears at end of data sheet.**

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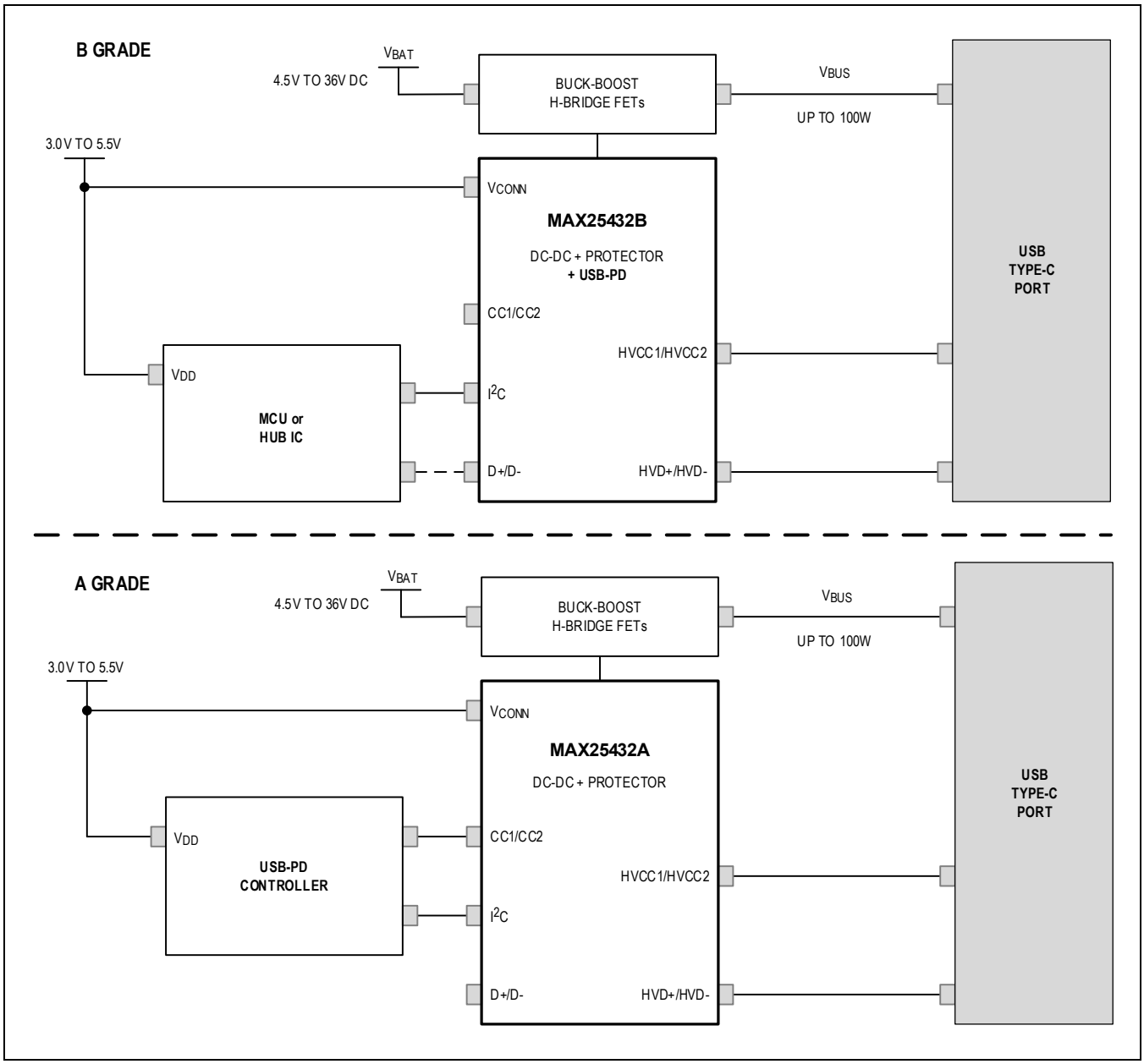
Simplified Block Diagram



Absolute Maximum Ratings

IN to PGND ..... -0.3V to +40V

HVEN, CSP1, CSN1 to PGND ..... -0.3V to V_{IN} +0.3V

LX1 to PGND (Note 1)..... -0.3V to V_{IN} +0.3V

OUT, CSP2, CSN2 to PGND..... -0.3V to +30V

LX2 to PGND (Note 1)..... -0.3V to V_{IN} +0.3V

CSP_ to CSN_ ..... -0.3V to +0.3V

BST1 to LX1, BST2 to LX2..... -0.3V to +6V

BST1, DH1 to PGND..... -0.3V to +46V

BST2, DH2 to PGND..... -0.3V to +36V

DH_ to LX_..... -0.3V to $V_{BST_}$ +0.3V

DL_, V_{COMP}, I_{COMP} to PGND ..... -0.3V to V_{BIAS} +0.3V

BIAS, V_{DD_USB}, V_{DD_IO}, V_{DD_BMC}, to AGND .... -0.3V to +6V

PGND to AGND ..... -0.3V to +0.3V

HVCC1, HVCC2, HVDP, HVDM to AGND ..... -0.3V to +24V

SHLD_SNS to AGND..... -0.3V to +24V

CC1, CC2, V_{CONN} to AGND..... -0.3V to +6V

DP, DM to AGND ..... -0.3V to V_{VDD_USB} +0.3V

ADDR, $\overline{ALERT}$, GDRV, SYNC, to AGND ..... -0.3V to +6V

SCL, SDA to AGND ..... -0.3V to V_{VDD_IO} +0.3V

Continuous Power Dissipation (Note 2)..... 2963mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... -40°C to +150°C

Soldering Temperature (reflow)..... +260°C

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Note 2: Multilayer board; T_A = +70°C, derate 37mW/°C above +70°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

Package Code	T4066+5C
Outline Number	21-0141
Land Pattern Number	90-0055
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	27°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to the Package Index on the Analog Devices website. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to Thermal Characterization of IC Packages.

Electrical Characteristics

(V_{IN} = 14V, V_{HVEN} = V_{IN}, V_{VCONN} = 5V, V_{VDDIO} = 3.3V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Input Voltage Range on IN	V_{IN}		4.5		36	V
IN Supply Current – Off State	I_{IN_OFF}	V_{IN} = 18V, HVEN = 0V, V_{VCONN} = 0V, Off state		16		µA
IN Supply Current – Standby State	I_{IN_STDBY}	Powered; enabled; V_{BUS} off		2.4		mA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Undervoltage Lockout Rising Threshold	$V_{IN_UVLO_R}$	V_{IN} rising. Default setpoint. Programmable from 4.5V to 8.5V in 0.4V steps with IN_UV_THRESH[3:0] register.		4.5		V
IN Undervoltage Lockout Falling Threshold	$V_{IN_UVLO_F}$	V_{IN} falling. Default setpoint.		4.3		V
IN Undervoltage Lockout Accuracy – Rising and Falling	$V_{IN_UVLO_ACC}$	Setpoint programmable in 0.4V steps with IN_UV_THRESH[3:0] register	Setpoint - 0.3	Setpoint	Setpoint + 0.3	V
IN Undervoltage Blanking Time	$t_{DEB_IN_UVLO}$			150		µs
INTERNAL REGULATORS						
BIAS Output Voltage	V_{BIAS}	V_{IN} > 6V, I_{BIAS} = 0 to 80mA	4.7	5.0	5.4	V
BIAS Dropout Voltage	V_{BIAS_DROP}	V_{IN} = 4.5V, I_{BIAS} = 20mA		0.125	0.25	V
BIAS Undervoltage Lockout	V_{UV_BIAS}	V_{BIAS} falling	2.7	3.0	3.3	V
BIAS Undervoltage Lockout Hysteresis	$V_{UV_BIAS_HYST}$			0.25		V
BIAS Short-Circuit Current Limit	I_{BIAS_SC}	V_{BIAS} shorted to AGND	100	200		mA
V_{DD_USB} OutputVoltage	V_{DD_USB}		3.0	3.3	3.6	V
V_{DD_USB} Overvoltage	$V_{DD_USB_OV}$	Rising	3.8	4.0	4.3	V
V_{DD_BMC} Output Voltage	V_{DD_BMC}	MAX25432B only, SHLD_SNS = 0V	1.05	1.125	1.2	V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature	T_{SHDN}	(*Note 4*), T_J rising		165		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYST}	(*Note 4*)		10		°C
BUCK-BOOST CONTROLLER						
Programmable V_{BUS} Voltage Range	V_{OUT}		3.3		21.0	V
V_{BUS} Voltage Step Size	V_{STEP}	VBUS_HIRES = 0b (10-bit resolution mode)		20.51		mV
		VBUS_HIRES = 1b (11-bit resolution mode)		10.255		
V_{BUS} Voltage Accuracy	V_{OUT_ACC}	3.3V ≤ V_{OUT} < vSafe5V, CV mode, no load, VBUS_HIRES = 0b and 1b	-3.03		+3.03	%
		vSafe5V ≤ V_{OUT} ≤ 21V, CV mode, no load, VBUS_HIRES = 0b and 1b	-2.0		+2.0	
V_{BUS} Slew Rise and Fall Times During Transitions	t_{SLEW}	VBUS_HIRES = 0b		0.2		mV/µs
		VBUS_HIRES = 1b		0.1		
Soft-Start Ramp Time	t_{START}		4.0	6.5	9.0	ms
Minimum On-Time	t_{ON_MIN}	Buck mode, 400kHz switching		80		ns
Minimum Off-Time	t_{OFF_MIN}	Boost mode, 400kHz switching		120		ns
Dead Time	DT	Rising and falling edges of DH_ to DL_ and DL_ to DH_		17		ns
DH Pullup Resistance	R_{DH_PU}	V_{BIAS} = 5V, I_{DH} = -100mA		2	4	Ω

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DH Pulldown Resistance	R_{DH_PDWN}	V_{BIAS} = 5V, I_{DH} = +100mA		1	2	Ω
DL Pullup Resistance	R_{DL_PU}	V_{BIAS} = 5V, I_{DL} = -100mA		2	4	Ω
DL Pulldown Resistance	R_{DL_PDWN}	V_{BIAS} = 5V, I_{DL} = +100mA		1	2	Ω
DL1, DL2 Leakage Current	I_{DL_LKG}	V_{DL1} = V_{DL2} = 0 to 5V, T_A = +25°C			1	µA
DH1 Leakage Current	I_{DH1_LKG}	V_{DH1} = V_{LX1} = 0V, T_A = +25°C			1	µA
DH2 Leakage Current	I_{DH2_LKG}	V_{DH2} = V_{LX2} = 0V, T_A = +25°C			1	µA
BUCK-BOOST OSCILLATOR						
Buck-Boost Oscillator Switching Frequency	f_{SW}	FSW[1:0] = 00b	200	220	240	kHz
		FSW[1:0] = 01b	270	300	330	
		FSW[1:0] = 10b	350	400	450	
		FSW[1:0] = 11b	2000	2200	2400	
SYNC Input Frequency Lock Range	f_{SYNCI_RANGE}	External frequency lock range with respect to internal f_{SW} setting when SYNC_DIR = 1b (SYNC Input mode). SYNC input duty cycle range is 30% to 70%.	80		120	%
Spread-Spectrum Frequency Modulation Range (with respect to f_{SW})	SPS	SS_SEL[1:0] = 01b		±3		%
		SS_SEL[1:0] = 10b		±6		
		SS_SEL[1:0] = 11b		±9		
Slope Compensation Peak Ramp Voltage	V_{SLOPE_PK}	Peak ramp voltage per switching period. Default setpoint shown. Programmable from 100mV to 800mV in steps of 100mV with SLP[2:0] register.		400		mV
BUCK-BOOST CURRENT SENSE						
Input Current-Limit Threshold	V_{OC1}	V_{CSP1} - V_{CSN1} rising		50	60	mV
Output Runaway Limit Threshold	V_{OC2}	V_{CSP2} - V_{OUT} rising, V_{OUT} > 0V		75	90	mV
CS Negative Limit Threshold	V_{OC3}	$\lvert V_{CSP2} - V_{OUT} \rvert$ rising, V_{OUT} > 4.5V	-26	-20	-14	mV
Output Overcurrent Limit Accuracy	$I_{LIM_OUT_1A}$	R_{CS3} = 5mΩ	0.9	1.0	1.1	A
	$I_{LIM_OUT_3A}$	R_{CS3} = 5mΩ	2.85	3.00	3.15	
	$I_{LIM_OUT_5A}$	R_{CS3} = 5mΩ	4.75	5.00	5.25	
Output Overcurrent Programmable Step Size	I_{OUT_LSB}	R_{CS3} = 5mΩ		25		mA
Output Overcurrent Protection	I_{OUT_OCP}	R_{CS3} = 5mΩ		6.4		A
CABLE COMPENSATION						
Cable Comp Loop Gain – V_{ADJ}	V_{ADJ}	3mV < V_{OUT} - V_{CSN2} < 30mV, GAIN[5:0] = 111111b	99	103	107	V/V
R-Cable Adjustment/LSB	R_{COMP_LSB}			8.2		mΩ
HVEN AND SYNC I/O PINS						

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Input Logic-High	VIH_{SYNC}	V_{SYNC} rising	2.0			V
SYNC Input Logic-Low	VIL_{SYNC}	V_{SYNC} falling			0.5	V
HVEN Rising Threshold	V_{HVEN_R}	V_{HVEN} rising threshold; guaranteed logic-high level when V_{HVEN} ≥ 1.8V	1.20	1.45	1.80	V
HVEN Falling Threshold	V_{HVEN_F}	V_{HVEN} falling threshold; guaranteed logic-low level when V_{HVEN} ≤ 1.0V	1.00	1.26	1.60	V
HVEN Input Leakage	I_{HVEN_LKG}	V_{HVEN} = 5.5V, T_A = +25°C			+1	µA
SYNC Pulldown Resistance	$R_{SYNC-PD}$			1		MΩ
V_{CONN} SWITCH						
V_{CONN} Valid Voltage Range	V_{VCONN}		3.0		5.5	V
V_{CONN} Switch On-Resistance	R_{ON_VCONN}	V_{VCONN} = 5.0V and V_{VCONN} = 3.3V, $I_{HVCC_}$ = 0.25A		400	800	mΩ
V_{CONN} Programmable Overcurrent Threshold (Low)	$I_{VCONN_OCP_L}$	Measured on CC1 and CC2; V_{VCONN} = 5.0V or 3.3V	50		500	mA
V_{CONN} OCP Low Programmable Step Size	$I_{VCONN_OCP_L_LSB}$			50		mA
V_{CONN} Overcurrent Threshold (High)	$I_{VCONN_OCP_H}$	Measured on CC1 and CC2; V_{VCONN} = 3.3V and V_{VCONN} = 5.0V		750		mA
V_{CONN} Start-up Time at 90%	t_{VCONN_ON}	Time from V_{CONN} switch enable to CC settled at 90% of final value with V_{VCONN} = 5.0V		300		µs
V_{CONN} Leakage Current	I_{VCONN_LKG}	V_{CONN} switch disabled; V_{VCONN} = 5.0V			5	µA
V_{CONN} Fast UV Comparator Trip Threshold	$V_{VCONN_FAST_UV}$	V_{CONN} enabled, measured at V_{CONN} pin, V_{VCONN} falling	Setpoint - 0.25	Setpoint	Setpoint + 0.25	V
USB TYPE-C/CURRENT LEVEL CHARACTERISTICS						
CC DFP Default Current Source	$I_{DFP_DEF_CC}$		64	80	96	µA
CC DFP 1.5A Current Source	$I_{DFP1.5_CC}$		166	180	194	µA
CC DFP 3.0A Current Source	$I_{DFP3.0_CC}$		304	330	356	µA
CC PASS-THROUGH ANALOG SWITCHES						
Analog Signal Range			0		5.5	V
CC Switch On-Resistance	R_{ON_CC}	Resistance from CC1 to HVCC1 or CC2 to HVCC2		4		Ω
HVCC OV Protection Trip Threshold	V_{OV_HVCC}		5.65	5.80	5.95	V
HVCC OV Blanking Timeout Period	t_{FP_HVCC}	From OV condition to switch opened		1.0		µs
CC Switch ON Leakage	$I_{CC_ON_LKG}$	CC switch ON, CC pullup voltage 5.5V; leakage to GND			10	µA
HVCC Pin OFF Leakage	$I_{HVCC_OFF_LKG}$	HVCC switch OFF; V HVCC_ = 20V; HVCC_ pins leakage to GND			25	µA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVCC Open Termination Impedance	Z_{OPEN}	Impedance to GND	500			kΩ
HVCC Discharge Resistance	R_{DCH_HVCC}			3.0	6.2	kΩ
USB PD BMC (MAX25432B ONLY)						
BMC Tx Rise Time	t_{RISE}	10% to 90% with no load on CC wires	300	430		ns
BMC Tx Fall Time	t_{FALL}	90% to 10% with no load on CC wires	300	430		ns
BMC Tx Swing	V_{SWING}	Applies to no load and with max load defined by cable/receiver model	1.05	1.125	1.2	V
BMC Driver Output Impedance	z_{DRIVER}	Source output impedance	33	48	75	Ω
BMC Receiver Noise Filter	$t_{RXFILTER}$	Time constant of noise filter in Rx path	100			ns
Receiver Input Impedance	z_{BMCRX}			2		MΩ
Receiver Detect Rising Threshold	$V_{BMCRxDet_Rth}$		0.645	0.685	0.725	V
Receiver Detect Falling Threshold	$V_{BMCRxDet_Fth}$		0.565	0.605	0.645	V
DP, DM ANALOG USB SWITCHES						
Analog Signal Range	V_{D_RANGE}		0		V_{DD_USB}	V
Protection Trip Threshold	$V_{OV_D_L}$	V_{HVDP} /V_{HVDM} rising; only for AUTO_CDP_DCP_MODE[1:0] = 01b (Auto-CDP mode)	3.65	3.85	4.05	V
	$V_{OV_D_H}$	V_{HVDP} /V_{HVDM} rising; all other modes	4.0	4.15	4.30	
Protection Response Time	t_{FP_D}	V_{HVEN} = 4.0V, V_{HVDP} = V_{HVDM} = 3.3V to 4.3V step, R_L = 15kΩ on DP and DM, delay to V_{DP} = V_{DM} < 3V		2		µs
Data Switch Differential Bandwidth	BW_{D_DIFF}	USB TEST_PACKET at 240MHz fundamental; -3dB BW		1000		MHz
On-Resistance Switch A	R_{ON_SA}	I_L = 10mA, $V_{D_}$ = 0V to V_{DD_USB}, V_{DD_USB} = 3.3V		4	8	Ω
On-Resistance Match between Channels Switch A	ΔR_{ON_SA}	I_L = 10mA, $V_{D_}$ = 1.5V or 3.0V			0.25	Ω
On-Resistance Flatness Switch A	$R_{FLAT(ON)A}$	I_L = 10mA, $V_{D_}$ = 0V or 0.4V			0.25	Ω
On-Resistance of HVDP/HVDM Short	R_{SHORT}	V_{DP} = 1V, I_{DM} = 500µA		90	180	Ω
HVDP/HVDM On-Leakage Current	I_{HVD_ON}	V_{HVDP} = V_{HVDM} = 3.6V or 0V	-7		+7	µA
HVDP/HVDM Off-Leakage Current	I_{HVD_OFF}	V_{HVDP} = 18V or V_{HVDM} = 18V, V_{DP} = V_{DM} = 0V			100	µA
DP/DM Off-Leakage Current	I_{D_OFF}	V_{HVDP} = V_{HVDM} = 18V, V_{DP} = V_{DM} = 0V	-1		+1	µA
USB 2.0 HOST CHARGER DETECTION, HVDP/HVDM						
Input Logic-High	V_{IH_CD}		2.0			V
Input Logic-Low	V_{IL_CD}				0.8	V

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Sink Current	I_{DAT_SINK}	V_{DAT_SINK} = 0.25V to 0.4V	50	85	150	µA
Data Detect Voltage High	V_{DAT_REFH}		0.4			V
Data Detect Voltage Low	V_{DAT_REFL}				0.25	V
Data Detect Voltage Hysteresis	V_{DAT_HYST}			60		mV
Data Source Voltage	V_{DAT_SRC}	I_{SRC} = 200µA	0.5		0.7	V
V_{BUS} ADC						
ADC Resolution	Res_ADC			10		bits
ADC V_{BUS} LSB	$V_{OUT_LSB_ADC}$	VBUS_VOLTAGE[9:0] register		25		mV
ADC I_{BUS} LSB	$I_{OUT_LSB_ADC}$	VBUS_CURRENT[7:0] register		50		mA
ADC Acquisition Time (V_{BUS} and I_{BUS})	t_{ACQ_ADC}	Total time for both acquisitions		2		ms
V_{BUS} OUTPUT MONITORS						
V_{BUS} OV	$V_{BUS_OV_PROG}$	Programmable in 1.25% steps from +8.75% to +17.5% by changing the VBUS_OV_THRESH[2:0] register		+12.5%		%
V_{BUS} UV	$V_{BUS_UV_PROG}$	Programmable in 1.25% steps from -8.75% to -17.5% by changing the VBUS_UV_THRESH[2:0] register		-12.5%		%
V_{BUS} Removal Detect Threshold	vSafe0V	Falling	0.6	0.75	0.8	V
V_{BUS} Removal Detect Hysteresis	vSafe0V	Rising hysteresis		0.05		V
SHIELD FET CONTROL						
GDRV Unloaded Output Voltage High	$V_{GDRV,H}$		4.5		5.5	V
GDRV Output Voltage High	$V_{GDRV,LOAD}$	I_{GDRV} = 10µA (sink)	4			V
GDRV Output Voltage Low	$V_{GDRV,L}$	I_{SINK} = 1mA (pullup)			0.8	V
I^2C DIGITAL INPUTS (SDA, SCL) AND V_{DD_IO} SUPPLY INPUT						
Input Leakage Current (SCL, SDA)	I_{I2C_LKG}	V_{PIN} = 5.5V, 0V	-5		5	µA
Logic-High (SCL, SDA)	V_{IH}		0.7 x V_{VDD_IO}			V
Logic-Low (SCL, SDA)	V_{IL}				0.3 x V_{VDD_IO}	V
Hysteresis (SCL, SDA)	V_{I2C_HYST}			300		mV
V_{DD_IO} Input Voltage Range	V_{VDD_IO}		1.8		5.0	V
ADDR RESISTOR CONVERTER						
ADDR Current Leakage	I_{ADDR_LKG}	V_{ADDR} = 0 to 5V			±5	µA
Minimum Guaranteed Decoding Window Range	R_{ADDR_TOL}		-5		5	%

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS ($\overline{ALERT}$, SDA)						
Output-High Leakage Current	I_{OH_LKG}	Pull up 0V and 5.5V	-10		10	µA
Output Low Level	V_{OL}	Sinking 1mA			0.4	V
I²C DYNAMIC CHARACTERISTICS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			ns
DATA Valid Time	$t_{SU;DAT}$				0.45	µs
DATA Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Noise Suppression on SCL and SDA	NS_{I2C}			50		ns
ESD PROTECTION (ALL PINS)						
ESD Protection Level	V_{ESD}	Human Body Model (HBM)		±2		kV
ESD PROTECTION (HVDP, HVDM, HVCC1, HVCC2, SHLD_SNS)						
ESD Protection Level	V_{ESD}	ISO 10605 Air Gap (330pF, 2kΩ)		±15		kV
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air Gap (150pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		

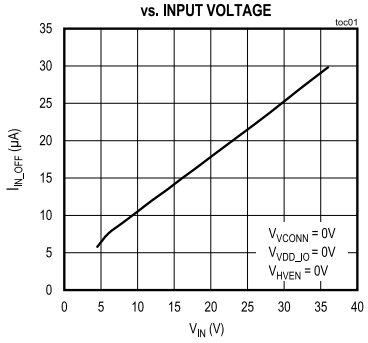
Note 3: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

Note 4: Guaranteed by design and bench characterization. Limits are not production tested.

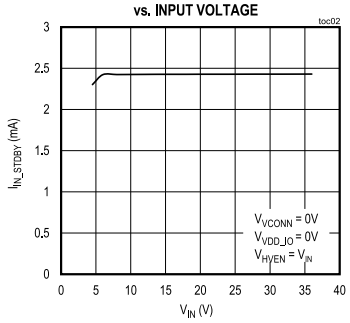
Typical Operating Characteristics

(V_{IN} = 14V; V_{HVEN} = V_{IN}; V_{VCONN} = 5V; V_{VDD_IO} = 3.3V; T_A = +25°C, unless otherwise noted.)

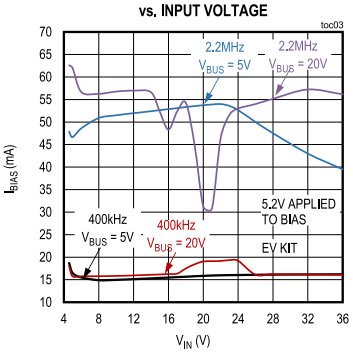
SHUTDOWN CURRENT vs. INPUT VOLTAGE



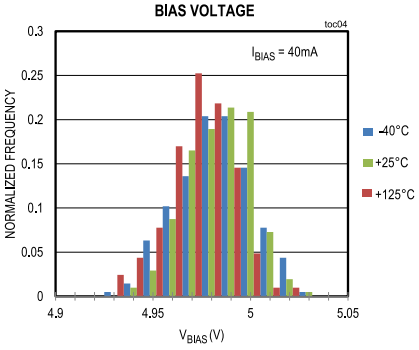
STANDBY CURRENT vs. INPUT VOLTAGE



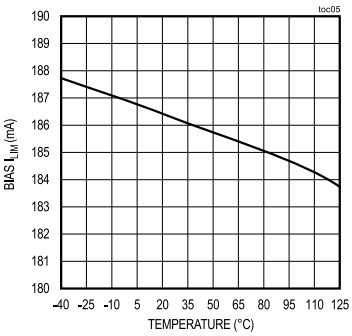
BIAS CURRENT vs. INPUT VOLTAGE



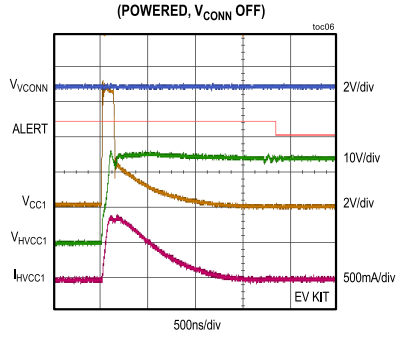
BIAS VOLTAGE



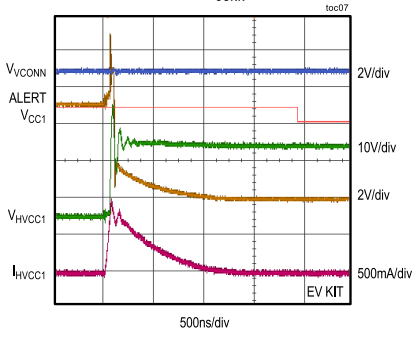
BIAS I_{LIM} vs. TEMPERATURE



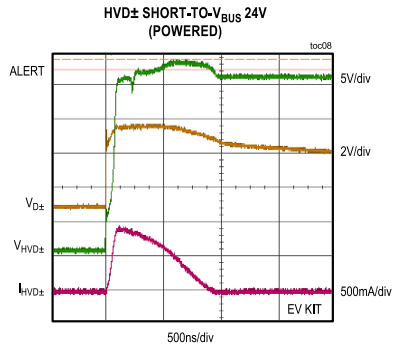
HVCC SHORT-TO-V_{BUS} 24V (POWERED, V_{CONN} OFF)



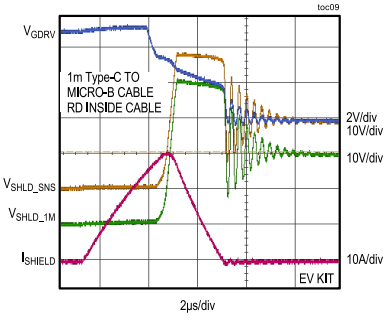
HVCC SHORT-TO-V_{BUS} 24V (POWERED, V_{CONN} ON)



HVD± SHORT-TO-V_{BUS} 24V (POWERED)

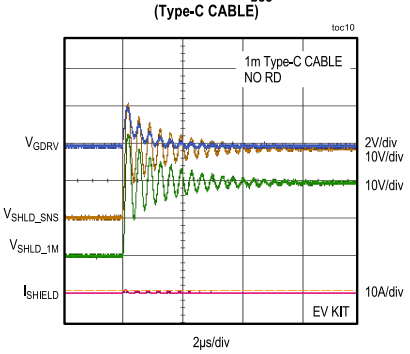


SHIELD SHORT-TO-V_{BUS} 24V (LEGACY CABLE)

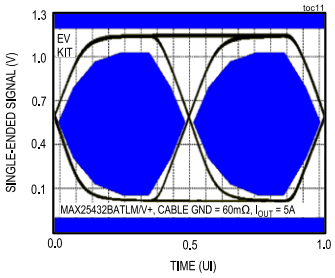


(V_{IN} = 14V; V_{HVEN} = V_{IN}; V_{VCONN} = 5V; V_{VDD_IO} = 3.3V; T_A = +25°C, unless otherwise noted.)

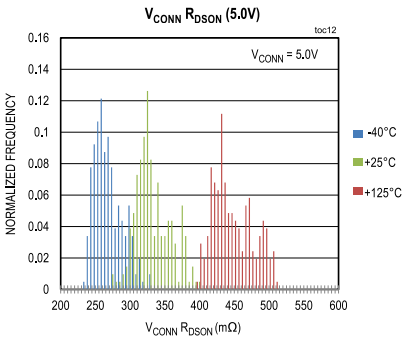
SHIELD SHORT-TO-V_{BUS} 24V (Type-C CABLE)



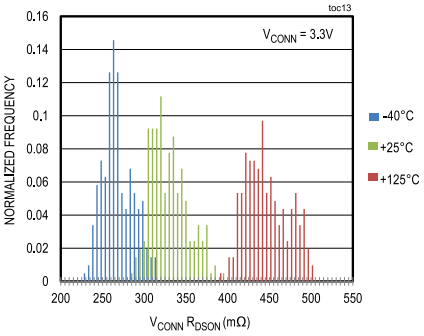
BMC EYE DIAGRAM WITH GROUND OFFSET COMPENSATION



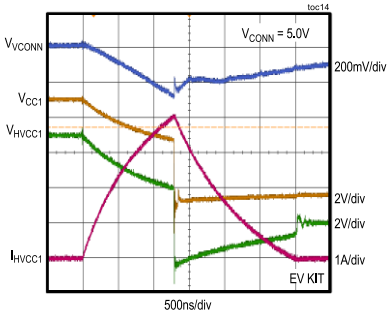
V_{CONN} R_{DSON} (5.0V)



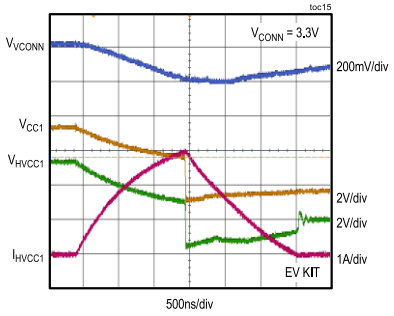
V_{CONN} R_{DSON} (3.3V)



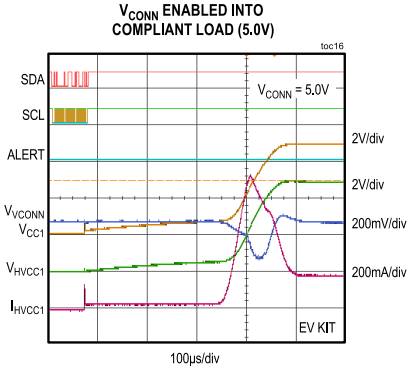
V_{CONN} SHORT-TO-GROUND RESPONSE (5.0V)



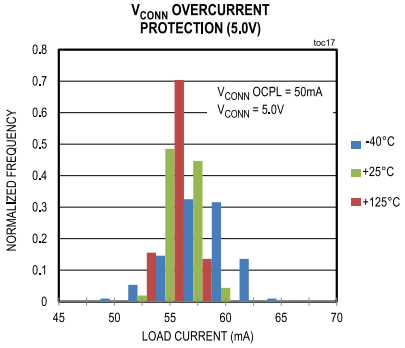
V_{CONN} SHORT-TO-GROUND RESPONSE (3.3V)



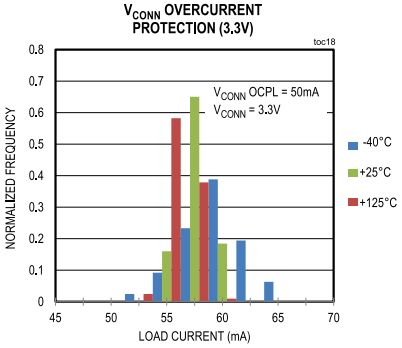
V_{CONN} ENABLED INTO COMPLIANT LOAD (5.0V)



V_{CONN} OVERCURRENT PROTECTION (5.0V)

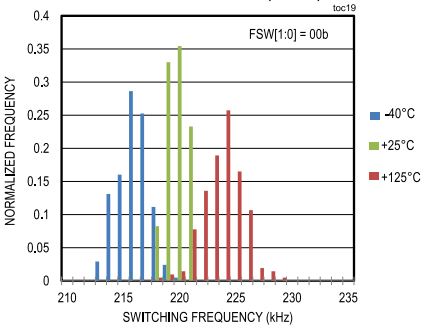


V_{CONN} OVERCURRENT PROTECTION (3.3V)

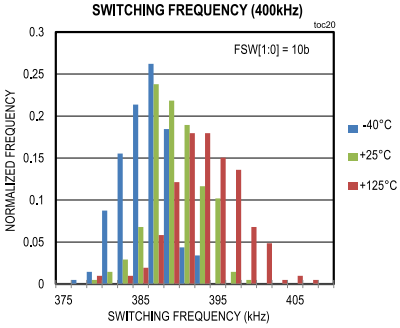


(V_{IN} = 14V; V_{HVEN} = V_{IN}; V_{VCONN} = 5V; V_{VDD_IO} = 3.3V; T_A = +25°C, unless otherwise noted.)

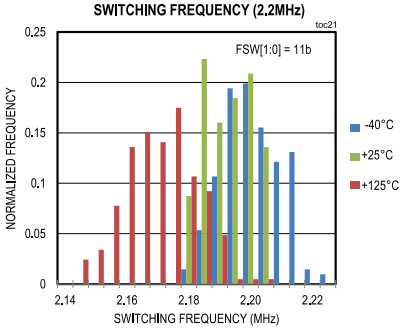
SWITCHING FREQUENCY (220kHz)



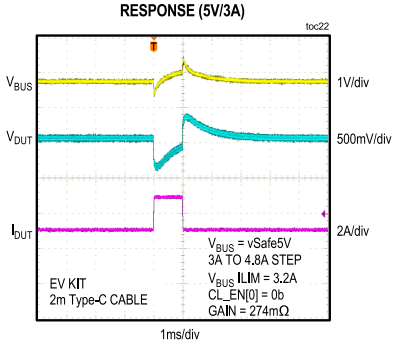
SWITCHING FREQUENCY (400kHz)



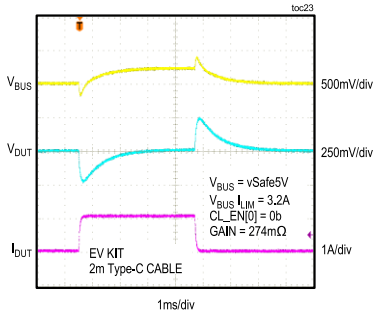
SWITCHING FREQUENCY (2.2MHz)



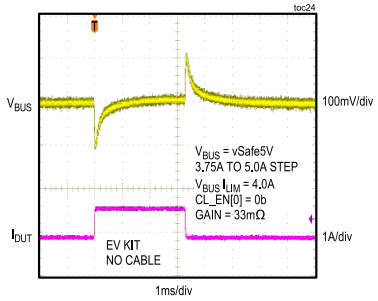
MFi R3x OVERCURCURRENT RESPONSE (5V/3A)



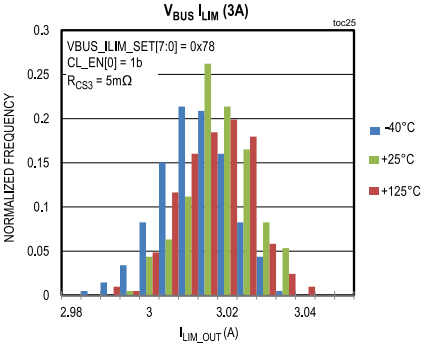
LOAD TRANSIENT RESPONSE (5V, 80mA TO 1A)



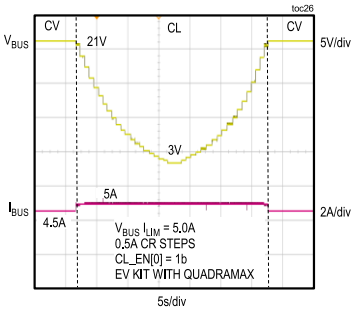
USB PD LOAD TRANSIENT (5V/5A)



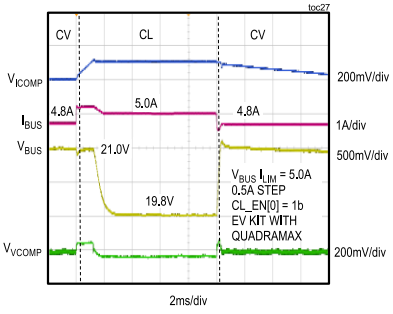
V_{BUS} I_{LIM} (3A)



USB PD PPS CURRENT-LIMIT RESPONSE

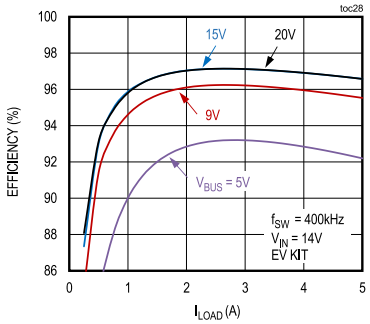


USB PD PPS CURRENT-LIMIT TRANSIENT RESPONSE

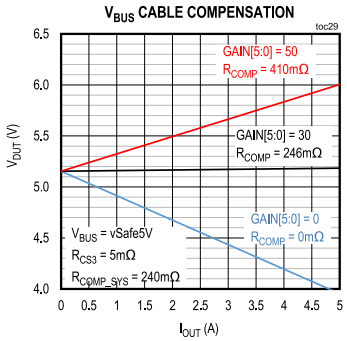


(V_{IN} = 14V; V_{HVEN} = V_{IN}; V_{VCONN} = 5V; V_{VDD_IO} = 3.3V; T_A = +25°C, unless otherwise noted.)

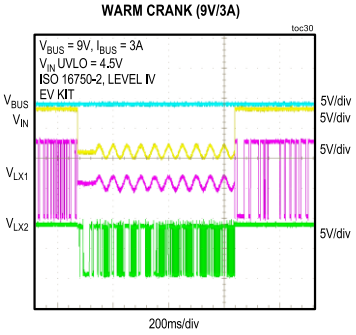
BUCK-BOOST EFFICIENCY vs. LOAD CURRENT



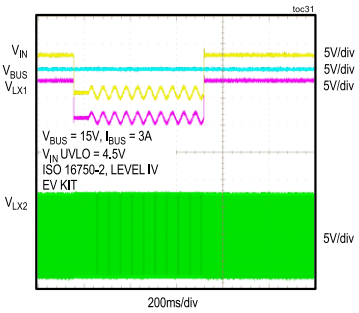
V_{BUS} CABLE COMPENSATION



WARM CRANK (9V/3A)

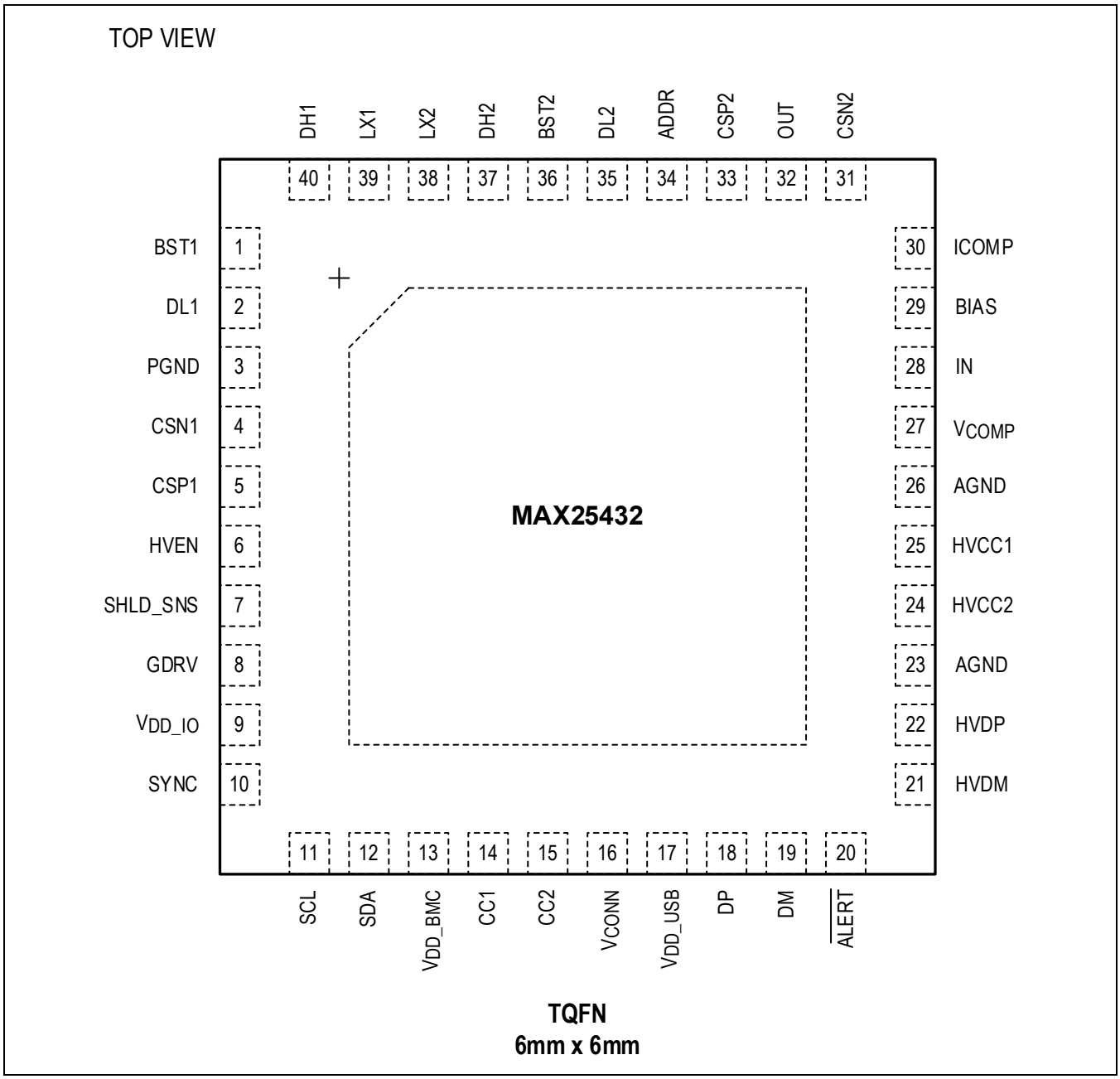


WARM CRANK (15V/3A)



Pin Configurations

MAX25432



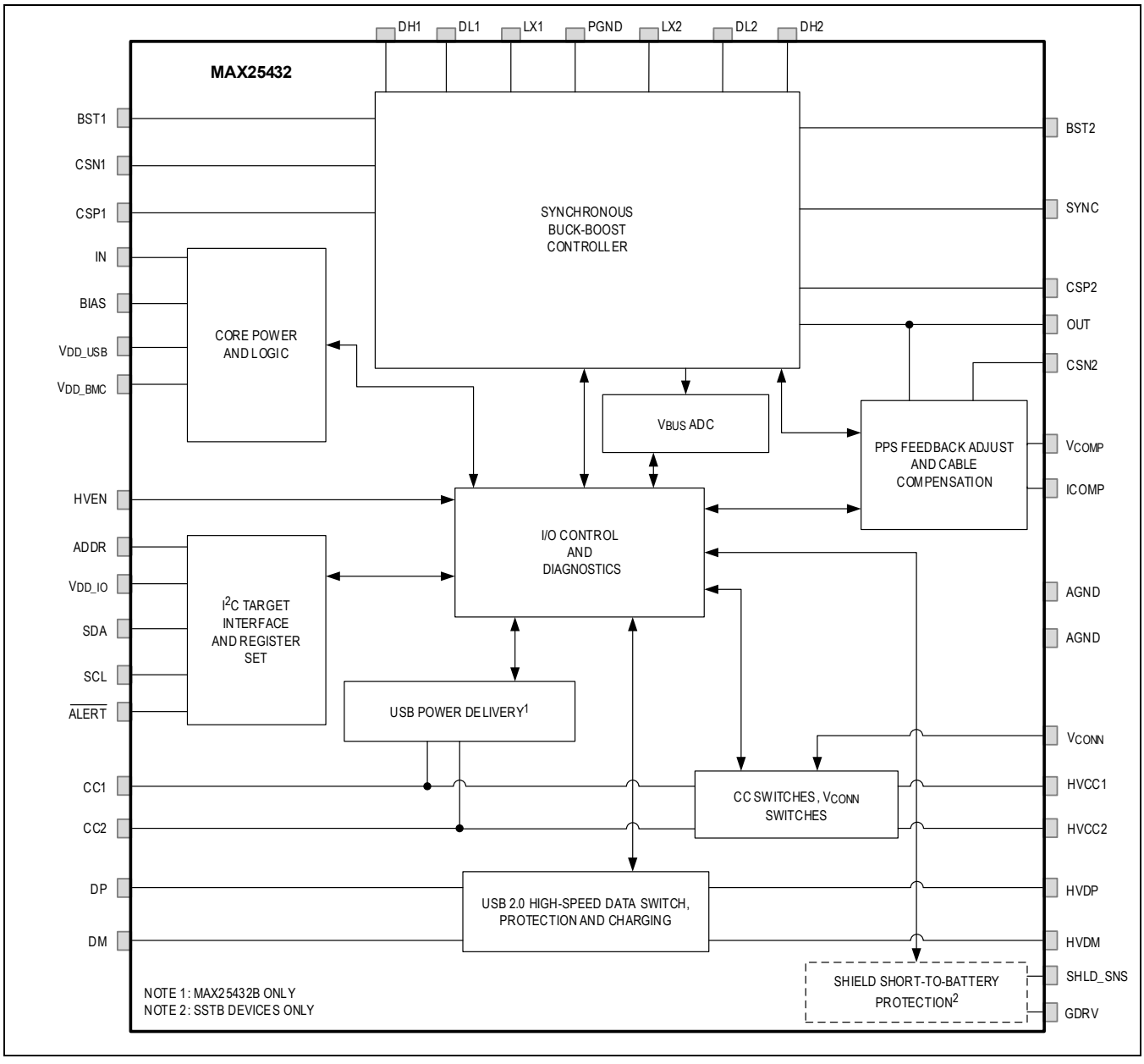
Pin Descriptions

PIN	NAME	FUNCTION
1	BST1	Bootstrap Capacitor Pin for High-Side Driver of LX1 Node. Connect a 0.1µF capacitor between BST1 and LX1.
2	DL1	Buck Low-Side Gate Drive Output. Connect to the gate of Q_{b1} external N-channel MOSFET.
3	PGND	Buck-Boost Power Ground. Connect directly to GND. Connect to GND copper underneath IC.
4	CSN1	Negative Terminal of the Input High-Side Current-Sense Amplifier. Connect CSN1 as close to R_{CS1} as possible using a Kelvin sense routing.
5	CSP1	Positive Terminal of the Input High-Side Current-Sense Amplifier. Connect CSP1 as close to R_{CS1} as possible using a Kelvin sense routing.
6	HVEN	High-Voltage Enable Input. Driving HVEN high powers up the IC. This pin can be connected directly to battery voltage or car accessory power. This pin can also be driven by a 3.3V or 5V general-purpose output from a microcontroller.
7	SHLD_SNS	Shield Sense Pin. SSTB devices: in order to protect against shield short-to-battery events, connect SHLD_SNS to the drain of the external shield N-channel FET, which is connected to the SHIELD and GND pins of the USB Type-C receptacle. All MAX25432B devices have optional USB PD physical layer (PHY) ground offset compensation input. Connect to downstream Type-C captive cable ground sense line. For all other devices, or if not used, connect to the IC GND.
8	GDRV	Shield FET Gate Drive Output. Active on all MAX25432 devices. Refer to GDRV Truth Table. Connect to the gate of an external N-channel FET to let the MAX25432 control the ground connection on the downstream Type-C connector. If not used, connect a 1MΩ resistor from GDRV to the IC GND.
9	V_{DD_IO}	External Input Supply for I^2C Interface. Bypass with 10nF ceramic capacitor to AGND.
10	SYNC	Optional Switching Frequency Input/Output for Synchronization with Other Switching Regulators. Leave as an input and tie to the IC GND if not used.
11	SCL	I^2C Clock Pin. Connect to V_{DD_IO} through a pullup resistor.
12	SDA	I^2C Data Pin. Connect to V_{DD_IO} through a pullup resistor.
13	V_{DD_BMC}	MAX25432A: Connect V_{DD_BMC} to AGND. MAX25432B: Internal 1.125V Regulated Supply Output. Powers the biphase mark coding (BMC) Tx driver output. Bypass with a 1µF ceramic capacitor to AGND. Do not connect external loads to V_{DD_BMC}.
14	CC1	MAX25432A: Protected CC1. Connect to upstream CC1 configuration channel of the external USB PD controller. MAX25432B: No Connect.
15	CC2	MAX25432A: Protected CC2. Connect to upstream CC2 configuration channel of the external USB PD controller. MAX25432B: No Connect.
16	V_{CONN}	V_{CONN} Input Supply. Connect to BIAS or an external 5V or 3.3V supply. Bypass with a 10µF ceramic capacitor to GND when connected to a 3.3V supply. Bypass with a 1µF ceramic capacitor to GND when connected to BIAS or a 5V supply.
17	V_{DD_USB}	Internal 3.3V Regulated Supply Output. Bypass V_{DD_USB} to GND with a 1µF ceramic capacitor. Do not connect external loads to V_{DD_USB}.
18	DP	Protected D+ USB 2.0 Data Path. For charging downstream port (CDP) applications, connect to the low-voltage USB transceiver or HUB IC D+ connection. For dedicated charging port (DCP) applications, tie to the DM pin.
19	DM	Protected D- USB 2.0 Data Path. For CDP applications, connect to the low-voltage USB transceiver or HUB IC D- connection. For DCP applications, tie to the DP pin.
20	$\overline{ALERT}$	Open-Drain Interrupt Output. Indicates alerts to the I^2C controller. Connect a 100kΩ pullup from $\overline{ALERT}$ to V_{DD_IO}.
21	HVDM	High-Voltage-Tolerant D- Connection to Downstream USB Type-C Connector or Captive Cable.
22	HVDP	High-Voltage-Tolerant D+ Connection to Downstream USB Type-C Connector or Captive Cable.

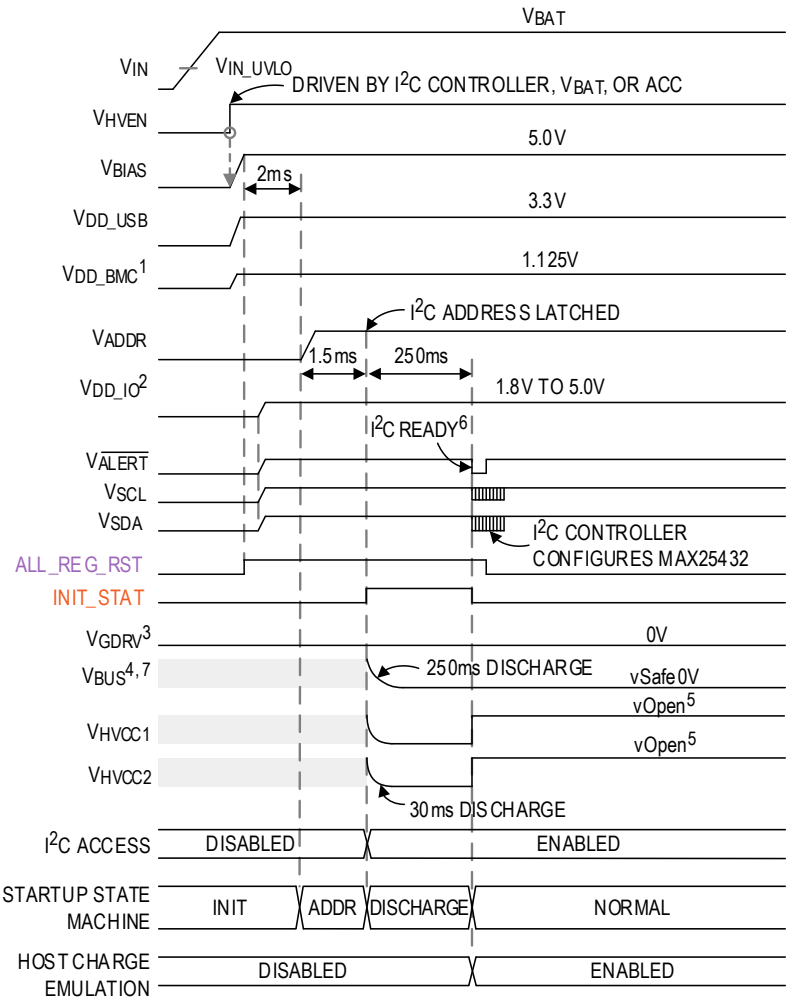
23, 26	AGND	Analog Ground Pin (IC GND). Connect directly to GND; tie to GND pour underneath the IC.
24	HVCC2	High-Voltage-Tolerant CC2 Connection to Downstream USB Type-C Connector or Captive Cable.
25	HVCC1	High-Voltage-Tolerant CC1 Connection to Downstream USB Type-C Connector or Captive Cable.
27	V_{COMP}	Voltage Loop Error Amplifier Output. Connect the external compensation network of the voltage feedback loop between V_{COMP} and AGND.
28	IN	Supply Input for Main IC Power and Internal BIAS Linear Regulator. Bypass IN to GND locally with 1µF and 100nF ceramic capacitors (one of each).
29	BIAS	Regulated Output of the Internal 5.0V LDO. BIAS powers the internal circuitry. Bypass with a 4.7µF ceramic capacitor from BIAS to AGND.
30	I_{COMP}	Error Amplifier Output for the PPS Current Loop. Connect the external compensation network of the PPS current loop between I_{COMP} and AGND.
31	CSN2	Negative Terminal of the PPS Current-Sense Amplifier. CSN2 connects to the negative side of the R_{CS3} sense resistor. Referenced to OUT.
32	OUT	Output Sense Pin. Negative terminal of the high-side output current-sense amplifier (output CSA), input to the internal feedback resistor network and positive terminal of the PPS CSA. Connect OUT as close to R_{CS3} as possible using a Kelvin sense routing. OUT is also connected to the negative side of the sense resistor R_{CS2}.
33	CSP2	Positive Terminal of the High-Side Output Current-Sense Amplifier. Connect CSP2 as close to R_{CS2} as possible using a Kelvin sense routing. Referenced to OUT.
34	ADDR	I^2C Target Address Selection. Connect a resistor to ground to select the last two address bits. See the *I2C Target Addressing (ADDR Pin)* section for selecting the ADDR resistor.
35	DL2	Boost Low-Side Gate Drive Output. Connect to the gate of the Q_{b2} external N-channel FET.
36	BST2	Bootstrap Capacitor Pin for High-Side Driver of the LX2 Node. Connect a 0.1µF capacitor from BST2 to LX2.
37	DH2	Boost High-Side Gate Drive Output. Connect to the gate of the Q_{t2} external N-channel FET.
38	LX2	Boost-Side Switching Output Node. LX2 is Hi-Z when the buck-boost is disabled.
39	LX1	Buck-Side Switching Output Node. LX1 is Hi-Z when the buck-boost is disabled.
40	DH1	Buck High-Side Gate Drive Output. Connect to the gate of the Q_{t1} external N-channel FET.
—	EP	Exposed Pad. EP must be connected to the ground plane of the PCB for power dissipation. Not electrically connected internally.

Functional Diagrams

Functional Block Diagram



Power-Up Sequence



NOTE 1: MAX25432B ONLY.
NOTE 2: EXTERNALLY POWERED. VDD_IO DOES NOT GATE MAX25432 POWER-UP.
NOTE 3: GDRV = 0V UNTIL A CONNECTION IS DETECTED. REFER TO GDRV TRUTH TABLE.
NOTE 4: V_{BUS} WILL STAY AT vSafe0V UNTIL THE TCPM SENDS THE ENABLE COMMAND.
NOTE 5: MAX25432A: EXTERNAL PD CONTROLLER TURNS ITS Rp PULLUPS ON.
NOTE 5: MAX25432B: INTERNAL Rp PULLUPS ON.
NOTE 6: $\overline{\text{ALERT}}$ PIN WILL STAY HIGH UNTIL STARTUP DISCHARGE SEQUENCE IS COMPLETE.
NOTE 7: GRAY AREAS ARE UNDEFINED VOLTAGES.

KEY

7: READ ONLY
6: WRITE 1 TO CLEAR, READ

Detailed Description

The MAX25432 is a single-chip USB PD charging and protection solution with PPS for multimedia hub, rear-seat entertainment module, and head-unit applications. Combined with either a microcontroller or a USB PD controller it is a two-chip solution for dedicated charging module applications. The MAX25432 provides all the functionality for USB PD car battery to V_{BUS} regulation, configuration channel communication, and USB 2.0 Hi-Speed protection. It can optionally provide BC1.2 host charge emulation. The device integrates all of the protection needed in an automotive USB PD application.

The MAX25432 offers the design engineer two options for firmware development. The MAX25432B can operate with a system-on-chip (SoC), USB hub IC, or microcontroller, whereas the MAX25432A is designed to operate with a USB PD controller. The MAX25432 evaluation (EV) kit offers a platform where the design engineer can begin early firmware development.

Recent advancements in the automotive infotainment market demand high-efficiency and low footprint power delivery solutions. The push for lower BOM cost has driven USB power applications to integrate more features and responsibilities into a single IC. The proliferation of USB PD-based battery-powered portable devices has resulted in an increase in the number of USB ports in an automobile to charge the passenger's devices. These multiport charging modules can unnecessarily increase per-port cost when a dedicated MCU with firmware is used for each port. The MAX25432B's architecture minimizes per-port cost by enabling a single microcontroller running a USB Type-C policy manager (TCPM) firmware to control multiple MAX25432B devices which integrate a USB Type-C port controller (TCPC). The TCPM and TCPC communicate with each other using I^2C.

The MAX25432B is an advanced automotive integrated USB PD solution that combines the TCPC along with other USB features such as Type-C, PD with PPS, BC1.2, Apple, and Samsung® charging port emulator. All MAX25432 devices implement Analog Devices' proprietary current-mode buck-boost H-bridge controller that can achieve a target USB output voltage with high-efficiency while operating over a wide range of input voltage. The MAX25432 buck-boost controller has robust protection mechanisms such as overvoltage (OV), undervoltage (UV), overcurrent, short-to-ground (STG), short-to-battery, overtemperature, and automotive ESD protections. The MAX25432 implements internal gate drivers to drive external power FETs to accommodate high-power USB requirements. The MAX25432 has an intelligent voltage-adjustment circuit that can adjust the output voltage of the buck-boost converter such that the voltage on the USB receptacle is within specifications regardless of the output current.

All MAX25432 devices have integrated data and CC switches that protect the upstream USB transceiver and/or PD controller from high-voltage events on the cable or the receptacle. All devices also have an integrated V_{CONN} switch to supply power on one of the unused CC pins in different configurations. The high-voltage DP/DM pins (HVDP/HVDM) and CC pins (HVCC1/HVCC2) are monitored and protected for OV conditions such as ESD or short-to-battery/V_{BUS} events. Based on the configuration requested by the TCPM, the MAX25432B has the capability to source different currents on the HVCC pins for a Type-C interface. The MAX25432B also supports biphase mark coding (BMC) communication using integrated USB PD AFE circuits with remote ground offset sensing for long captive cables.

Features

- Integrated buck-boost DC-DC controller with drivers for four external MOSFETs in an H-bridge configuration
  - 4.5V to 36V (40V load-dump) input voltage allows operation in “warm-crank” and start/stop conditions
  - USB PD with PPS
    - 10mV V_{BUS} voltage step size from 3.3V to 21V
    - 25mA V_{BUS} current-limit step size from 1.0A to 6.35A
  - Four switching frequency options for scalable efficiency, adjustable EMI interference avoidance and power optimization including 220kHz, 300kHz, 400kHz, and 2.2MHz
  - Forced-PWM at light or no-load conditions for reduced EMI through USB cable
  - Spread-spectrum option for EMI reduction
  - SYNC input and SYNC output for frequency parking and multiport applications
  - Reduced inrush current with soft-start
  - Thermal shutdown
- Integrated USB PD V_{BUS} features
  - USB PD PPS compliant

  - Programmable V_{BUS} overcurrent protection limits
    - Apple MFi R3x compatible
  - Programmable V_{BUS} undervoltage protection limits
  - Programmable V_{BUS} overvoltage protection limits
  - Digital voltage scaling (DVS) for smooth, predictable voltage transitions
  - Integrated USB V_{BUS} discharge
- Integrated output voltage adjustment for cable voltage drop on captive-cable applications
  - Programmable voltage gain up to 3m/up to 516mΩ cable resistance
- 1MHz I^2C target interface with $\overline{ALERT}$ pin
  - TCPCI-compliant register set
  - MAX25432-specific registers for alerts, advanced diagnostics, and management
  - Maskable alerts for application-specific behavior
  - Selectable I^2C address for multiport applications
  - Integrated watchdog timer for guaranteed safe operation
- MAX25432A devices provide integrated two-input to two-output USB Type-C CC1 and CC2 4Ω (typ) switches for external USB PD controller
- MAX25432B devices provide a single-port TCPC-compliant USB PD PHY for an external TCPM
  - Designed to comply with USB PD, Type-C, and TCPC specifications as a source and DFP
    - USB Type-C Specification, Revision 1.3
    - USB Power Delivery Specification, Revision 2.0, Revision 3.0 Version 1.2, and Revision 3.1
    - USB Type-C Port Controller Interface Specification, Revision 2.0 Version 1.1
  - Implements Type-C CC interface and USB PD PHY functions to a TCPM that handles PD policy management
    - Type-C cable plug orientation detection
    - Type-C detection supporting default, 1.5A or 3.0A current capabilities
    - MAX25432BATLP: Improved CC detection ensures devices with very high CC line capacitance attach correctly
- SAR ADC for V_{BUS} (10-bit) and I_{BUS} (7-bit) monitoring
  - Programmable V_{BUS} voltage alarm thresholds
- Integrated 1.5W, 400mΩ (typ) V_{CONN} switch with overcurrent protection removes need for dedicated V_{CONN} DC-DC and allows use of the common-voltage rail in the application
  - 3.0V to 5.5V input voltage support
  - Programmable I_{LIM} in 50mA steps
  - Diagnostic current prevents enabling into an STG condition
  - Fast V_{CONN} input undervoltage protection
  - Intelligent soft-start and auto-retry for noncompliant V_{CONN} loads
  - Integrated V_{CONN} discharge on HVCC1 and HVCC2 pins
  - I^2C control saves two GPIOs on the USB PD controller
- Integrated module input fuse protection
  - Programmable V_{IN} undervoltage protection threshold
  - Fast detection of a fuse blow condition
  - Quick alert reporting to I^2C controller for resolution and possible USB PD renegotiation
- Integrated protection for passenger cable shield-short-to-battery faults prevents cable, passenger device, and car module damage
  - Fast and intelligent detection of cable shield overcurrent
  - Fast turn-off of external protection switch
  - Safe dissipation of inrush energy
  - Fault reporting and auto retry for fault removal
- Integrated automotive protection on V_{BUS} output
  - Fixed 6.4A V_{BUS} circuit-breaker limit (V_{BUS} OCP)
  - Automatic short-to-GND fault detection and diagnostic
- Optionally supports USB BC1.2 CDP, DCP, and high-speed pass-through modes (SDP)
  - USB D+/D- protection and host charger emulator

- Integrated HVDP/HVDM Apple and Samsung termination resistors
- Compatible with USB OTG specification and Apple CarPlay
- Supports Chinese Telecommunication Industry Standard YD/T 1591-2009
- Integrated 1GHz, 3dB BW data switches supporting USB 2.0 480Mbps/12Mbps/1.5Mbps communication
- Provides clean routing of Type-C Dp1, Dn1, Dp2, Dn2 connections to USB 2.0 downstream connector
- Auto-DCP mode compatible with Oppo® and OnePlus® devices

- Integrated robust high-voltage protection for the USB PD or TCPM controller from events at the receptacle or captive cable
  - 24V (max) overvoltage protection on HVCC1/HVCC2
  - 24V (max) USB 2.0 overvoltage protection on HVDP/HVDM
  - Automatic fault detection and retry
  - Fault indication through active-low, open-drain $\overline{ALERT}$ output (maskable)
  - Short-to-battery and short-to-V_{BUS} protection
- Automotive-grade ESD protection on USB HVDP, HVDM, HVCC1, HVCC2, and SHLD_SNS pins
  - ±15kV Air-Gap/±8kV Contact Discharge IEC 61000-4-2
  - ±15kV Air-Gap/±8kV Contact Discharge ISO 10605

MAX25432A and MAX25432B Differences

Table 1. Differences between MAX25432A and MAX25432B Devices

FUNCTION	MAX25432A	MAX25432B
Startup	No difference	
Buck-Boost and V_{BUS} Power	No difference	
CC Protection Switches	No difference	
USB Data Switches and Host Charge Emulation	No difference	
Cable Shield Short-to-Battery Protection (G-Suffix only)	No difference	
Normally Open Ground	No difference	
V_{CONN}	No difference	
I^2C	No difference	
Watchdog	No difference	
Fault Reporting, Action, and Recovery	No difference	
V_{BUS}, I_{BUS} ADC	No difference	
V_{BUS} Alarms	No difference	
Type-C Interface (Rp, V_{Rd}/V_{Ra})	No	Yes
USB Power Delivery PHY (BMC Driver)	No	Yes
V_{DD_BMC} Internal Supply	Off	On (1.125V)

PRELIMINARY

Document Conventions

Whenever "MAX25432" is mentioned in this document, the corresponding description, figure, or diagram applies to all MAX25432 devices.

Whenever "MAX25432A" is mentioned in this document, the corresponding description, figure, or diagram only applies to MAX25432A devices.

Whenever “MAX25432B” is mentioned in this document, the corresponding description, figure, or diagram only applies to MAX25432B devices.

Whenever “G-suffix” is mentioned in this document, the corresponding description, figure, or diagram only applies to MAX25432 devices with the G-suffix. Example: MAX25432BATLG/V+ or MAX25432AATLG/V+ are G-suffix devices.

Whenever “M-suffix” is mentioned in this document, the corresponding description, figure, or diagram only applies to MAX25432 devices with the M-suffix. Example: MAX25432BATLM/V+ is a M-suffix device.

References

Table 2 shows the reference specifications, their locations, and the common names they are referred to in this document.

Table 2. References

REFERENCE SPECIFICATION	TITLE	LOCATION
The USB PD Specification	Universal Serial Bus Power Delivery Specification Revision 3.0, Version 1.2 June 21, 2018	http://www.usb.org
The USB Type-C™ Specification	Universal Serial Bus Type-C Cable and Connector Specification Release 1.3 July 14, 2017	http://www.usb.org
The TCPCI Specification	Universal Serial Bus Type-C Port Controller Interface Specification Revision 2.0, Version 1.1 March 2020	http://www.usb.org
The USB 2.0 Specification	Universal Serial Bus Specification Revision 2.0 April 27, 2000	http://www.usb.org
The USB 3.x Specification	Universal Serial Bus 3.2 Specification Revision 1.0 September 22, 2017	http://www.usb.org
The USB BC1.2 Specification	Battery Charging Specification Revision 1.2 December 7, 2010	http://www.usb.org

Power-Up and Enabling

When a valid voltage is applied to IN and HVEN is high, the MAX25432 goes through its power-up sequence as described in the *Power-Up Sequence* functional diagram.

The MAX25432 power-up sequence is done when $\overline{ALERT}$ asserts low after HVEN goes high with V_{IN} > UVLO. The V_{DD_IO} input must be within a valid voltage to perform I^2C communication with the MAX25432 and provide a pullup voltage to the $\overline{ALERT}$ pin.

IN Supply Input

IN is the input supply for the MAX25432 and the external H-bridge buck-boost converter. The MAX25432 can operate with a V_{IN} voltage in the range of 4.5V to 36V and is load-dump tolerant up to 40V. A 1µF ceramic capacitor with appropriate voltage rating should be connected for decoupling from IN to GND. An additional 100nF closer to the IN pin is recommended for improved high-frequency decoupling for internal circuitry.

To prevent large input current from tripping an upstream automotive fuse during high output power at low input voltage, the MAX25432 integrates a programmable input undervoltage lockout. When the input voltage is below the undervoltage lockout threshold, the buck-boost controller is turned off, which prevents high current being drawn at the input. The undervoltage lockout is set by the IN_UV_THRESH[3:0] register. This voltage can be programmed in the range of 4.5V to 8.5V in steps of 0.4V. The default setting for the undervoltage lockout threshold is 4.5V and can be changed on the fly after power-up through I^2C. The UVLO threshold includes a blanking time of 150µs (typ), which prevents the device from turning off during input voltage transients.

High-Voltage Enable Input (HVEN)

HVEN is used as the main enable to the device and initiates the MAX25432 start-up and configuration. If HVEN is at a logic-low level, the device enters the Off mode with low quiescent current level on IN. HVEN is compatible with inputs from 3.3V logic up to automotive battery voltages.

BIAS Linear Regulator Output

The device includes an internal 5V linear regulator (BIAS) that provides power to the internal circuit blocks. The IC powers up once the voltage on BIAS crosses the undervoltage-lockout (UVLO) rising threshold and HVEN = H. The IC shuts down when BIAS falls below the UVLO falling threshold or HVEN = L. Connect a 4.7µF ceramic capacitor from BIAS to GND for proper operation of the linear regulator. See the *PCB Layout Guidelines* for more information.

External loads, such as an MCU or PD controller, can be connected to BIAS as a power supply as long as:

- The total BIAS current, including internal circuitry, is below 80mA. Make sure to account for the internal buck-boost drivers current consumption when the H-bridge is switching. The usable current for external loads varies depending on operating conditions.
- The power dissipated by the internal BIAS LDO does not cause the MAX25432 to exceed the maximum continuous power dissipation or junction temperature as specified in the *Absolute Maximum Ratings* section.

With the proper current budgeting, BIAS can also be used to provide V_{CONN} power. To do so, tie BIAS to the V_{CONN} pin and program the V_{CONN} OCP low threshold to the 50mA setting. Cables and accessories needing 100mW V_{CONN} can be powered with this method. A 1µF ceramic capacitor close to the V_{CONN} pin with a low impedance to ground is required to minimize voltage dips on BIAS.

External BIAS Supply

In certain applications, the 5V BIAS internal regulator can be turned off and an external voltage can be applied to the BIAS pin to provide power to the internal circuit blocks. To power the BIAS pin with an external voltage source, set the EXT_BIAS_SEL bit on register BIAS_CONTROL to 1. The default setting for this bit is 0 in which case the internal LDO is on. Connect an external voltage on BIAS after startup and before setting the EXT_BIAS_SEL bit to 1. The external voltage should be in the range of 4.7V to 5.4V for proper operation of the MAX25432.

Power-On Sequencing with External BIAS

When using an external 5V rail to power BIAS, the EXT_BIAS_SEL bit must be set after turning on the 5V rail. External back-to-back FETs can be used to switch the 5V rail on/off so as to prevent any supply conflict.

V_{DD_USB} Linear Regulator Output

The MAX25432 integrates a 3.3V low-dropout linear regulator. The V_{DD_USB} output is used as a clamping voltage during high-voltage events such as short-to-battery or ESD strikes on HVDP/HVDM pins. The V_{DD_USB} output is also used to power the internal 10-bit ADC on MAX25432 devices. This regulator uses the 5V BIAS regulator as its input. Connect a 1µF ceramic capacitor from V_{DD_USB} to GND for proper operation of the linear regulator. See the *PCB Layout Guidelines* for more information.

The MAX25432 includes an output undervoltage comparator that sets the VDD_USB_UV status bit when the regulator output goes below $V_{DD_USB_UV}$ = 2.7V (typ). An output overvoltage comparator is also included, which sets the VDD_USB_OV status bit when the regulator output goes above $V_{DD_USB_OV}$ = 4.0V (typ).

The V_{DD_USB} 3.3V LDO cannot be used to power external loads.

V_{DD_BMC} Linear Regulator Output (MAX25432B only)

The MAX25432B integrates a 1.125V (typ) regulated voltage reference required for BMC communication. Connect a 1µF ceramic capacitor from V_{DD_BMC} to GND for proper operation of the linear regulator. See the *PCB Layout Guidelines* for more information. Connect the pin directly to GND on MAX25432A devices.

V_{DD_IO} Input

The V_{DD_IO} pin must be connected to the external 1.8V, 3.3V, or 5.0V V_{DD} rail used for I^2C communication by the I^2C controller (MCU, HUB, or PD controller). V_{DD_IO} is used as the pullup voltage for the SCL, SDA, and $\overline{ALERT}$ pins.

I^2C communication can begin as soon as the power-up sequence is done (i.e., $\overline{ALERT}$ asserts low after HVEN goes high with $V_{IN} > U_{VLO}$) and the V_{DD_IO} input is within a valid voltage.

In an application where neither 1.8V, 3.3V, nor 5.0V external supplies are available, the V_{DD_IO} pin can be tied to V_{DD_USB} or BIAS directly. It is recommended to place a 10nF ceramic capacitor from the V_{DD_IO} pin to GND to provide local decoupling. The V_{DD_IO} input voltage can withstand a maximum voltage of 6V.

V_{CONN} Supply Input

The device requires an external supply on the V_{CONN} input to provide the required power for the V_{CONN} switch. The input voltage range for the V_{CONN} input is 3.0V to 5.5V but, in an application, the input voltage is typically 3.3V or 5.0V. See the *VCONN* section for more information.

Buck-Boost Controller

The MAX25432 integrates a buck-boost controller and drivers that provide power from the car battery to V_{BUS}. The buck-boost controller operates for input voltage ranges from 4.5V to 36V and is 40V load-dump tolerant. The buck-boost controller can regulate output voltages from 3.3V up to 21.0V and can limit output current from 1.0A up to 6.35A.

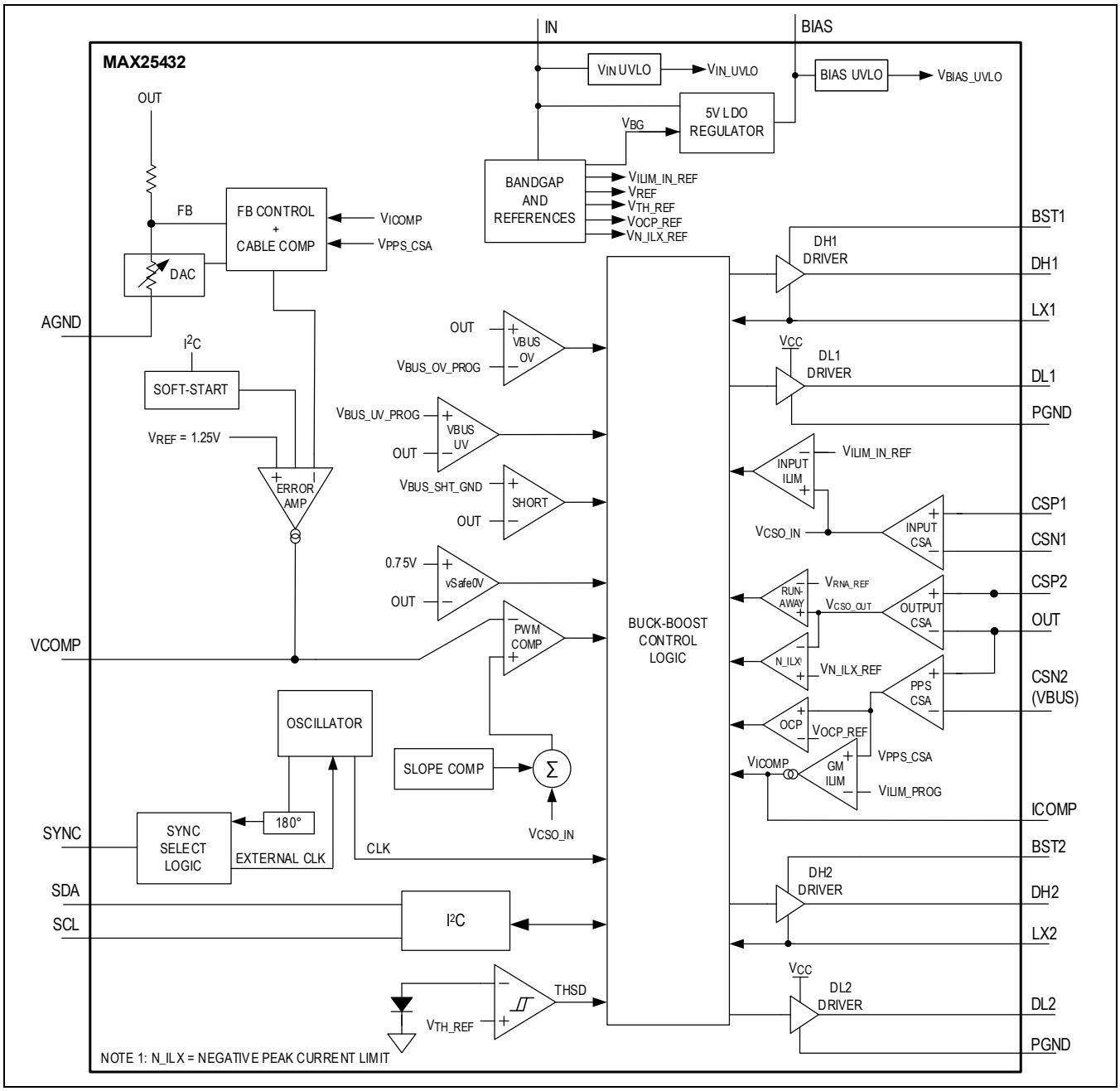


Figure 1. Buck-Boost Block Diagram

The integrated buck-boost controller operates in either a buck or boost, depending on the input and output voltages. The buck-boost transitions seamlessly between these modes to maintain a constant output voltage. This seamless four-switch buck-boost transition method ensures that V_{BUS} does not droop during V_{IN} transients and helps achieve excellent efficiency, load regulation, and line regulation. The architecture consists of a peak current-mode control loop that senses the inductor current using an external current-sense resistor on the input side (R_{CS1}). The slope compensation value can be adjusted in steps of 100mV by the SLP[2:0] register from 100mV to 800mV so as to prevent subharmonic oscillations. The switching frequency is also set by writing to the FSW[1:0] register. Four switching frequency options (220kHz, 300kHz, 400kHz, and 2.2MHz) are available in the device. To alleviate EMI problems the IC integrates a programmable spread spectrum on the switching frequency oscillator. The SS_SEL[1:0] register is used to set the desired amount of spread spectrum, which can be programmed to be ±3%, ±6%, and ±9% of the set switching frequency. The output voltage

is fed back to the controller using an internal resistor divider on the OUT pin. The buck-boost control-loop is compensated externally using an RC network on the V_{COMP} pin. An output current-sense resistor (R_{CS2}) between CSP2 and OUT provides protection from runaway currents (V_{OC2}), and excessive negative currents (V_{OC3}). A third current- sense resistor (R_{CS3}) is required between OUT and CSN2 for V_{BUS} I_{LIM} DC regulation used in PPS Current-Limit (CL) mode. R_{CS3} is also used for USB cable/voltage drop compensation in order to maintain a constant V_{BUS} voltage at the user port across output current variations. The MAX25432BATLP when paired with ADI TCPM enables dynamic loop control for improved dips/drops during input current restrictions.

Enabling/Disabling V_{BUS}

Before enabling V_{BUS}, ensure that the I^2C controller performs the following initial configuration after power-up:

1. The V_{BUS} current limit has been set accordingly. See the *VBUS Current-Limit (CL) Regulation* section.
2. The cable-compensation gain has been selected to offset any PCB trace/connector and/or cable drop. See the *Cable Compensation* section.
3. The slope-compensation peak ramp voltage is correctly set per the system requirements. See the *Slope Compensation* section.
4. The switching frequency and desired spread-spectrum settings are correctly set per the system requirements. See the *Switching Frequency and Spread Spectrum* section.
5. The SYNC pin direction is selected. By default, the SYNC pin acts as an input. See the *Synchronization Input/Output (SYNC)* section.
6. The V_{BUS} undervoltage and overvoltage thresholds and masks are correctly configured for the application. By default, the 12.5% UV/OV thresholds are selected. See the VBUS_THRESH register description.
7. No fault has been reported by the MAX25432 through the SHIELDING bit or dedicated V_{BUS} Fault flags. See the *Fault Table (Analog Devices Auto-Shield)*.
8. V_{BUS} needs to be at vSafe0V before being enabled. Make sure the VSAFE0V bit in the EXTENDED STATUS[7:0] register reads logic '1'.
9. If a V_{BUS} prebias condition exists, the I^2C controller needs to attempt a force discharge first using MAX25432 integrated force discharge functionality. The MAX25432 issues an I^2C error if V_{BUS} is not at vSafe0V prior to being enabled. See the *VBUS Discharge* and *Fault Table (Analog Devices Auto-Shield)* sections.

To comply with the USB-IF TCPCI specification, the MAX25432 only sources V_{BUS} when the proper command is received from the I^2C controller. In order to enable V_{BUS}:

1. Write 0x77 (Source V_{BUS} Default Voltage) to the COMMAND[7:0] register. The MAX25432 then soft-starts to vSafe5V (5.15V, typ).

To set V_{BUS} to non-default voltages (voltages other than vSafe5V), perform the following steps. Note that once V_{BUS} is being sourced, only then can the I^2C controller request for non-5V outputs.

2. Select the desired non-default output voltage by writing to the NONDEFAULT_TARGET registers.
3. Write 0x88 (Source V_{BUS} Non Default) to the COMMAND[7:0] register. The MAX25432 then transitions to the non-default voltage with a USB PD-compliant slew rate.

To change to a different non-default output voltage target, repeat steps 2 and 3. To go back to vSafe5V, perform step 1. Note that the output current limit can be changed while sourcing V_{BUS}.

To disable V_{BUS}, write 0x66 (Disable Source V_{BUS}) to the COMMAND[7:0] register. The MAX25432 will then turn off the buck-boost. To discharge V_{BUS} to vSafe0V, see the *VBUS Discharge* section.

For more information on specific actions to be performed with the MAX25432 to comply with USB Type-C and USB power delivery, contact Analog Devices.

Soft-Start

The buck-boost output is enabled by the I^2C controller by writing to the COMMAND register. When enabled, the controller soft-starts by gradually ramping up the output voltage from vSafe0V to vSafe5V (5.15V, typ). This soft-start feature reduces inrush current during startup. Soft-start is guaranteed into compliant USB loads. Only after the voltage reaches vSafe5V can the buck-boost output voltage be adjusted to other voltage options by the I^2C controller. The typical soft-start time is 6.5ms.

Switching Frequency and Spread Spectrum

The MAX25432 provides a programmable switching frequency and spread spectrum through I^2C. The internal oscillator frequency is set by the FSW[1:0] register. The switching frequency can be programmed to 220kHz, 300kHz, 400kHz, or 2.2MHz.

Spread spectrum can be enabled and adjusted by writing to the SS_SEL[1:0] register. Spread spectrum can be programmed to ±3%, ±6%, and ±9% centered on f_{SW}. The default oscillator frequency at power-up is 400kHz with no spread spectrum.

Table 3 shows the typical variation of the switching frequency for each spread-spectrum setting.

Table 3. Spread-Spectrum Settings vs. Switching Frequency

f_{SW} (kHz)	SPREAD-SPECTRUM MODULATION FREQUENCY (kHz)		
	±3% SETTING	±6% SETTING	±9% SETTING
220	±6.6	±13.2	±19.8
300	±9	±18	±27
400	±12	±24	±36
2200	±66	±132	±198

Synchronization Input/Output (SYNC)

The MAX25432 integrates a clock synchronization input/output to be used in two-port applications or with other power supplies in the module. The benefits of the synchronization between two switching power supplies are as follows:

- Reduced input capacitance requirement due to 180° out-of-phase current demands, which leaves time for the input capacitors to recharge between each cycle.
- Reduced EMI due to less input current ripple. This translates to a smaller inductor required for the module input EMI filter.

Both the reduced input capacitance requirement and reduced input current ripple help reduce system cost significantly.

The SYNC pin direction can be configured through I^2C as either an input or an output through the SYNC_DIR register. SYNC_DIR is a one-bit register which is set by default to logic '1'. In this case, the SYNC pin on the MAX25432 is expecting an external input signal to synchronize its oscillator to the input on the SYNC pin. If there is no input on this pin, the buck-boost operates with the internal oscillator. Connect SYNC to GND and configure it as an input if not used.

The SYNC_DIR bit can be set to logic '0' by the I^2C controller. In this case, the SYNC pin acts as an output and, when sourcing V_{BUS}, generates a fixed 50% duty cycle square waveform at the controller's switching frequency that is phase shifted by 180°, as shown in *Figure 2*. Note that only buck operation is shown. The SYNC feature also supports boost and buck/boost operation.

The internal spread spectrum is disabled if SYNC is configured as an input and synchronized to an external clock.

When configured as an output, the SYNC signal includes the spread-spectrum modulation for the sync-in device to synchronize to.

When configured as an input, the external clock signal must be within f_{SYNC_RANGE} of the programmed switching frequency f_{SW} and have a duty cycle between 30% to 70% for the MAX25432 to synchronize properly. If not, the sync-in device reverts to its internal clock synchronization autonomously without changing the SYNC_DIR bit.

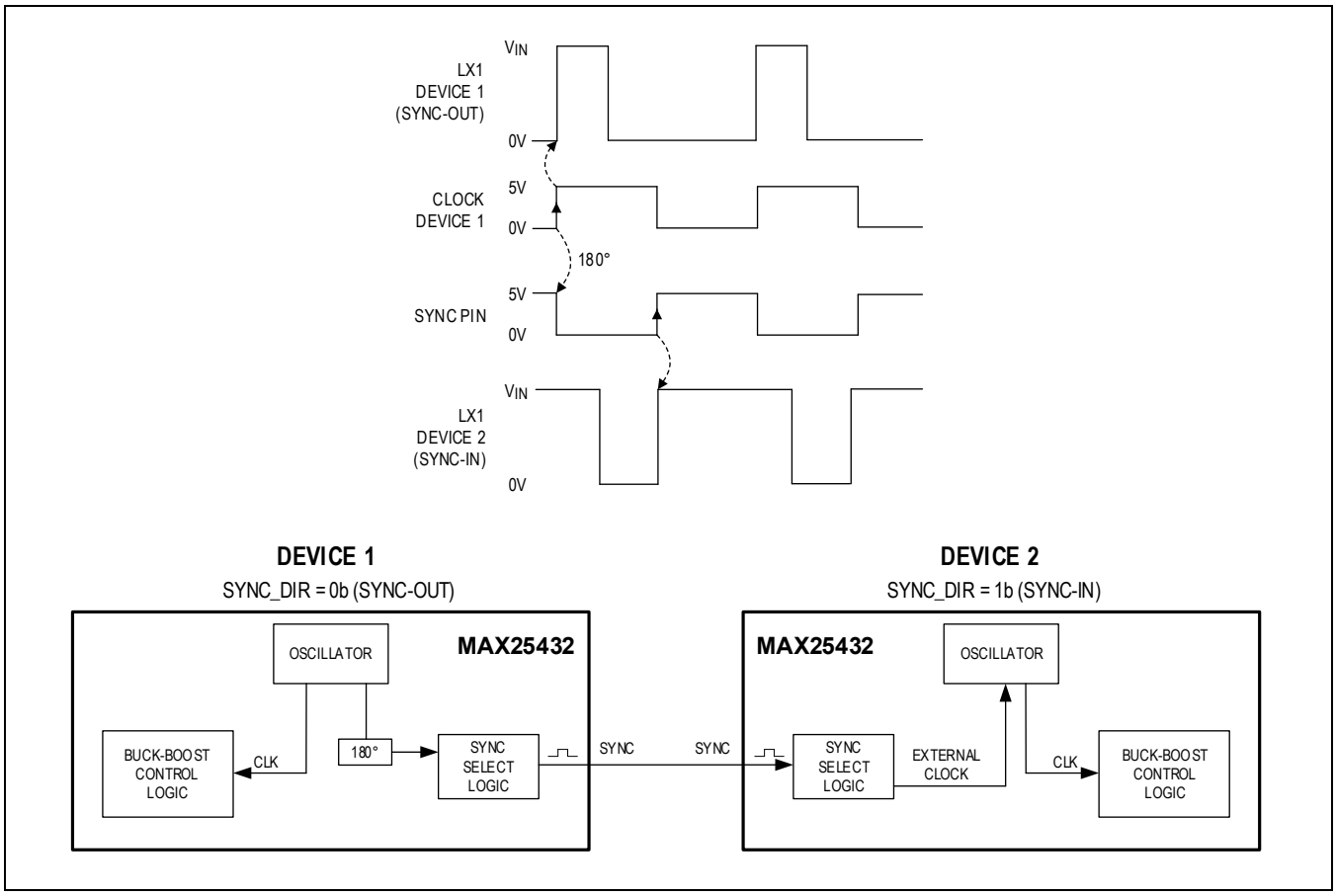


Figure 2. SYNC Operation Diagram

Input Current Limit

The MAX25432 features a peak input current limit. The device limits the input current by reducing the output voltage if the sensed voltage drop across the input current-sense resistor (V_{CSP1} - V_{CSN1}) is above the fixed V_{OC1} threshold (50mV, typ). The current threshold can be selected with the input current-sense resistor value R_{CS1}. See the *Current-Sense Resistors Selection* section.

An input overcurrent event sets the latched, read-only IN_OC status bit to logic '1' after a debounce of 16ms.

The MAX25432 reports the event to the VNDR_ALRT bit in the ALERT_H register if the IN_OC_MASK is unmasked. Additionally, if MSK_VNDR_ALRT bit is unmasked, the $\overline{ALERT}$ pin is asserted low.

V_{BUS} Current-Limit (CL) Regulation

The MAX25432 features a programmable DC current-regulation loop on V_{BUS} to support PPS CL operation.The buck-boost is allowed to enter the CL mode only when the CL_EN bit is set to 1, as seen in *Figure 3*.

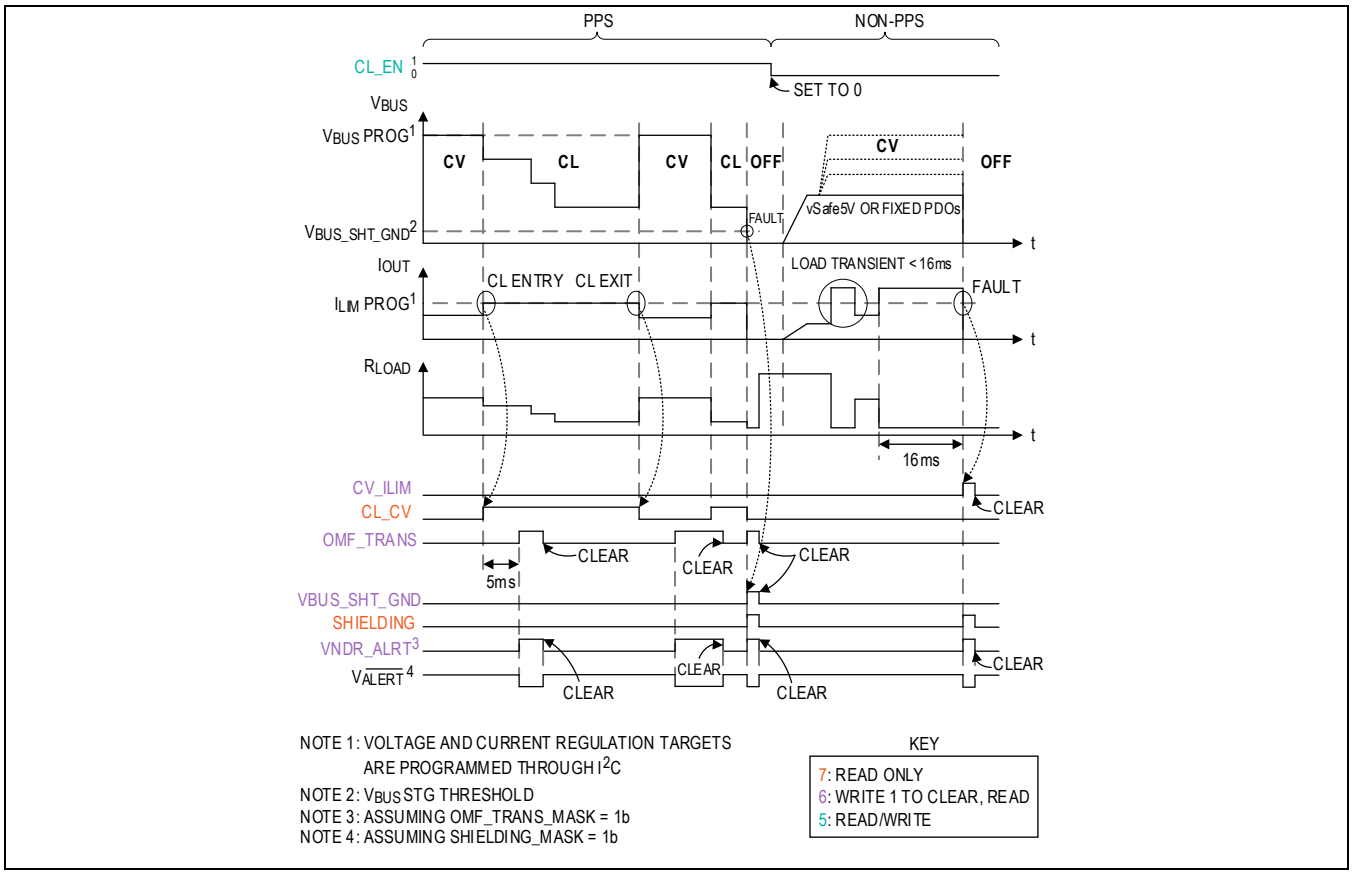


Figure 3. CL_EN Diagram

When CL_EN = 1 and the V_{BUS} DC output current monitored on R_{CS3} is less than the programmed current-limit threshold set in the VBUS_ILIM_SET[7:0] register, the buck-boost stays in Constant-Voltage (CV) mode and V_{BUS} is regulated to the programmed voltage target (default or non-default V_{BUS}).

When the V_{BUS} DC output current is above the current-limit threshold, the ICOMP voltage increases and drives the internal feedback node higher to reduce V_{BUS} and maintain constant current. As the PD device increases its load, V_{BUS} reduces further and the MAX25432 maintains accurate regulation until the PD device reduces its load or the sensed OUT voltage reaches the V_{BUS} STG threshold (2.85V, typ), which will turn off the buck-boost. See the *Fault Table (Analog Devices Auto-Shield)* for more information on the V_{BUS} STG fault.

The buck-boost regulation mode is indicated by the OMF_TRANS and the CL_CV bits in the VENDOR_STATUS and AUTO_SHIELD_STATUS_1 registers, respectively. See the register descriptions in the for more details.

When CL_EN = 0, the MAX25432 is prevented from entering CL mode. The MAX25432 does not regulate the output current in this mode and maintains CV regulation for the debounce duration. If the current exceeds the programmed threshold in the VBUS_ILIM_SET[7:0] register for more than 16ms (typ), the MAX25432 turns off the buck-boost controller to protect itself and the sink. This setting is recommended when sourcing vSafe5V or fixed PDOs, and also to meet the MFi Overcurrent specification (introduced in the R30 revision in 2018).

Additionally, a fixed overcurrent protection (V_{BUS} OCP), independent of CL_EN setting, is always active when sourcing V_{BUS}. The fault is triggered when V_{BUS} current exceeds 6.4A DC (typ) which immediately causes the buck-boost controller to turn off.

See the *Fault Table (Analog Devices Auto-Shield)* for more information on action, reporting, and recovery upon a V_{BUS} current-limit or OCP condition.

V_{BUS} Short-to-GND (STG) Comparator

The buck-boost output is protected against an STG condition. An STG event is detected when OUT goes below 2.85V (typ) for CL_EN = 1 or below 2.0V (typ) for CL_EN = 0 while V_{BUS} is being sourced. In this case, the buck-boost controller is turned off immediately. See Fault Action A in the *Fault Table (Analog Devices Auto-Shield)*.

Integrated V_{OUT} Pulldown

While the buck-boost is disabled, an active pulldown of 16kΩ (typ) is switched on to keep V_{BUS} at vSafe0V.

Cable Compensation

USB charging current of devices could be as high as 5A while connectors and cables contribute to voltage drops. Stringent USB port supply voltage specifications increase the need for compensation, and excessive voltage drop causes device disconnects. The voltage drop compensation is implemented by measuring the current and feeding back the current information to the internal feedback block of the converter. In this implementation, the load regulation of the power supply is effectively changed to compensate a voltage drop on a power line.

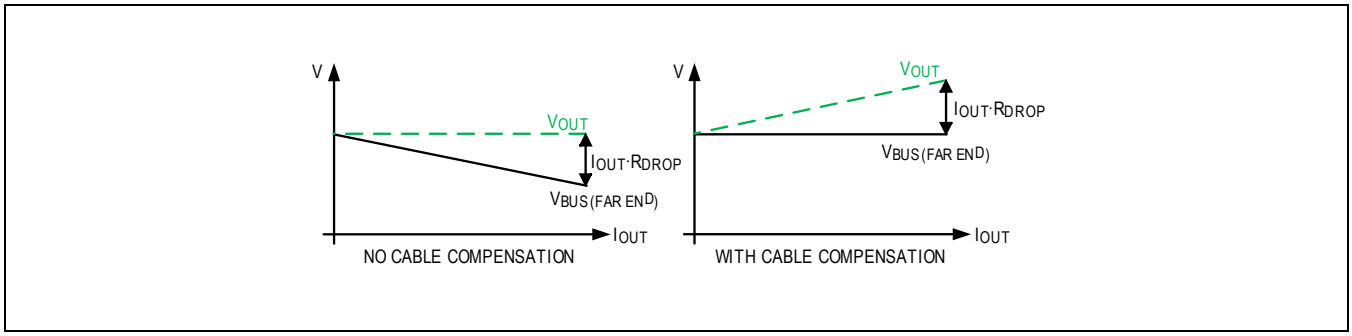


Figure 4. Cable Compensation Benefit

The MAX25432 compensates voltage drops for up to 516mΩ from parasitic resistance present from the OUT pin to the user cable, including but not limited to the USB captive cable, PCB trace, and inline connectors. The cable compensation is designed for use in the constant voltage region at up to 5A. Cable compensation stays active upon entry into current-limit region. The gain of the cable-compensation circuit can be adjusted through I^2C by changing the values in GAIN[5:0] in the cable-compensation control register CABLE_COMP_CONTROL. The R_{CS3} external current-sense resistor is required when using the cable-compensation feature. See the *USB Cable Compensation* section for guidelines.

Thermal Shutdown

Thermal shutdown protection limits the temperature the device is allowed to reach before forced shutdown. If the die temperature exceeds +165°C, the device shuts down and needs to cool down. Once the device has cooled down by 15°C, the device is automatically enabled again (as long as HVEN is still high and V_{IN} is above UVLO). The thermal overload protects the device in the event of overheating. For continuous operation, do not exceed the absolute maximum junction temperature of +150°C. For more information regarding actions and recovery steps taken upon a thermal shutdown fault, see the *Fault Table (Analog Devices Auto-Shield)* and the *Fault Types* table.

USB Type-C and Power Delivery

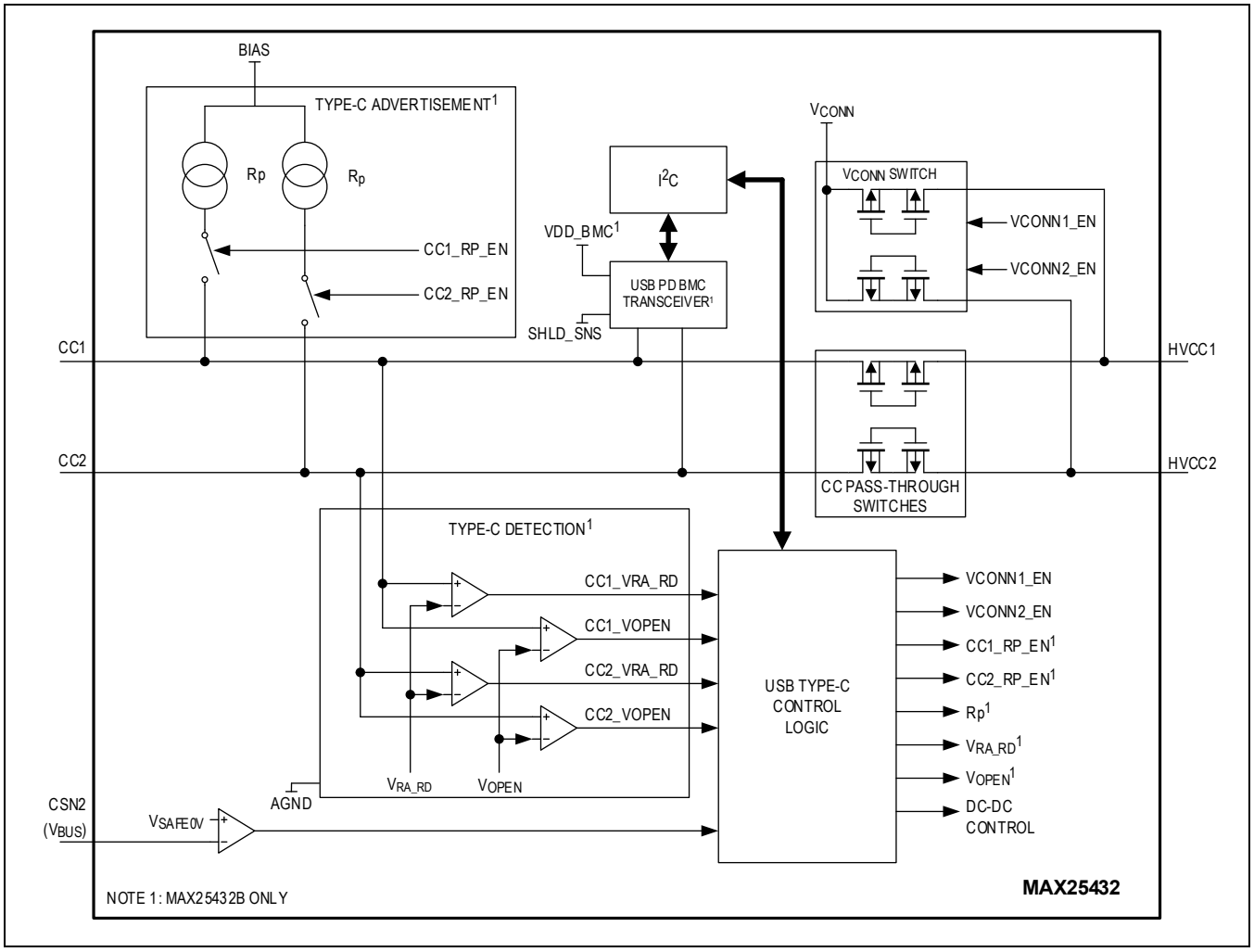


Figure 5. USB Type-C Functional Block Diagram

A detailed breakdown of the block diagram and operation is provided in the following sections.

Configuration Channel (CC1 and CC2)

To maintain the USB host/device relationship, Type-C requires a configuration channel (CC). It is through the CC pins that current capabilities are advertised and detected, as well as how the host detects the cable orientation, which is required for USB3 and active cables. In the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the source-to-sink connection.

Functionally, the CC is used to serve the following purposes.

- Detect attachment of USB ports (e.g., a source to a sink)
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports
- Discover and configure V_{BUS}: USB Type-C current modes or USB PD
- Configure V_{CONN}
- Discover and configure optional Alternate and Accessory modes

PRELIMINARY

The CC pins utilize combinations of pullups and pulldowns to detect Type-C device attachment, advertise the current capabilities of the source, and detect the type and orientation of the cable and the device. There are three possible pullups (Rp) which represent the three source current capabilities: default, 1.5A, and 3A. Additionally, there are two possible device pulldown resistors (Ra and Rd) to provide device and cable information to the host. This configuration allows for simultaneous advertisement and detection. The Type-C specification also allows for dynamic Rp changes without any resets.

CC Pass-Through Switches

The Type-C block includes the CC-to-HVCC pass-through switches that provide a protected communication path between the USB PD controller and handheld device.

V_{CONN}

While there are two HVCC pins that must be monitored on the host receptacle, there is only one CC wire running through the Type-C cable. This is how orientation can be determined. This leaves the second HVCC pin available for other uses. The Type-C specification allows the unused HVCC pin to operate as V_{CONN}, a low-power source intended to power active cables which may include authentication ICs or super-speed muxes.

The MAX25432 includes complete support for V_{CONN} power control and protection. When a power source within the acceptable operating voltage is connected to the V_{CONN} pin, the MAX25432 can connect the voltage source to the appropriate HVCC pin. Back-to-back V_{CONN} FETs provide overvoltage and overcurrent protection to the V_{CONN} source in addition to controlling the application of V_{CONN} per the Type-C specification.

The advantage of the MAX25432 is the ability to provide V_{CONN} power from a low-power system supply to a wide-range of E-marked cables (i.e., using the same supply used to power the USB PD controller or MCU), essentially reducing the current budget needed for supplying V_{CONN} and hence reducing the cost and solution size.

However, certain V_{CONN} loads draw currents that exceed the Type-C specification of 1W (max), shortly after V_{CONN} is sourced. This causes unwanted inrush currents and droops on the system supply, ultimately causing a module reset.

To overcome this limitation while being able to provide in the range of 100mW to 1W V_{CONN} power, the MAX25432 implements a dual-threshold overcurrent protection (OCP) with specific debounce timers and a fast UV comparator on the V_{CONN} pin. The first overcurrent threshold (OCP low) is programmable from 50mA to 500mA (typ) with a debounce of 400µs, which allows exceeding the 1W limit momentarily and during startup of the V_{CONN} load circuitry. The second OCP threshold (OCP high) threshold is fixed and set to 750mA (typ) and has a debounce of 5µs, which protects the system supply from noncompliant V_{CONN} loads and/or short circuits. STG diagnostic circuitry is also implemented in order to detect if a STG condition is present before closing the V_{CONN} switch and avoid collapsing the upstream supply.

Enabling V_{CONN}

- Program the V_{CONN} OCP low setting by writing to the VCONN_OCPL_SEL[3:0] register. To power 100mW, 5A E-marked cables, the 50mA setting is recommended. Adjust the OCPL threshold based on desired V_{CONN} power supported.
- Program the V_{CONN} UV setting by writing to the VCONN_IN_UV_THRESH bit. UV settings of 4.65V and 3.05V are recommended for 5V supply and 3.3V, respectively. The default value at power-up is 3.05V.
- Make sure the V_{CONN} supply is enabled and above the V_{CONN} UV-programmed threshold. Read the VCONN_IN_UV status bit to verify.
- Unmask Fault and Status bits as desired.
- Select the HVCC channel where V_{CONN} is needed by setting the cable polarity bit PLUG_ORNT in the TCPC_CONTROL register.
- Set the EN_VCONN bit to logic '1' to enable V_{CONN}.
- If V_{CONN} has successfully started up, the MAX25432 sets the POWER_STATUS.VCONN_PRESENT bit to indicate V_{CONN} is being sourced. On the MAX25432B, the corresponding HVCC comparator (found in HVCC_STATUS register) will go from "Ra" to "Open".
- Monitor the OCP and UV fault flags.
- To disable V_{CONN}, set EN_VCONN to logic '0'.

V_{CONN} Startup

Once the V_{CONN} input is within its operating range and after V_{CONN} is enabled on a HVCC channel, the diagnostic current is enabled on the corresponding channel and the STG comparator is active and monitoring HVCC. If HVCC is above the STG threshold (0.5V, typ), the V_{CONN} switch is soft-started and the diagnostic current turned off after 500µs. The MAX25432 indicates that V_{CONN} has soft-started successfully by setting POWER_STATUS.VCONN_PRESENT to logic '1'.

After V_{CONN} is enabled on a HVCC channel, the IC monitors for additional faults related to V_{CONN} operation.

V_{CONN} Short-to-Ground Detection (STG Detection)

Every time V_{CONN} starts or restarts, the MAX25432 checks for an STG condition. An actual hot STG condition usually trips the V_{CONN} UV fault or V_{CONN} OCP high first. If an STG condition is maintained, the V_{CONN} switch does not soft-start.

When a V_{CONN} STG condition is detected, a 30mA diagnostic current (typ) is enabled for 8ms (typ). If HVCC rises above the STG threshold during the 8ms, the V_{CONN} switch is soft-started normally. If the HVCC voltage does not go above the STG threshold by the end of the 8ms, the MAX25432 disables the diagnostic current source, then waits for 16ms before re-enabling it again and repeating the cycle until either the STG condition is removed or V_{CONN} is disabled through I^2C. The STG retry time is fixed at 16ms and cannot be changed.

V_{CONN} Reverse Overvoltage (Reverse OV)

On the first V_{CONN} reverse-OV fault, the V_{CONN} switch is immediately turned off, the diagnostic current is enabled on the corresponding channel and the STG comparator is active and monitoring HVCC.

The MAX25432 reports the fault by setting the VCONN_REV_OV status bit on the first fault and as long as the fault condition is present. Once the fault clears, the V_{CONN} switch attempts to restart autonomously after the time set in the RETRY_TMR register, as long as the VCONN _EN bit is still set to logic '1'.

V_{CONN} Autoretry

Due to the fact that the V_{CONN} supply is a shared supply, asynchronous system loads can happen while sourcing V_{CONN}. For this reason, a V_{CONN} autoretry feature is implemented to minimize the software interaction when sourcing V_{CONN} with a shared supply.

If a V_{CONN} load tries to draw an excessive amount of current for more than the debounce time, the V_{CONN} switch automatically opens to avoid drooping the upstream power supply, then will retry automatically. After three consecutive faults, the $\overline{ALERT}$ pin asserts indicating the I^2C controller to take action if needed.

The autoretry feature is only active for the V_{CONN} OCP and V_{CONN} UV faults.

V_{CONN} Overcurrent Protection (OCP Low/High)

On the first V_{CONN} OCP fault and after the debounce time, the V_{CONN} switch is immediately turned off, the diagnostic current is enabled on the corresponding channel and the STG comparator is active and monitoring HVCC.

If another OCP fault is detected, the fault process repeats again. After three consecutive faults, the VCONN_OCP_FAULT bit is latched and the retry timer starts (default 16ms). Once the timer expires, the SHIELDING bit is set and the process repeats again with the fault counter restarting. Note that only the I^2C controller can clear the VCONN_OCP_FAULT bit.

Upon the VCONN_OCP_FAULT bit being set, the I^2C controller can take action to clear the bit, then disable V_{CONN}. The I^2C controller can proceed without powering the non-compliant E-marked cable until a new cable is detected.

To disable the OCP fault detection, set the VCONN_OCP_DET_EN bit to 1 in the FAULT_CONTROL register.

V_{CONN} Undervoltage (UV)

On the first UV fault, the V_{CONN} switch is immediately turned off, the diagnostic current is enabled on the corresponding channel and the STG comparator is active and monitoring HVCC. If the fault is no longer present, the V_{CONN} switch soft-starts normally as described in V_{CONN} Startup in the *USB Type-C and Power Delivery* section. However, if another UV fault is detected, the fault autoretry is engaged and the fault process repeats again. After three consecutive faults, the VCONN_IN_UV status bit is set and the retry timer will start (default 16ms). Once the timer expires, the process repeats again with the autoretry fault counter restarting at 0.

PRELIMINARY

The MAX25432 reports the fault by setting the VCONN_IN_UV status bit on the third fault and as long as the fault condition is present.

To disable the V_{CONN} UV fault reporting, set the VCONN_OCP_DET_EN bit to 1 in the FAULT_CONTROL register. Note the V_{CONN} UV fault actions and recovery will still be active in this case; only the reporting will be disabled.

V_{CONN} Automatic Discharge

To comply with the Type-C specification, the corresponding HVCC pin is discharged for 1ms every time V_{CONN} is disabled. The internal discharge circuit consists of a 2.65kΩ resistance and a low-side FET.

Legacy Devices

The Type-C specification ensures interoperability with Type-A/Type-B devices by defining requirements for legacy adapters. As a DFP, relevant adapters connect from the Type-C receptacle to either a Type-B plug or to a Type-A receptacle, which can then be used with any legacy Type-A cable. A compliant legacy adapter of this type must include an Rd termination inside the adapter. In this case, the MAX25432 detects a Type-C attachment whenever the adapter is connected, regardless of whether a portable device is connected. The portable device sees the DFP as a BC1.2 port (when configured as such). See the *Host Charge Emulation* section for additional information.

Port Controller and Power Delivery

Type-C Port Controller Interface (TCPCI) (MAX25432B only)

The MAX25432B devices implement a TCPCI as defined in the USB Type-C Port Controller Interface Rev. 2.0 Ver. 1.1. TCPCI is the interface between a USB Type-C port manager (TCPM) and a USB Type-C port controller (TCPC).

The goal of the TCPCI is to provide a defined interface between a TCPC and a TCPM to standardize and simplify USB Type-C port manager implementations.

The TCPC is a functional block which encapsulates V_{BUS} and V_{CONN} power controls, USB Type-C CC logic, the USB PD BMC physical layer and protocol layer other than the message creation.

Contact Analog Devices for more information on how to program the TCPM to work with the MAX25432B.

BMC Transmitter (MAX25432B only)

The MAX25432B supports USB PD message transmission and reception (Tx/Rx) through the bi-phase mark coding (BMC) interface on the HVCC channels. The BMC communication is used by the source and sink to exchange USB PD messages. The BMC communication is single ended and occurs between two port partners (a source and a sink) after a Type-C attachment has been successfully made. The CC line that is going through the USB cable is used by the two port partners to communicate using BMC.

The BMC transmitter driver overdrives the DC bias voltage on the HVCC pin that is set for device attachment while transmitting. The BMC transmitter driver returns to a Hi-Z state when not transmitting.

Note: The MAX25432B meets the BMC eye diagram specifications as defined in the USB Power Delivery Specification. The MAX25432B's BMC driver is referenced to the SHLD_SNS pin and therefore BMC communication is not affected by the IR drop caused by the external shield short-to-battery FET, if used. A Type-C captive cable with dedicated ground sense allows compensation for ground offset during charging as pictured in *Figure 6*.

For more information on the BMC Protocol and Signaling, refer to the USB Power Delivery Specification Revision 3.0, Version 1.2.

PRELIMINARY

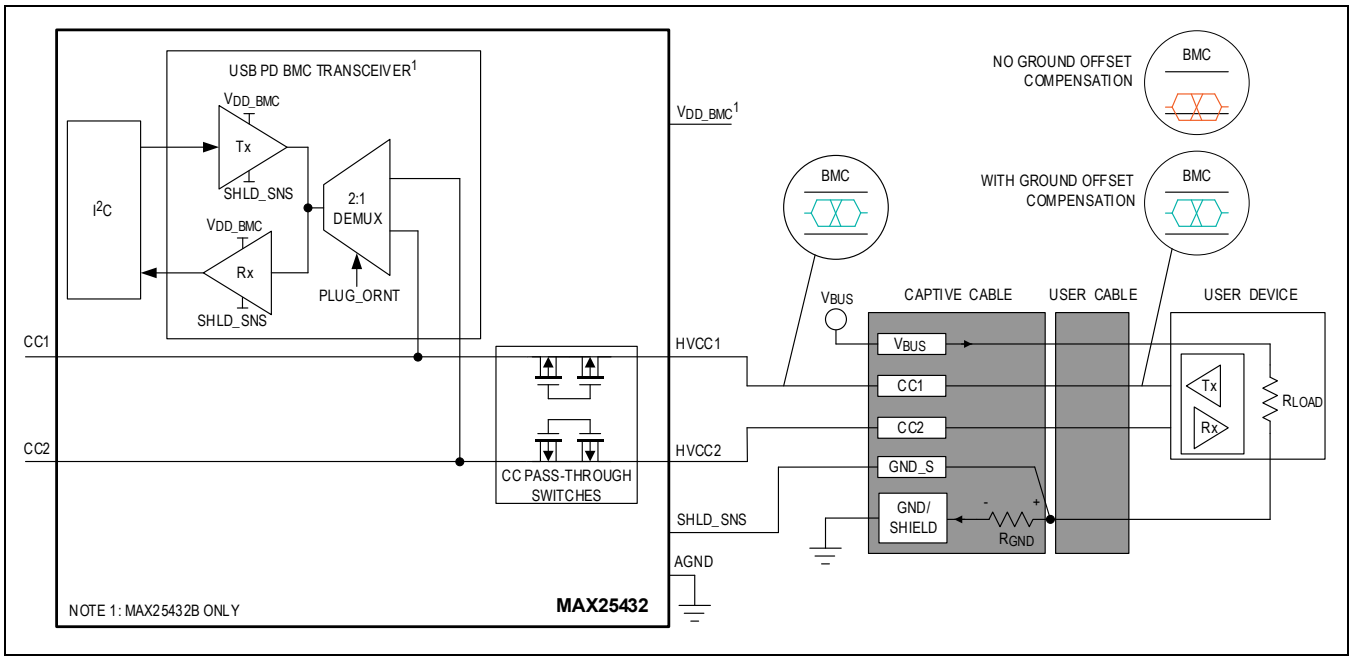


Figure 6. USB PD PHY Ground Offset Compensation

Sink Tx Ok (MAX25432B only)

When a PD contract is established, the sink shall ignore Rp current advertisement as USB PD takes precedence over Type-C.

After a PD contract, the TCPM can change the Rp advertisement of the TCPC to signal Sink Tx Ok. Rp advertisement is therefore used as a low-level signaling feature. This feature was added in USB PD Revision 3.0.

V_{BUS} Voltage and Current ADC

Figure 7 shows the block diagram of the V_{BUS} voltage and current ADC. The MAX25432 integrates signal conditioning, multiplexing, conversion, and result registers. The conversion results are used to trigger interrupts using the V_{BUS} voltage alarms registers or can be read by the TCPM for periodic monitoring.

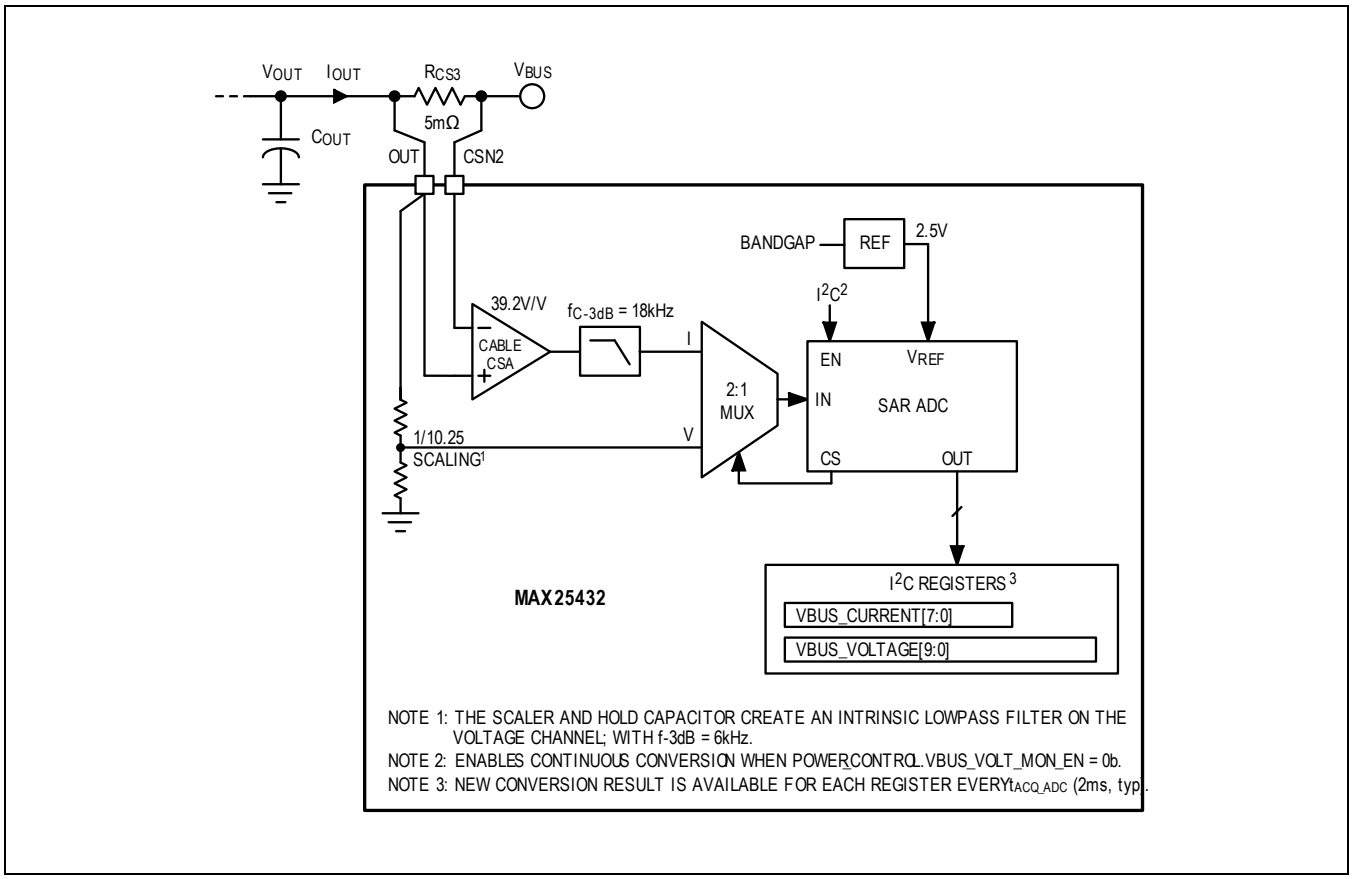


Figure 7. V_{BUS} ADC Block Diagram

All MAX25432 devices integrate a V_{BUS} voltage and current continuous-sampling SAR ADC with a resolution of 10 bits for voltage and 7 bits for current.

The ADC sampling is disabled at POR. To enable sampling, write logic '0' to bit D6 (VBUS_VOLT_MON_EN) of the POWER_CONTROL register 0x1C. To stop ADC sampling, write logic '1' to bit D6 of the POWER_CONTROL register 0x1C.

The POWER_CONTROL register is shown in *Figure 8*.

ADDR	REGISTER NAME	POR	D7	D6	D5	D4	D3	D2	D1	D0
0x1C	POWER_CONTROL	0x60		VBUS VOLTAGE MONITORING ENABLE	DISABLE VOLTAGE ALARMS	AUTO DISCHARGE ON DISCONNECT ENABLE		FORCE DISCHARGE ENABLE	VCONN POWER SUPPORTED	VCONN ENABLE

NOTE: REGISTER ACCESS READ/WRITE READ ONLY

Figure 8. POWER_CONTROL Register for ADC Control

The voltage conversion result after each sample is stored in registers VBUS_VOLTAGE_L and VBUS_VOLTAGE_H and can be accessed through an I2C Read transaction. The MAX25432 maintains synchronization of the 10-bit result between the VBUS_VOLTAGE_L and VBUS_VOLTAGE_H registers by latching the VBUS_VOLTAGE_H value at the time of the VBUS_VOLTAGE_L is read. Therefore, an I2C Read Word transaction starting at VBUS_VOLTAGE_L address is recommended. See the *I2C Interface* section for more information on the Read Word transaction.

The current conversion result after each sample is stored in the VBUS_CURRENT register and can be accessed through an I2C Read Byte transaction.

The VBUS_VOLTAGE_L, VBUS_VOLTAGE_H, and VBUS_CURRENT registers are shown in *Figure 9*.

ADDR	REGISTER NAME	POR	D7	D6	D5	D4	D3	D2	D1	D0
0x70	VBUS_VOLTAGE_L	0x00	VBUS_VOLTAGE[7:0]							
0x71	VBUS_VOLTAGE_H	0x00							VBUS_VOLTAGE[9:8]	
…	…	…	…							
0x80	VBUS_CURRENT	0x00	VBUS_CURRENT[7:0]							

NOTE: REGISTER ACCESS READ/WRITE READ ONLY

Figure 9. Voltage and Current Registers for ADC Result

A 10-bit value for the voltage conversion result is obtained by combining bits D[1:0] of the VBUS_VOLTAGE_H register with bits D[7:0] of the VBUS_VOLTAGE_L register.

V_ADC_Result = (UInt16)((VBUS_VOLTAGE_H & 0x03) x 256) + VBUS_VOLTAGE_L)

To convert the ADC_Result to the measured V_{BUS} voltage, multiply it by 25mV.

To convert the VBUS_CURRENT[7:0] result to the measured V_{BUS} current, multiply its decimal value by 50mA. Note that the VBUS_CURRENT[7] bit always equals 0b (7-bit effective on a 8-bit register).

Note that since voltage and current are measured one after the other, new conversion results in VBUS_VOLTAGE[9:0] and VBUS_CURRENT[7:0] registers are 1ms apart (typ).

The $\overline{ALERT}$ pin will not assert when a new conversion result is ready. The I2C controller must use polling to read the most recent conversion results.

See the register descriptions in the for more information on the ADC.

V_{BUS} Alarms (MAX25432B only)

The 10-bit ADC conversion results are compared with the alarms thresholds set by the TCPM. Those alarms can be used to alert the TCPM during USB PD V_{BUS} voltage transitions or in CL mode. To enable V_{BUS} alarms, write a logic '0' to VOLT_ALRMS_EN bit in the POWER_CONTROL register. The V_{BUS} ADC must be enabled for the alarms to operate.

The MAX25432B V_{BUS} alarms are compliant with the USB PD specification. Contact Analog Devices for more information on how to program the V_{BUS} alarms.

vSafe0V Comparator

To comply with the Type-C specification, the MAX25432 implements a vSafe0V comparator to indicate when V_{BUS} (sensed on the OUT pin) is below the vSafe0V threshold. Unlike the V_{BUS} discharge stop threshold, the vSafe0V threshold is fixed to 0.75V falling with a 50mV hysteresis (typ).

The I2C controller can check the status of the vSafe0V comparator by reading the VSAFE0V bit in the EXTENDED_STATUS[7:0] register located in the TCPCI-compliant register section.

A logic '1' of this bit signifies V_{BUS} is at or below vSafe0V threshold. A logic '0' signifies V_{BUS} is above the vSafe0V threshold. This status bit is read-only and non-latched.

Whenever the VSAFE0V bit changes and the MSK_VSAFE0V is set to '1' (unmasked), the EXTENDED_STATUS alert bit is set.

The vSafe0V status is valid only when the V_{BUS} Detection Enabled bit (VBUS_DET_EN) located in the POWER_STATUS[7:0] register becomes a '1'. The VBUS_DET_EN bit is read-only and indicates the MAX25432 is monitoring for V_{BUS} present and vSafe0V thresholds.

PRELIMINARY

V_{BUS} Present Comparator

In order to enable the V_{BUS} present comparator, the TCPM must send the EnableVbusDetect command (0x33) to the COMMAND register.

Whenever the VBUS_DET_EN read-only bit becomes logic '1', the V_{BUS} present comparator is active and monitoring the OUT pin. If the voltage sensed on OUT goes above 4V (typ), the MAX25432 sets the VBUS_PRESENT bit in the POWER_STATUS register to alert the TCPM that V_{BUS} is present on the Type-C connector.

To disable the comparator, the TCPM must send the DisableVbusDetect command (0x22). Note that the EnableVbusDetect and DisableVbusDetect commands also enable and disable the vSafe0V comparator, respectively.

V_{BUS} Overvoltage/Undervoltage (OV/UV) Comparator

Programmable V_{BUS} OV and UV comparators are implemented in the MAX25432.

To program the V_{BUS} OV and UV thresholds, write to VBUS_OV_THRESH[2:0] and VBUS_UV_THRESH[2:0], respectively, located in the VBUS_THRESH[7:0] register. By default, the thresholds are set to +12.5% and -12.5% of the current V_{BUS} target.

Upon an overvoltage event on V_{BUS}, the MAX25432 will turn off V_{BUS} and discharge it to vSafe0V immediately (Fault Action A). See the *Fault Detection and Diagnostics* section for more information on this fault.

The MAX25432 will report an overvoltage event through the VBUS_OVP_FAULT in FAULT_STATUS register if the VBUS_OVP_DET_EN in the FAULT_CONTROL register is set to logic '1'. If the MSK_VBUS_OVP bit in FAULT_STATUS_MASK register is unmasked, the FAULT_STAT bit in the ALERT_H register will be set and latched to logic '1'. The $\overline{\text{ALERT}}$ pin will be asserted low if the MSK_FAULT_STAT bit is unmasked. Write a '1' to FAULT_STAT and VBUS_OVP_FAULT to clear the fault.

The MAX25432 will report an undervoltage event through the VBUS_UV status bit in the AUTO_SHIELD_STATUS register. If the VBUS_UV_MASK bit in the AUTO_SHIELD_STATUS_MASK register is unmasked, the VNDR_ALRT bit will be set and latched to logic '1'. The $\overline{\text{ALERT}}$ pin will be asserted low if the MSK_FAULT_STAT bit is unmasked. Write a '1' to VNDR_ALRT to clear the fault.

See the *Mask Registers and Nested Alerts* section for a complete overview of the fault reporting tree through mask registers.

V_{BUS} Discharge

When VBUS is disabled, the residual charge stored in the buck-boost output capacitance must be removed to comply with the Type-C specification. The MAX25432 has an internal discharge path that when activated, discharges V_{BUS} to a set threshold. *Figure 10* shows the discharge internal circuitry used for both force and auto-discharge features, which are compliant with the USB PD and TCPCI specifications.

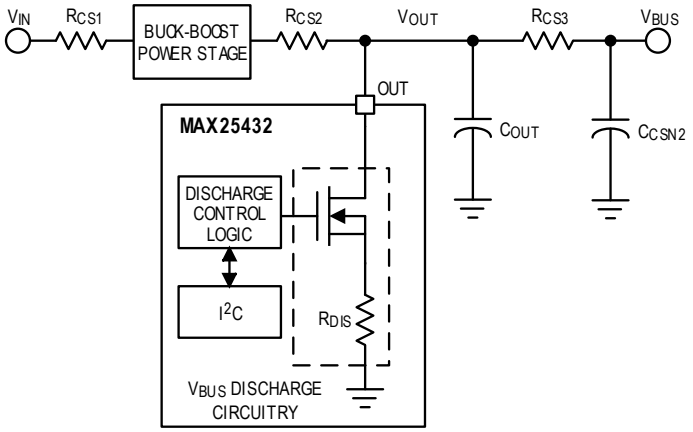


Figure 10. V_{BUS} Discharge Block Diagram

PRELIMINARY

V_{BUS} Force Discharge

Whenever the FORC_DISCH_EN bit D2 in the POWER_CONTROL register is set from logic '0' to '1', the 125Ω discharge R_{DIS} is switched on and the discharge monitoring starts. The MAX25432 automatically disables the force discharge circuit (without clearing FORC_DISCH_EN bit) once the voltage on V_{OUT} has reached the value indicated by the 10-bit VBUS_STOP_DISCH_THRESHOLD register. It is recommended to use the minimum stop threshold of 0.5V to pass compliance.

If V_{OUT} does not reach the programmed Stop threshold (default 0.8V) within 650ms, the discharge stops to avoid possible overheating and flags the FORCE_DISCH_FAIL bit, which, if unmasked, sets the FAULT_STAT bit in the ALERT_H register. If FAULT_STAT is unmasked, $\overline{ALERT}$ is asserted. A typical use case of the V_{BUS} force discharge is after a device disconnect when using a PD controller with the MAX25432A or a hard reset when using either the MAX25432A or MAX25432B.

See the Register Map for more information on the V_{BUS} force discharge function.

V_{BUS} Auto-Discharge

The V_{BUS} auto-discharge function (MAX25432B devices only) is enabled by setting the AUTO_DISCH_DISC_EN bit D4 to 1 after a device attachment. When the MAX25432 detects a device disconnect, sourcing V_{BUS} is disabled, then the 125Ω discharge resistor R_{DIS} is switched on automatically and discharge monitoring starts. The MAX25432 automatically disables the auto-discharge circuit (without clearing AUTO_DISCH_EN bit) once the voltage on V_{OUT} has reached the value indicated by the 10-bit VBUS_STOP_DISCH_THRESHOLD register. It is recommended to use the minimum stop threshold of 0.5V to pass compliance.

If V_{OUT} does not reach the programmed stop threshold within 650ms, the discharge stops to avoid possible overheating and flags the AUTO_DISCH_FAIL bit, which, if unmasked, sets the FAULT_STAT bit in the ALERT_H register. If FAULT_STAT is unmasked, $\overline{ALERT}$ is asserted.

See the for more information on the V_{BUS} auto-discharge function.

Figure 11 shows the POWER_CONTROL register which contains the V_{BUS} auto and force discharge enable bits.

ADDR	REGISTER NAME	POR	D7	D6	D5	D4	D3	D2	D1	D0
0x1C	POWER_CONTROL	0x60		V_{BUS} VOLTAGE MONITORING ENABLE	DISABLE VOLTAGE ALARMS	AUTO DISCHARGE ON DISCONNECT ENABLE		FORCE DISCHARGE ENABLE	V_{CONN} POWER SUPPORTED	V_{CONN} ENABLE

NOTE: REGISTER ACCESS READ/WRITE READ ONLY

Figure 11. POWER_CONTROL Register for V_{BUS} Discharge

Figure 12 shows a typical V_{BUS} discharge waveform. The blue curve shows a V_{BUS} discharge reaching the programmed stop threshold before the 650ms timeout and is therefore successful and no error flag is set. The red curve shows a discharge that did not reach the stop threshold on time and therefore is flagged as fail on either the FORCE_DISCH_FAIL or AUTO_DISCH_FAIL depending on the type of discharge used.

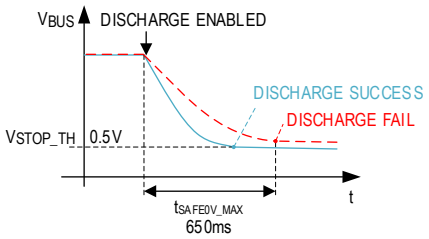


Figure 12. V_{BUS} Discharge Timing Diagram

Note: t_{SAFE0V} maximum value is defined in the USB PD specification.

Discharge Time

Due to the high-side FET circuit topology, V_{OUT} is discharged at a constant current rate first, down to 3.3V, then at a rate of $R_{DIS}.C_{TOT}$.

The discharge time t_{DIS} can be estimated using the following equation:

$$t_{DIS} = C_{TOT} \cdot \left[\frac{V_{START} - 3.3V}{I_{DIS}} - R_{DIS} \cdot \ln\left(\frac{V_{STOP}}{3.3V}\right)\right]$$

where:

C_{TOT} = Total output capacitance, in F

V_{START}, V_{STOP} = Start and stop voltages, in V

R_{DIS} = Internal discharge resistance, in Ω. R_{DIS} = 125Ω (typ)

I_{DIS} = Constant current discharge rate when V_{BUS} > 3.3V, in A. I_{DIS} = 28mA ±20%

Example

Table 4 shows typical discharge times for different output voltages.

Table 4. Discharge Times for Different Output Voltages

V_{BUS}	TYPICAL DISCHARGE TIME TO 0.5V*
vSafe5V	64ms
9V	94ms
15V	141ms
21V	187ms

**With C_{TOT} = 200µF (bulk) + 30µF (ceramic) = 215µF effective capacitance.*

PRELIMINARY

Host Charge Emulation

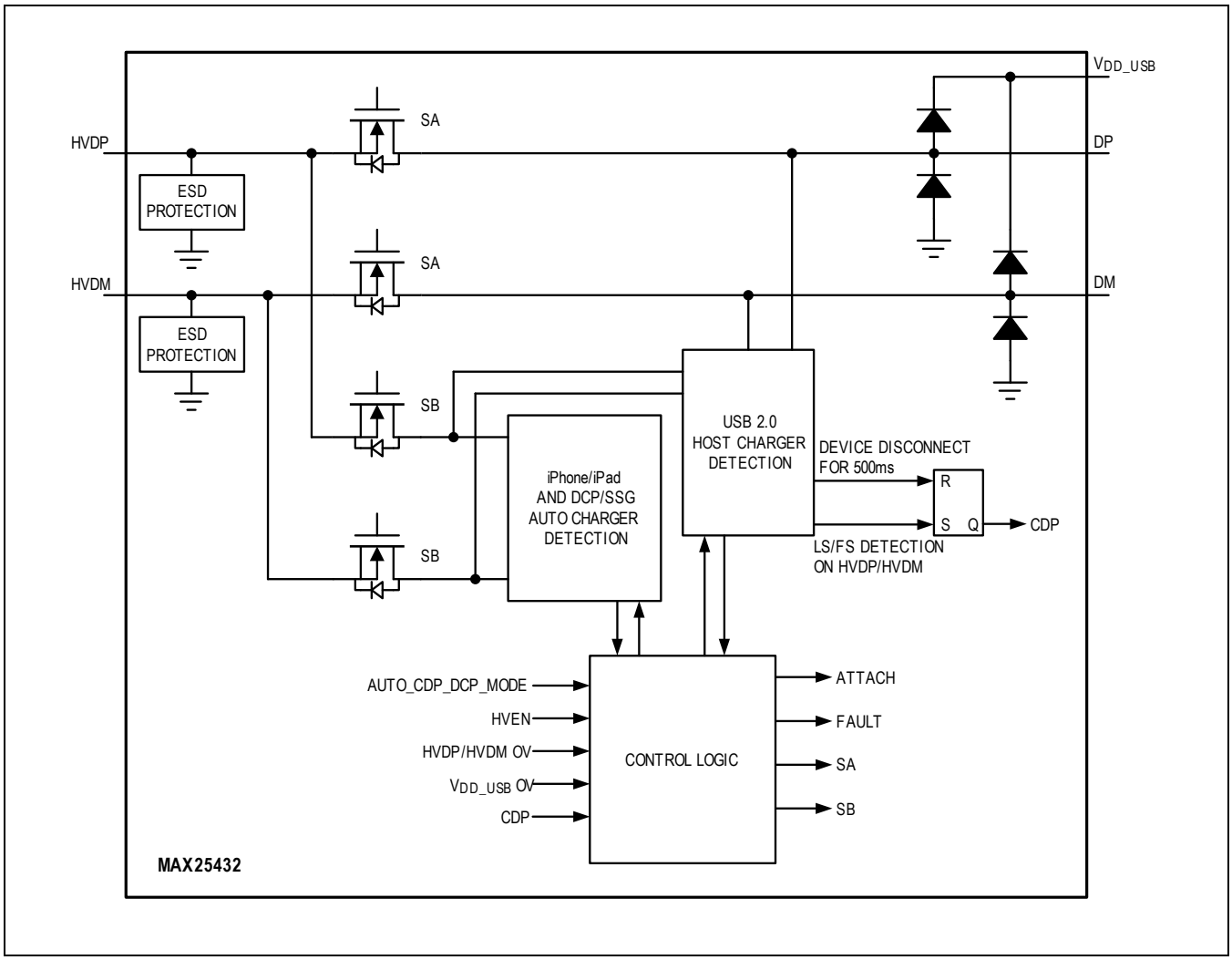


Figure 13. Host Charge Emulation Block Diagram

Note: USB-IF does not allow non-USB charging protocols on a USB Type-C connector. Analog Devices provides these features as optional for the user.

Charge Mode Selection

The MAX25432 integrates the latest USB-IF Battery Charging Specification Revision 1.2 (BC1.2) CDP and DCP circuitry. The Auto-DCP modes provide either 1.0A and 2.4A resistor bias options for Apple-compliant devices. Legacy Samsung Galaxy 1.2V divider and China YD/T1591-2009 compatibility is also provided by the Auto-DCP modes.

Refer to the following Analog Devices articles for more information on BC1.2:

- *USB Battery Charging and Adapter Emulators*
- *Overview of USB Battery Charging Revision 1.2 and the Important Role of Charger Detectors*

Table 5. Charge Mode Truth Table

HVEN	AUTO_CDP_DCP_MODE[1:0]	SA SWITCH	SB SWITCH	CHARGE MODE
Low	X	OFF	OFF	Off
High	00 (Default)	ON	OFF	Hi-Speed Pass-Through (SDP)

	01	ON if CDP = 0	ON if CDP = 1	Auto-CDP
	10	OFF	ON	Auto-DCP/Apple 2.4A
	11	OFF	ON	Auto-DCP/Apple 1.0A

Note: The host charge emulation block, which includes the Auto-CDP and Auto-DCP state machines, is independent of the Type-C interface, V_{BUS} or V_{CONN} status, and vice versa. Certain faults will turn off, then reset the host charge emulation block. See the *Fault Table (Analog Devices Auto-Shield)* for more information.

Auto-CDP Mode

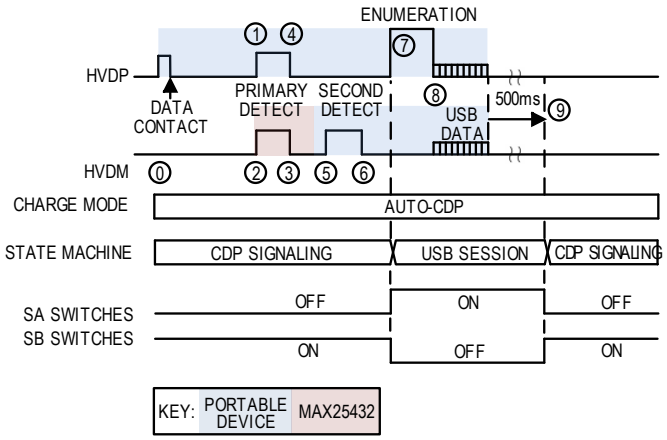


Figure 14. Auto-CDP State Diagram

This mode allows simultaneous charging through V_{BUS} (up to 1.5A per BC1.2*) and data transfer through the USB data path. In the Auto-CDP mode, the HVDP/HVDM pins are initially used to support primary and secondary detection implemented by the PD prior to switching over to their data roles during the USB session. Note that LS/FS and USB Hi-Speed 2.0 communication is only supported in the USB session state (starting in step 7, ending in step 9).

Within the Auto-CDP mode, the MAX25432 will automatically transition between CDP signaling and the USB session state without software interaction. The principles of operation are described as follows:

- The USB data switches (SA switches) are initially open (step 0 in *Figure 14*), and the detection circuitry is connected to HVDP/HVDM (SB switches). This is the resting state in the Auto-CDP mode and is called CDP Signaling state. In the CDP Signaling state, 19kΩ (typ) pulldowns are applied on HVDP/HVDM and IDAT_SINK is active on HVDP.
- Upon being plugged in, the portable device may perform data contact detection (DCD) to check whether the data pins have made contact. Some portable devices skip this step and instead implement a delay.
- Once DCD is done, the portable device will apply 0.6V (typ) on HVDP and look for the same voltage on HVDM (step 1). If it sees the same voltage, it knows the host is either a CDP or a DCP.
- Once the MAX25432 sees the 0.6V voltage on HVDP, it will apply 0.6V on HVDM by turning on V_{DAT_SRC} (step 2). This step is called primary detection and is used to differentiate between a charging port and a standard downstream port (SDP). Per the BC1.2 specification, a charging port may support USB data (CDP) or be used only for charging (DCP).
- In secondary detection, the MAX25432 turns off the 0.6V source on HVDM (step 3), the portable device turns off the 0.6V source on HVDP (step 4) and applies 0.6V on HVDM (step 5). Since no voltage will appear on HVDP, the portable device knows it is attached to a CDP (step 6). This is the last step of the BC1.2 detection and is used to differentiate between a CDP and a DCP.
- Once the CDP detection is done, the MAX25432 will look for the enumeration signal on either HVDP or HVDM (1.6V, typ). Once this signal is detected, the MAX25432 will close the data switches (step 7) to allow the host and device to establish USB Hi-Speed communication (step 8). This state is called USB Session mode and is exited when no data traffic has happened on the bus for 500ms or more (step 9).

PRELIMINARY

* Note that a higher Type-C or USB PD current advertisement takes precedence over BC1.2.

USB On-The-Go, Dual-Role Applications and Field Programmability

The MAX25432 is fully compatible with USB OTG and dual-role applications. A negotiated role swap (HNP or Apple CarPlay) requires no software interaction with the IC. When there is no negotiation before the SoC enters peripheral mode, the MAX25432 must be in Hi-Speed pass-through (SDP mode) before and during the role swap.

The MAX25432 devices default to SDP mode on startup. This configuration allows a role swap immediately upon startup without microcontroller interaction. This also allows the application firmware to be programmable though the USB data lines once the vehicle is in the field.

Note that the I^2C controller can change the Data Switch mode anytime by writing to the AUTO_CDP_DCP_MODE[1:0] register.

Protection

In an automotive Type-C PD application, several threats to the module can be encountered.

In case of a short-to-V_{BUS} event on CC connector pins, the V_{CONN} switch must protect the upstream supply against overvoltage. The CC switches must clamp and dissipate the energy in order to protect the upstream CC controller from pin damage.

In case of a short to GND, the shared 3.3V or 5.0V rail supplying V_{CONN} shall not brownout or be damaged.

For applications with a USB 2.0 host, the host's DP/DM pins typically have an absolute maximum rating of V_{DD} + 0.3V = 3.6V and therefore will not survive any short-to-battery, short-to-V_{BUS}, or automotive ESD event.

Short-to-battery (18V) can happen during module assembly, repair, or in the field (e.g., the end-user dropping the end of cable in the cigarette lighter).

Short-to-V_{BUS} (21V PD, up to 24V) is very common for USB Type-C ports and can happen upon device removal due to mechanical twisting, debris, or insertion of a non-PD compliant source into the port.

The MAX25432 protects the module against all of these threats.

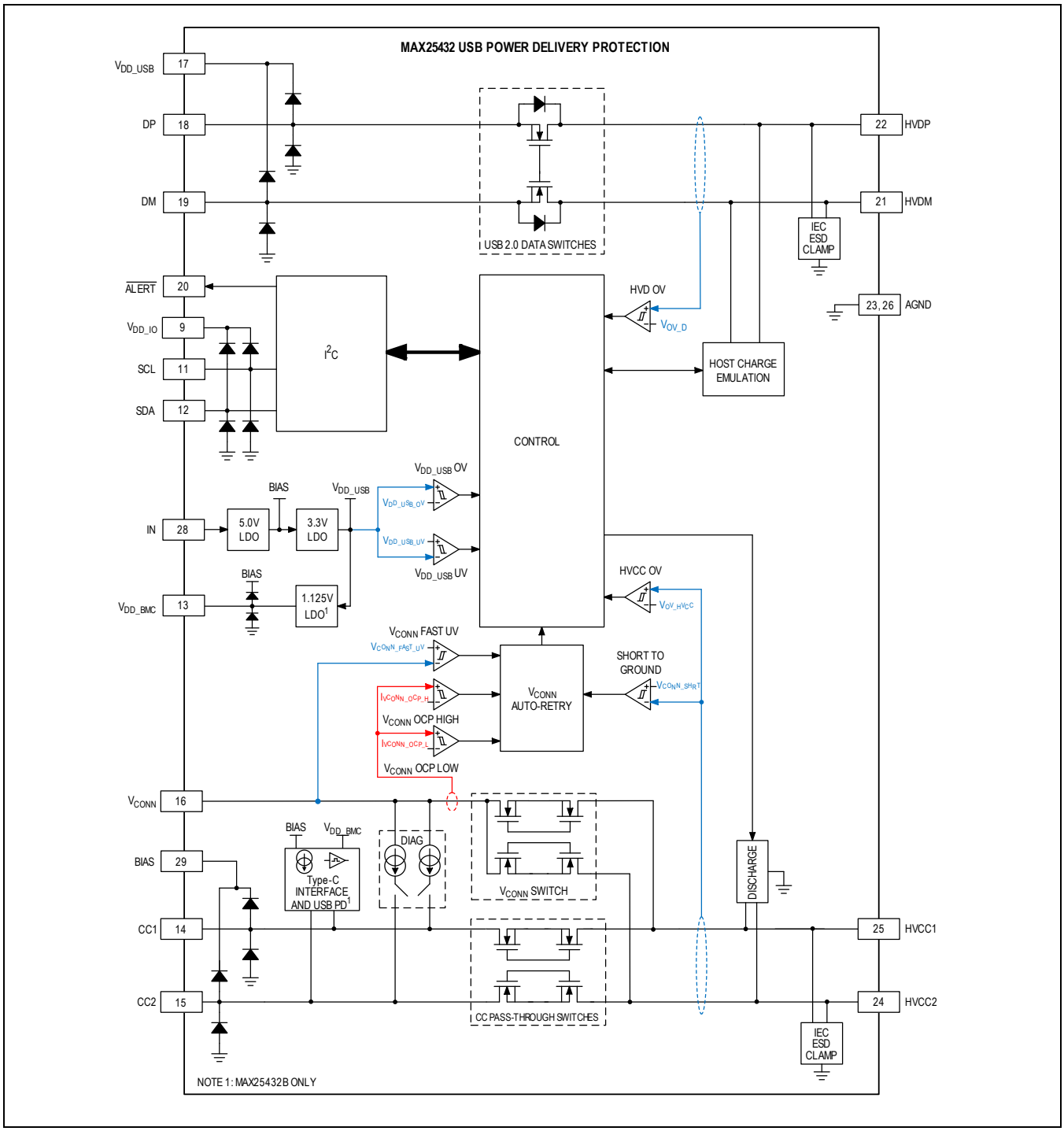


Figure 15. USB Power Delivery Protection Block Diagram

USB 2.0 Data Switches

The DP and DM pins are the protected side of the USB data switches and connect directly to the low-voltage upstream USB PHY or captive cable. No external circuitry is used on either data pin.

The HVDP and HVDM pins should be routed to the downstream Type-C connector or captive cable. No external circuitry is required on either pin. The HVDP and HVDM pins are tolerant to automotive high ESD and up to 24V transients.

CC Pass-Through Switch

The CC1 and CC2 pins are the protected side of the CC switches and either connect directly to the upstream USB PD controller for MAX25432A devices or internally to the TCPC block for MAX25432B devices. No external circuitry is needed on either CC pin. The HVCC1 and HVCC2 pins connect directly to the downstream USB Type-C port connector or captive cable. No external circuitry is needed on either HVCC pin. HVCC1 and HVCC2 are tolerant to automotive high ESD and up to 24V transients.

Shield Short-to-Battery Protection

A USB shield/GND short-to-battery event can occur when a customer's portable device cable is connected to the downstream receptacle and the far end of this cable falls into the 12V cigarette lighter receptacle and contacts the 12V center terminal. This condition results in a damaging amount of current flow, with insufficient response time by the cigarette lighter fuse. The MAX25432 variants with shield short-to-battery (SSTB) protection are designed to sense this fault condition with the SHLD_SNS pin and control an external NFET with the GDRV pin. The normally open (NO) ground logic will ensure no damaging current flows on Type-C to Type-C user cables by keeping the downstream connector ground open when no device is attached.

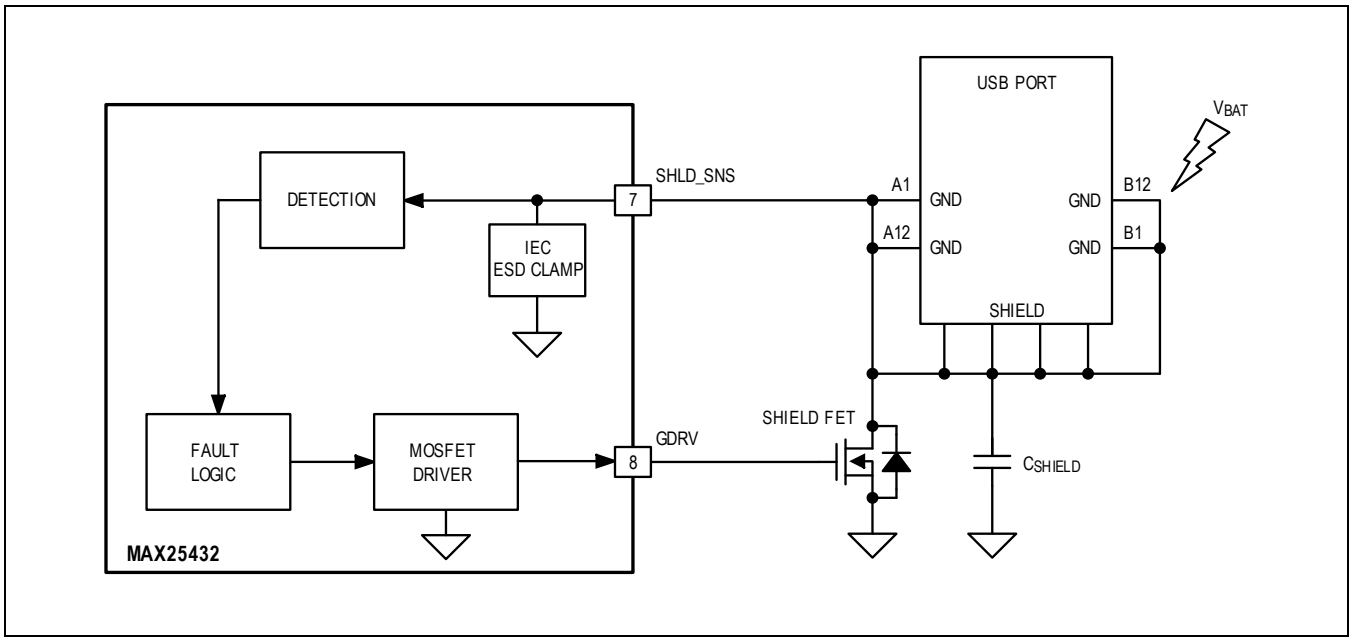


Figure 16. Shield Short-to-Battery Functional Diagram

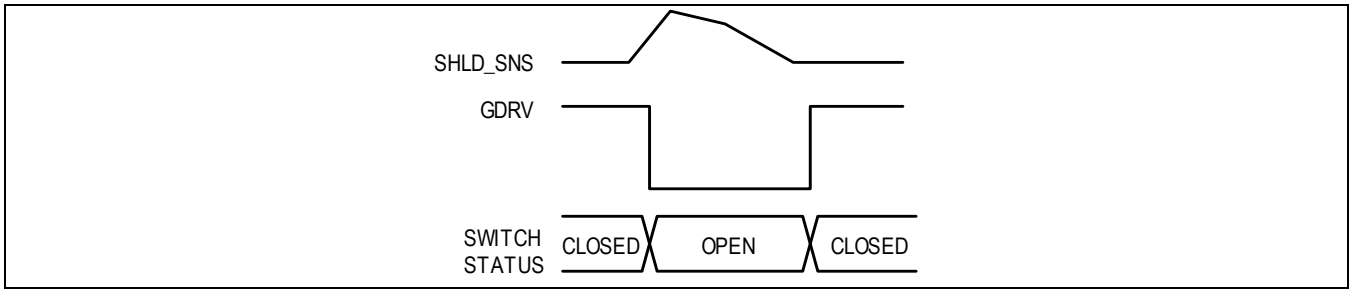


Figure 17. Shield/GND Short-to-Battery Timing Diagram

Figure 17 illustrates the response for the shield short-to-battery protection feature. When a Type-C attachment is present and the cable shield makes contact with V_{BAT}, a large surge current flows through the FET's $R_{DS(ON)}$ to ground. This surge current develops a voltage across it and is sensed through the MAX25432 SHLD_SNS pin. When the sense voltage exceeds a certain voltage threshold or slope, the fault-detection comparator is triggered. After a debounce period, the GDRV pin output goes low, causing the FET to switch off and reports the fault condition to the SHLD_EVENT bit. Once the fault condition is removed, the GDRV pin goes high to turn the FET on. The SHLD_EVENT flag can be cleared by the I^2C controller.

Principles of Operation

Normally Open Ground (All Devices)

The MAX25432 devices continuously monitor for a Type-C device attach and controls GDRV based on attach/detach events and timer circuitry.

When a Type-C connection is not present, the MAX25432 devices protect against shield short-to-battery events by leaving GDRV low. In this state, the USB shield and all other USB Type-C grounds are floating; however, a weak pulldown from SHLD_SNS is always active. This pulldown enables an Rd attach to be detected, while not providing a low-resistance path to ground.

When a valid Type-C attach is present, GDRV remains high for as long as the connection is present. A valid type-C attach may be to a native USB Type-C device, a Type-C to legacy adapter/cable, or an Apple Lightning cable.

If unused, GDRV should be tied with a 1MΩ resistor to ground.

Fault Detection (G-Suffix only)

The MAX25432 G-suffix will protect against damaging surge currents on any user cable by using two unique detection methods on the SHLD_SNS pin:

- Threshold Detection: Surge current exceeds a fixed threshold for several microseconds.
- Slope Detection: Surge current exceeds a fixed upper slew-rate limit.

Either of these protection mechanisms can trigger the shield short-to-battery fault handling described in the *Fault Table (Analog Devices Auto-Shield)*. Threshold and slope detections are automatically disabled when any of the following conditions are true:

- An attached USB device draws more than 400mA (typ). This condition resets when the current falls below 200mA (typ).
- An attached USB device has initiated a BC1.2 handshake (in Auto-CDP or Auto-DCP mode).
- A valid PD message was sent when V_{BUS} is being sourced. This condition resets when V_{BUS} is turned off or upon POR.

When a shield short-to-battery event is detected, GDRV is driven low until 1ms after the fault condition has cleared.

GDRV Truth Table

Table 6 shows the state of the GDRV pin with respect to the level detected on HVCC1 and HVCC2. This table applies to all MAX25432B devices. For the MAX25432A, it is assumed a PD controller is present upstream.

Table 6. GDRV Truth Table

V_{IN} > UVLO	HVEN	SOURCING V_{BUS} OR V_{CONN}	HVCC1	HVCC2	GDRV P-SUFFIX	GDRV ALL OTHER DEVICES
No	X[1]	X	X	X	Low	Low
Yes	Low	X	X	X		
	High	No	Open	Open		
			Open	Ra	High	
			Ra	Open		
			Open	Rd	High[2, 3]	High[2, 3]
			Rd	Open		
			Rd	Ra		
			Ra	Rd		
			Ra	Ra		
			Rd	Rd		
		Yes	X	X		

Note 1: "X" = Don't Care.

Note 2: If no shield short-to-battery fault has been detected on SSTB devices.

Note 3: Minimum GDRV on-time is 32ms (typ).

Fault Detection and Diagnostics

The MAX25432 features advanced fault reporting and management mechanisms to protect the system from various events that are not within normal operating conditions. The MAX25432 is designed to eliminate false fault reporting by using internal deglitch and fault blanking timers. This ensures the SHIELDING bit is not incorrectly asserted during normal operation, such as starting into heavy capacitive loads. To report the fault to the $\overline{ALERT}$ pin, set the corresponding mask bit. *Table 7* describes the different faults, reporting mechanisms, debounce values, action, and recovery type. Each action and recovery type is defined in *Table 8*.

Table 7. Fault Table (Analog Devices Auto-Shield)

NAME	EVENT	REPORTING	DEBOUNCE PRIOR TO ACTION	FAULT ACTION	FAULT RECOVERY
Thermal Shutdown	IC temperature exceeds the Thermal Shutdown Temperature	TSHDN SHIELDING VNDR_ALRTa	100µs	A	A
HVCC OV	HVCC1 or HVCC2 exceeds the VOV_HVCC threshold	HVCC_OV SHIELDING VNDR_ALRTa	Immediate	A	A
HVD OV	HVDP or HVDM exceeds the VOV_D threshold	DATA_OV SHIELDING VNDR_ALRTa	Immediate	A	A
V_{DD_USB} OV	VDD_USB exceeds the VDD_USB_OV threshold	VDD_USB_OV SHIELDING VNDR_ALRTa	Immediate	A	A
V_{DD_USB} UV	VDD_USB falls below the VDD_USB_UV threshold	VDD_USB_UV SHIELDING VNDR_ALRTa	Immediate	C	C
V_{BUS} I_{LIM}	CL_EN = 0: VBUS current exceeds the threshold set in the VBUS_ILIM_SET registers	CV_ILIM SHIELDING VNDR_ALRTa	16ms	A	A
	CL_EN = 1: VBUS current exceeds the threshold set in the VBUS_ILIM_SET registers. Enters current-limit (CL) regulation. Not a fault.	CL_CV OMF_TRANSc VNDR_ALRTa	N/A	None	N/A
V_{BUS} OCP	CL_EN = 0: VBUS current exceeds the IOUT_OCP threshold(e).	VBUS_OCP_FAULT FAULT_STATb	50µs	A	A
	CL_EN = 1: VBUS current exceeds the IOUT_OCP threshold(e).		250µs		
V_{BUS} OV	CL_EN = 0: VOUT exceeds the threshold set in the VBUS_OV_THRESH[2:0] register(f), except when VBUS is off, soft-starting or during VBUS transitions	VBUS_OVP_FAULT FAULT_STATb	Immediate	A	A
	CL_EN = 1: VOUT exceeds the threshold set in the VBUS_OV_THRESH[2:0] register(f), except when VBUS is off or soft-starting		250µs		
V_{BUS} UV	CL_CV = 0: VOUT falls below the threshold set in the VBUS_UV_THRESH[2:0] register,	VBUS_UV SHIELDING VNDR_ALRTa	16ms	C	C

	except when VBUS is off, soft-starting (or during VBUS transitions if CL_EN = 0).				
	CL_CV = 1: VOUT falls below the threshold set in the VBUS_UV_THRESH[2:0] register, except when VBUS is off or soft-starting.	None	N/A	None	N/A
V_{BUS} STG	CL_EN = 0: VOUT falls below 2.0V (typ)	VBUS_SHT_GND SHIELDING VNDR_ALRTa	Immediate	A	A
	CL_EN = 1: VOUT falls below 2.85V (typ)				
V_{BUS} Pre-Bias OV	COMMAND. Source Vbus Default Voltage is received, but VOUT is above the vSafe0V threshold.	I2C_ERR FAULT_STATb	10µs	C	C
V_{CONN} OCP Low	VCONN current exceeds the IVCONN_OCP_L thresholdg	VCONN_OCPLd SHIELDINGd VNDR_ALRTd,a VCONN_OCP_FAULTd FAULT_STATd,b	400µs	B	B
V_{CONN} OCP High	VCONN current exceeds the IVCONN_OCP_H thresholdg	VCONN_OCP_FAULTd FAULT_STATd,b	5µs	B	B
V_{CONN} UV	VCONN_EN = 0: VCONN pin falls below the VCONN_FAST_UV threshold	VCONN_IN_UVg VNDR_ALRTe,g	Immediate	B	B
	VCONN_EN = 1: VCONN pin falls below the VVCONN_FAST_UV threshold	VCONN_IN_UVg VCONN_OCPLg SHIELDINGg VNDR_ALRTa,g VCONN_OCP_FAULTg FAULT_STATb, g			
V_{CONN} Reverse OV	HVCC to VCONN pin voltage exceeds the reverse overvoltage threshold (100mV, typ)	VCONN_REV_OV SHIELDING VNDR_ALRTa	Immediate	D	B
V_{CONN} STG	HVCC is below the STG (0.5V (typ) for more than 8ms) prior VCONN switch soft-start	VCONN_PRESENT stays at 0	30µs	Disable V_{CONN} and take Action D except Retry Time is 16ms	B
IN UV	VIN (main IC supply) falls below the threshold set in the IN_UV_THRESH[3:0] register	IN_UV SHIELDING VNDR_ALRTa	100µs	A	A
Shield Short-to-Battery	A shield short-to-battery event has been detected. (G-suffix devices only). See the *Shield Short-to-Battery Protection* section.	SHLD_EVENT SHIELDING VNDR_ALRTa	Threshold: 5µs Slope: 2µs	A and turn off SHIELD FET	A
Input Overcurrent	The differential voltage across the input current sense resistor exceeds the VOC1 threshold (16.6A (typ) for RCS1 = 3mΩ)	IN_OC SHIELDING VNDR_ALRTf	16ms	C	C
V_{BUS} Runaway	CL_EN = 0 & VBUS is below 50% of the target regulation voltage.		50µs	A	A

	The voltage across RCS2 is above the VOC2 threshold	VBUS_RNA SHIELDING VNDR_ALRTa	Immediate		

Note a: If SHIELDING_MASK = '1'

Note b: If the corresponding FAULT_STATUS_MASK[7:0] is set

Note c: If OMF_TRANS_MASK = '1'

Note d: On the third consecutive fault

Note e: If VBUS_OCP_DET_EN = '0'

Note f: If VBUS_OVP_DET_EN = '0'

Note g: If VCONN_OCP_DET_EN = '0'

Table 8. Fault Types

FAULT TYPE	ACTION1	RECOVERY
A	• Assert ALERT2 • Disable DC-DC, discharge to vSafe0V • Open data switches • Open CC pass-through switches • Discharge HVCC1 and HVCC2 pins • Open V_{CONN} switch for RETRY_TMR setting • Reset BC1.2 state machine	• DC-DC can be re-enabled by the I2C controller through the COMMAND register • Close data switches • Close CC pass-through switches • Close V_{CONN} switch based on TCPC POWER_CONTROL[0] and TCPC_CONTROL[0] settings

B	• First and second fault:
	  • Open V_{CONN} switch
	  • Start V_{CONN} STG detect sequence
	  • Start V_{CONN} retry sequence
	• Third fault: Same as first two faults except:
	  • Open V_{CONN} switch for the time set in RETRY_TMR bit field
	  • Assert ALERT2
	(Note 3)
		Close V_{CONN} switch depending on TCPC POWER_CONTROL[0] and TCPC_CONTROL[0] settings

C	Assert ALERT2	None
D	• Open V_{CONN} switch for the time set in RETRY_TMR bit field • Assert ALERT2 (Note 3)	Close V_{CONN} switch depending on TCPC POWER_CONTROL[0] and TCPC_CONTROL[0] settings

Note 1: Faults do not reset the TCPC state machine nor disable R_P current sources.

Note 2: If MSK_VNDR_ALRT = 1

Note 3: The MAX25432 always maintains CC switches closed during those faults.

Additional information:

- A fault is detected when a fault condition in the EVENT column is true. A fault condition is removed when that condition returns to false.
  - For example, the Thermal Shutdown fault is no longer true when the MAX25432 temperature is reduced to below the temperature shutdown threshold.
- For V_{BUS} Short-to-Ground (STG) fault: The IC detects this fault when V_{BUS} is being sourced and V_{BUS} falls below the V_{BUS} STG voltage threshold, as described in the *Fault Table (Analog Devices Auto-Shield)*.
  - The MAX25432 takes action A upon detecting this fault, which turns off V_{BUS} immediately and therefore, clears the fault.

  - However, the MAX25432 cannot know if the STG condition is still there or not, since V_{BUS} is not being sourced anymore due to Fault Action A.
- V_{BUS} can be re-enabled by I^2C after the RETRY_TIMER has expired.
- The MAX25432 will never automatically enable sourcing of V_{BUS}. It is the I^2C controller that always need to send an I^2C command to enable V_{BUS}.
- The MAX25432 will never retry (i.e., perform the recovery steps) if a fault is still being detected. For instance, if a fault is applied continuously, the MAX25432 will not start the RETRY_TIMER and therefore will not retry.
- All the V_{BUS} faults are being monitored only when V_{BUS} is being sourced. The same is true for V_{CONN} faults, except for V_{CONN} UV.
- The faults that are always being monitored, regardless of V_{BUS} or V_{CONN} being sourced are the following: Thermal Shutdown, HVCC OV, HVD OV, V_{DD_USB} OV, V_{CONN} UV, IN UV.

I^2C, Control, and Diagnostics

I^2C Diagnostics and Events Handling

Contact Analog Devices for more information on how to program I^2C diagnostics and events handling.

Mask Registers and Nested Alerts

The registers in this section provide the masks that may be set for the ALERT registers. A masked register still indicates in the ALERT register, but does not set the $\overline{ALERT}$ pin low. POWER_STATUS_MASK, FAULT_STATUS_MASK, EXTENDED_STATUS_MASK and ALERT_EXTENDED_MASK registers are nested alerts.

- A POWER_STATUS change has to be unmasked in both the POWER_STATUS_MASK and the ALERT_MASK_L.MSK_PWR_STAT to assert the $\overline{ALERT}$ pin.
- A FAULT_STATUS change has to be unmasked in both the FAULT_STATUS_MASK and the ALERT_MASK_H.MSK_FAULT_STAT to assert the $\overline{ALERT}$ pin.
- An EXTENDED_STATUS change has to be unmasked in both the EXTENDED_STATUS_MASK and the ALERT_MASK_H.MSK_EXTND_STAT to assert the $\overline{ALERT}$ pin.
- An ALERT_EXTENDED change has to be unmasked in both the ALERT_EXTENDED_MASK and the ALERT_MASK_H.MSK_ALRT_EXTND to assert the $\overline{ALERT}$ pin.

In the application, the TCPM will first clear all bits in FAULT_STATUS register and then clear FAULT_STAT bit in ALERT_H to clear the ALERT, provided all fault conditions are cleared.

Figure 18 and *Figure 19* describe the alerts, and the corresponding masks and links between them. A Level 1 alert requires to have one mask bit unmasked to assert the $\overline{ALERT}$ pin. A Level 2 alert requires to have two mask bits unmasked to assert the $\overline{ALERT}$ pin.

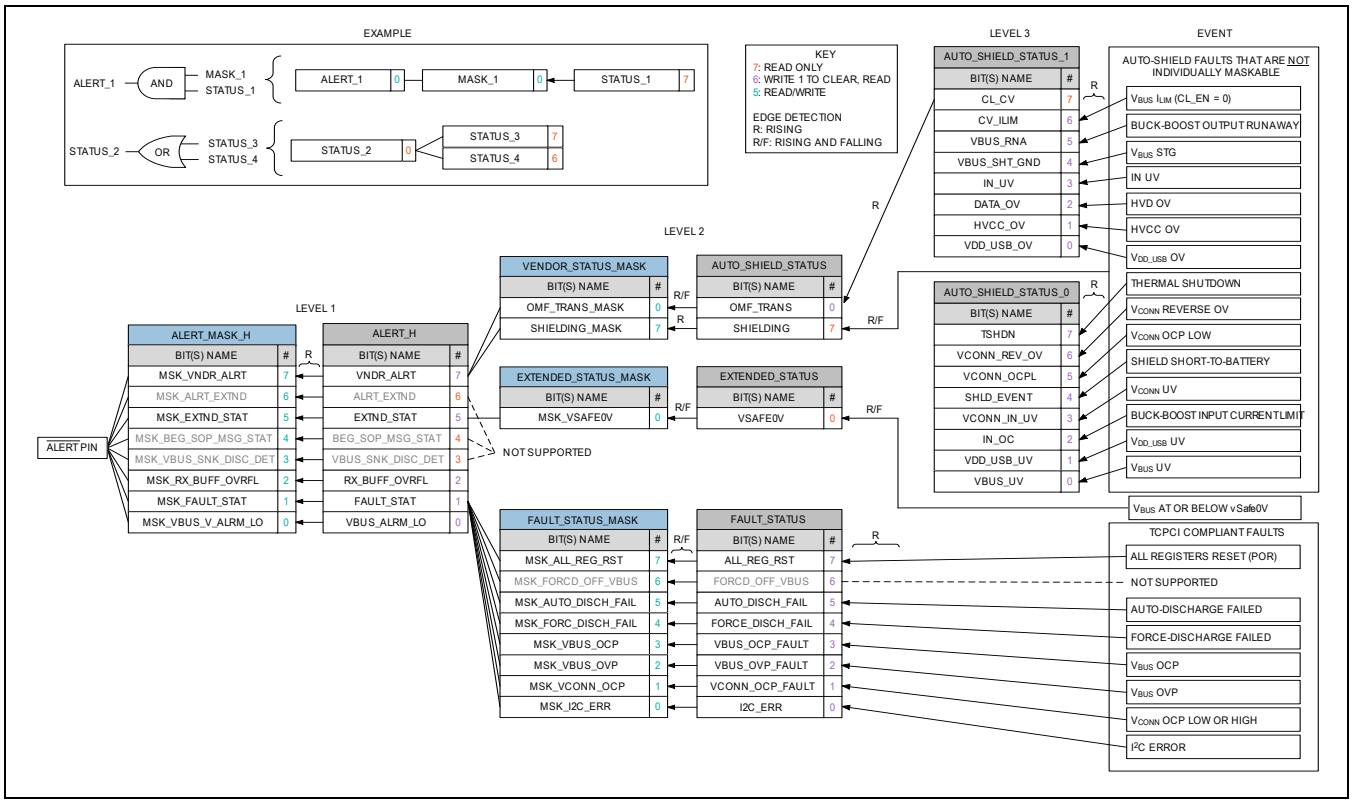


Figure 18. Nested Alerts Diagram - ALERT_H

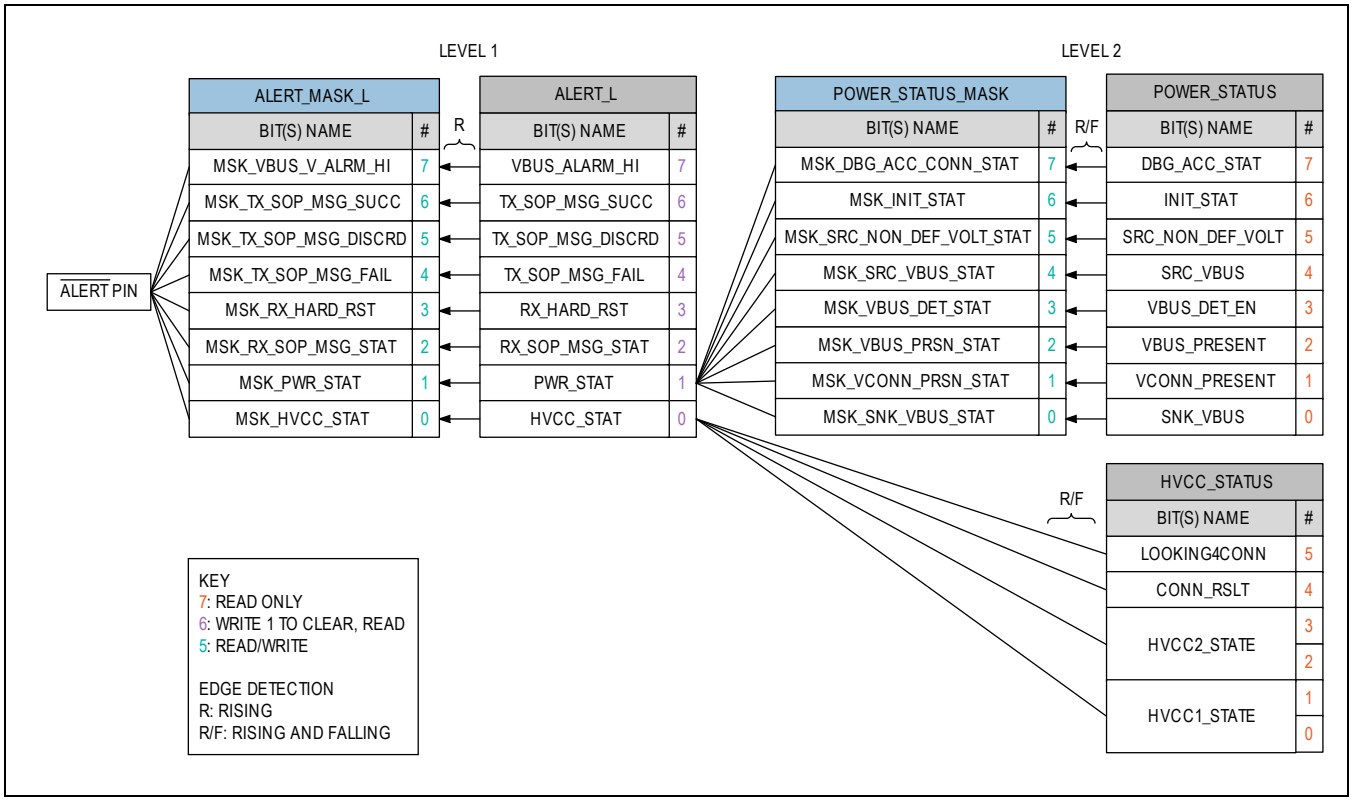


Figure 19. Nested Alerts Diagram - ALERT_L

I²C Interface

The MAX25432 is an I²C target device and requires an I²C controller to communicate with its internal registers. It can accept SCL clock rates up to 1MHz, and its 7-bit device address can be set to 0x50, 0x51, 0x52, or 0x53 through the ADDR input pin.

The I²C controller: a PD controller, SoC or microcontroller, generates SCL and always initiates data transfer on the bus. The MAX25432's SCL line operates as an input only. A pullup resistor greater than 500 Ω is required on SCL if the I²C controller has an open-drain SCL output.

The MAX25432's SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA line.

These resistors should be placed close to the MAX25432 SCL and SDA pins to minimize the effects of I²C bus capacitance. Analog Devices recommends using a value of 4.7kΩ for both resistors in most cases. Series resistors in line with SCL and SDA are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

The MAX25432 I²C target logic is powered by the voltage applied to V_{DD_IO} (1.8V to 5.0V), allowing the MAX25432's logic levels to be matched with those of the I²C controller. Note that I²C communications is possible even if the buck-boost is not switching (i.e., when V_{BUS} is off).

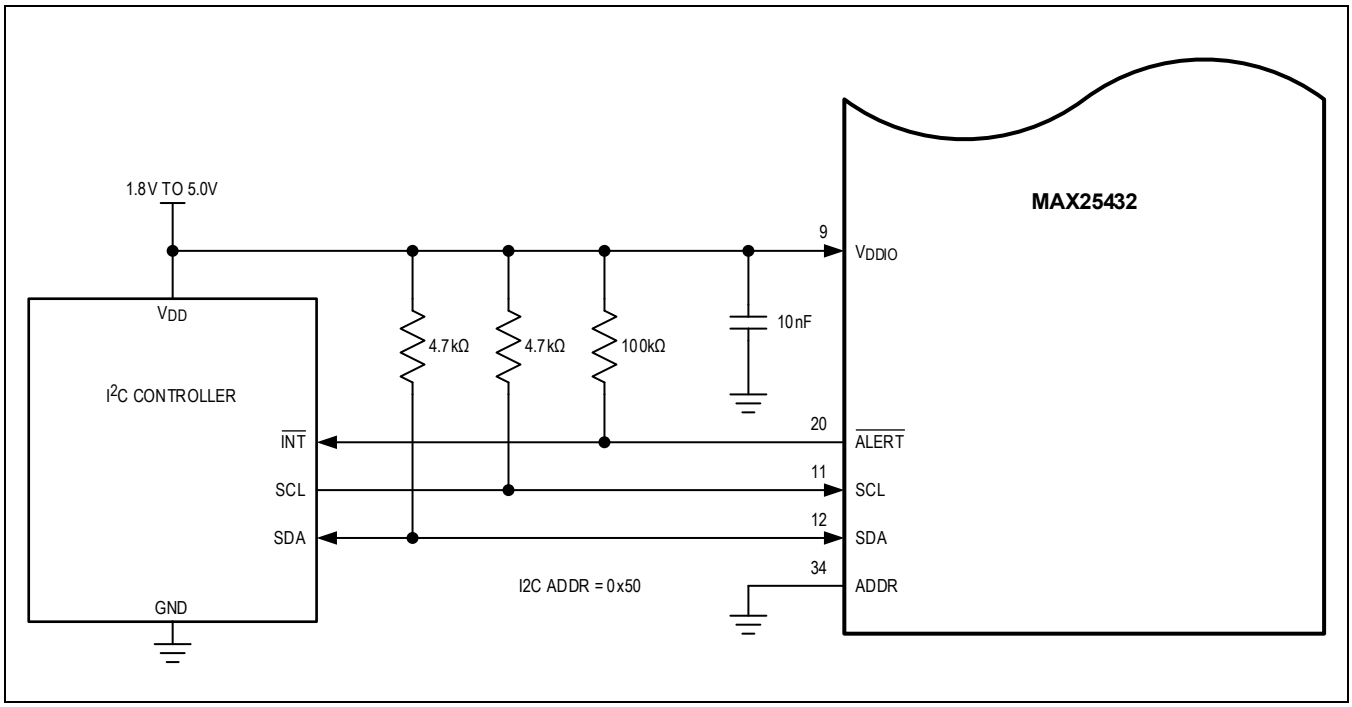


Figure 20. Typical I²C Application Diagram

Interrupt Output (ALERT Pin)

ALERT is an active-low, open-drain output that asserts to notify the I²C controller of an interrupt. A pullup to V_{DD_IO} is required for proper operation. Note that certain bits require their corresponding mask bit to be set for the ALERT pin to be asserted, as the mask bits act as AND gates.

I²C Target Addressing (ADDR Pin)

Once the device is enabled, the I²C target address is set and latched based on the ADDR pin. The address is defined as the 7 most significant bits (MSBs) followed by the R/W bit. Set the R/W bit to 1 to configure the devices to Read mode. Set the R/W bit to 0 to configure the device to Write mode. The address is the first byte of information sent to the devices after the START condition.

Table 9. I²C Target Addresses

ADDR PIN	A6	A5	A4	A3	A2	A1	A0	7-BIT ADDRESS	WRITE	READ
GND	1	0	1	0	0	0	0	0x50	0xA0	0xA1
8870Ω to GND	1	0	1	0	0	0	1	0x51	0xA2	0xA3
15800Ω to GND	1	0	1	0	0	1	0	0x52	0xA4	0xA5
BIAS	1	0	1	0	0	1	1	0x53	0xA6	0xA7

I²C Protocol

Data is transferred MSB first with each data bit present on SDA sampled on every SCL clock pulse while the SDA line is stable. A byte of data on SDA contains 8 bits, MSB first, that can represent but is not limited to a register address or data written to the device. Additionally, SDA should never change while the SCL is high. There are two exceptions to this rule: the START condition and the STOP condition.

START Condition

Every I²C transaction between an I²C controller and target device begins with the controller sending a START condition. The I²C controller generates a START condition by first detecting when the I²C bus is idle, and then asserting the SDA signal low while allowing SCL to remain pulled high.

STOP Condition

An I²C STOP condition is created whenever an I²C controller produces a rising edge on SDA while SCL remains high. This terminates any transaction with a target device and frees up the I²C bus. SDA and SCL idle high when the I²C bus is not busy. The bus remains active if a REPEATED START (RS) condition is generated instead of a STOP condition.

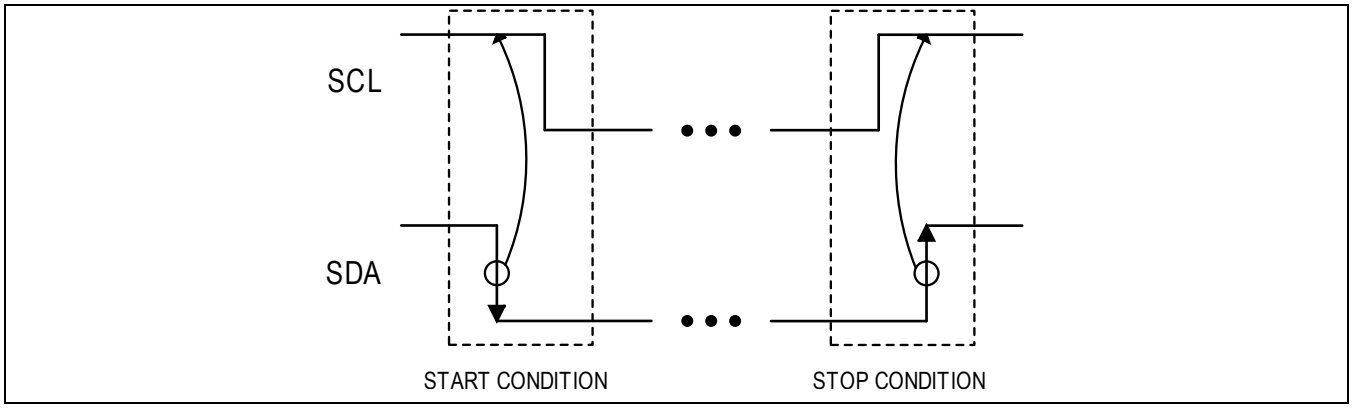


Figure 21. START and STOP Conditions

REPEATED START Condition

An I²C REPEATED START condition is created when an I²C controller produces a second START during a transaction with a target device. REPEATED STARTs are needed to signal the target device that the controller desires a change in data direction during a transaction. The REPEATED START is sent after the acknowledge bit (ACK).

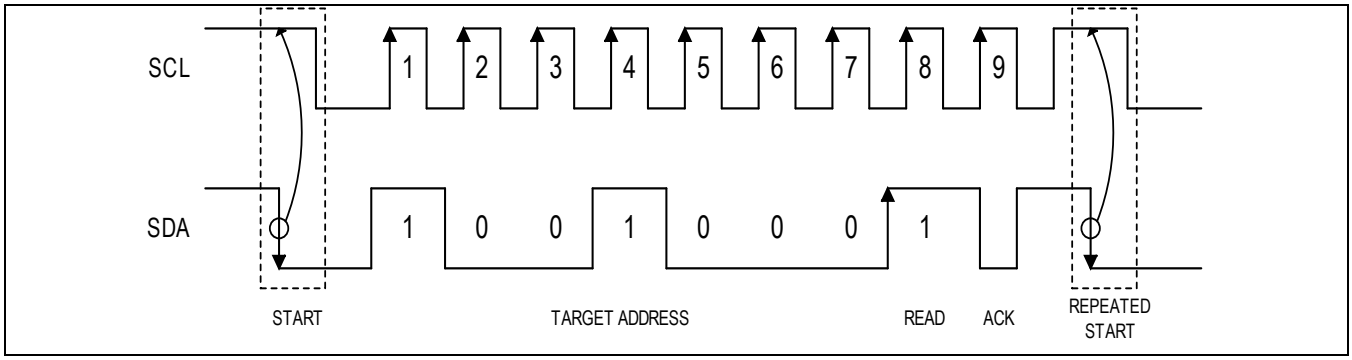


Figure 22. REPEATED START Condition

Acknowledge Bit (ACK)

ACK is a clocked 9th bit that the device uses to handshake receipt each byte of data. The device pulls down SDA during the controller-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the I²C controller can reattempt communication.

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the controller device. The I²C specification allows slow target devices to alter the clock signal by holding down the clock line. The process in which a target device holds down the clock line is typically called clock stretching. The MAX25432 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX25432 does not implement the I²C specification “general call address.” If the MAX25432 sees the general call address (0b0000_0000), it will not issue an acknowledge.

I²C Transactions

The MAX25432 supports several types of I²C transactions, described as follows.

Write Byte

The Write Byte transaction begins with the I²C controller sending a START condition. This is followed by a 7-bit address and R/W bit = 0, indicating a controller write operation. If this address matches the MAX25432 device address, it will ACK by holding the SDA line low for one SCL clock. The controller then sends the register address, which serves as a pointer to the MAX25432 register where data will be written. The MAX25432 again ACKs the byte sent. Then the controller sends the data byte and waits for the MAX25432 to ACK the data byte. Finally, the I²C controller terminates the transaction by sending a STOP condition.

When it is desired to write data to two or more noncontiguous MAX25432 registers, sequential Write transactions should be used. The MAX25432 will acknowledge its address and data bytes sent by the controller. A STOP condition by the controller terminates each write.

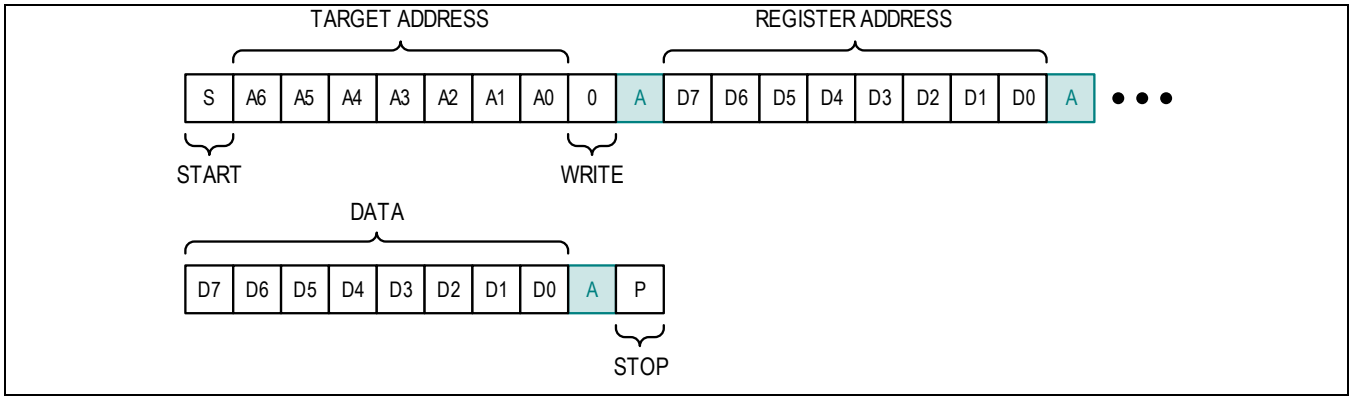


Figure 23. Write Byte

Write Word

The Write Word transaction is similar to the Write Byte transaction except that data is written to two sequential MAX25432 registers in one operation. The transaction begins exactly as a Write Byte transaction; namely a START condition, the target address followed by a write bit, then the register address. However, two data bytes are then sent — a low-address data byte (DATA n), followed by a high-address data byte (DATA n+1). The MAX25432 ACKs each byte received, and automatically increments the register address pointer between the low and high data bytes. Finally, the I²C controller sends a STOP condition to complete the transaction. Note that the low and high data bytes follow the same bit order as the previous bytes (target and register addresses) which is MSB first (D7 to D0). Once the data is received, the I²C controller will need to flip the bit order and concatenate to obtain a 16-bit word with LSB first.

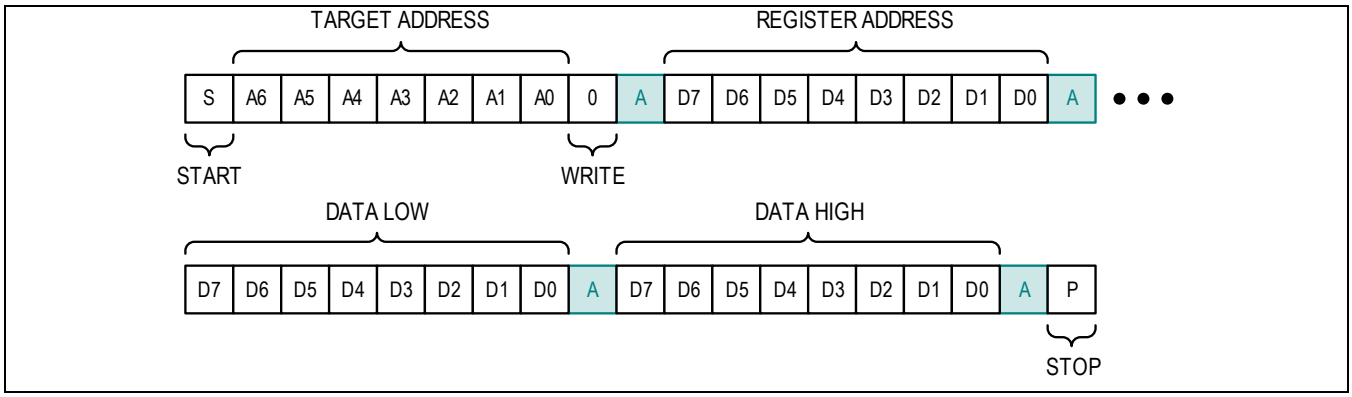


Figure 24. Write Word

Write Block

The MAX25432 also supports I2C block data writes for up to 255 contiguous registers. The MAX25432B's transmit buffer requires this type of I2C transaction for proper operation.



Figure 25. Write Block

The Write Block transaction begins by sending a START condition, followed by the MAX25432's 7-bit device address plus the R/W bit = 0. The MAX25432 will ACK its address, then the I2C controller sends the register address for the beginning of the contiguous block where data will be written. The MAX25432 again ACKs the received data.

The I2C controller can now write up to 255 bytes of data to the MAX25432 by continuing to clock the SCL signal. The MAX25432 will store data from SDA, one byte for each eight SCL clocks, and will ACK the data sent on the 9th SCL clock. The MAX25432 automatically increments the register address pointer between successive bytes. When the desired number of bytes from the MAX25432 has been sent, the controller sends a STOP condition to terminate the transaction.

Read Byte

The Read Byte transaction begins with the I2C controller sending a START condition. This is followed by a 7-bit address and R/W bit = 0, indicating a controller write operation. If this address matches the MAX25432 device address, the device will acknowledge (ACK) by holding the SDA line low for one SCL clock. The controller then sends the byte address, which serves as a pointer to the MAX25432 device register where data will be read. The MAX25432 again ACKs the byte sent. Then, the controller sends a REPEATED START condition, alerting the MAX25432 device that the next byte will again be an address. The controller device clocks in the MAX25432 address, this time appended with a logic '1'. This signals the MAX25432 that the controller wants to read the data from the register address previously sent. The MAX25432 again

ACKs the byte sent. On the rising of the next SCL clock, the target device begins sending the desired data byte to the controller. The controller will then signal the MAX25432 that the previous byte was the final byte needed by not acknowledging (NACK), followed by a STOP condition, indicating the end of the Read Byte transaction.

When the I²C controller desires to read data from two or more MAX25432 registers that are not contiguously located, sequential Read Byte transactions must be used. For instance, two bytes of data can be read from the MAX25432, one at register address 0x1E and the other at register address 0x20, however the I²C bus is released (STOP condition) between read operations. The MAX25432 will ACK its address and data bytes sent by the controller. It expects the controller to NACK the last data byte prior to sending a STOP condition.

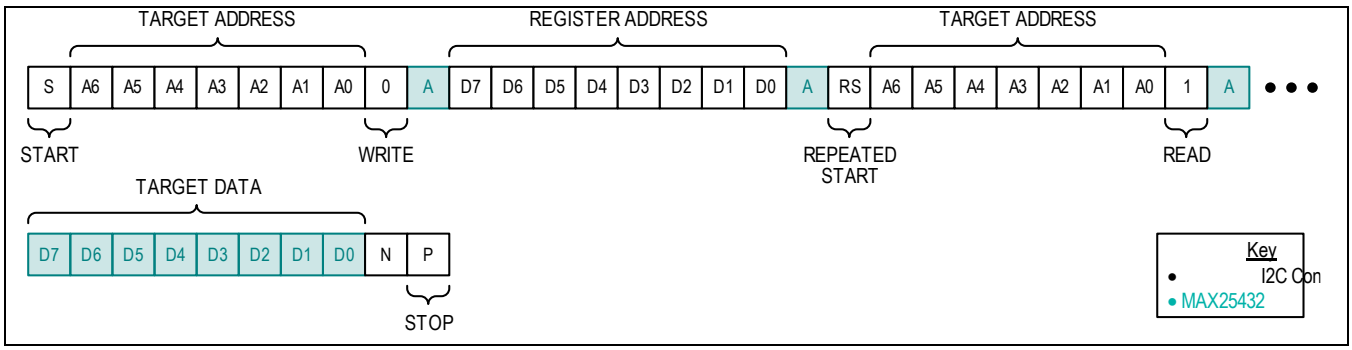


Figure 26. Read Byte

Read Word

The Read Word transaction follows the same sequence as the Read Byte except that two data bytes are received from the MAX25432, a low-address data byte (DATA n) followed by a high-address data byte (DATA n+1). This is accomplished by ACKing the first data byte received from the target device, and then NACKing the second data byte, followed by sending a STOP condition. Note that the MAX25432 automatically increments the register pointer to the next address. Reading ALERT_L and ALERT_H registers in a single operation is an example of using the Read Word transaction.

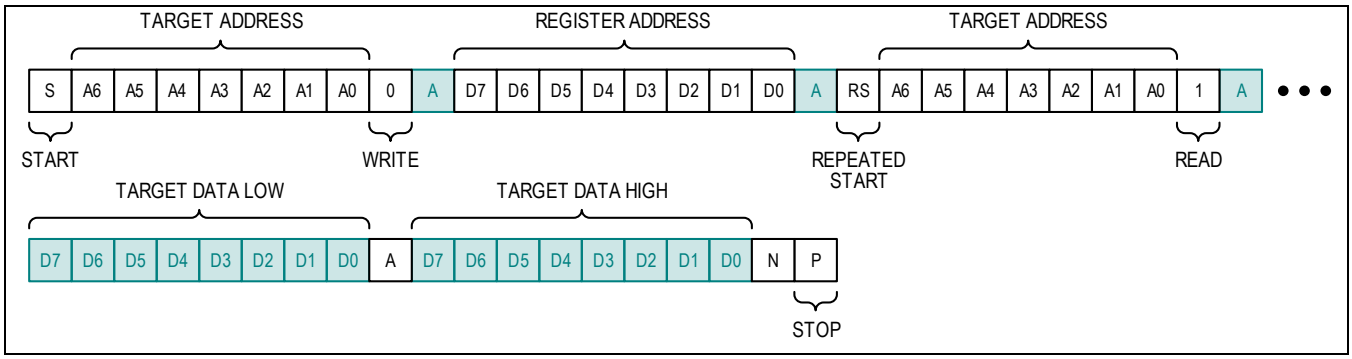


Figure 27. Read Word

Read Block

The Read Block transaction is a powerful function, enabling the I²C controller to read from 1 to 255 bytes of data from contiguous MAX25432 registers in one operation. Note that I²C Read operations from the MAX25432B's TCPC Receive Buffer require this type of I²C transaction for proper operation.



Figure 28. Read Block

The Read Block transaction begins as any I2C Read operation, first the controller sends a START condition, followed by the MAX25432's 7-bit device address plus the R/W bit = 0. The MAX25432 will ACK its address, then the controller sends the register address for the beginning of the contiguous block where data is to be read from. The MAX25432 again ACKs the received data. Next, the controller sends a REPEATED START condition, informing the MAX25432 that the next byte sent will be an address. The I2C controller then sends the MAX25432's 7-bit device address plus the R/W bit = 1, configuring the MAX25432 I2C for target read operation. The MAX25432 again acknowledges its address and prepares to deliver data from its registers.

The controller can now read up to 255 bytes of data from the MAX25432 by continuing to clock the SCL signal. The MAX25432 will output data on SDA, one byte for each 8 SCL clocks, and expect that the controller ACK the data sent on the 9th SCL clock. The MAX25432 will automatically increment the register address pointer between successive bytes. When the desired number of bytes from the MAX25432 has been sent, the controller must send a NACK followed by a STOP condition to terminate the transaction.

Register Access Type

Registers on MAX25432 have different access types, as shown in the Register Map. The list of access types is the following:

- Read Only: Non-latched. Register reports a live value.
- Write Only: Always reads back 0. The I2C controller can only write to these registers.
- Write 1 to Clear, Read: Latched. The I2C controller can read the latched value, and clear it by writing a 1.
- Write, Read: Modifiable by I2C controller only.
- Write, Read, Dual: Modifiable by I2C controller or MAX25432.

Write, Read, Ext: Modifiable by I2C controller or MAX25432 upon Hard Reset, or being acted upon in the case of the COMMAND register.

Watchdog Timer

The MAX25432 implements a programmable watchdog timer to give the design engineer the ability to monitor the I2C interface for lack of communication from the I2C controller. The watchdog provides a fail-safe mechanism in case the TCPM software stack or PD controller firmware hangs in a state where, for instance, a voltage is sourced on V_{BUS} when the sink is no longer attached.

The watchdog timer functionality is enabled by setting TCPC_CONTROL.EN_WD_TMR to logic '1'. The watchdog timer starts when the $\overline{\text{ALERT}}$ pin is asserted. The watchdog timer is cleared on any I2C access by the I2C controller (either Read or Write). If the $\overline{\text{ALERT}}$ pin is still asserted after this I2C access, the watchdog timer reinitializes and start monitoring again until the $\overline{\text{ALERT}}$ pin is deasserted.

If the I2C controller is unable to clear the watchdog timer within the programmed time set in WATCHDOG_SETUP.WD_TIMEOUT[1:0], it causes the watchdog timer to expire. When the watchdog timer expires, the

MAX25432 immediately disconnects the CC terminations by setting ROLE_CONTROL[3:0] to 1111b, discharge V_{BUS} to vSafe0V, and then set FAULT_STATUS.I2C_ERR bit. The MAX25432 will remove the V_{BUS} discharge circuit when V_{BUS} is below vSafe0V and it will not reapply the discharge circuit if V_{BUS} rises above vSafe0V. Stop discharge in this case is an edge-triggered event.

Any further changes on V_{BUS} need to be initiated by the I^2C controller when its communication link with the MAX25432 is restored.

Transmitting and Receiving a Hard Reset (MAX25432B only)

To transmit a Hard Reset, write 0x05 to the TRANSMIT[7:0] register.

Upon receiving a Hard Reset from the port partner, the MAX25432B will set the RX_HARD_RST flag in the ALERT_L[7:0] register.

Upon sending or receiving a Hard Reset, the MAX25432B resets the following registers to their default values:

- RECEIVE_DETECT[7:0]
- ALERT_MASK_L_SEL[7:0]
- ALERT_MASK_H_SEL[7:0]
- POWER_STATUS_MASK[7:0]
- EXTENDED_STATUS_MASK[7:0]
- ALERT_EXTENDED_MASK[7:0]

Built-In Self-Test (BIST)

The MAX25432B supports BIST Carrier Mode 2 and BIST Test Data Mode per USB PD Revision 3.0 Version 1.2.

- Transmitting BIST Carrier mode 2
  - Upon receiving a BIST data object (BDO) with the BIST type set to Carrier mode, the TCPM writes 0x07 to the TRANSMIT[7:0] register to enable BIST Carrier mode 2.
  - Immediately after, the MAX25432B transmits the BIST pattern for 50ms (typ) on the HVCC line corresponding to the orientation defined by the PLUG_ORNT bit.
  - At the end of the 50ms timer, the MAX25432B asserts ALERT and flags the TX_SOP_MSG_SUCC bit.
  - After reading this flag, the TCPM should enter the PE_SRC_Transition_to_default state.
- Entering/exiting BIST Test Data mode
  - Upon receiving a BDO with the BIST type set to Test Data, the TCPM sets the BIST_TM bit in the TCPC_CONTROL[7:0] register to enable BIST Test Data mode.
  - See the BIST_TM bit description for information on this mode.

The TCPM must clear the BIST_TM bit upon receiving a Hard Reset in order to exit this mode.

Register Map

Register_Map

The following register map summary table displays all the registers for the MAX25432 product family. Bit descriptions that show "MAX25432B only" are only applicable to MAX25432B devices. If using MAX25432A devices, "MAX25432B only" bits should be ignored and left to their reset values. Row "Reset" in Register Details contains MAX25432B reset values while row "Reset A" contains MAX25432A reset values.
Register values will reset to their default values upon a POR.
Registers starting from address 0x00 to address 0x79 are compliant to the Type-C Port Controller Interface Specification Revision 2.0, Version 1.1. Refer to the specification for additional information on how to use those registers.
Registers starting from address 0x80 to address 0x8B are vendor-defined by Analog Devices.
For more information on the MAX25432 register set and for instructions on how to program the interface, contact Analog Devices.

ADDRESS	NAME	MSB							LSB
USB Type-C and USB-PD Registers									
0x00	VENDOR_ID_L[7:0]	VENDOR_ID[7:0]							
0x01	VENDOR_ID_H[7:0]	VENDOR_ID[15:8]							
0x02	PRODUCT_ID_L[7:0]	PRODUCT_ID[7:0]							
0x03	PRODUCT_ID_H[7:0]	PRODUCT_ID[15:8]							
0x04	DEVICE_ID_L[7:0]	DEVICE_ID[7:0]							
0x05	DEVICE_ID_H[7:0]	DEVICE_ID[15:8]							
0x06	USBTYPEC_REV_L[7:0]	TYPEC_REV[7:0]							
0x08	USBPD_REV_VER_L[7:0]	PD_VER[7:0]							
0x09	USBPD_REV_VER_H[7:0]	PD_REV[7:0]							
0x0A	PD_INTERFACE_REV_L[7:0]	IBS_VER[7:0]							
0x0B	PD_INTERFACE_REV_H[7:0]	IBS_REV[7:0]							
0x10	ALERT_L[7:0]	VBUS_ALARM_HI	TX_SOP_MSG_SUCC	TX_SOP_MSG_DISCRD	TX_SOP_MSG_FAIL	RX_HARD_RST	RX_SOP_MSG_STAT	PWR_STAT	HVCC_STAT
0x11	ALERT_H[7:0]	VNDR_ALRT	ALRT_EXTND	EXTND_STAT	BEG_SOP_MSG_STAT	VBUS_SNK_DISC_DET	RX_BUFF_OVRFL	FAULT_STAT	VBUS_ALARM_LO
0x12	ALERT_MASK_L[7:0]	MSK_VBUS_V_ALRM_HI	MSK_TX_SOP_MSG_SUCC	MSK_TX_SOP_MSG_DISCRD	MSK_TX_SOP_MSG_FAIL	MSK_RX_HARD_RST	MSK_RX_SOP_MSG_STAT	MSK_PWR_STAT	MSK_HVCC_STAT
0x13	ALERT_MASK_H[7:0]	MSK_VNDR_ALRT	MSK_ALRT_EXTND	MSK_EXTND_STAT	MSK_BEG_SOP_MSG_STAT	MSK_VBUS_SNK_DISC_DET	MSK_RX_BUFF_OVRFL	MSK_FAULT_STAT	MSK_VBUS_V_ALRM_LO

ADDRESS	NAME	MSB							LSB
0x14	POWER_STATUS_MASK[7:0]	MSK_DEBG_ACC_CONN_STAT	MSK_TCPC_INIT_STAT	MSK_SRC_NON_DEF_VOLT_STAT	MSK_SRC_VBUS_STAT	MSK_VBUS_DET_STAT	MSK_VBUS_PRSN_STAT	MSK_VCONN_PRSN_STAT	MSK_SNK_VBUS_STAT
0x15	FAULT_STATUS_MASK[7:0]	MSK_All_REG_RST	MSK_FORCD_OFF_VBUS	MSK_AUTO_DISCH_FAIL	MSK_FORC_DISCH_FAIL	MSK_VBUS_OCP	MSK_VBUS_OVP	MSK_VCONN_OCP	MSK_I2C_ERR
0x16	EXTENDED_STATUS_MASK[7:0]	–	–	–	–	–	–	–	MSK_VSAFE0V
0x17	ALERT_EXTENDED_MASK[7:0]	–	–	–	–	–	MSK_TMR_EXP	MSK_SRC_FST_RSWP	MSK_SNK_FST_RSWP
0x19	TCPC_CONTROL[7:0]	EN_SMB_PEC	EN_LK4CONN_ALRT	EN_WD_TMR	DBG_ACC_CNTRL	I2C_CLK_STRCH[1:0]		BIST_TM	PLUG_ORNT
0x1A	ROLE_CONTROL[7:0]	–	DRP	RP_VAL[1:0]		HVCC2[1:0]		HVCC1[1:0]	
0x1B	FAULT_CONTROL[7:0]	–	–	–	FRC_OFF_VBUS_DIS	VBUS_DISCH_FLT_DET_TMR_EN	VBUS_OCP_DET_EN	VBUS_OVP_DET_EN	VCONN_OCP_DET_EN
0x1C	POWER_CONTROL[7:0]	FAST_RSWP_EN	VBUS_VOLT_MON_EN	VOLT_ALRMS_EN	AUTO_DISCH_DISC_EN	BLED_DISCH_EN	FORC_DISCH_EN	VCONN_PWR_SUPP	EN_VCONN
0x1D	HVCC_STATUS[7:0]	–	–	LOOKING4CONN	CONN_RSLT	HVCC2_STATE[1:0]		HVCC1_STATE[1:0]	
0x1E	POWER_STATUS[7:0]	DBG_ACC_STAT	INIT_STAT	SRC_NON_DEF_VOLT	SRC_VBUS	VBUS_DET_EN	VBUS_PRESENT	VCONN_PRESENT	SNK_VBUS
0x1F	FAULT_STATUS[7:0]	ALL_REG_RST	FORCD_OFF_VBUS	AUTO_DISCH_FAIL	FORCE_DISCH_FAIL	VBUS_OCP_FAULT	VBUS_OVP_FAULT	VCONN_OCP_FAULT	I2C_ERR
0x20	EXTENDED_STATUS[7:0]	–	–	–	–	–	–	–	VSAFE0V
0x21	ALERT_EXTENDED[7:0]	–	–	–	–	–	TMR_EXP	SRC_FST_RSWP	SNK_FST_RSWP
0x23	COMMAND[7:0]	COMMAND[7:0]							
0x24	DEVICE_CAPABILITIES_1_L[7:0]	PWR_ROLE_CAP[2:0]			SOP_DBG_CAP	SRC_VCONN_CAP	SNK_VBUS_CAP	SRC_HI_VBUS_CAP	SRC_VBUS_CAP

ADDRESS	NAME	MSB							LSB
0x25	DEVICE_CAPABILITIES_1_H[7:0]	VBUS_NONDEF_TRGT_CAP	VBUS_OCP_RPT_CAP	VBUS_OVP_RPT_CAP	BLEED_DISCH_CAP	FORCE_DISCH_CAP	VBUS_MEAS_ALRM_CAP	SRC_RES_SUP_CAP[1:0]	
0x26	DEVICE_CAPABILITIES_2_L[7:0]	SNK_DISC_DET_CAP	STP_DISCH_THR_CAP	VBUS_VOLT_ALRM_LSB_CAP[1:0]		VCONN_PWR_CAP[2:0]			VCONN_OCP_CAP
0x27	DEVICE_CAPABILITIES_2_H[7:0]	–	–	GENERIC_TMR_CAP	LONG_MSG_CAP	SMB_PEC_CAP	SRC_FRS_CAP	SNK_FRS_CAP	WDOG_TMR_CAP
0x28	STANDARD_INPUT_CAPABILITIES[7:0]	–	–	–	SRC_FRS_INP_CAP[1:0]		VBUS_EXT_OVP_CAP	VBUS_EXT_OCP_CAP	FRC_OFF_VBUS_CAP
0x29	STANDARD_OUTPUT_CAPABILITIES[7:0]	VBUS_SNK_DIS_DET_CAP	DBG_ACC_CAP	VBUS_PRESENT_CAP	AUD_ACC_CAP	ACT_CBL_CAP	MUX_CONFG_CAP	CONN_PRESENT_CAP	CONN_ORIENT_CAP
0x2A	CONFIG_EXTENDED1[7:0]	–	–	–	–	–	–	FRS_BIDIR	SRC_FRS_IN
0x2E	MESSAGE_HEADER_INFO[7:0]	–	–	–	CBL_PLG	DATA_ROLE	USB_PD[1:0]		PWR_ROLE
0x2F	RECEIVE_DETECT[7:0]	–	EN_CBL_RST	EN_HRD_RST	EN_SOP_DBG2	EN_SOP_DBG1	EN_SOP2	EN_SOP1	EN_SOP
0x30	RECEIVE_BUFFER[7:0]	RECEIVE_BUFFER[7:0]							
0x50	TRANSMIT[7:0]	–	–	RETRY_COUNTER[1:0]		–	TX_SOP_MESSAGE[2:0]		
0x51	TRANSMIT_BUFFER[7:0]	TRANSMIT_BUFFER[7:0]							
0x70	VBUS_VOLTAGE_L[7:0]	VBUS_VOLTAGE[7:0]							
0x71	VBUS_VOLTAGE_H[7:0]	–	–	–	–	SCALE_FACTOR[1:0]		VBUS_VOLTAGE[9:8]	
0x74	VBUS_STOP_DISCHARGE_THRESHOLD_L[7:0]	VBUS_STOP_DISCH_THRESHOLD[7:0]							

ADDRESS	NAME	MSB							LSB
0x75	VBUS_STOP_DISCHARGE_THRESHOLD_H[7:0]	–	–	–	–	–	–	VBUS_STOP_DISCH_THRESHOLD[9:8]	
0x76	VBUS_VOLTAGE_ALARM_HI_CFG_L[7:0]	VBUS_ALARM_HI_CFG[7:0]							
0x77	VBUS_VOLTAGE_ALARM_HI_CFG_H[7:0]	–	–	–	–	–	–	VBUS_ALARM_HI_CFG[9:8]	
0x78	VBUS_VOLTAGE_ALARM_LO_CFG_L[7:0]	VBUS_ALARM_LO_CFG[7:0]							
0x79	VBUS_VOLTAGE_ALARM_LO_CFG_H[7:0]	–	–	–	–	–	–	VBUS_ALARM_LO_CFG[9:8]	
0x7A	VBUS_NONDEFAULT_TARGET_L[7:0]	VBUS_NONDEFAULT_TARGET_L[7:0]							
0x7B	VBUS_NONDEFAULT_TARGET_H[7:0]	VBUS_NONDEFAULT_TARGET_H[7:0]							
Power, Protection and Legacy USB Registers									
0x80	VBUS_CURRENT[7:0]	VBUS_CURRENT[7:0]							
0x81	CABLE_COMP_CONTROL[7:0]	–	–	GAIN[5:0]					
0x82	VBUS_ILIM_SETUP[7:0]	VBUS_ILIM_SET[7:0]							
0x83	BUCK_BOOST_SETUP[7:0]	SLP[2:0]			FSW[1:0]		SYNC_DIR	SS_SEL[1:0]	
0x84	WATCHDOG_SETUP[7:0]	–	–	–	–	–	–	WD_TIMEOUT[1:0]	
0x85	AUTO_SHIELD_SETUP[7:0]	–	–	–	–	–	–	RETRY_TMR[1:0]	
0x86	GENERAL_SETUP[7:0]	–	VBUS_HIRES	–	EXT_BIAS_SEL	–	CL_EN	AUTO_CDP_DCP_MODE[1:0]	

ADDRESS	NAME	MSB							LSB
0x87	IN_THRESH[7:0]	–	–	–	–	IN_UV_THRESH[3:0]			
0x88	VCONN_THRESH[7:0]	VCONN_OCPL_SEL[3:0]				–	VCONN_IN_UV_THRESH[2:0]		
0x89	VBUS_THRESH[7:0]	–	VBUS_OV_THRESH[2:0]			–	VBUS_UV_THRESH[2:0]		
0x8A	VENDOR_STATUS_MASK[7:0]	SHIELDING_MASK	–	–	–	–	–	–	OMF_TRANS_MASK
0x8B	VENDOR_STATUS[7:0]	SHIELDING	–	–	–	–	–	–	OMF_TRANS
0x8C	AUTO_SHIELD_STATUS_0[7:0]	TSHDN	VCONN_REV_OV	VCONN_OCPL	SHLD_EVENT	VCONN_IN_UV	IN_OC	VDD_USB_UV	VBUS_UV
0x8D	AUTO_SHIELD_STATUS_1[7:0]	CL_CV	CV_ILIM	VBUS_RNA	VBUS_SHT_GND	IN_UV	DATA_OV	HVCC_OV	VDD_USB_OV

Register Details

VENDOR_ID_L (0x0)

Lower 8 Bits of VID. A vendor ID, or VID, is used to identify the TCPC vendor. The VID is a unique 16-bit unsigned integer assigned by USB-IF.

BIT	7	6	5	4	3	2	1	0
Field	VENDOR_ID[7:0]							
Reset	0x6A							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VENDOR_ID	7:0	Lower 8 Bits of Analog Devices VID.	Always reads 0x6A in MAX25432

VENDOR_ID_H (0x1)

Upper 8 Bits of VID.

BIT	7	6	5	4	3	2	1	0

Field	VENDOR_ID[15:8]
Reset	0x0B
Access Type	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VENDOR_ID	7:0	Upper 8 Bits of Analog Devices VID.	Always reads 0x0B in MAX25432

PRODUCT_ID_L (0x2)

Lower 8 Bits of PID. The product ID, or PID, is used to identify the product.

BIT	7	6	5	4	3	2	1	0
Field	PRODUCT_ID[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PRODUCT_ID	7:0	Lower 8 bits of MAX25432's PID	0x01: Buck-Boost Capable 0x02: Buck-Only Capable

PRODUCT_ID_H (0x3)

Upper 8 Bits of PID.

BIT	7	6	5	4	3	2	1	0
Field	PRODUCT_ID[15:8]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PRODUCT_ID	7:0	Upper 8 Bits of MAX25432's PID	Always reads 0x00 in MAX25432

DEVICE_ID_L (0x4)

Lower 8 Bits of bcdDevice. The Device ID, bcdDevice, is used to identify the release version of the product.

BIT	7	6	5	4	3	2	1	0

Field	DEVICE_ID[7:0]
Reset	0x00
Access Type	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DEVICE_ID	7:0	Lower 8 Bits of MAX25432's Device ID.	See *Ordering Information* table

DEVICE_ID_H (0x5)

Upper 8 Bits of Device ID.

BIT	7	6	5	4	3	2	1	0
Field	DEVICE_ID[15:8]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEVICE_ID	7:0	Upper 8 Bits of MAX25432's Device ID.	See *Ordering Information* table

USBTYPEC_REV_L (0x6)

This register refers to USB Type-C Cable and Connector Specification Revision; USB Type-C represented by a unique 16-bit unsigned register. The format is packed binary coded decimal (BCD).

BIT	7	6	5	4	3	2	1	0
Field	TYPEC_REV[7:0]							
Reset	0x13							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
TYPEC_REV	7:0	USB Type-C Revision 1.3	Always reads 0x13 in MAX25432

USBPD_REV_VER_L (0x8)

USBPD_REV_VER[15:8]: Lower 8 Bits

BIT	7	6	5	4	3	2	1	0

Field	PD_VER[7:0]
Reset	0x12
Access Type	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PD_VER	7:0	USB PD Version 1.2	Always reads 0x12 in MAX25432

USBPD_REV_VER_H (0x9)

This register refers to USB PD Specification revision and version represented by a unique 16-bit unsigned integer. The format is packed BCD.

BIT	7	6	5	4	3	2	1	0
Field	PD_REV[7:0]							
Reset	0x30							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PD_REV	7:0	USB PD Revision 3.0	Always reads 0x30 in MAX25432

PD_INTERFACE_REV_L (0xA)

PD_INTERFACE_REV[7:0]: Lower 8 Bits

BIT	7	6	5	4	3	2	1	0
Field	IBS_VER[7:0]							
Reset	0x11							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
IBS_VER	7:0	USB PD Inter-Block Specification Version 1.1	Always reads 0x11 in MAX25432

PD_INTERFACE_REV_H (0xB)

The USB Port Controller Specification Revision register refers to the specification revision and version represented by a unique 16-bit unsigned integer. The format is packed BCD.

BIT	7	6	5	4	3	2	1	0
Field	IBS_REV[7:0]							
Reset	0x20							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
IBS_REV	7:0	USB PD Inter-Block Specification Revision 2.0	Always reads 0x20 in MAX25432

ALERT_L (0x10)

Lower 8 Bits of ALERT Register.
This register is set by TCPC and cleared by TCPM. This register is used to communicate a status change from the TCPC to the TCPM. After an event or condition occurs, the TCPC sets the corresponding bit in the ALERT register. Any unmasked bit that is set in this register will drive the ALERT pin low.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_ALARM_HI	TX_SOP_MSG_SUCC	TX_SOP_MSG_DISCRD	TX_SOP_MSG_FAIL	RX_HARD_RST	RX_SOP_MSG_STAT	PWR_STAT	HVCC_STAT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ALARM_HI	7	V_{BUS} Voltage Alarm Hi	0: Cleared 1: A high-voltage alarm has occurred
TX_SOP_MSG_SUCC	6	Transmit SOP* Message Successful. (MAX25432B only)	0: Cleared 1: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
TX_SOP_MSG_DISCRD	5	Transmit SOP* Message Discarded (MAX25432B only)	0: Cleared 1: Reset or SOP* message transmission not sent due to an incoming receive message. Transmit SOP* message buffer registers are empty.
TX_SOP_MSG_FAIL	4	Transmit SOP* Message Failed. (MAX25432B only)	0: Cleared 1: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.

BITFIELD	BITS	DESCRIPTION	DECODE
RX_HARD_RST	3	Received Hard Reset. (MAX25432B only)	0: Cleared 1: Received Hard Reset message
RX_SOP_MSG_STAT	2	Received SOP* Message Status. (MAX25432B only)	0: Cleared 1: RECEIVE_BUFFER register changed. READABLE_BYTE_COUNT being set to 0 does not set this bit.
PWR_STAT	1	Power Status.	0: Cleared 1: Power Status changed
HVCC_STAT	0	HVCC Status. (MAX25432B only)	0: Cleared 1: HVCC Status changed Set when ROLE_CONTROL.HVCC1[1..0], ROLE_CONTROL.HVCC2[1..0], HVCC_STATUS.HVCC1_STATE[1..0] or HVCC_STATUS.HVCC2_STATE[1..0] has changed. The MAX25432B does not assert this bit when HVCC_STATUS.LOOKING4CONN changes state if TCPC_CONTROL.EN_LK4CONN_ALRT is set to 0.

ALERT_H (0x11)

Upper 8 Bits of ALERT Register.
This register is set by TCPC and cleared by TCPM. This register is used to communicate a status change from the TCPC to the TCPM. After an event or condition occurs, the TCPC sets the corresponding bit in the ALERT register. Any unmasked bit that is set in this register will drive the ALERT pin low.

BIT	7	6	5	4	3	2	1	0
Field	VNDR_ALRT	ALRT_EXTND	EXTND_STAT	BEG_SOP_MSG_STAT	VBUS_SNK_DISC_DET	RX_BUFF_OVRFL	FAULT_STAT	VBUS_ALARM_LO
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Read Only	Write 1 to Clear, Read	Read Only	Read Only	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VNDR_ALRT	7	Vendor-Defined Alert	0: Cleared 1: A vendor-defined alert has been detected. Defined in the VENDOR_DEFINED registers starting at address 0x80. This bit can be cleared, regardless of the current status of the alert source.

BITFIELD	BITS	DESCRIPTION	DECODE
ALRT_EXTND	6	Alert Extended. (Reserved)	Always reads 0 (Extended Alerts not supported)
EXTND_STAT	5	Extended Status.	0: Cleared 1: Extended Status changed
BEG_SOP_MSG_STAT	4	Beginning SOP* Message Status. (MAX25432B only)	Always reads 0 (Extended messaging not supported)
VBUS_SNK_DISC_DET	3	V_{BUS} Sink Disconnect Detected. (MAX25432B only)	Always reads 0 (Source-only)
RX_BUFF_OVRFL	2	Rx Buffer Overflow. (MAX25432B only)	0: TCPC Rx buffer is functioning properly. 1: TCPC Rx buffer has overflowed. Future GoodCRC shall not be sent. This bit is cleared when the TCPM writes a 1 to it and a 1 to ALERT.RX_SOP_MSG_STAT.
FAULT_STAT	1	Fault Status.	0: No fault 1: A fault has occurred. Read the FAULT_STATUS register.
VBUS_ALARM_LO	0	V_{BUS} Voltage Alarm Lo.	0: Cleared 1: A low-voltage alarm has occurred.

ALERT_MASK_L (0x12)

Lower 8 Bits of ALERT_MASK Register.
The registers in this section define the masks that may be set for the ALERT registers. A masked register will still indicate in the ALERT register, but will not set the ALERT pin low.
This register will be reset to its default value when a Hard Reset is sent; or a Hard Reset is received (if Hard Reset detection is enabled).

BIT	7	6	5	4	3	2	1	0
Field	MSK_VBUS_V_ALRM_HI	MSK_TX_SOP_MSG_SUCC	MSK_TX_SOP_MSG_DISCRD	MSK_TX_SOP_MSG_FAIL	MSK_RX_HARD_RST	MSK_RX_SOP_MSG_STAT	MSK_PWR_STAT	MSK_HVCC_STAT
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_VBUS_V_ALRM_HI	7	V_{BUS} Voltage Alarm Hi Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_TX_SOP_MSG_SUCC	6	Transmit SOP* Message Successful Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_TX_SOP_MSG_DISCRD	5	Transmit SOP* Message Discarded Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_TX_SOP_MSG_FAIL	4	Transmit SOP* Message Failed Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_RX_HARD_RST	3	Received Hard Reset Message Status Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_RX_SOP_MSG_STAT	2	Receive SOP* Message Status Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_PWR_STAT	1	Power Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_HVCC_STAT	0	CC Status Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked

ALERT_MASK_H (0x13)

Upper 8 Bits of ALERT_MASK Register.
The registers in this section define the masks that may be set for the ALERT registers. A masked register will still indicate in the ALERT register, but will not set the ALERT pin low.
This register will be reset to its default value when a Hard Reset is sent; or a Hard Reset is received (if Hard Reset detection is enabled).

BIT	7	6	5	4	3	2	1	0
Field	MSK_VNDR_ALRT	MSK_ALRT_EXTND	MSK_EXTND_STAT	MSK_BEG_SOP_MSG_STAT	MSK_VBUS_SNK_DISC_DET	MSK_RX_BUFF_OVRFL	MSK_FAULT_STAT	MSK_VBUS_V_ALRM_LO
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_VNDR_ALRT	7	Vendor-Defined Alert Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_ALRT_EXTND	6	Alert Extended Interrupt Mask. (Reserved)	Writes are not applicable (Alert Extended not supported)
MSK_EXTND_STAT	5	Extended Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_BEG_SOP_MSG_STAT	4	Beginning SOP* Message Status Interrupt Mask. (Reserved)	Writes are not applicable (Extended messaging not supported)
MSK_VBUS_SNK_DISC_DET	3	V_{BUS} Sink Disconnect Detected Interrupt Mask. (Reserved)	Writes are not applicable (source only)
MSK_RX_BUFF_OVRFL	2	Rx Buffer Overflow Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_FAULT_STAT	1	Fault Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_VBUS_V_ALRM_LO	0	V_{BUS} Voltage Alarm Lo Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked

POWER_STATUS_MASK (0x14)

Event Interrupt Mask. It is masked and unmasked by the TCPM. This register allows individual masking of power events.
The assertion of the ALERT pin is prevented when the corresponding bit is set to zero by the TCPM.
This register will be reset to its default value when a Hard Reset is sent; or a Hard Reset is received (if Hard Reset detection is enabled).

BIT	7	6	5	4	3	2	1	0
Field	MSK_DEBG_ACC_CONN_STAT	MSK_TCPC_INIT_STAT	MSK_SRC_NON_DEF_VOLT_STAT	MSK_SRC_VBUS_STAT	MSK_VBUS_DET_STAT	MSK_VBUS_PRSN_STAT	MSK_VCONN_PRSN_STAT	MSK_SNK_VBUS_STAT
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_DEBG_ACC_CONN_STAT	7	Debug Accessory Connected Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_TCPC_INIT_STAT	6	MAX25432 Initialization Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_SRC_NON_DEF_VOLT_STAT	5	Sourcing High-Voltage Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_SRC_VBUS_STAT	4	Sourcing VBUS Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_VBUS_DET_STAT	3	V_{BUS} Detection Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_VBUS_PRSN_STAT	2	V_{BUS} Present Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_VCONN_PRSN_STAT	1	V_{CONN} Present Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_SNK_VBUS_STAT	0	Sinking V_{BUS} Status Interrupt Mask. (Reserved)	Writes are not applicable (Force off V_{BUS} not supported)

FAULT_STATUS_MASK (0x15)

Event Interrupt Mask. It is masked and unmasked by the TCPM. This register allows individual masking of fault events. The assertion of the ALERT pin is prevented when the corresponding bit is set to zero by the TCPM.

BIT	7	6	5	4	3	2	1	0
Field	MSK_All_REG_RST	MSK_FORCD_OFF_VBUS	MSK_AUTO_DISCH_FAIL	MSK_FORC_DISCH_FAIL	MSK_VBUS_OCP	MSK_VBUS_OVP	MSK_VCONN_OCP	MSK_I2C_ERR
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_All_REG_RST	7	All Registers Reset to Default Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_FORCD_OFF_VBUS	6	Force Off V_{BUS} Interrupt Status Mask. (Reserved)	Writes are not applicable (Force off V_{BUS} not supported)
MSK_AUTO_DISCH_FAIL	5	Auto Discharge Failed Interrupt Mask. (MAX25432B only)	0: Interrupt masked 1: Interrupt unmasked

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_FORC_DISCH_FAIL	4	Force Discharge Failed Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_VBUS_OCP	3	V_{BUS} Overcurrent Protection Fault Interrupt Status Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_VBUS_OVP	2	V_{BUS} Overvoltage Protection Fault Interrupt Status Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_VCONN_OCP	1	V_{CONN} Overcurrent Fault Interrupt Status Mask.	0: Interrupt masked 1: Interrupt unmasked
MSK_I2C_ERR	0	I^2C Interface Error Interrupt Status Mask.	0: Interrupt masked 1: Interrupt unmasked

EXTENDED_STATUS_MASK (0x16)

Event Interrupt Mask. It is masked and unmasked by the TCPM.
The assertion of the ALERT pin is prevented when the corresponding bit is set to zero by the TCPM.
Bits[7:1] are reserved and ignored by TCPC.
This register will be reset to its default value when a Hard Reset is sent; or a Hard Reset is received (if Hard Reset detection is enabled).

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MSK_VSAFE0V
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_VSAFE0V	0	vSafe0V Status Interrupt Mask.	0: Interrupt masked 1: Interrupt unmasked

ALERT_EXTENDED_MASK (0x17)

Event Interrupt Mask. It is masked and unmasked by the TCPM.
The assertion of the ALERT pin is prevented when the corresponding bit is set to zero by the TCPM.
Bits[7:3] are reserved and ignored by TCPC.
This register will be reset to its default value when a Hard Reset is sent; or a Hard Reset is received (if Hard Reset detection is enabled).

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MSK_TMR_EXP	MSK_SRC_FST_RSWP	MSK_SNK_FST_RSWP

Reset	–	–	–	–	–	0b1	0b1	0b1
Access Type	–	–	–	–	–	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_TMR_EXP	2	Timer Expired Interrupt Mask. (Reserved)	Writes are not applicable (Generic Timer not supported)
MSK_SRC_FST_RSWP	1	Source Fast Role Swap Interrupt Mask. (Reserved)	Writes are not applicable (Fast Role Swap not supported)
MSK_SNK_FST_RSWP	0	Sink Fast Role Swap Interrupt Mask. (Reserved)	Writes are not applicable (source only)

TCPC_CONTROL (0x19)

After the TCPC has set the POR default values, this register is set and cleared only by the TCPM.

BIT	7	6	5	4	3	2	1	0
Field	EN_SMB_PEC	EN_LK4CONN_ALRT	EN_WD_TMR	DBG_ACC_CNTRL	I2C_CLK_STRCH[1:0]		BIST_TM	PLUG_ORNT
Reset	0b0	0b0	0b0	0b0	0b00		0b0	0b0
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Read Only		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_SMB_PEC	7	Enable SMBus PEC. (Reserved)	Writes are ignored and always reads 0 (SMBus PEC not supported)
EN_LK4CONN_ALRT	6	Enable Looking4Connection Alert. (MAX25432B only)	0: Disable ALERT_L.HVCC_STAT assertion when HVCC_STATUS.LOOKING4CONN changes (default). 1: Enable ALERT_L.HVCC_STAT assertion when HVCC_STATUS.LOOKING4CONN changes.
EN_WD_TMR	5	Enable Watchdog Timer.	0: Watchdog Timer is disabled (default). 1: Watchdog Timer is enabled. See the *Watchdog Timer* section for more information.
DBG_ACC_CNTRL	4	Debug Accessory Control. (MAX25432B only)	0: Disabled (power on default) 1: Controlled by TCPM
I2C_CLK_STRCH	3:2	I²C Clock Stretching Control. (Reserved)	Writes are ignored and always reads 0 (I²C Clock Stretching not supported)

BITFIELD	BITS	DESCRIPTION	DECODE
BIST_TM	1	BIST Test Mode. (MAX25432B only) Setting this bit to 1 is intended to be used only when a USB compliance tester is using USB BIST test data to test the PHY layer of the TCPC. The TCPM should clear this bit when a disconnect is detected.	0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert. The TCPM can mask or ignore received message alerts when this bit is set to 1 since the TCPC may or may not assert the alert. The TCPM may also treat received messages in this mode in the same way as received messages during normal operation.
PLUG_ORNT	0	Plug Orientation.	0: When V_{CONN} is enabled, apply it to the CC2 pin. MAX25432B only: The MAX25432B monitors the CC1 pin for BMC communications if PD message delivery is enabled. 1: When V_{CONN} is enabled, apply it to the CC1 pin. MAX25432B only: The MAX25432B monitors the CC2 pin for BMC communications if PD message delivery is enabled. **Note:** The V_{BUS} Auto Discharge Disconnect function uses PLUG_ORNT to detect a disconnect on the correct HVCC pin. Therefore PLUG_ORNT needs to be set to the correct value by the TCPM before enabling the Auto Discharge Disconnect.

ROLE_CONTROL (0x1A)

After the TCPC has set the POR default values, this register is set and cleared only by the TCPM. The TCPM writes to this register to configure the CC pullup (Rp) current sources. The TCPM can write to this register as early as when MAX25432B enters the HVCC Discharge state (see the *Power-Up Sequence* diagram). An example for this situation would be to keep the current sources disabled until the TCPM is ready.

Since the CC current sources are on the low-voltage side (CC pins), the pullups will be seen on the HVCC pins when the CC pass-through switches are closed. Note that certain faults can cause the switches to open. See the *Fault Types* table.

BIT	7	6	5	4	3	2	1	0
Field	–	DRP	RP_VAL[1:0]		HVCC2[1:0]		HVCC1[1:0]	
Reset	–	0b0	0b10		0b01		0b01	
Access Type	–	Read Only	Write, Read		Write, Read, Dual		Write, Read, Dual	

BITFIELD	BITS	DESCRIPTION	DECODE
DRP	6	DRP. (Reserved)	Writes are ignored and always reads 0 (DRP toggle not supported) Note: MAX25432BATLP when using ADI TCPM can implement DRP to satisfy Alternate Mode requirements to negotiate UFP_U for DisplayPort. Contact Factory for details.
RP_VAL	5:4	Rp Value Setting. (MAX25432B only)	00: Rp default 01: Rp 1.5A 10: Rp 3.0A 11: Reserved
HVCC2	3:2	HVCC2 Control. (MAX25432B only)	00: Reserved 01: Rp 10: Reserved 11: Open (disconnect or don't care)
HVCC1	1:0	HVCC1 Control. (MAX25432B only)	00: Reserved 01: Rp 10: Reserved 11: Open (disconnect or don't care)

FAULT_CONTROL (0x1B)

After the TCPC has set the POR default values, this register is set and cleared only by the TCPM. The TCPM writes to FAULT_CONTROL to enable/disable detection of certain faults.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FRC_OFF_VBUS_DIS	VBUS_DISCH_FLT_DET_TMR_EN	VBUS_OCP_DET_EN	VBUS_OVP_DET_EN	VCONN_OCP_DET_EN
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FRC_OFF_VBUS_DIS	4	Force Off V_{BUS}. (Reserved)	Writes are ignored and always reads 0b (force off V_{BUS} control not supported)
VBUS_DISCH_FLT_DET_TMR_EN	3	V_{BUS} Discharge Fault Detection Timer Enable.	0: Enable 1: Disable This enables the timers for both FAULT_STATUS.AUTO_DISCH_FAIL and FAULT_STATUS.FORCE_DISCH_FAIL.

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_OCP_DET_EN	2	V_{BUS} Overcurrent Protection Enable.	0: Enable 1: Disable
VBUS_OVP_DET_EN	1	V_{BUS} Overvoltage Protection Enable.	0: Enable 1: Disable
VCONN_OCP_DET_EN	0	V_{CONN} Overcurrent Protection Enable.	0: Enable 1: Disable

POWER_CONTROL (0x1C)

After the TCPC has set the POR default values, this register is set and cleared by the TCPM.
The timing parameters for the TCPM in conjunction with the TCPC must meet the USB PD requirements.
The TCPM reads the HVCC_STATUS, POWER_STATUS and optionally the VBUS_VOLTAGE registers to determine the connection state and the orientation of a USB Type-C port.
The TCPM shall take the following steps to request sourcing V_{CONN} over one of the HVCC pins:
1. The TCPM shall write to TCPC_CONTROL.PLUG_ORNT to inform TCPC which HVCC pin (not connected through the cable) is repurposed as V_{CONN}.
2. The TCPM shall set POWER_CONTROL.EN_VCONN = 1b.
The TCPC will then source V_{CONN} as TCPM requested irrespective of the status of V_{BUS} and the HVCC1, HVCC2 pins.
The TCPC will not autonomously disable V_{CONN} sourcing when V_{BUS} is removed, or the HVCC1, HVCC2 status has changed. The TCPM shall set POWER_CONTROL.EN_VCONN = 0b to request disabling V_{CONN} sourcing.
This register's write access is blocked during a Fault Action A. The I^2C controller's write transactions will be taken into account after the Fault A is removed.

BIT	7	6	5	4	3	2	1	0
Field	FAST_RSWP_EN	VBUS_VOLT_MON_EN	VOLT_ALRMS_EN	AUTO_DISCH_DISC_EN	BLED_DISCH_EN	FORC_DISCH_EN	VCONN_PWR_SUPP	EN_VCONN
Reset	0b0	0b1	0b1	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION	DECODE
FAST_RSWP_EN	7	Fast Role Swap Enable. (Reserved)	Writes are ignored and always reads 0 in MAX25432 (Fast Role Swap not supported)
VBUS_VOLT_MON_EN	6	VBUS_VOLTAGE and VBUS_CURRENT Monitor.	0: Enables V_{BUS} Voltage and Current Monitoring (ADC). 1: Disables V_{BUS} Voltage and Current Monitoring (default).
VOLT_ALRMS_EN	5	Disable V_{BUS} Voltage Alarms.	0: Enables V_{BUS} Voltage Alarms Power status reporting. V_{BUS} ADC must be enabled when using Voltage

BITFIELD	BITS	DESCRIPTION	DECODE
			Alarms 1: Disables V_{BUS} Voltage Alarms Power status reporting (default).
AUTO_DISCH_DISC_EN	4	Auto-Discharge Disconnect. (MAX25432B only)	0: Disabled (default) 1: Enabled When enabled, the MAX25432B automatically disables sourcing V_{BUS} then discharges V_{BUS} when a disconnect is detected. A disconnect is defined as HVCC1_STATE or HVCC2_STATE register value being equal to 00b ("Open"), with PLUG_ORNT set to 0b or 1b, respectively. Therefore, PLUG_ORNT must be set to the correct value before enabling the V_{BUS} Auto Discharge Disconnect function.
BLED_DISCH_EN	3	Enable Bleed Discharge. (Reserved)	Writes are ignored and always reads 0 in MAX25432 (Bleed Discharge not supported).
FORC_DISCH_EN	2	V_{BUS} Force Discharge.	0: Disable 1: Enable
VCONN_PWR_SUPP	1	V_{CONN} Power Supported.	0: Deliver up to 1W. 1: Deliver at least the power indicated in DEVICE_CAPABILITIES.VCONN_PWR_CAP. Writing to this register has no effect in the MAX25432. Actual wattage is dependent on the VCONN_THRESH.VCONN_OCPL_SEL threshold and V_{CONN} pin voltage.
EN_VCONN	0	Enable V_{CONN}.	0: Disable V_{CONN} source (default). 1: Enable V_{CONN} source. Enabling V_{CONN} will cause the corresponding HVCC_STAT to go to 00b (Open). The MAX25432 autonomously disables V_{CONN} by clearing EN_VCONN when SHIELDING is active.

HVCC_STATUS (0x1D)

This register is set and cleared by the TCPC. The TCPC indicates the current HVCC state in this register. Connection result (CONN_RSLT) is not supported as MAX25432B is source only. The TCPC will update the HVCC_STATUS register within tSetReg (50µs, max) of a change on the HVCC1 or HVCC2 pins, after tTCPCfilter debounce (375µs, typ). The TCPM shall read the HVCC1_STATE and HVCC2_STATE to determine the state of the HVCC1 and HVCC2 pins. The TCPM reads this register upon detecting the ALERT pin being asserted and seeing ALERT_L.HVCC_STAT = 1b. The HVCC status reporting is disabled when ROLE_CONTROL.HVCC1 = ROLE_CONTROL.HVCC2 = 11b (Open). When the HVCC status reporting is disabled, the HVCC_STATUS register will be set to all zeros. Disabling the HVCC status reporting will not cause a change to the ALERT registers.

BIT	7	6	5	4	3	2	1	0

Field	–	–	LOOKING4CONN	CONN_RSLT	HVCC2_STATE[1:0]	HVCC1_STATE[1:0]
Reset	–	–	0b0	0b0	0b00	0b00
Access Type	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LOOKING4CONN	5	Looking4Connection. (MAX25432B only)	0: MAX25432B is not actively looking for a connection. 1: MAX25432B is looking for a connection. A transition from 1 to 0 indicates a potential connection has been found.
CONN_RSLT	4	ConnectResult. (Reserved)	Always reads 0 in MAX25432 (source only)
HVCC2_STATE	3:2	HVCC2 State. (MAX25432B only)	00: SRC.Open (Open, Rp) 01: SRC.Ra (below maximum vRa) 10: SRC.Rd (within the vRd range) 11: Reserved Note: Ra and Rd are reported to this register only when GDRV=H. This is to avoid incorrect status reporting when cable ground/shield is floating. Note that Ra/Open on the CC lines will be reported as Open/Open if LOOKING4CONN = H, which is the case when just an E-marked cable is connected but with no Type-C device plugged-in.
HVCC1_STATE	1:0	HVCC1 State. (MAX25432B only)	00: SRC.Open (Open, Rp) 01: SRC.Ra (below maximum vRa) 10: SRC.Rd (within the vRd range) 11: Reserved Note: Ra and Rd are reported to this register only when GDRV=H. This is to avoid incorrect status reporting when cable ground/shield is floating. Note that Ra/Open on the CC lines will be reported as Open/Open if LOOKING4CONN = H, which is the case when just an E-marked cable is connected but with no Type-C device plugged-in.

POWER_STATUS (0x1E)

This register is set and cleared by the TCPC. The TCPM reads this register upon detecting an ALERT and reading the ALERT_L.PWR_STAT bit set to 1. The TCPC indicates the current Power Status in this register.

BIT	7	6	5	4	3	2	1	0
Field	DBG_ACC_STAT	INIT_STAT	SRC_NON_DEF_VOLT	SRC_VBUS	VBUS_DET_EN	VBUS_PRESENT	VCONN_PRESENT	SNK_VBUS
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b0	0b0

Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DBG_ACC_STAT	7	Debug Accessory Status.	0: No debug accessory connected (default) 1: Debug accessory connected
INIT_STAT	6	MAX25432 Initialization Status.	0: The MAX25432 has completed initialization and all registers are valid. 1: The MAX25432 is still performing internal initialization and the only registers that are guaranteed to return the correct values are 0x00...0x0B.
SRC_NON_DEF_VOLT	5	Sourcing Non-Default V_{BUS} Voltage.	0: Sourcing vSafe5V voltage on V_{BUS} 1: Sourcing non-default voltage on V_{BUS} This bit is asserted as long as the MAX25432 is sourcing. Non-default voltage over V_{BUS} (i.e., not vSafe5V) as a response to TCPM sending the SourceVbusNondefaultVoltage command. This bit is not valid if POWER_STATUS.SRC_VBUS = 0.
SRC_VBUS	4	Sourcing V_{BUS}.	0: The MAX25432 is not sourcing V_{BUS}. 1: The MAX25432 is sourcing V_{BUS}.
VBUS_DET_EN	3	V_{BUS} Detection Enabled.	0: V_{BUS} detection disabled 1: V_{BUS} detection enabled (default) Indicates the V_{BUS} Present and vSafe0V comparators are enabled. See V_{BUS} Present and vSafe0V Comparator sections.
VBUS_PRESENT	2	V_{BUS} Present Status.	0: V_{BUS} is not present (below 4V). 1: V_{BUS} is present (4V or above).
VCONN_PRESENT	1	V_{CONN} Present Status.	0: V_{CONN} is not present. 1: This bit is asserted whenever V_{CONN} is present on HVCC1 or HVCC2.
SNK_VBUS	0	Sinking V_{BUS} Status. (Reserved)	Always reads 0 in MAX25432 (source only)

FAULT_STATUS (0x1F)

This register is set by TCPC and cleared by TCPM. The TCPM reads this register upon detecting an ALERT and reading the ALERT_H.FAULT_STAT bit set to 1. The TCPC indicates the current fault status in this register.

BIT	7	6	5	4	3	2	1	0
Field	ALL_REG_RST	FORCD_OFF_VBUS	AUTO_DISCH_FAIL	FORCE_DISCH_FAIL	VBUS_OCP_FAULT	VBUS_OVP_FAULT	VCONN_OCP_FAULT	I2C_ERR

Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ALL_REG_RST	7	All Registers Reset to Default.	0: Registers have not been reset to their default values. 1: All registers have been initialized to their default values. This bit is asserted when the MAX25432 resets all registers to their default value. This happens at initial power-up or if an unexpected power reset occurs.
FORCD_OFF_VBUS	6	Force Off V_{BUS}. (Reserved)	Writes are ignored and always reads 0 in the MAX25432 (force off V_{BUS} not supported)
AUTO_DISCH_FAIL	5	V_{BUS} Auto-Discharge Failed. (MAX25432B only)	0: No fault 1: V_{BUS} Auto-Discharge commanded by the TCPM failed
FORCE_DISCH_FAIL	4	V_{BUS} Force Discharge Failed.	0: No fault 1: V_{BUS} Force Discharge commanded by the TCPM failed
VBUS_OCP_FAULT	3	V_{BUS} Overcurrent Protection Fault.	0: No fault 1: Fault detected
VBUS_OVP_FAULT	2	V_{BUS} Overvoltage Protection Fault.	0: No fault 1: Fault detected
VCONN_OCP_FAULT	1	V_{CONN} Overcurrent Protection Fault.	0: No fault 1: Fault detected
I2C_ERR	0	I^2C Interface Error.	0: No error 1: An I^2C error has occurred The following conditions will cause the MAX25432 to assert this bit: • The watchdog timer has expired • Writing SourceVbusDefault command while not sourcing V_{BUS} and a pre-bias exists on V_{BUS} that cannot be discharged • Writing SourceVbusNonDefault command while not sourcing V_{BUS} • Writing DisableVbusDetect command while sourcing V_{BUS} (V_{BUS} needs to be disabled first to turn off V_{BUS} present detection) • Writing SendFRSwapSignal command

BITFIELD	BITS	DESCRIPTION	DECODE
			• Writing to CONFIG_EXTENDED1.FRS_BIDIR • Writing to the TRANSMIT register requesting a transmission that is not Hard Reset, Cable Reset, or BIST Carrier Mode 2 and there are less than 2 bytes in the TX_BUF_BYTE_x register (MAX25432B only) • Connected_Invalid_State: This TCPC state is entered when disabling Rp on active CC with Auto Discharge set to 1 and not in Debug Accessory mode. The MAX25432 will not assert I2C_ERR in the following conditions: • Reading or writing to an address that is not the first byte of a multibyte register (e.g., VBUS_NONDEFAULT_TARGET_H[7:0]) • Reading or writing to multiple registers in one transaction • Writing SourceVbusDefault command while sourcing V_{BUS} default voltage. • Writing WakeI2C or I^2C Idle commands • Reading the last COMMAND (always returns 0) • Writing to a nondefined register

EXTENDED_STATUS (0x20)

This register is set and cleared by the TCPC. The TCPM reads this register upon detecting an ALERT and reading the ALERT_H.EXTND_STAT bit set to 1.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VSAFE0V
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
VSAFE0V	0	0: V_{BUS} is above vSafe0V. 1: V_{BUS} is at or below vSafe0V. The MAX25432 will report V_{BUS} is at or below vSafe0V when the OUT pin is below 0.8V (typ). This bit is not valid when POWER_STATUS.VBUS_DET_EN = 0.

ALERT_EXTENDED (0x21)

This register has no effect on MAX25432.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TMR_EXP	SRC_FST_RSWP	SNK_FST_RSWP
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TMR_EXP	2	Generic Timer Expired. (Reserved)	Writes are ignored and always reads 0 (generic timer not supported)
SRC_FST_RSWP	1	Source Fast Role Swap. (Reserved)	Writes are ignored and always reads 0 (Fast Role Swap not supported)
SNK_FST_RSWP	0	Sink Fast Role Swap. (Reserved)	Writes are ignored and always reads 0 (source only)

COMMAND (0x23)

Commands are issued and written by the TCPM. The COMMAND register is cleared by the TCPC after being acted upon.

BIT	7	6	5	4	3	2	1	0
Field	COMMAND[7:0]							
Reset	0x00							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
COMMAND	7:0	List of supported commands: 0x22 **DisableVbusDetect**: Disables V_{BUS} present and vSafe0V detection. 0x33 **EnableVbusDetect**: Enables V_{BUS} present and vSafe0V detection. 0x66 **DisableSourceVbus**: Disables sourcing of V_{BUS}. This command does not disable V_{BUS} present detection. 0x77 **SourceVbusDefaultVoltage**: Enables sourcing vSafe5V over V_{BUS} and enables V_{BUS} present detection by setting POWER_STATUS.VBUS_DET_EN = 1. The MAX25432 will transition to vSafe5V if sourcing non-default voltage. 0x88 **SourceVbusNonDefaultVoltage**: Sets V_{BUS} to a non-default voltage target. This is an invalid command when not already sourcing V_{BUS}. 0x99 **Look4Connection** (MAX25432B only): The TCPC restarts connection detection. This command is ignored when HVCC1 and HVCC2 in ROLE CONTROL register are not the same value. 0xAA **RxOneMore** (MAX25432B only): Configures the TCPC to automatically clear the RECEIVE_DETECT register after sending the next GoodCRC. This is used to

BITFIELD	BITS	DESCRIPTION
		disable message passing at a known point regardless of message separation or the depth of the RECEIVE_BUFFER in the TCPC. 0xDD **ResetTransmitBuffer** (MAX25432B only): The TCPC resets the pointer of the TRANSMIT_BUFFER register to offset 1 and the contents of TRANSMIT_BUFFER becomes invalid when this command is issued by the TCPM. 0xEE **ResetReceiveBuffer** (MAX25432B only): The TCPC resets the pointer of RECEIVE_BUFFER to 1 when this command is issued by the TCPM. TCPC does not clear the content of the buffer upon receiving this command. The TCPM issues this command in order to re-read the RECEIVE_BUFFER.RX_BUF_BYTE_x. List of unsupported commands: 0x11 WakeI2C - No action 0x44 DisableSinkVbus - No action 0x55 SinkVbus - No action 0xCC SendFRSwapSignal - Asserts I2C_ERR 0xFF I2C Idle - No action

DEVICE_CAPABILITIES_1_L (0x24)

This register is in the nonvolatile memory of the TCPC. This register describes features supported by the TCPC.

BIT	7	6	5	4	3	2	1	0
Field	PWR_ROLE_CAP[2:0]			SOP_DBG_CAP	SRC_VCONN_CAP	SNK_VBUS_CAP	SRC_HI_VBUS_CAP	SRC_VBUS_CAP
Reset	0b001			0b1	0b1	0b0	0b1	0b1
Access Type	Read Only			Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PWR_ROLE_CAP	7:5	Power Roles Supported.	001: Source only. Rp 3.0A, 1.5A, and default indicated in DEVICE_CAPABILITIES_1_H.SRC_RES_SUP_CAP (MAX25432B) 111: Source only with no Type-C port controller (MAX25432A)
SOP_DBG_CAP	4	SOP'_DBG/SOP"_DBG Support. (MAX25432B only)	1: All SOP* messages including SOP’_DBG/SOP”_DBG are supported
SRC_VCONN_CAP	3	Source V_{CONN} Capability.	1: The MAX25432 is capable of sourcing V_{CONN} through its switch.
SNK_VBUS_CAP	2	Sink V_{BUS} Capability.	0: The MAX25432 is not capable of controlling the sink path to the system load (source only).
SRC_HI_VBUS_CAP	1	Source Non-Default V_{BUS} Capability.	1: The MAX25432 is capable of sourcing non-default voltages on V_{BUS}.
SRC_VBUS_CAP	0	Source V_{BUS} Capability.	1: The MAX25432 is capable of controlling the source path to V_{BUS}.

DEVICE_CAPABILITIES_1_H (0x25)

This register is in the nonvolatile memory of the TCPC. This register describes features supported by the TCPC.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_NONDEF_TRGT_CAP	VBUS_OCP_RPT_CAP	VBUS_OVP_RPT_CAP	BLEED_DISCH_CAP	FORCE_DISCH_CAP	VBUS_MEAS_ALRM_CAP	SRC_RES_SUP_CAP[1:0]	
Reset	0b1	0b1	0b1	0b0	0b1	0b1	0b10	
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_NONDEF_TRGT_CAP	7	V_{BUS} Non-Default Target Capability.	1: VBUS_NONDEFAULT_TARGET register supported
VBUS_OCP_RPT_CAP	6	V_{BUS} OCP Reporting Capability.	1: Supported
VBUS_OVP_RPT_CAP	5	V_{BUS} OVP Reporting Capability.	1: Supported
BLEED_DISCH_CAP	4	Bleed Discharge Capability.	0: Not supported
FORCE_DISCH_CAP	3	Force Discharge Capability.	1: Supported
VBUS_MEAS_ALRM_CAP	2	V_{BUS} Measurement and Alarm Capabilities.	1: Supported
SRC_RES_SUP_CAP	1:0	Source Resistor Supported.	10: Rp 3.0A, 1.5A, and default on the MAX25432B 11: Not supported on the MAX25432A

DEVICE_CAPABILITIES_2_L (0x26)

This register is in the nonvolatile memory of the TCPC. This register describes features supported by the TCPC.

BIT	7	6	5	4	3	2	1	0
Field	SNK_DISC_DET_CAP	STP_DISCH_THR_CAP	VBUS_VOLT_ALRM_LSB_CAP[1:0]		VCONN_PWR_CAP[2:0]			VCONN_OCP_CAP
Reset	0b0	0b1	0b00		0b001			0b1
Access Type	Read Only	Read Only	Read Only		Read Only			Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SNK_DISC_DET_CAP	7	Sink Disconnect Detection Capability.	0: VBUS_SINK_DISCONNECT_THRESHOLD not supported (source only)
STP_DISCH_THR_CAP	6	V_{BUS} Stop Discharge Threshold Capability.	1: VBUS_STOP_DISCHARGE_THRESHOLD supported
VBUS_VOLT_ALRM_LSB_CAP	5:4	V_{BUS} Voltage Alarm LSB Capability.	00: MAX25432 has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG.
VCONN_PWR_CAP	3:1	V_{CONN} Power Supported.	001: Up to 1.5W (programmable)
VCONN_OCP_CAP	0	V_{CONN} Overcurrent Fault Capability.	1: Supported

DEVICE_CAPABILITIES_2_H (0x27)

This register is in the nonvolatile memory of the TCPC. This register describes features supported by the TCPC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	GENERIC_TMR_CAP	LONG_MSG_CAP	SMB_PEC_CAP	SRC_FRS_CAP	SNK_FRS_CAP	WDOG_TMR_CAP
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
GENERIC_TMR_CAP	5	Generic Timer Capability.	0: Not supported
LONG_MSG_CAP	4	Long Message Capability.	0: Long messages (264 bytes) not supported. The MAX25432B supports up to 30 bytes content of the SOP* message.
SMB_PEC_CAP	3	SMBus PEC Capability.	0: Not supported
SRC_FRS_CAP	2	Source FR Swap Capability.	0: Not supported
SNK_FRS_CAP	1	Sink FR Swap Capability.	0: Not supported
WDOG_TMR_CAP	0	Watchdog Timer Capability.	1: Supported

STANDARD_INPUT_CAPABILITIES (0x28)

This register is in the nonvolatile memory of the TCPC. MAX25432 does not support any standard inputs.

BIT	7	6	5	4	3	2	1	0

Field	–	–	–	SRC_FRS_INP_CAP[1:0]	VBUS_EXT_OVP_CAP	VBUS_EXT_OCP_CAP	FRC_OFF_VBUS_CAP
Reset	–	–	–	0b00	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_FRS_INP_CAP	4:3	Source Fast Role Swap Standard Input Capability.	00: Not supported
VBUS_EXT_OVP_CAP	2	V_{BUS} External Overvoltage Fault Standard Input Capability.	0: Not supported
VBUS_EXT_OCP_CAP	1	V_{BUS} External Overcurrent Fault Standard Input Capability.	0: Not supported
FRC_OFF_VBUS_CAP	0	Force Off V_{BUS} Standard Input Capability.	0: Not supported

STANDARD_OUTPUT_CAPABILITIES (0x29)

This register is in the nonvolatile memory of the TCPC. MAX25432 does not support any standard outputs.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_SNK_DIS_DET_CAP	DBG_ACC_CAP	VBUS_PRESENT_CAP	AUD_ACC_CAP	ACT_CBL_CAP	MUX_CONFG_CAP	CONN_PRESENT_CAP	CONN_ORIENT_CAP
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_SNK_DIS_DET_CAP	7	V_{BUS} Sink Disconnect Detect Standard Output Capability.	0: Not supported
DBG_ACC_CAP	6	Debug Accessory Standard Output Capability.	0: Not supported
VBUS_PRESENT_CAP	5	V_{BUS} Present Monitor Standard Output Capability.	0: Not supported
AUD_ACC_CAP	4	Audio Adapter Accessory Standard Output Capability.	0: Not supported
ACT_CBL_CAP	3	Active Cable Indicator Standard Output Capability.	0: Not supported

BITFIELD	BITS	DESCRIPTION	DECODE
MUX_CONFG_CAP	2	MUX Configuration Control Standard Output Capability.	0: Not supported
CONN_PRESENT_CAP	1	Connection Present Standard Output Capability.	0: Not supported
CONN_ORIENT_CAP	0	Connector Orientation Standard Output Capability.	0: Not supported

CONFIG_EXTENDED1 (0x2A)

MAX25432 does not support any extended functions.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	FRS_BIDIR	SRC_FRS_IN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read, Ext	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
FRS_BIDIR	1	Fast Role Swap Bidirectional Pin. (Reserved)	Writes to this bit are ignored and will assert FAULT_STATUS.I2C_ERR. Always reads 0.
SRC_FRS_IN	0	Standard Input Source FR Swap. (Reserved)	Writes are ignored and always reads 0 (Standard Input Source FR Swap not supported)

MESSAGE_HEADER_INFO (0x2E)

The TCPC sets this register at power on. The TCPM may overwrite this register after TCPC initialization is complete. On attach and after implementing the tCCDebounce (100-200ms), the TCPM shall update the MESSAGE_HEADER_INFO Register first before writing to the RECEIVE_DETECT register.
The TCPC reads from this register to generate the Message header for the GoodCRC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	CBL_PLG	DATA_ROLE	USB_PD[1:0]		PWR_ROLE
Reset	–	–	–	0b0	0b1	0b10		0b1
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CBL_PLG	4	Cable Plug. (MAX25432B only)	0: Message originated from source, sink, or dual-role power (DRP) 1: Message originated from a cable plug
DATA_ROLE	3	Data Role. (MAX25432B only)	0: UFP 1: DFP
USB_PD	2:1	USB PD Specification Revision. (MAX25432B only)	00: Revision 1.0 01: Revision 2.0 10: Revision 3.0 11: Reserved
PWR_ROLE	0	Power Role. (MAX25432B only)	0: Sink 1: Source

RECEIVE_DETECT (0x2F)

Set by TCPM, cleared by TCPM (and/or TCPC in some instances).
This register enables detection of certain message types and/or signaling types over the HVCC lines. The TCPC responds to the enabled message type with a GoodCRC if it is a SOP* message, except in the case of a GoodCRC message.
When all bits are set to zero, the TCPC disables automatic transmission of GoodCRC message and discards RxOneMore Command if it has not been acted upon.
The TCPM should not set any bits in this register until it is able to respond. The TCPC will set the RECEIVE_DETECT and the READABLE_BYTE_COUNT registers to all zeros in the following cases: when a Hard Reset is sent; a Hard Reset or Cable Reset is received (if Hard Reset or Cable Reset detection is enabled, respectively); after transmitting GoodCRC due to RxOneMore; on a disconnect detection.

BIT	7	6	5	4	3	2	1	0
Field	–	EN_CBL_RST	EN_HRD_RST	EN_SOP_DBG2	EN_SOP_DBG1	EN_SOP2	EN_SOP1	EN_SOP
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION	DECODE
EN_CBL_RST	6	Enable Cable Reset Detection. (MAX25432B only)	0: Cable Reset detection disabled (default) 1: Cable Reset detection enabled
EN_HRD_RST	5	Enable Hard Reset Detection. (MAX25432B only)	0: Hard Reset detection disabled (default) 1: Hard Reset detection enabled
EN_SOP_DBG2	4	Enable SOP_DBG'' Message. (MAX25432B only)	0: SOP_DBG'' message detection disabled (default) 1: SOP_DBG'' message detection enabled
EN_SOP_DBG1	3	Enable SOP_DBG' Message. (MAX25432B only)	0: SOP_DBG' message detection disabled (default) 1: SOP_DBG' message detection enabled

BITFIELD	BITS	DESCRIPTION	DECODE
EN_SOP2	2	Enable SOP'' Message. (MAX25432B only)	0: SOP'' message detection disabled (default) 1: SOP'' message detection enabled
EN_SOP1	1	Enable SOP' Message. (MAX25432B only)	0: SOP' message detection disabled (default) 1: SOP' message detection enabled
EN_SOP	0	Enable SOP Message. (MAX25432B only)	0: SOP message detection disabled (default) 1: SOP message detection enabled

RECEIVE_BUFFER (0x30)

The RECEIVE_BUFFER comprises of three sets of registers:

-READABLE_BYTE_COUNT
-RX_BUF_FRAME_TYPE
-RX_BUF_BYTE_x

These registers can only be accessed by reading RECEIVE_BUFFER starting at address 0x30. These registers indicate the status of the received SOP* message buffer. These registers shall be read by the TCPM when the TCPC indicates a SOP* message was received in the Alert Status registers.
The TCPM reads the READABLE_BYTE_COUNT to determine the number of bytes in the RX_BUFFER_BYTE_x. The TCPM reads the RX_BUF_FRAME_TYPE to determine the type of message. The TCPM then reads the content of the USB PD message in RX_BUF_BYTE_x.
The READABLE_BYTE_COUNT register will be set to 0 when a Hard Reset is sent; a Hard Reset is received (if Hard Reset detection is enabled); a disconnect; or when RX_SOP_MSG_STAT is cleared.

BIT	7	6	5	4	3	2	1	0
Field	RECEIVE_BUFFER[7:0]							
Reset	0x00							
Access Type	Read, Ext							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVE_BUFFER	7:0	Receive Buffer. (MAX25432B only)	READABLE_BYTE_COUNT[7:0]: Indicates the number of bytes in the RX_BUF_BYTE_x registers plus one (for the RX_BUF_FRAME_TYPE). RX_BUF_FRAME_TYPE[2:0]: Received SOP* Message 0x00: Received SOP 0x01: Received SOP' 0x02: Received SOP'' 0x03: Received SOP_DBG' 0x04: Received SOP_DBG'' 0x05: Received Cable Reset All others are reserved.

BITFIELD	BITS	DESCRIPTION	DECODE
			RX_BUF_BYTE_x[7:0]: Content of the USB PD message.

TRANSMIT (0x50)

The TCPM writes to this register to transmit a SOP* message where the SOP* message payload (i.e., the header bytes and the data bytes) was written into the TCPC's internal transmit buffer using the TRANSMIT_BUFFER register. The TCPC transmits the aggregate of data written to the TRANSMIT_BUFFER since the pointer was last reset, either due to the TCPM writing to the TRANSMIT register or the TCPM writing to COMMAND.ResetTransmitBuffer (0xDD). The entire register will be written at once and then sent. The TCPC will clear the TRANSMIT register I2C_WRITE_BYTE_COUNT and its internal transmit buffer after executing the transmission regardless of the outcome (either successful, failed or discarded).

BIT	7	6	5	4	3	2	1	0
Field	–	–	RETRY_COUNTER[1:0]		–	TX_SOP_MESSAGE[2:0]		
Reset	–	–	0b00		–	0b000		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RETRY_COUNTER	5:4	Retry Counter. (MAX25432B only)	0x0: No message retry is required 0x1: Automatically retry message transmission once 0x2: Automatically retry message transmission twice 0x3: Automatically retry message transmission three times
TX_SOP_MESSAGE	2:0	Transmit SOP* Message. (MAX25432B only)	0x0: Transmit SOP 0x1: Transmit SOP' 0x2: Transmit SOP'' 0x3: Transmit SOP_DBG' 0x4: Transmit SOP_DBG'' 0x5: Transmit Hard Reset 0x6: Transmit Cable Reset 0x7: Transmit BIST Carrier Mode 2

TRANSMIT_BUFFER (0x51)

The TRANSMIT_BUFFER holds the I2C_WRITE_BYTE_COUNT and the portion of the SOP* USB PD message payload (including the header and/or the data bytes) most recently written by the TCPM in TX_BUF_BYTE_x. TX_BUF_BYTE_x is "hidden" and can only be accessed by writing to register address 51h. The USB PD message payload supported by MAX25432B can be up to 30-byte long.

BIT	7	6	5	4	3	2	1	0
Field	TRANSMIT_BUFFER[7:0]							

Reset	0x00
Access Type	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
TRANSMIT_BUFFER	7:0	Transmit Buffer. (MAX25432B only)	I2C_WRITE_BYTE_COUNT[7:0] The number of bytes the TCPM intends to write to the TX_BUF_BYTE_x in the given I^2C transaction TX_BUF_BYTE_x[7:0]: Transmit buffer bytes

VBUS_VOLTAGE_L (0x70)

BIT	7	6	5	4	3	2	1	0
Field	VBUS_VOLTAGE[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_VOLTAGE	7:0	V_{BUS} Voltage Measurement from 10-Bit ADC (Lower 8 Bits).	Bits [7:0] of the 10-bit V_{BUS} ADC measurement result with 25mV LSB. Valid when POWER_CONTROL.VBUS_VOLT_MON_EN = 0b.

VBUS_VOLTAGE_H (0x71)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SCALE_FACTOR[1:0]		VBUS_VOLTAGE[9:8]	
Reset	–	–	–	–	0b00		0b00	
Access Type	–	–	–	–	Read Only		Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
SCALE_FACTOR	3:2	Scale Factor. (Reserved)	00: V_{BUS} measurement not scaled
VBUS_VOLTAGE	1:0	V_{BUS} Voltage Measurement from 10-Bit ADC (Upper 2 Bits).	Bits [9:8] of the 10-bit V_{BUS} ADC measurement result with 25mV LSB. Valid when POWER_CONTROL.VBUS_VOLT_MON_EN = 1.

VBUS_STOP_DISCHARGE_THRESHOLD_L (0x74)

BIT	7	6	5	4	3	2	1	0
Field	VBUS_STOP_DISCH_THRESHOLD[7:0]							
Reset	0x20							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_STOP_DISCH_THRESHOLD	7:0	V_{BUS} Stop Discharge Threshold. (Lower 8 bits)	Bits [7:0] of the 10-bit V_{BUS} stop discharge threshold. 0x000 to 0x018: 0.5V 0x01C to 0x3FF: Value (decimal) x 25mV Bit 1 and Bit 0 are always ignored. Bit 2 is the LSB and equals to 100mV. Examples: 0x000 = 0.5V 0x020 = 0.8V (default) 0x021 = 0.9V

VBUS_STOP_DISCHARGE_THRESHOLD_H (0x75)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VBUS_STOP_DISCH_THRESHOLD[9:8]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_STOP_DISCH_THRESHOLD	1:0	V_{BUS} Stop Discharge Threshold. (Upper 2 bits)	Bits [9:8] of the 10-bit V_{BUS} stop discharge threshold

VBUS_VOLTAGE_ALARM_HI_CFG_L (0x76)

This register defines the level triggered alarm high threshold.
The TCPM can write to POWER_CONTROL.VOLT_ALRMS_EN = 0b to enable the voltage alarms or write 1b to disable them. The TCPM writes to VBUS_VOLTAGE_ALARM_HI_CFG to set the high-voltage alarm level.
When V_{OUT} is above this threshold, the MAX25432 will set the alarm high flag ALERT_L.VBUS_ALARM_HI to 1. The MAX25432 will reassert the alarm high flag if the high-voltage condition on V_{OUT} prevails after the TCPM has cleared the flag, unless the TCPM disables the voltage alarms.

BIT	7	6	5	4	3	2	1	0

Field	VBUS_ALARM_HI_CFG[7:0]
Reset	0x00
Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ALARM_HI_CFG	7:0	V_{BUS} Alarm High-Voltage Trip Point. (Lower 8 bits)	Bits [7:0] of the 10-bit V_{BUS} alarm high-voltage threshold with 25mV LSB

VBUS_VOLTAGE_ALARM_HI_CFG_H (0x77)

See the VBUS_VOLTAGE_ALARM_HI_CFG_L register description.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VBUS_ALARM_HI_CFG[9:8]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ALARM_HI_CFG	1:0	V_{BUS} Alarm High Voltage Trip Point. (Upper 2 bits)	Bits [9:8] of the 10-bit V_{BUS} alarm high-voltage threshold with 25mV LSB

VBUS_VOLTAGE_ALARM_LO_CFG_L (0x78)

This register defines the level triggered alarm low threshold.
The TCPM can write to POWER_CONTROL.VOLT_ALRMS_EN = 0b to enable the voltage alarms or write 1b to disable them. The TCPM writes to VBUS_VOLTAGE_ALARM_LO_CFG to set the low-voltage alarm level.
When V_{OUT} is below this threshold, the MAX25432 will set the alarm low flag ALERT_H.VBUS_ALARM_LO to 1. The MAX25432 will reassert the alarm low flag if the low-voltage condition on V_{OUT} prevails after the TCPM has cleared the flag, unless the TCPM disables the voltage alarms.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_ALARM_LO_CFG[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ALARM_LO_CFG	7:0	V_{BUS} Low-Voltage Trip Point. (Lower 8 bits)	Bits [7:0] of the 10-bit V_{BUS} alarm low-voltage threshold with 25mV LSB.

BITFIELD	BITS	DESCRIPTION	DECODE
			When V_{OUT} is below this threshold, The MAX25432 will set ALERT_H.VBUS_ALARM_LO to 1.

VBUS_VOLTAGE_ALARM_LO_CFG_H (0x79)

See the VBUS_VOLTAGE_ALARM_LO_CFG_L register description.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VBUS_ALARM_LO_CFG[9:8]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ALARM_LO_CFG	1:0	V_{BUS} Alarm Low-Voltage Trip Point (Upper 2 bits)	Bits [9:8] of the 10-bit V_{BUS} alarm low-voltage threshold with 25mV LSB

VBUS_NONDEFAULT_TARGET_L (0x7A)

Writing to this 16-bit register sets the VBUS Non-Default Target Voltage. VBUS will slew to the new voltage once the SourceVbusNonDefault command is received.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_NONDEFAULT_TARGET_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VBUS_NONDEFAULT_TARGET_L	7:0	V_{BUS} Non-Default Voltage Target. (Lower 8 bits) For VBUS_HIRES = 0 (not recommended), resolution is 10-bit, and LSB = 20.51mV (typ) Valid range is from 0x00A5 (3.3V) to 0x03FF (21.0V). For VBUS_HIRES = 1 (required to pass SPT compliance), resolution is 11-bit, and LSB = 10.255mV (typ) Valid range is from 0x014A (3.3V) to 0x07FF (21.0V). For proper operation, do not write values outside of the valid range.

BITFIELD	BITS	DESCRIPTION
		For VBUS_HIRES = 1, the equation to convert from mV to decimal code is the following: **uint16_t vbus_code = v/10 - [floor(304*v/100000) - 10]** Where v is the RDO in mV and vbus_code the resulting output in decimal to write to this register. No floating point required.

VBUS_NONDEFAULT_TARGET_H (0x7B)

See the VBUS_NONDEFAULT_TARGET_L register description.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_NONDEFAULT_TARGET_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VBUS_NONDEFAULT_TARGET_H	7:0	V_{BUS} Non-Default Voltage Target. (Upper 8 bits)

VBUS_CURRENT (0x80)

BIT	7	6	5	4	3	2	1	0
Field	VBUS_CURRENT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_CURRENT	7:0	V_{BUS} Current Measurement from 7-Bit ADC. (All MAX25432 devices)	I_{OUT} = VBUS_CURRENT[7:0] x IOUT_LSB_ADC (50mA, typ) VBUS_CURRENT[7] is always 0b. Max register value = 0x7F = 127. Full Scale = 127 x 50mA = 6.35A Conversion result valid when the MAX25432 is sourcing VBUS and POWER_CONTROL.VBUS_VOLT_MON_EN = 0b. Ignore otherwise.

CABLE_COMP_CONTROL (0x81)

BIT	7	6	5	4	3	2	1	0
Field	–	–	GAIN[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GAIN	5:0	Cable Compensation Gain.	Multiply this register's decimal value by R_{COMP_LSB} = 8.2mΩ to get the cable compensation gain (R_{COMP}) in mΩ for R_{CS3} = 5mΩ, scale for other resistance values. See the *USB Cable Compensation* section on how to calculate the correct gain setting based on your application. Maximum register setting = 0x3F = 0d63; therefore, maximum cable compensation is 63 x 8.2mΩ = 516.6mΩ.

VBUS_ILIM_SETUP (0x82)

BIT	7	6	5	4	3	2	1	0
Field	VBUS_ILIM_SET[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ILIM_SET	7:0	V_{BUS} Current Limit Target.	LSB = 25mA. Default is 3.20A (0x80). Valid range for this register is 1.00A (0x28) to 6.35A (0xFE). For proper operation, do not write values outside the valid range.

BUCK_BOOST_SETUP (0x83)

BIT	7	6	5	4	3	2	1	0
Field	SLP[2:0]			FSW[1:0]		SYNC_DIR	SS_SEL[1:0]	
Reset	0b011			0b10		0b1	0b00	
Access Type	Write, Read			Write, Read		Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SLP	7:5	Slope Compensation Peak Ramp Voltage.	000: 100 mV 001: 200 mV 010: 300 mV 011: 400 mV (Default) 100: 500 mV 101: 600 mV 110: 700 mV 111: 800 mV
FSW	4:3	DC-DC Converter Switching Frequency.	00: 220kHz 01: 300kHz 10: 400kHz (default) 11: 2.2MHz
SYNC_DIR	2	SYNC Pin Direction Selection.	0: Output 1: Input (default)
SS_SEL	1:0	Spread-Spectrum Selection.	00: Disabled (default) 01: ±3% spread spectrum 10: ±6% spread spectrum 11: ±9% spread spectrum

WATCHDOG_SETUP (0x84)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	WD_TIMEOUT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WD_TIMEOUT	1:0	Watchdog Timer Timeout Value.	00: 1 second (default) 01: 2 seconds 10: 4 seconds 11: 5 seconds

AUTO_SHIELD_SETUP (0x85)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RETRY_TMR[1:0]	
Reset	–	–	–	–	–	–	0b11	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RETRY_TMR	1:0	Retry Timer Value.	00 = 2.0s 01 = 1.0s 10 = 0.5s 11 = 16ms (default) Determines the length of the RETRY timer after a fault condition

GENERAL_SETUP (0x86)

BIT	7	6	5	4	3	2	1	0
Field	–	VBUS_HIRES	–	EXT_BIAS_SEL	–	CL_EN	AUTO_CDP_DCP_MODE[1:0]	
Reset	–	0b0	–	0b0	–	0b1	0b00	
Access Type	–	Write, Read	–	Write, Read	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_HIRES	6	V_{BUS} Non-Default Target Resolution.	0: 20mV (default) 1: 10mV
EXT_BIAS_SEL	4	External BIAS Selection.	0: Internal (default) 1: External (disables internal BIAS LDO) **Note:** A valid power source needs to be driving BIAS before writing a '1' to this bit. Failure to do so will result in an I^2C register reset.
CL_EN	2	V_{BUS} Current-Limit (CL) Regulation Enable.	0: V_{BUS} current-limit regulation disabled 1: V_{BUS} current-limit regulation enabled (default) When enabled, the MAX25432 will enter CL mode when V_{BUS} current is above the VBUS_ILIM_SET target. When disabled, the MAX25432 will not enter CL mode when V_{BUS} current is above the VBUS_ILIM_SET target. This bit also changes the handling of certain faults. See the *Fault Table (Analog Devices Auto-Shield)* for more information.
AUTO_CDP_DCP_MODE	1:0	BC1.2 Charge Detection Mode Selection.	00: High-Speed Pass-Through (default) 01: Auto-CDP 10: Auto-DCP / Apple 2.4A 11: Auto-DCP / Apple 1.0A

IN_THRESH (0x87)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	IN_UV_THRESH[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
IN_UV_THRESH	3:0	Input Supply (V_{IN}) Undervoltage Threshold.	0x0 : 4.5V (default) 0x1 : 4.9V 0x2 : 5.3V 0x3 : 5.7V 0x4 : 6.1V 0x5: 6.5V 0x6: 6.9V 0x7: 7.3V 0x8: 7.7V 0x9: 8.1V 0xA: 8.5V 0xB : Reserved 0xC : Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

VCONN_THRESH (0x88)

BIT	7	6	5	4	3	2	1	0
Field	VCONN_OCPL_SEL[3:0]				–	VCONN_IN_UV_THRESH[2:0]		
Reset	0x6				–	0b011		
Access Type	Write, Read				–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VCONN_OCPL_SEL	7:4	V_{CONN} Overcurrent Threshold Low.	0x0: 50mA 0x1: 100mA 0x2: 150mA 0x3: 200mA 0x4: 250mA 0x5: 300mA 0x6: 350mA (default) 0x7: 400mA 0x8: 450mA

BITFIELD	BITS	DESCRIPTION	DECODE
			0x9: 500mA 0xA - 0xF: Reserved
VCONN_IN_UV_THRESH	2:0	V_{CONN} Undervoltage Threshold.	0x0: 2.75V 0x1: 2.85V 0x2: 2.95V 0x3: 3.05V (default) 0x4: 4.35V 0x5: 4.45V 0x6: 4.55V 0x7: 4.65V

VBUS_THRESH (0x89)

BIT	7	6	5	4	3	2	1	0
Field	–	VBUS_OV_THRESH[2:0]			–	VBUS_UV_THRESH[2:0]		
Reset	–	0b011			–	0b011		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_OV_THRESH	6:4	V_{BUS} Overvoltage Threshold.	0x0: +8.75% 0x1: +10.00% 0x2: +11.25% 0x3: +12.50% (default) 0x4: +13.75% 0x5: +15.00% 0x6: +16.25% 0x7: +17.50%
VBUS_UV_THRESH	2:0	V_{BUS} Undervoltage Threshold.	0x0: -8.75% 0x1: -10.00% 0x2: -11.25% 0x3: -12.50% (default) 0x4: -13.75% 0x5: -15.00% 0x6: -16.25% 0x7: -17.50%

VENDOR_STATUS_MASK (0x8A)

BIT	7	6	5	4	3	2	1	0
Field	SHIELDING_MASK	–	–	–	–	–	–	OMF_TRANS_MASK

Reset	0b1	–	–	–	–	–	–	0b1
Access Type	Write, Read	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SHIELDING_MASK	7	Shielding Mask.	0: Not included in VNDR_ALRT 1: Included in VNDR_ALRT (default)
OMF_TRANS_MASK	0	Operating Mode Flag (OMF) Transition Mask.	0: Not included in VNDR_ALRT 1: Included in VNDR_ALRT (default)

VENDOR_STATUS (0x8B)

BIT	7	6	5	4	3	2	1	0
Field	SHIELDING	–	–	–	–	–	–	OMF_TRANS
Reset	0b0	–	–	–	–	–	–	0b0
Access Type	Read Only	–	–	–	–	–	–	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SHIELDING	7	Shielding Status.	0b: Normal operation 1b: Fault condition detected
OMF_TRANS	0	Operating Mode Flag (OMF) Transition.	0: No change in CV/CL operating mode 1: A change in CV/CL operating mode has occurred Indicates a change in the Constant Voltage/Current Limit Operating mode. Any transition between modes will trigger a VNDR_ALRT if this bit is unmasked, but does not trigger a fault. Only valid for CL_EN = 1. Ignore for CL_EN = 0.

AUTO_SHIELD_STATUS_0 (0x8C)

BIT	7	6	5	4	3	2	1	0
Field	TSHDN	VCONN_REV_OV	VCONN_OCPL	SHLD_EVENT	VCONN_IN_UV	IN_OC	VDD_USB_UV	VBUS_UV
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0

Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TSHDN	7	Thermal Shutdown Fault.	0: No fault 1: Fault detected
VCONN_REV_OV	6	V_{CONN} Reverse OV Fault.	0: No fault 1: Fault detected
VCONN_OCPL	5	V_{CONN} OCP Low Fault.	0: No fault 1: Fault detected
SHLD_EVENT	4	Shield Short-to-Battery Event Fault.	0: No fault 1: Fault detected
VCONN_IN_UV	3	V_{CONN} Undervoltage Fault.	0: No fault 1: Fault detected
IN_OC	2	Buck-Boost Input Overcurrent Fault.	0: No fault 1: Fault detected
VDD_USB_UV	1	V_{DD_USB} Undervoltage Fault.	0: No fault 1: Fault detected
VBUS_UV	0	V_{BUS} Undervoltage Fault.	0: No fault 1: Fault detected

AUTO_SHIELD_STATUS_1 (0x8D)

BIT	7	6	5	4	3	2	1	0
Field	CL_CV	CV_ILIM	VBUS_RNA	VBUS_SHT_GND	IN_UV	DATA_OV	HVCC_OV	VDD_USB_OV
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CL_CV	7	Operating Mode Status Bit.	0: Constant Voltage (CV) mode 1: Current-Limit (CL) mode Only valid when CL_EN = 1. Ignore when CL_EN = 0. This bit is read-only and non-latched. Read OMF_TRANS for the latched status. Does not trigger a fault or VNDR_ALRT.

BITFIELD	BITS	DESCRIPTION	DECODE
CV_ILIM	6	V_{BUS} CV I_{LIM} Fault.	0: No fault 1: Fault detected 0 to 1 only. Only valid when CL_EN = 0. Ignore when CL_EN = 1.
VBUS_RNA	5	V_{BUS} Runaway Fault.	0: No fault 1: Fault detected
VBUS_SHT_GND	4	V_{BUS} STG Fault.	0: No fault 1: Fault detected
IN_UV	3	Input UV Fault.	0: No fault 1: Fault detected
DATA_OV	2	HVD Overvoltage Fault.	0: No fault 1: Fault detected
HVCC_OV	1	HVCC Overvoltage Fault.	0: No fault 1: Fault detected
VDD_USB_OV	0	V_{DD_USB} Overvoltage Fault.	0: No fault 1: Fault detected

Applications Information

TCPC Functionality (MAX25432B only)

The MAX25432B devices incorporate a USB-IF compliant CC PHY capable of encoding/decoding BMC messages. CRC is automatically appended to all outgoing messages and checked on all incoming messages.

The MAX25432B's TCPC hardware permits the simple integration with an external MCU, running a TCPM stack, to create a complete USB Type-C PD source.

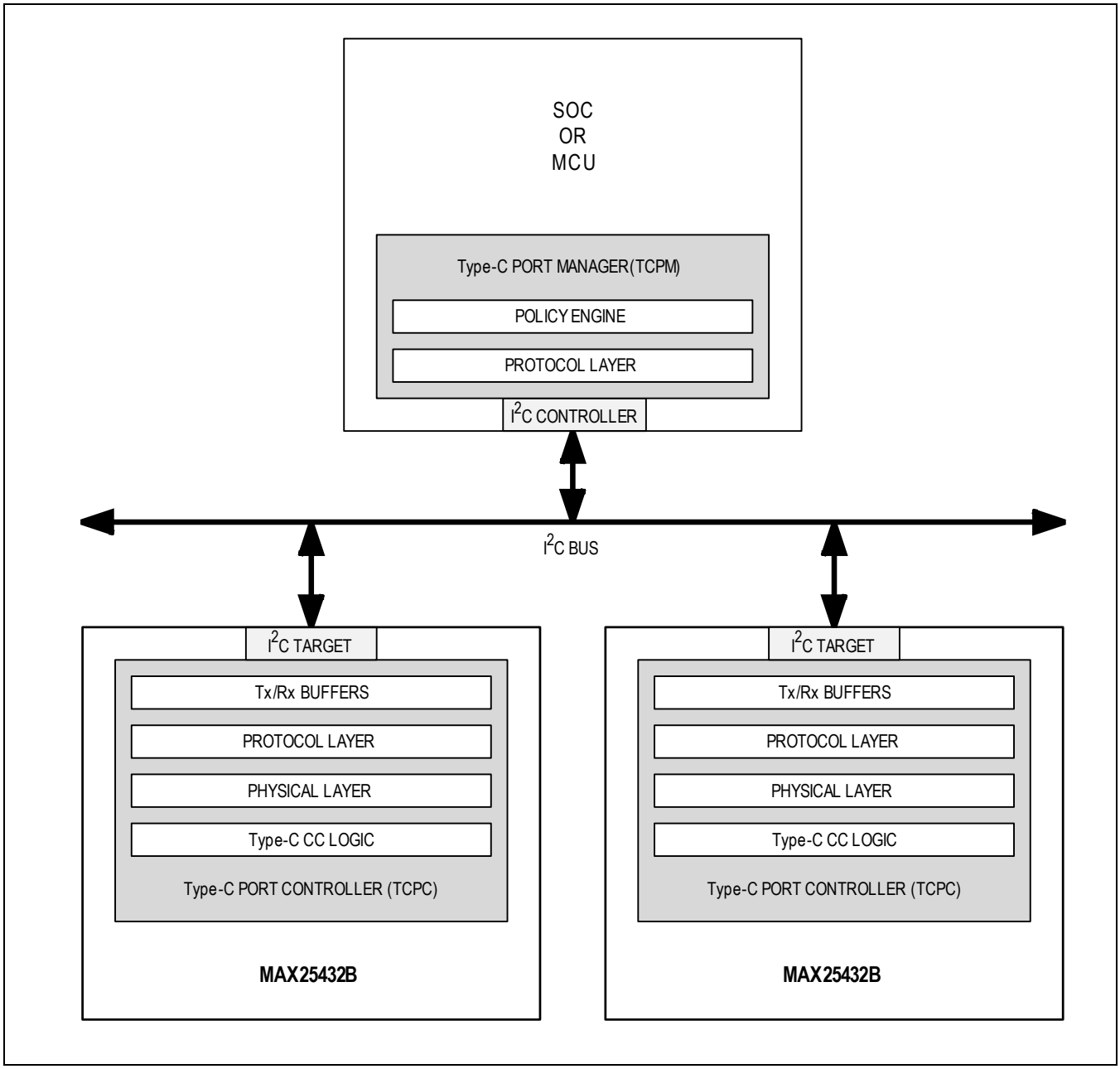


Figure 29. TCPM to TCPC Interface through I^2C

Receiving USB PD Messages

The MAX25432B TCPC logic facilitates the reception and decoding of USB PD messages, by incorporating a Type-C PHY, and I2C-accessible registers. The TCPM responds to interrupts due to changes in status and then read from or

write to the appropriate register. The generation and decoding of PD CRC bits is automatically handled by the TCPC logic. Upon receiving a valid USB PD message, the MAX25432 TCPC logic asserts the $\overline{\text{ALERT}}$ pin low to indicate a change in status. Changes in status are latched in the ALERT_L and ALERT_H registers located at addresses 0x10 and 0x11 respectively. The TCPM must read the ALERT_L and ALERT_H registers to determine the type of status change.

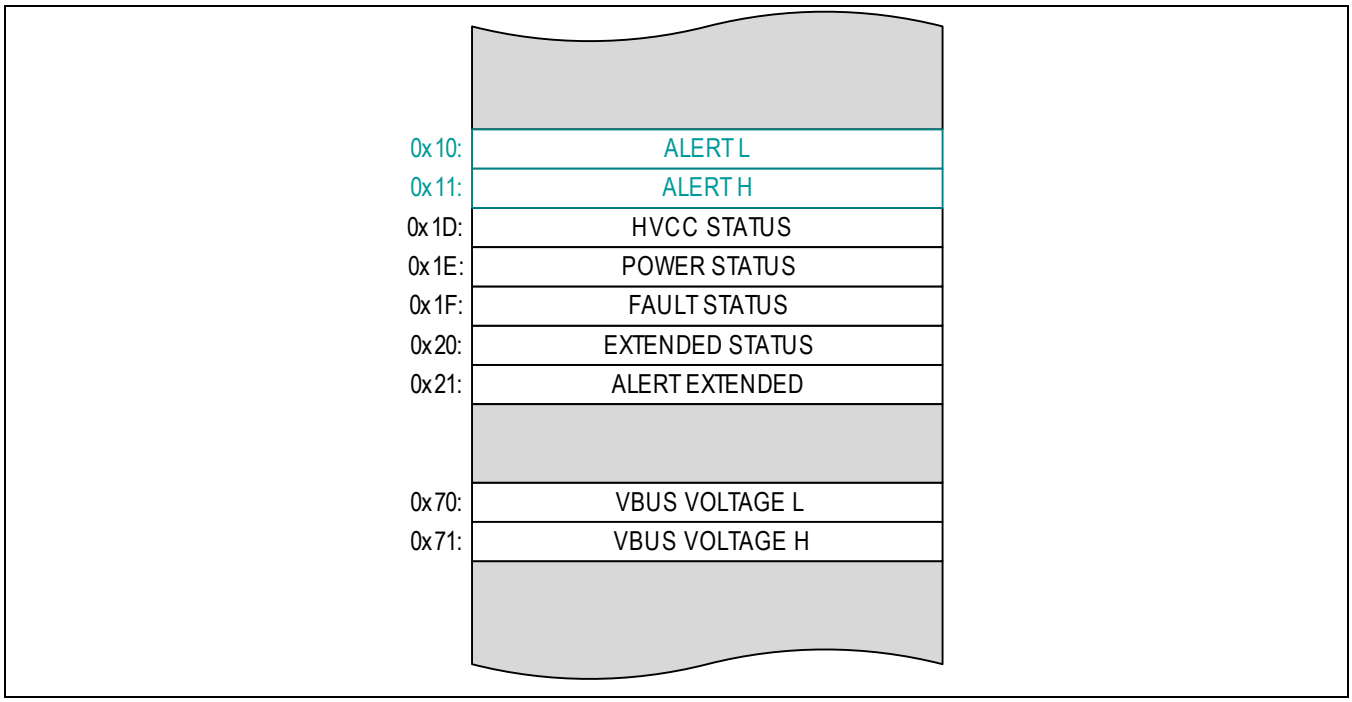


Figure 30. Status Registers

For example, the TCPM detects that the MAX25432 $\overline{\text{ALERT}}$ pin has been asserted low. The TCPM would then perform an I²C Read Word transaction on the ALERT_L and ALERT_H registers.

I²C Read Word from Register 0x10:

0x04, 0x00

Table 10. Reading the RX SOP MESSAGE

REGISTER	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
ALERT_L	0x10	VBUS V ALARM HIGH	TX SOP MESSAGE SUCCESS	TX SOP MESSAGE DISCARD	TX SOP MESSAGE FAIL	RX HARD RESET	RX SOP MESSAGE	POWER STATUS	HVCC STATUS
		0	0	0	0	0	1	0	0
ALERT_H	0x11	VENDOR ALERT	ALERT EXTENDED	EXTEND STATUS	BEGIN SOP MESSAGE STATUS	VBUS SINK DISCHAR DETECT	RX BUFFER OVRFL	FAULT STATUS	VBUS VOLT ALARM LOW
		0	0	0	0	0	0	0	0

Bit D2 in ALERT_L is set, indicating that a message has been received in the RX BUFFER.

Next, the message must be extracted from the MAX25432 RX_BUFFER and decoded.

The message content is stored in the RX_BUFFER, 32 contiguous bytes starting at address 0x30. The RX_BUFFER can be read with an I²C Read Block transaction, or it can be read with several I²C Read Byte transactions. The buffer address pointer will increment automatically after each byte is read.

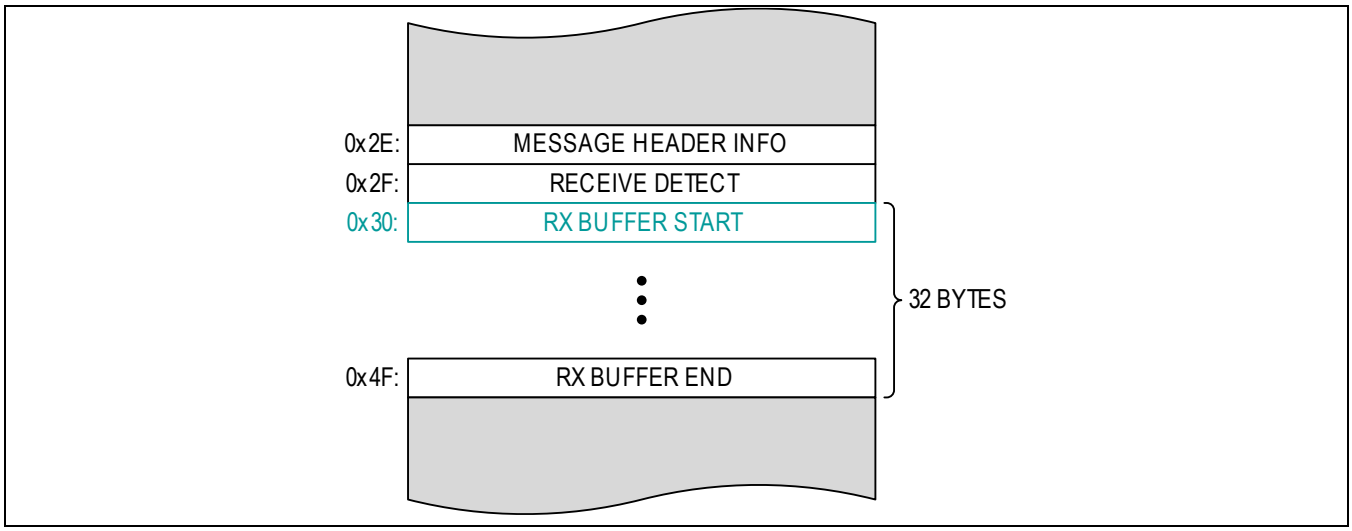


Figure 31. Receive Buffer

Continuing with the example, the message data is extracted from the RX_BUFFER.

I2C Read Block from Registers 0x30 – 0x4F:

0x03, 0x00, 0x47, 0x0C, 0x16, 0x87, 0x57, 0xF7, 0xEF, 0xD6,

0x2C, 0x40, 0x26, 0x28, 0x03, 0x9B, 0x00, 0x00, 0x00, 0x00,

0x44, 0xD3, 0x15, 0xEA, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,

0x00, 0x00

The first byte indicates that there are three bytes significant to this message. The second byte is the SOP message type, the third and fourth bytes form the message header 0x0C47.

Note: The TCPC does not erase previous information from the buffer and therefore the TCPM must parse the relevant bytes to decode the message.

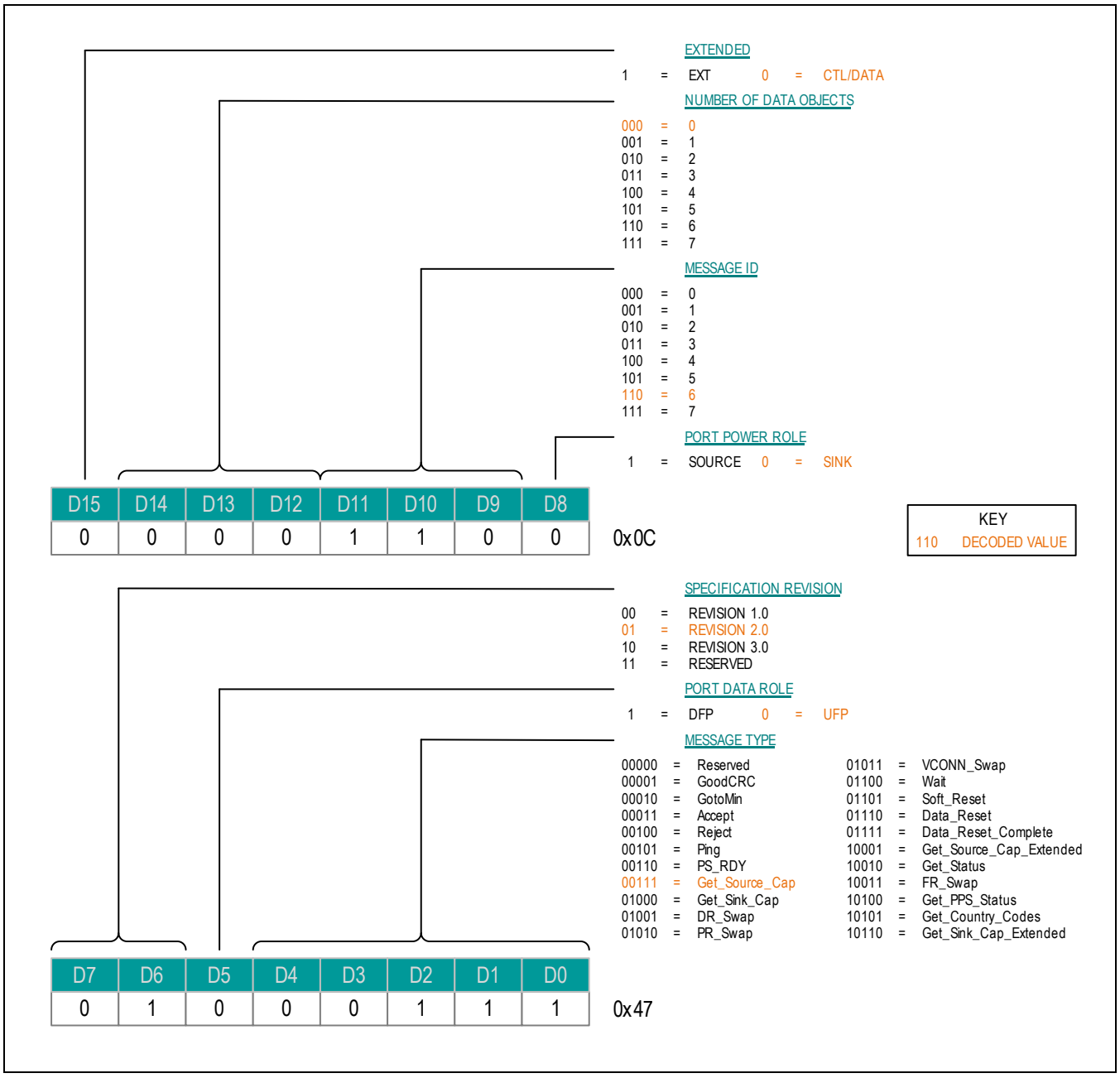


Figure 32. Message Header - "Get_Source_cap"

Decoding the header word indicates the PD sink is requesting that the source capabilities be sent.

Now that the message has been decoded, the $\overline{\text{ALERT}}$ pin interrupt can be cleared, so that the MAX25432B TCPM's state machine can continue to service PD messages.

Table 11. Writing 1 to Clear the RX SOP MESSAGE

REGISTER	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
ALERT_L	0x10	VBUS V ALARM HIGH	TX SOP MESSAGE SUCCESS	TX SOP MESSAGE DISCARD	TX SOP MESSAGE FAIL	RX HARD RESET	RX SOP MESSAGE	POWER STATUS	HVCC STATUS
		0	0	0	0	0	1	0	0

ALERT_H	0x11	VENDOR ALERT	ALERT EXTENDED	EXTEND STATUS	BEGIN SOP MESSAGE STATUS	VBUS SINK DISCHAR DETECT	RX BUFFER OVRFL	FAULT STATUS	VBUS VOLT ALARM LOW
		0	0	0	0	0	0	0	0

I²C Write Word to Register 0x10:

0x04, 0x00

The TCPM clears the ALERT_L register by writing a logic '1' to bit D2. $\overline{\text{ALERT}}$ returns high.

Sending USB PD Messages

The MAX25432B TCPC logic simplifies the TCPM code required to transmit USB PD messages. Sending PD messages is a two-stage process: employing the TX_BUFFER (31 contiguous byte-wide registers) and the TRANSMIT register.

First, the TX_BUFFER is loaded with an encoded PD message (Control or Data), and then a command byte is written the TRANSMIT register (0x50) to trigger the MAX25432 TCPC transmit process.

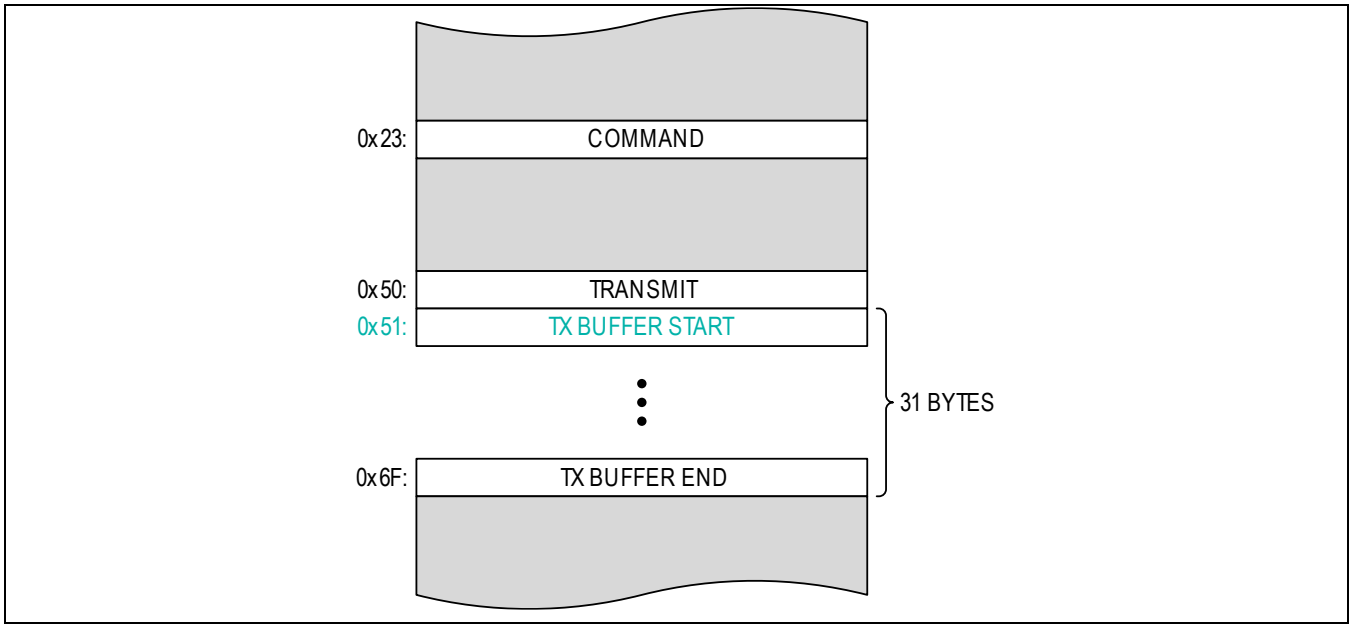


Figure 33. Transmit Buffer

The PD message contents must be written to TX_BUFFER in a single I²C transaction, therefore an I²C Write Block transaction (see the *I2C Interface* section) should be used, or the TCPC logic will generate an I²C error after the TRANSMIT byte is written to and the message will not be sent.

To illustrate the proper TCPM coding approach, we will continue with the MAX25432B's response to the PD sink's Get Source Capabilities example.

The TCPM needs to encode and load the requested Source Capabilities message, Header plus Data Objects, into the TX BUFFER.

Number of bytes: 0x12 (18 bytes)

Message Header: 0x4361 (Source Capabilities with 4 data objects) = 2 bytes

Data Object 1: 0x000190F0 (5.00V at 2.4A) = 4 bytes

Data Object 2: 0x0002D12C (9.00V at 3A) = 4 bytes

Data Object 3: 0x0004B12C (15.00V at 3A) = 4 bytes

Data Object 4: 0x0006412C (20.00V at 3A) = 4 bytes

Figure 34 and *Figure 35* show the corresponding Message Header and Data Object 1 decoding.

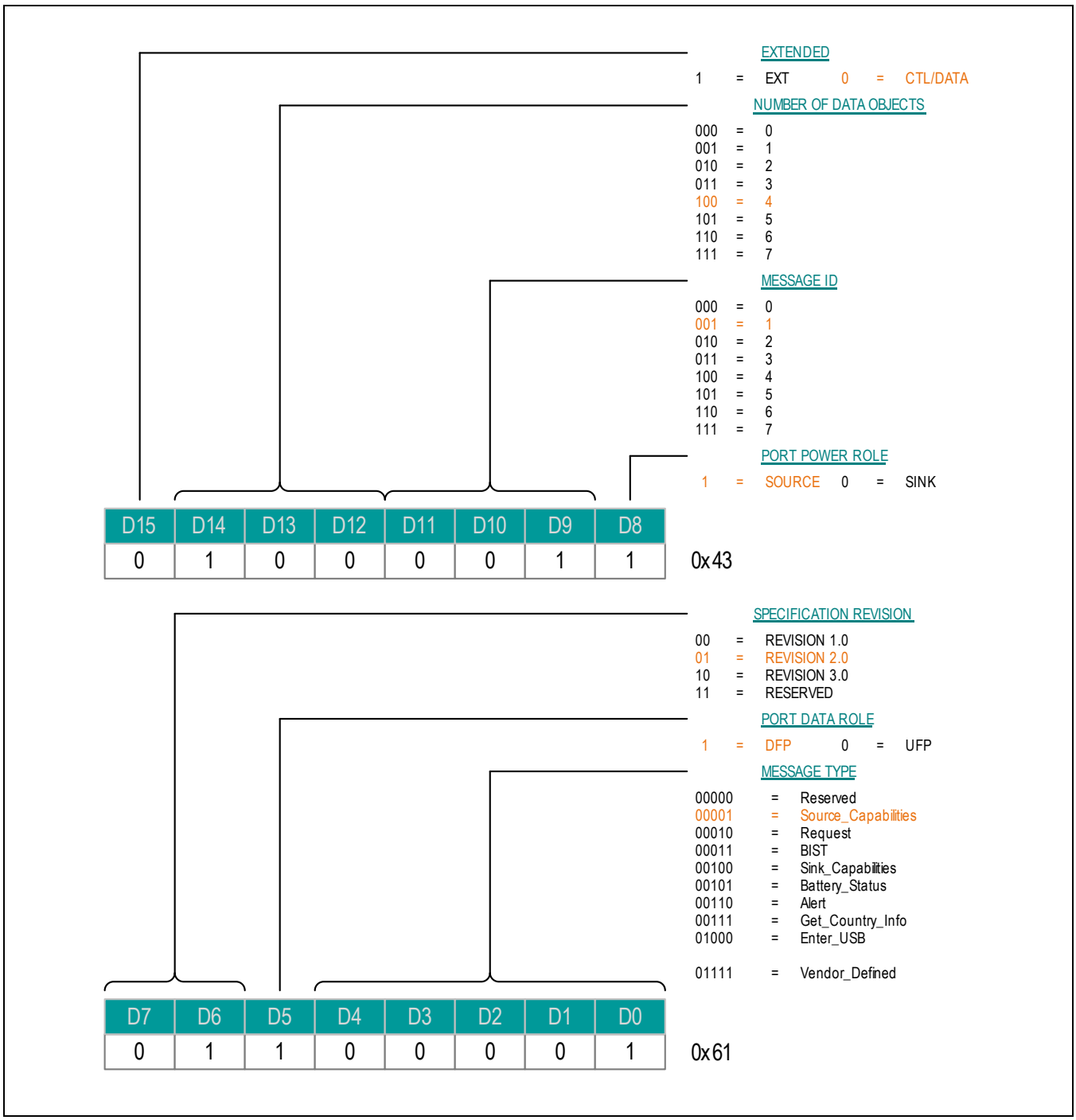


Figure 34. Message Header – "Source_Capabilities"

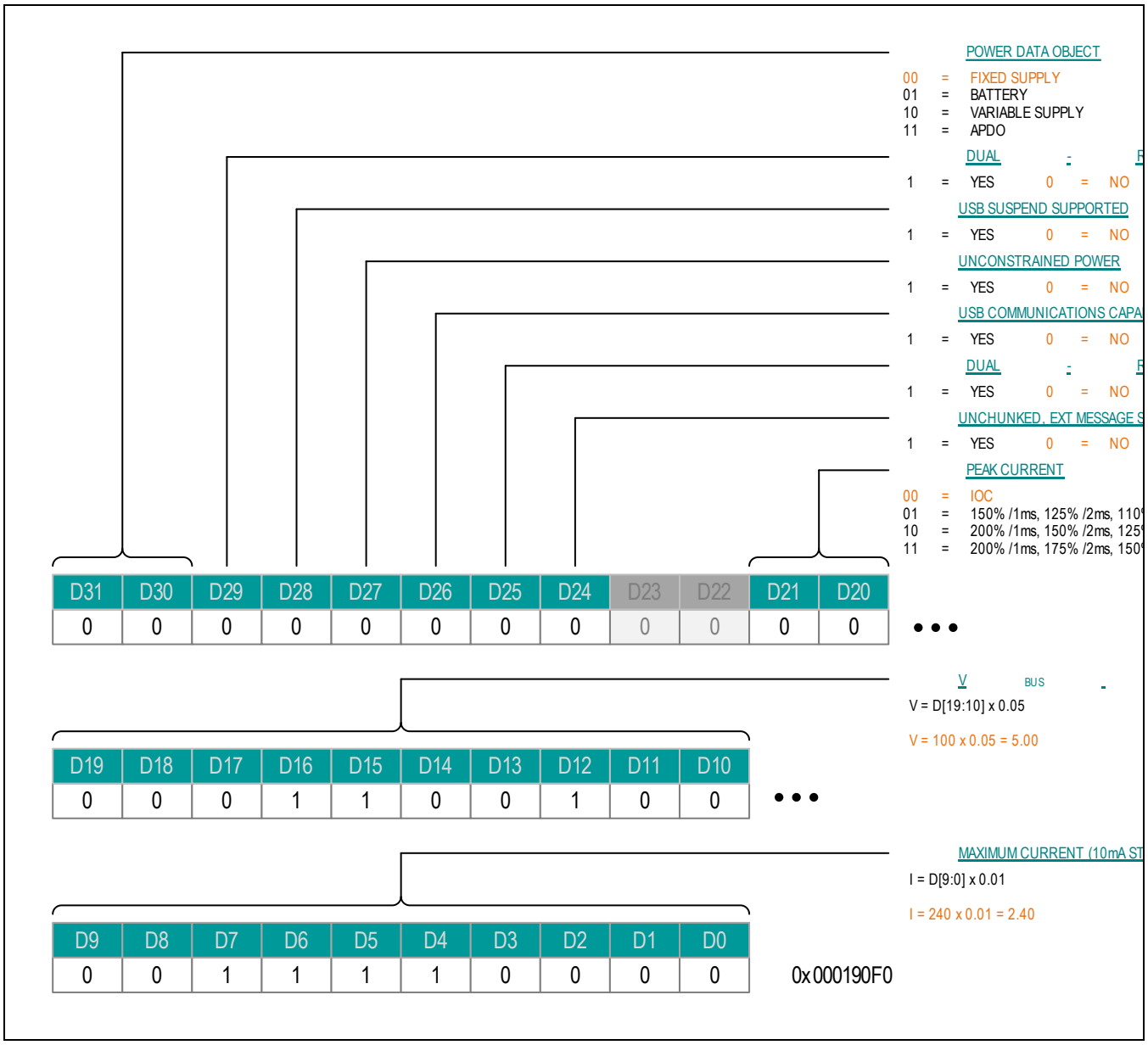


Figure 35. Data Object 1 – 5V/2.4A Fixed PDO

The assembled message packet is then loaded into the TX_BUFFER.

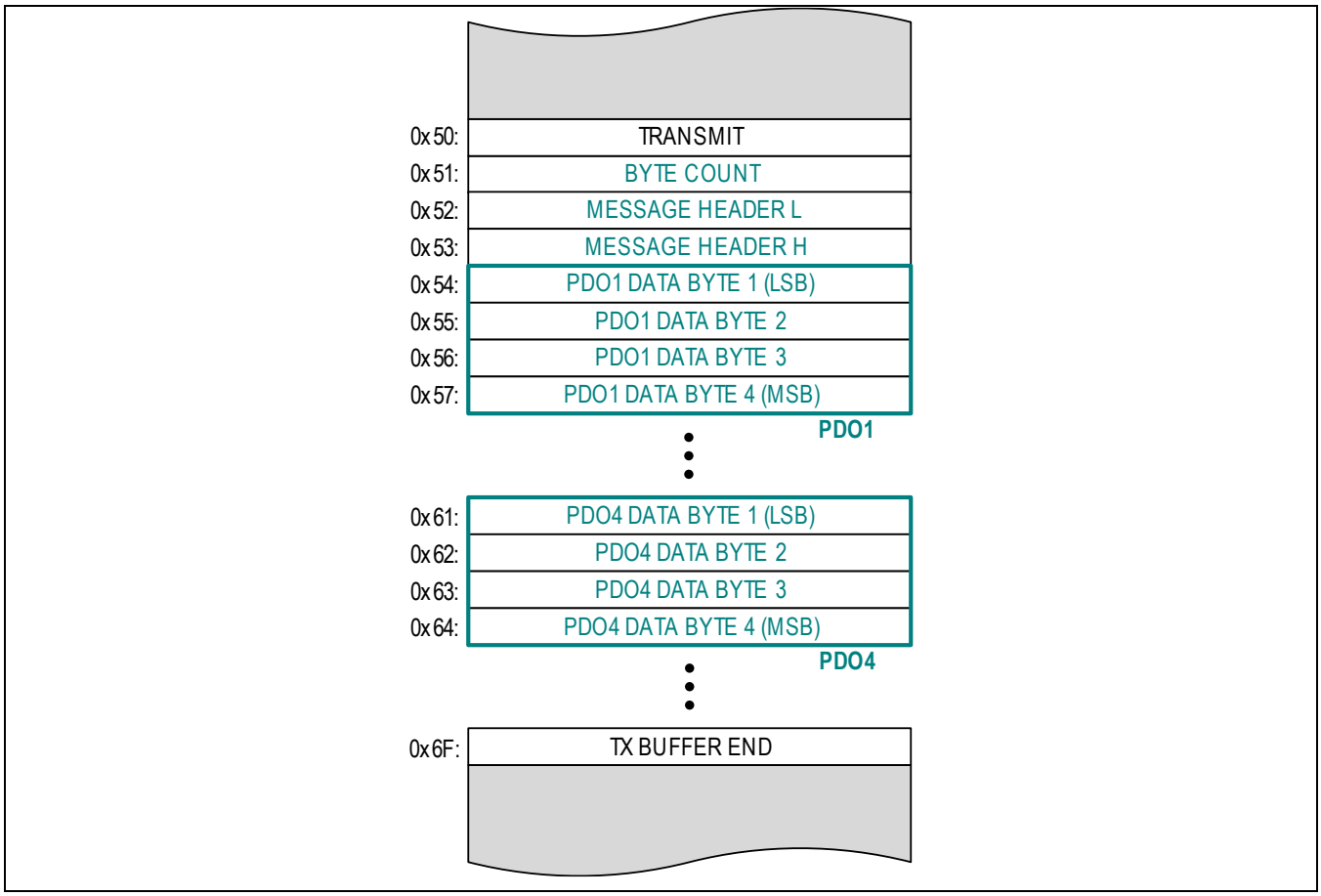


Figure 36. Transmit Buffer - "Source_Capabilities"

I²C Write Block to TX BUFFER 0x51:

0x12, 0x61, 0x43, 0xF0, 0x90, 0x01, 0x00, 0x2C, 0xD1, 0x02,

0x00, 0x2C, 0xB1, 0x04, 0x00, 0x2C, 0x41, 0x06, 0x00

Finally, the message is released to the MAX25432B's TCPC logic by writing 0x30 to the TRANSMIT register. Then the entire packet will be appended with the proper CRC, BMC encoded, and transmitted through the corresponding HVCC pin.

I²C Write Byte to TRANSMIT 0x50:

0x30

The MAX25432B's TCPC logic will now assert ALERT low and update the ALERT_L register with the message status.
I²C Read Word from Register 0x10:

0x40, 0x00

Table 12. Writing 1 to Clear the TX SOP MESSAGE SUCCESS

REGISTER	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
ALERT_L	0x10	VBUS V ALARM HIGH	TX SOP MESSAGE SUCCESS	TX SOP MESSAGE DISCARD	TX SOP MESSAGE FAIL	RX HARD RESET	RX SOP MESSAGE	POWER STATUS	HVCC STATUS
		0	1	0	0	0	0	0	0

ALERT_H	0x11	VENDOR ALERT	ALERT EXTENDED	EXTEND STATUS	BEGIN SOP MESSAGE STATUS	VBUS SINK DISCHAR DETECT	RX BUFFER OVRFL	FAULT STATUS	VBUS VOLT ALARM LOW
		0	0	0	0	0	0	0	0

The TCPM reads the ALERT_L and ALERT_H registers and sees that bit D6 is set in ALERT_L, indicating that the previously sent message was successful.

Lastly, the TX_SOP_MESSAGE_SUCCESS bit in the ALERT_L register needs to be cleared by the TCPM. This is done by writing logic '1' to bit D6.

I²C Write Word to Register 0x10:

0x40, 0x00

Additional Resources

Contact Analog Devices for more information on how to program the TCPM.

Buck-Boost Component Selection

Contact Analog Devices to request a calculator to help in buck-boost component selection for your design.

Inductor Selection

Choice of inductor is a compromise between the size, efficiency, control bandwidth, and stability of the converter. For a buck-boost application, selecting the right value of inductor becomes even more critical due to the presence of a right-half-plane (RHP) zero in boost and buck-boost mode. A larger inductance value reduces RMS current loss in MOSFETs and core/winding losses in the inductor. On the other hand, it slows the control loop and reduces the frequency of the RHP zero that can cause stability concerns.

Start the inductor selection based on the inductor current ripple as a percentage of the maximum inductor current in buck mode using the following equations. Choose the highest inductance between L_{BUCK} and L_{BOOST}. Minimum duty cycle in buck or boost will yield the highest inductor current ripple.

$$L_{BUCK} > \frac{(V_{IN_MAX} - V_{OUT_MIN}) \cdot D_{BUCK_MIN}}{f_{SW} \cdot \Delta I_L} \quad \text{(eq. 1)}$$

$$L_{BOOST} > \frac{(V_{IN_MIN} - D_{BOOST_MAX})}{f_{SW} \cdot \Delta I_L} \quad \text{(eq. 2)}$$

$$\Delta I_L = I_{OUT_MAX} \cdot LIR \quad \text{(eq. 3)}$$

$$D_{BUCK_MIN} = \frac{(V_{OUT_MIN})}{V_{IN_MAX} \cdot \eta_{BUCK}} \quad \text{(eq. 4)}$$

$$D_{BOOST_MAX} = 1 - \frac{(V_{IN_MIN} \cdot \eta_{BOOST})}{V_{OUT_MAX}} \quad \text{(eq. 5)}$$

where:

L_{BUCK}, L_{BOOST} = Minimum inductance needed in buck mode and boost mode, respectively, in H

f_{SW} = Switching frequency in Hz

V_{IN_MIN},V_{IN_MAX} = Minimum and maximum voltage seen at the power stage input, respectively

IOUT_MAX = Maximum DC output current supported in the application.

LIR = Desired peak-to-peak inductor current ripple ratio; ratio of ΔIL/IOUT_MAX

D_{BUCK_MIN}, D_{BOOST_MAX} = Minimum and maximum duty cycle in Buck and Boost mode, respectively

η_{BUCK}, η_{BOOST} = Efficiency at maximum load in buck mode and boost mode, respectively

V_{OUT_MIN} = Lowest output voltage seen in the application. For fixed PDO applications, use 5.15V (vSafe5V).

V_{OUT_MAX} = Highest output voltage seen in the application. 5.15V, 9V, 15V, or 20V for fixed PDOs applications

Select the final value of inductance considering the ripple in both regions of operation, inductor derating and RHP zero. Once the final value of inductance is selected, calculate the peak inductor current and choose an inductor with saturation current approximately 20% higher than the peak inductor current. Low DCR helps achieve higher efficiency by reducing inductor conduction loss during high output power with low input voltage.

Example:

P_{OUT_MAX} = 100W; VIN_MIN = 6V; V_{IN_MAX} = 18V; V_{OUT_MIN} = 5.15V; V_{OUT_MAX} = 20V; f_{SW} = 400kHz; I_{OUT_MAX} = 5A ; η_{BUCK} = η_{BOOST} = 95%; LIR is chosen to be 55% to keep the inductor small.

For this example, L_{BUCK} > 3.5µH and L_{BOOST} > 3.9µH. Therefore, an inductor with a value of 4.7µH will be selected.

Inductor saturation current must be considered when choosing the inductor.

The high input current seen during low V_{IN}/high P_{OUT} conditions has an impact on the current saturation rating of the inductor and therefore its size. The MAX25432 advantage is its flexibility with regards to output power due to its scalable peak input current limit. When selecting the input current sense resistor value (R_{CS1}), consider the output power, inductor saturation current, minimum input voltage seen at the power stage and the minimum V_{BUS} voltage specification to meet at the user port. When the peak input current reaches the I_{OC1} threshold defined by R_{CS1}, the controller will automatically enter cycle-by-cycle input current limit which may cause V_{BUS} to droop below the minimum specification at the port. Cable compensation will not increase V_{BUS} in this condition as the input current (and therefore the input power) is limited.

Once the input sense resistor value is selected, the inductor saturation current rating (I_{SAT}) value can be chosen. The ISAT value must be higher than the input peak I_{LIM} threshold by some safe margin to avoid saturating the core.

$$I_{SAT} > I_{OC1_MAX}$$

$$I_{SAT} > \frac{V_{OC1_MAX}}{R_{CS1}}$$

Example:

R_{CS1} = 3mΩ and V_{OC1_MAX} = 60mV yields I_{OC1_MAX} = 20A, therefore:

I_{SAT} > 20A

Input Capacitor Design

The input capacitor reduces peak currents drawn from the power source and minimizes noise and voltage ripple on the input caused by the circuit switching. In buck mode, input current is discontinuous with maximum ripple. The RMS current can be calculated using the following equation:

$$I_{RMS} = \frac{I_{OUT_MAX} \cdot \sqrt{V_{OUT} \cdot (V_{IN} - V_{OUT})}}{V_{IN}} \quad \text{(eq. 6)}$$

The maximum input RMS current occurs at V_{IN} = 2 x V_{OUT}. Substituting V_{IN} previously, the equation then becomes:

$$I_{RMS_MAX} = \frac{I_{OUT_MAX}}{2} \quad \text{(eq. 7)}$$

The input voltage ripple in buck mode is given by:

$$\Delta V_{IN} = \frac{(1 - D_{BUCK}) \cdot I_{OUT} \cdot D_{BUCK}}{f_{SW} \cdot C_{IN}} \quad \text{(eq. 8)}$$

It is recommended to keep the input voltage ripple below 1% of the input voltage to limit noise that could be conducted through the battery harness.

Maximum input voltage ripple occurs in buck mode at a duty cycle of 50% and at maximum output current. Select a higher value for the final total capacitance to account for DC bias and tolerance derating.

Use the following equation to determine the input capacitance needed to meet the input voltage ripple requirement:

$$C_{IN} > \frac{0.25 \cdot I_{OUT_MAX}}{f_{SW} \cdot \Delta V_{IN_MAX} \cdot \left(1 - \left(C_{IN_TOL} + C_{IN_DCBIAS}\right)\right)} \quad \text{(eq. 9)}$$

Example:

f_{SW} = 400kHz; I_{OUT_MAX} = 5A; D_{BUCK} = 0.5; C_{IN_TOL} = 10%; C_{IN_DCBIAS} = 10%; ΔV_{IN_MAX} = 12V x 0.01 = 0.12V

For this example, C_{IN} > 27µF.

Select the input capacitor that can handle the given RMS current at the operating frequency. Ceramic capacitors come with extremely low ESR and help reduce the peak-to-peak ripple voltage at the input. Good quality electrolytic capacitors are also available with low ESR, which give higher capacitance at low cost.

Electrolytic (bulk) input capacitors help reduce input voltage droop during large load transients. ESR in bulk capacitors help dampen line transients. A good combination of electrolytic and ceramic capacitors can help achieve the target specifications and minimize cost.

Place a high-frequency decoupling ceramic capacitor to filter high di/dt and reduce EMI caused by Qt1 turn on. Choose a small package, such as 0402, with low ESL.

Choose a voltage rating of 50V for applications where a 40V load dump can be seen at the input.

Output Capacitor Design

Output capacitance is selected to satisfy the output load-transient requirements. During a load step, the output current changes almost instantaneously whereas the inductor is slow to react. During this transition time, the load-charge requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. Select a capacitor based on the maximum allowable overshoot/undershoot on the output voltage. Typically, the worst-case response from a load transient is in Boost mode. Use the following equations to contain the undershoot within the given specifications in Boost mode:

$$C_{OUT} \geq \frac{L \cdot \Delta I_{L_STEP}^{2}}{2 \cdot V_{IN_MIN} \cdot D_{BOOST_MAX} \cdot V_{UNDER}} + \frac{\left(\Delta I_{L_STEP} \cdot t_{DELAY}\right)}{V_{UNDER}} \quad \text{(eq. 10)}$$

where:

t_{DELAY} = time delay for the next control pulse after a load step. For fixed-PWM mode, t_{DELAY} is the turn-off time in buck/boost mode.

ΔI_{L_STEP} is the inductor current step during a load step.

Select the output capacitance to handle load transients in deep boost mode. t_{DELAY} is the delay for the PWM modulator to react after a load step. In PWM mode, the worst-case delay would be (1 - D) x tSW when the load step occurs right after a turn-on cycle. With the previous example values:

C_{OUT} ≥ 120µF

Once the output capacitance is selected, the output voltage undershoot/overshoot can be calculated for buck region of operation using the following equations:

$$V_{UNDER_BUCK} = \frac{L \cdot \Delta I_{L_STEP}^{2}}{2 \cdot (V_{IN} - V_{OUT}) \cdot D_{BUCK_MAX} \cdot C_{OUT}} \quad \text{(eq. 11)}$$

$$V_{OVER_BUCK} = \frac{L \cdot \Delta I_{L_STEP}^{2}}{2 \cdot V_{OUT} \cdot C_{OUT}} \quad \text{(eq. 12)}$$

Select C_{OUT} to ensure low output voltage undershoot and ripple during a USB PD load transient at low V_{IN}. V_{BUS} load transients requirements may vary depending on the application. Contact Analog Devices for assistance with optimizing C_{OUT} for your application.

Output Voltage Setting

V_{BUS} target is selected using the VBUS_NONDEFAULT_TARGET_L[7:0] and VBUS_NONDEFAULT_TARGET_H[7:0] register. When VBUS_HIRES = 0b then the LSB is 20.51mV (typ). When VBUS_HIRES = 1, then the LSB is 10.255mV (typ).

Once both registers are written, use the COMMAND[7:0] register to enable the buck-boost and request a new target V_{OUT} voltage. See the *Enabling/Disabling VBUS* section and Register Map for details.

Example:

To program V_{OUT} at 15V with VBUS_HIRES = 0b then write VBUS_NONDEFAULT_TARGET_L[7..0]=EEh and VBUS_NONDEFAULT_TARGET_H[7..0]=02h.

Current-Sense Resistors Selection

The MAX25432 devices use three external current-sense resistors to provide current information for several functions. The input current-sense resistor R_{CS1} is used for inductor current control and setting the input cycle-by-cycle peak current limit. The output current-sense resistor R_{CS2} is used for output runaway and negative peak current limit. The R_{CS3} current-sense resistor is used for output DC current-sense and cable compensation. It is highly recommended that designs use an R_{CS3} resistor with an exact value of 5mΩ.

Select an input current-sense resistor based on the maximum input current for the application (typically at maximum output power and minimum input voltage). The voltage across R_{CS1} for input current-limit is 50mV (typ). Calculate the peak input current using this equation:

$$I_{IN_PEAK} = \frac{V_{OUT_MAX} \cdot I_{OUT_MAX}}{V_{IN_MIN}} + \frac{V_{IN_MIN} \cdot \left(1 - \frac{V_{IN_MIN}}{V_{OUT_MAX}}\right)}{2 \cdot L \cdot f_{SW}} \quad \text{(eq. 13)}$$

Calculate the input current-sense resistor (R_{CS1}) by setting the peak current limit slightly higher than the peak input current (I_{IN_PEAK}) calculated in equation 13.

Note: The MAX25432 uses a very fast cycle-by-cycle analog comparator for the peak input current limit with equal rising and falling thresholds.

Slope Compensation

Slope compensation is required for current-mode control due to its inherent instability. A properly designed current-mode control with slope compensation removes the instability and provides noise immunity from current-sense signals. The MAX25432 offers a simple way to set the slope compensation peak ramp voltage (V_{SLOPE_PK}) by programming the SLP[2:0] register through I^2C from 100mV to 800mV in 100mV increments. Once V_{SLOPE_PK} is calculated, select the next higher value available in the SLP[2:0] register.

The steps to calculate V_{SLOPE_PK} are the following.

Design the slope compensation to lower the quality factor of the double pole at half the switching frequency of current-mode control. Choose the quality factor to be at or below 0.6 for the entire range of input and output voltages. The quality factor is given by the following equation:

$$Q_P = \frac{1}{\pi \cdot (m_C \cdot D' - 0.5)} \quad \text{(eq. 14)}$$

where m_C, the compensation ramp factor, is given by:

$$m_C = 1 + \frac{S_e}{S_n} \quad \text{(eq. 15)}$$

The compensation ramp slope, S_e, is:

$$S_e = \frac{V_{SLOPE_{PK}}}{T_{SW}} = V_{SLOPE_{PK}} \bullet f_{SW} \quad \text{(eq. 16)}$$

And the inductor rising slope, S_n, is:

$S_n = \frac{(V_{IN}-V_{OUT})\cdot G_{CS}}{L}$ (eq. 17)

S_e = Slope of the external ramp, in V/s

S_n = Rising slope (upslope) of inductor current, in V/s

V_{SLOPE_PK} = Slope compensation peak ramp voltage for a theoretical 100% duty cycle, in V

f_{SW} = Switching frequency, in Hz

D' = 1 – duty cycle

Example:

Due to the several possible output voltages, an optimum SLP[2:0] setting needs to be calculated for each fixed output voltage supported. Verify Q_p does not exceed the design target across the input voltage range. From the previous example, and with a maximum Q_p target of 0.6, we can calculate the optimum SLP[2:0] for V_{OUT} = 5.15V.

Using equation 14, Q_p = 0.4 yields m_c = 1.82. With equation 17, we find S_n = 1.89.105V/s. Then, equation 15 gives us S_e = 1.54.105V/s. Finally, rearranging equation 16, we find V_{SLOPE_PK} = 385mV.

Set SLP[2:0] to achieve the desired peak-to-peak voltage for the external compensation as calculated above.

Select Set SLP[2:0] = 0b011 for V_{SLOPE_PK} = 400mV.

Repeat the steps above for each output voltage supported.

Voltage Loop Compensation Design (V_{COMP})

The MAX25432 uses an internal transconductance error amplifier in the voltage loop with its output terminal available to the user for external frequency compensation, as shown in *Figure 37*.

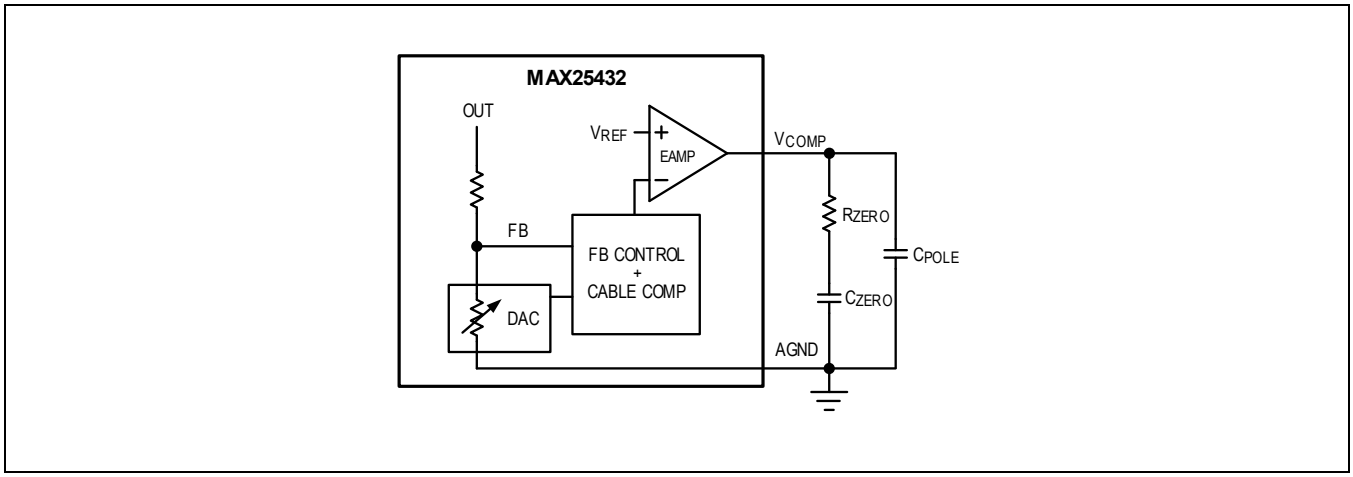


Figure 37. External Voltage Compensation Network (V_{COMP})

The controller uses a peak current-mode-controlled architecture to regulate the output voltage by forcing the required current through the external inductor. The external current-sense resistor senses the inductor current signal. The current-mode control splits the double pole in the feedback loop caused by the inductor and output capacitor into two single poles. One of the poles is moved to a high frequency outside of the typical bandwidth of the converter, making it a single-pole system. This makes compensation easy with only Type II compensation network. In boost mode, an extra right-half plane (RHP) zero is introduced by the power stage, which adds extra phase delay in the control loop. To avoid any significant effect of the RHP zero on the converter stability, the compensation is designed such that the bandwidth is approximately 1/4 of the worst-case RHP zero frequency.

The design of external compensation requires some iterations to reach an optimized design. Care must be taken while designing the compensation for working in 'deep' boost mode and heavy load (V_{IN_MIN} as RHP zero frequency reduces.

A convenient way to design compensation for both buck and boost modes is to design the compensation at minimum input voltage and heavy load (deep boost mode). At this operating point, RHP zero is at its lowest frequency. Design the compensation to achieve a bandwidth close to 1/4 of the RHP zero frequency in deep boost mode. Verify the gain and phase margin with the designed compensation in buck mode. The closed-loop gain of the converter is a combination of the power-stage gain of the converter and error-amplifier gain.

The following equation demonstrates the current-mode-controlled boost power-stage transfer function:

$$\frac{\hat{V_O}}{\hat{V_C}} = \frac{R_L \cdot (1-D)}{2 \cdot G_{CS}} \cdot \frac{\left(1+\frac{s}{\omega_{ESR}}\right)\left(1-\frac{s}{\omega_{RHP}}\right)}{\left(1+\frac{s}{\omega_{P_{BOOST}}}\right) \cdot F_H(s)} \quad \text{(eq. 18)}$$

where:

G_{CS}: current-sense gain = $23.R_{CS1}$

$$\omega_{P_{BOOST}} = \frac{2}{R_L \cdot C_{OUT}} \quad \text{(eq. 19)}$$

$$\omega_{ESR} = \frac{1}{R_C \cdot C_{OUT}} \quad \text{(eq. 20)}$$

$$\omega_{RHP} = \frac{R_L \cdot (1-D)^2}{L} \quad \text{(eq. 21)}$$

$$F_H(S) = 1 + \frac{S}{\omega_N \cdot Q_P} + \left(\frac{S}{\omega_N}\right)^2 \quad \text{(eq. 22)}$$

$$Q_P = \frac{1}{\pi \cdot (m_C \cdot D' - 0.5)} \quad \text{(eq. 23)}$$

$$\omega_N = \frac{\pi}{T_{SW}} \quad \text{(eq. 24)}$$

Error-amplifier transfer function:

$$H_{EA}(S) = g_M \cdot R_{DC} \cdot \frac{\left(1+\frac{s}{\omega_{Z_{COMP}}}\right)}{\left(1+\frac{s}{\omega_{P1_{COMP}}}\right) \cdot \left(1+\frac{s}{\omega_{P2_{COMP}}}\right)} \quad \text{(eq. 25)}$$

$$\omega_{Z_{COMP}} = \frac{1}{R_{ZERO} \cdot C_{ZERO}} \quad \text{(eq. 26)}$$

$$\omega_{P1_{COMP}} = \frac{1}{R_{DC} \cdot C_{ZERO}} \quad \text{(eq. 27)}$$

$$\omega_{P2_COMP} = \frac{1}{R_{ZERO} \cdot \left(\frac{C_{POLE} \cdot C_{ZERO}}{C_{POLE}+C_{ZERO}}\right)} \cong \frac{1}{R_{ZERO} \cdot C_{POLE}} \quad \text{if } C_{POLE} \ll C_{ZERO} \quad \text{(eq. 28)}$$

Closed loop gain = Power stage gain x EA gain

Example:

Start the compensator design by calculating the critical frequencies for the boost power stage at the minimum input voltage and maximum load.

$$f_{PBOOST} = \frac{2}{2\pi \cdot R_L \cdot C_{OUT}} \quad \text{(eq. 29)}$$

$$f_{ESR} = \frac{1}{2\pi \cdot R_C \cdot C_{OUT}} \quad \text{(eq. 30)}$$

For a converter operating in boost mode, the inductor selection determines the RHP frequency and hence the stability of converter in deep boost mode. Calculate the RHP zero frequency in deep boost mode using the calculated inductor value.

$$f_{RHP} = \frac{R_L \cdot (1-D_{BOOST_MAX})}{2\pi \cdot L_{MAX}} \quad \text{(eq. 31)}$$

where:

R_L = Output load in Ω; $R_L = \frac{V_{OUT}}{I_{OUT}}$

C_{OUT} = Output capacitance in F, chosen to be 214µF

R_C = Output capacitor ESR in Ω, chosen to be 3.5mΩ

D_{BOOST_MAX} = Maximum duty cycle in boost mode calculated earlier

L = Inductance value calculated earlier, in H

Using above values, we find f_{PBOOST} = 372Hz, f_{ESR} = 213kHz, and f_{RHP} = 9.2kHz.

With RHP zero at 9.2kHz, the loop cutoff frequency for a stable operation must be less than 1/4 of the RHP zero frequency in deep boost mode.

Therefore, a target bandwidth for the closed-loop converter close to 1.8kHz is selected. The zero of the error amplifier must be placed well below the bandwidth to give enough phase boost at the crossover frequency. Typically, the zero is placed close to the low-frequency pole. In such a case, resistor (R_{ZERO}) of the compensation can be calculated using the following equation:

$$R_{ZERO} = 2\pi \cdot f_{BW_BOOST} \cdot \frac{G_{CS} \cdot C_{OUT}}{g_m \cdot (1 - D_{BOOST_MAX})} \cdot \frac{(R_{BOT} + R_{TOP})}{R_{TOP}} \text{ (eq. 32)}$$

where:

f_{BW_BOOST} = Desired converter bandwidth in boost mode

g_m = Error-amplifier transconductance, 854µS, typ (or A/V)

R_{TOP}, R_{BOT} = Top and bottom internal feedback network resistances, in Ω

R_{TOP} = 96kΩ

$$R_{BOT} = \frac{R_{TOP}}{\frac{V_{OUT_MAX}}{1.25V} - 1} \text{ (eq. 33)}$$

Choosing f_{BW_BOOST} = 1.8kHz yields R_{ZERO} = 11kΩ

And with f_{ZCOMP} chosen to be 1.2kHz (below the converter's bandwidth),

$$C_{ZERO} = \frac{1}{R_{ZERO} \cdot 2\pi \cdot f_{ZCOMP}} \text{ (eq. 34)}$$

Therefore, C_{ZERO} = 12nF.

C_{POLE} determines the location of high-frequency pole. Select the high-frequency pole location higher than the bandwidth in buck mode so that it does not affect the phase margin and helps attenuate any high-frequency noise.

For f_{P2COMP} = 140kHz,

$$C_{POLE} = \frac{1}{R_{ZERO} \cdot 2\pi \cdot f_{P2COMP}} \text{ (eq. 35)}$$

which yields C_{POLE} = 100pF.

For this example, the following component values would be selected: R_{ZERO} = 11kΩ, C_{ZERO} = 12nF, and C_{POLE} = 100pF.

Current Loop Compensation Design (I_{COMP})

The MAX25432 includes a transconductance error amplifier in the current loop that requires external frequency compensation.

The current loop frequency crossover is targeted just above the cable compensation loop frequency of 1kHz. This results in the fixed compensation components shown in the *Typical Application Circuits.*

External MOSFET Selection

Four external MOSFETs are required for the H-bridge buck-boost architecture supported by the MAX25432, as shown in the *Typical Application Circuits*. During the buck-mode of operation, Q_{t2} remains on and Q_{b2} remains off. Q_{t1} and Q_{b1} switch to regulate the output voltage. During the boost mode, Q_{t1} remains on, Q_{b1} remains off, and Q_{t2} and Q_{b2} switch to regulate the output voltage. In the buck-boost region, all four switches are used to control the output voltage. The MOSFETs must be selected based on certain critical parameters such as on-resistance, breakdown voltage, output

capacitance, and input capacitance. A low R_{DSON} reduces the conduction losses in the MOSFET and a small gate/output capacitance reduces switching losses. Typically, a lower R_{DSON} MOSFET would have higher gate charge for the same breakdown voltage. Hence, a compromise must be made depending on conditions to which the MOSFET is subjected.

The MAX25432 comes with a 5V gate drive with a high-current capability to support switching of four MOSFETs at a high frequency. In the buck-boost region, the device switches between pure buck and boost modes to reduce the gate-drive current and increase the efficiency.

Boost Cap and Diode Selection

A bootstrap circuit is used to drive the floating gates of high-side switches Q_{t1} and Q_{t2}. A boost capacitor provides the gate charge to the high-side FET during the high-side turn-on and is recharged when the bottom switch turns on. Hence, the capacitance value of the boost capacitor must be selected such that the voltage drop during the discharge is within acceptable limits. Choosing a very large capacitor value slows down the charging of the capacitor, and it might not completely charge in the minimum off-time of the top switch.

Select the boost diode based on the average gate-drive current and blocking voltage for the diode. The maximum blocking voltage for the diode must be high enough to block the maximum drain-to-source voltage for the FET. A fast reverse-recovery diode would prevent any current being sourced into the bias supply from drain-to-source voltage. For the MAX25432 devices, the gate drive is powered by the BIAS regulator, which is 5V (typ).

Since the boost capacitor provides gate charge to the top switch, the value of the boost capacitance needed for less than a ΔV_{BOOST} ripple on boost capacitor can be written as:

$$C_{BOOST} \geq \frac{Q_G}{\Delta V_{BOOST}} \text{ (eq. 36)}$$

Average gate-drive current through the diode can be calculated as:

$I_G = Q_G \bullet f_{SW}$ (eq. 37)
where:

Q_G = Total gate charge of the top MOSFET

Shield Short-to-Battery

The shield short-to-battery protection circuit requires that the total ground-path resistance from USB ground to system ground is in the range of 10mΩ to 13mΩ. This is required to achieve the correct threshold detection values and avoid false detection or surge currents larger than desired. Contact Analog Devices for support in selecting a FET outside this R_{DSON} range for your application.

An N-channel FET with V_{DS} = 40V (min) must be chosen. The 1nF shield capacitor must be rated for 50V (min).

A single NVTFS5C466NLTAG can be used as a FET meeting those requirements.

USB Cable Compensation

Contact Analog Devices to request a calculator to help in cable compensation for your design.

Figure 38 shows a DC model of the voltage-correction function of the MAX25432.

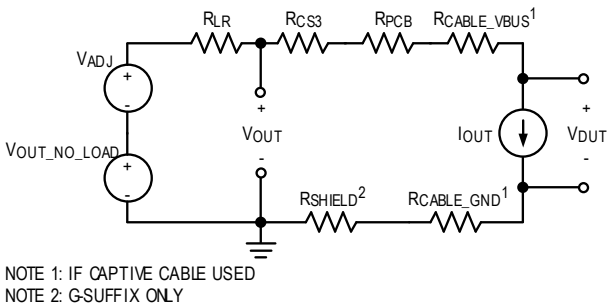


Figure 38. DC Voltage Adjustment Model

Without voltage adjustment (V_{ADJ} = 0, GAIN[5:0] = 0), the voltage seen by the device at the end of the captive cable (V_{DUT}) will decrease linearly as load current increases. To compensate for this, the output voltage target of the buck-boost controller should increase linearly with load current (see *Figure 39*).

The increase in V_{OUT} over load current is called V_{ADJ}, such that:

$V_{ADJ} = R_{COMP} \cdot I_{OUT}$ (eq. 38)
And R_{COMP} is the slope of V_{OUT} over the load current:

$R_{COMP} = GAIN[5:0] \cdot R_{COMP_LSB} \cdot R_{CS3}/5m\Omega$ (eq. 39)
where:

R_{COMP_LSB} is the gain setting LSB and is equal to 8.2mΩ (typ).

The R_{COMP} adjustment discrete values available on the MAX25432 can be selected with the GAIN[5:0] register and are based on a 5mΩ sense resistor. Use equation 41 to select the appropriate setting based on the calculated R_{COMP} value.

The R_{COMP} value must be calculated to take into account all series element and voltage drops in the charging path, including ground return. User cable can be of different length and type, and therefore should not be included in the calculations.

For $V_{DUT} = V_{OUT_NO_LOAD}; 0 \le I_{OUT} \le 5A$, R_{COMP} must equal the sum of the system resistances. Calculate the minimum R_{COMP} for the system so that V_{DUT} stays constant:

$R_{COMP_SYS} = R_{LR} + R_{CS3} + R_{PCB} + R_{CABLE_VBUS} + R_{CABLE_GND}$ (eq. 40)
where:

R_{CABLE_VBUS} and R_{CABLE_GND} are the V_{BUS} and GND resistance of the USB captive cable, respectively (including the effect from the cable shield, if it conducts current).

R_{LR} is the converter's load regulation expressed in mΩ (2mΩ, typ).

R_{PCB} is the resistance of any additional V_{BUS} parasitics (PCB trace, ferrite, and the connector).

For G-suffix devices, R_{SHIELD} is the series resistance of the shield short-to-battery protection external FET and any PCB GND trace parasitics.

Find the setting for GAIN[5:0] using the minimum R_{COMP}:

$GAIN[5:0] = ceiling (R_{COMP_SYS} / R_{COMP_LSB})$ (eq. 41)

The nominal DUT voltage can then be estimated at any load current by:

$V_{DUT} = V_{OUT_NO_LOAD} + I_{OUT}(R_{COMP_LSB} \cdot GAIN[5:0] - R_{COMP_SYS})$ (eq. 42)

These equations presume a 5mΩ sense resistor, which is recommended. Use equation 39 to scale for other resistance values. Note that the V_{BUS} current limit and OCP threshold will be scaled with a factor of $5m\Omega/R_{CS3}$.

The nominal cable resistance (with tolerance) for both V_{BUS} and GND should be determined from the cable manufacturer. In addition, be sure to include the resistance from the connector at the end of the captive cable. Determine the desired operating temperature range for the application, and consider the change in resistance over temperature. Contact Analog Devices for assistance with optimizing the cable compensation for your application.

Example:

With R_{LR} = 2mΩ, R_{CS3} = 5mΩ, R_{PCB} = 40mΩ, R_{CABLE} = 150mΩ, R_{SHIELD} = 13mΩ, the total system resistance is then R_{COMP_SYS} = 210mΩ.

In this application, the voltage drop at the far end of the captive cable is 630mV when the load current is 3A. Therefore, cable compensation is required to comply with USB and Apple specifications.

The desired GAIN[5:0] register setting is then ceiling(210/8.2) = 25.6 = 0x1A, which sets the adjustment level to 208mΩ.

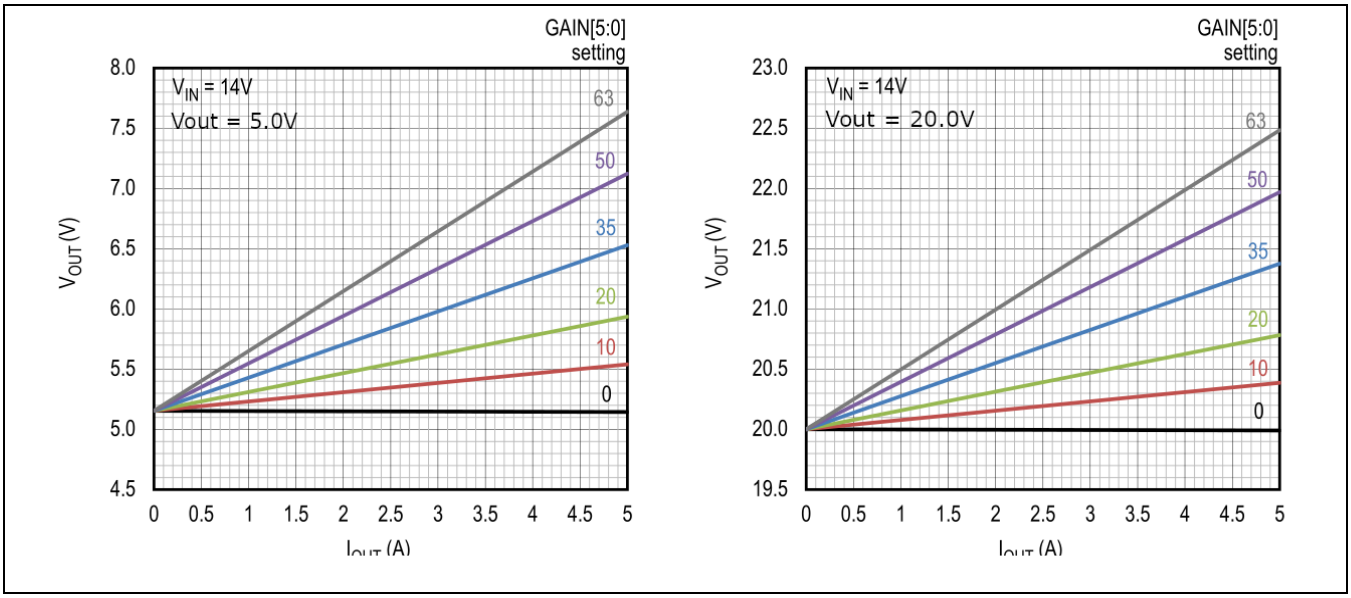


Figure 39. Increase in V_{OUT} vs. I_{OUT}

Capacitors on CC Lines

To comply with the USB PD specification, a cReceiver capacitance must be present on each CC line to ground when the BMC driver is not transmitting. Analog Devices recommends using 270pF ceramic capacitors to meet this requirement.

On MAX25432A, the capacitors can be placed on either the CC or HVCC side. On the MAX25432B, the capacitors should be placed on the HVCC side. See the *Typical Application Circuits* for details.

Table 13. cReceiver Specification from USB PD

NAME	MIN	MAX	UNIT
cReceiver	200	600	pF

Table 14. cReceiver Capacitance Breakdown

CAPACITANCE	MIN	MAX	UNIT
MAX25432 device capacitance on HVCC pins at +25°C	120	150	pF
External capacitor X7R 10% tolerance	243	297	pF
Total	363	447	pF

V_{CONN} Voltage Drop Budgeting

Care must be taken when designing a V_{CONN} source. Resistance in the V_{CONN} switch, PCB traces and connector will impact the voltage seen by the E-marked cable under load. This is even more important when using a 3.3V supply to provide V_{CONN} power. Use the following formula to estimate the V_{CONN} voltage drop from the power supply to the user's port (assuming no captive cable).

$$V_{CONN_DROP} = I_{VCONN} \cdot (R_{PCB1} + R_{ON} + R_{PCB2} + R_{CON}) = IV_{CONN} \cdot R_{VCONN_TOTAL} \text{ (eq. 43)}$$

where:

R_{PCB1}: The PCB trace resistance from the V_{CONN} source (DC-DC or LDO)

R_{ON} = MAX25432 V_{CONN} switch resistance

R_{PCB2} = PCB trace resistance from the HVCC pin of the MAX25432 to the Type-C receptacle

R_{CON} = Contact resistance of the Type-C receptacle CC pin

The Type-C specification requires the source to provide at least 3.0V under 1W of power at the receptacle for ports, including the SSTX/SSRX signals (USB 3.0 or higher), but also for V_{CONN}-powered USB devices (VPD) such as applications with remote LED lighting in a captive cable. For other applications where charging above 3A is needed, the V_{CONN} power required is 100mW at 3.0V.

Table 15. V_{CONN} Requirements

	PORT FEATURES		V_{CONN} POWER REQUIRED
D+/D-	SSTX/SSRX, VPD	>3A	
No	No	No	Not required
Yes	No	No	Not required
Yes	Yes	No	1W
No	No	Yes	100mW
Yes	No	Yes	100mW
Yes	Yes	Yes	1W

For a given V_{CONN} power and voltage to meet at the port, the required current is calculated:

$$I_{\mathrm{VCONN_{PMIN}}} = \frac{P_{\mathrm{MIN}}}{V_{\mathrm{DUT_{MIN}}}} = \frac{1W}{3.0V} = 0.33A \quad \text{(eq. 44)}$$

The minimum V_{CONN} supply voltage needed to guarantee V_{DUT_MIN} at P_{MIN} at the receptacle is:

$VCC_{MIN} = V_{DUT_MIN} + R_{VCONN_TOTAL} \cdot I_{VCONN_PMIN}$ (eq. 45)

Example:

R_{PCB1} = 10mΩ; R_{ON_MAX} = 600mΩ; R_{PCB2} = 20m; R_{CON} = 40m

VCC_{MIN} = 3.22V

For a 3.3V supply with a 2% output voltage tolerance, the lowest voltage supplied is:
$VCC_{LOW} = VCC_{TYP} \cdot (1-VCC_{TOL}) = 3.3 \cdot (1-0.02) = 3.234V > VCC_{MIN}$ (eq. 46)

PCB Layout Guidelines

Refer to the EV kit for a complete layout reference. Contact Analog Devices to request for a review of your design.

Buck-Boost PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and low-noise, stable operation. Use a multilayer board whenever possible for best noise immunity and thermals.

Use the following guidelines and see *Figure 40* for an optimized buck-boost layout:

- Arrange the high-power components in a compact layout away from the sensitive signals, such as the current-sense and gate-drive signals, to avoid stray noise pickup.
- Place the input capacitor and the input current-sense resistor close to the input MOSFETs (Q_{t1} and Q_{b1}) to make a small input current AC loop. High-frequency AC currents flow in this loop in buck mode and a small loop helps with the EMI and noise performance. Add high-frequency decoupling capacitors to improve the high-frequency performance.
- Place the output capacitor and the output current-sense resistor close to the output MOSFETs (Q_{t2} and Q_{b2}) to make a small output-current AC loop. High-frequency AC currents flow in this loop in boost mode and a small loop helps with the EMI and noise performance. Add high-frequency decoupling capacitors to improve the high-frequency performance.

- The switching nodes (LX1 and LX2) carry high-frequency, high-current switching signals. Make LX1 and LX2 areas small to reduce parasitic inductance in the switching nodes. Since high currents flow through these nodes, a compromise must be made between thermal dissipation and noise mitigation.
- Route CSP1/CSN1 and CSP2/OUT/CSN2 current sense lines on the same layer, preferably inner layer and with as much ground shielding to protect from noisy signals. Use a Kelvin sense connection for the current-sense resistors and route the sense traces close to each other to ensure a balanced measurement of the differential signal. Route these traces away from noisy signals, such as the MOSFETs gate drive outputs (LX, DH, DL)
- Route the MOSFET gate drive outputs away from sensitive signals, such as CSA sense traces. It is recommended to route gate drive outputs in an inner layer to not interrupt ground plane near the power stage as well as to provide shielding since these traces have high di/dt during MOSFET turn-on and turn-off. Do not run adjacent to or overlap sensitive traces. Route DH1 alongside LX1 and DH2 alongside LX2 to minimize loop area on high side drivers. Route DL1 and DL2 adjacent to a ground trace or plane to minimize loop area on low side drivers. Use appropriate trace width and length to minimize parasitic inductance which may cause ringing. Connect LX1 and LX2 traces to the MOSFET rather than the inductor. Avoid using more than two layers for routing gate drive outputs and limit the number of vias in series to two per trace.
- Using internal PCB layers as a ground plane helps to improve EMI performance. A solid ground plane immediately below the top layer acts as a shield against radiated noise. Have multiple vias spread around the board, especially near the ground connections, to have better overall ground connection.
- Connect the PGND and AGND pins directly to the exposed pad under the IC. This ensures the shortest connection path between AGND and PGND.
- Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as a heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add several small vias or one large via on the copper pad for efficient heat transfer.
- Place the BIAS ceramic capacitor as close as possible to the BIAS pin. The BIAS pin carries significant transients and supplies everything in the IC. Low inductance from the pin to the capacitor and low inductance to the GND return plane is key. Pay extra care in reducing parasitic inductance to reduce EMI. As the AGND pin is located after the IN and V_{COMP} and I_{COMP} pins, a trade-off must be made. Always give more importance to the BIAS capacitor placement over the IN-pin decoupling capacitor and compensation networks, as it helps filter out high di/dt switching currents.
- Place the compensation network components close to the V_{COMP} and I_{COMP} pins. Minimize trace inductance and provide a short ground return path using several vias to the ground plane underneath. Place the compensation network components away from the power stage in order to prevent high-frequency switching noise to couple into the feedback loop.
- Place the bootstrap capacitors close to the respective BST and LX pins to minimize inductance.
- Leave the option to place series gate and BST resistors on the PCB to mitigate possible EMI issues at a later design stage.
- Place the 100nF and 1µF ceramic capacitor close to the IN pin with a short path to the ground layer underneath. Place the 100nF capacitor closer to the pin.
- Place vias as close to the AGND pins as possible to provide a low impedance path to the ground plane underneath. *Figure 40* shows a recommended PCB layout for the buck-boost.

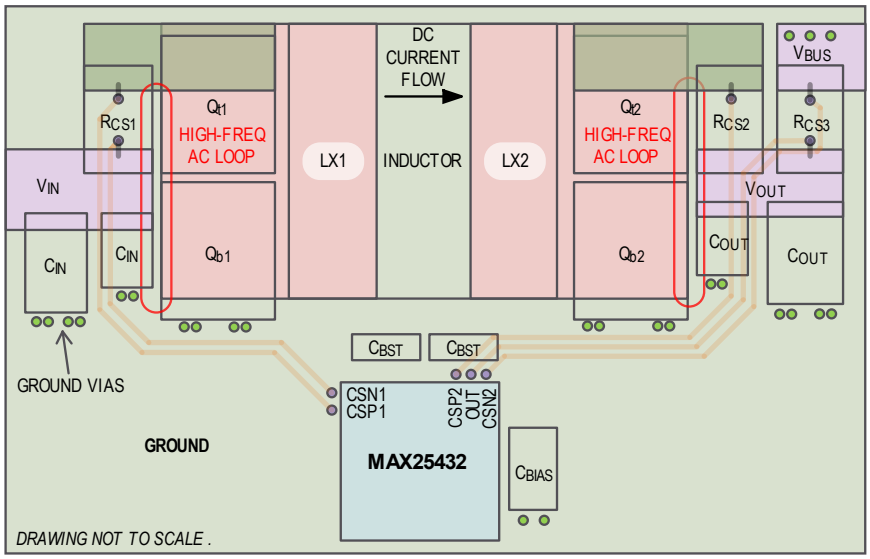


Figure 40. Recommended Buck-Boost PCB Layout

USB PCB Layout Guidelines

Use the following guidelines for an optimized layout on USB-related IC pins:

4. Place the V_{DD_USB} ceramic capacitor close to the respective pin and with a low impedance to ground. Use vias to the ground plane underneath. The V_{DD_USB} capacitor helps provide a low-impedance AC return path to ground during OV transients or ESD events on the USB data protection switches.
5. Place the V_{CONN} ceramic capacitor close to the respective pin and with a low impedance to ground. Use vias to the ground plane underneath. The V_{CONN} capacitor helps provide a low impedance AC return path to ground on the respective HVCC pin during a V_{CONN} short-to-V_{BUS} event. The V_{CONN} capacitor also helps minimize droop on the upstream supply during high inrush current events such as capacitive load switching or a hot STG event.
6. Keep the HVCC traces large and short to minimize V_{CONN} voltage drop from the MAX25432 to the Type-C receptacle.
7. See the *USB Eye Diagram* section for recommendations when the MAX25432 is used in the USB Hi-Speed signal path.
8. On MAX25432B devices, place the V_{DD_BMC} ceramic capacitor close to the respective pin with a low impedance to ground. Use vias to the ground plane underneath.

Shield Short-to-Battery PCB Layout Guidelines

The shield FET should be placed as close as possible to the Type-C connector and must be connected to the connector with a plane. Where the FET's source connects to the PCB system ground, there should be several vias placed for a low-impedance path to ground. The 1nF capacitor from SHLD_SNS to system ground should also be placed close to the Type-C connector. Keep the SHLD_SNS Kelvin sense line away from switching traces or planes.

Figure 41 shows a recommended layout for the shield short-to-battery feature.

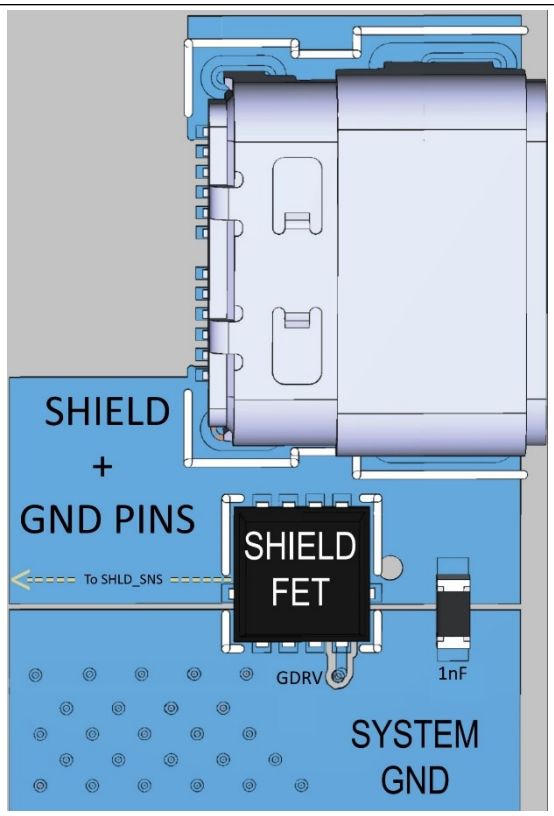


Figure 41. Recommended Shield Short-to-Battery Component Layout

USB Eye Diagram

USB Hi-Speed mode requires careful PCB layout with 90Ω controlled differential impedance, having matched traces of equal length, minimum vias, and no stubs or test points. The MAX25432 includes high-bandwidth USB data switches (>1GHz). This means that data-line tuning is generally not required.

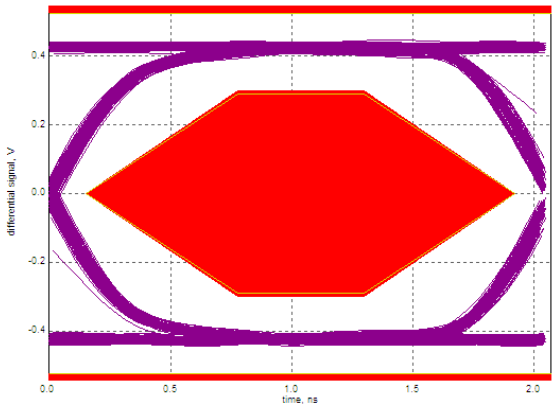


Figure 42. Near-Eye Diagram (with No MAX25432)

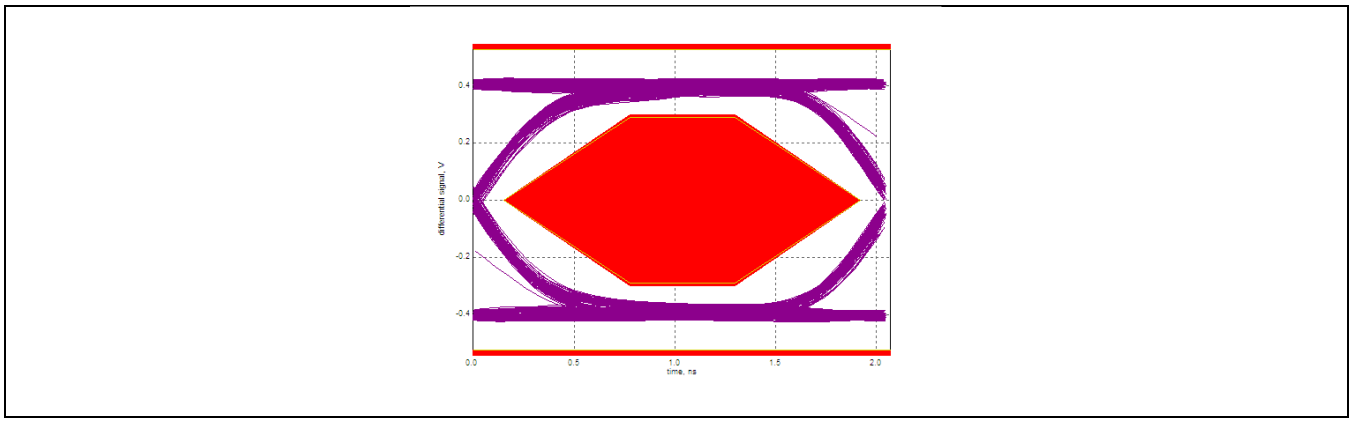


Figure 43. Untuned Near-Eye Diagram (with MAX25432)

System-Level ESD Protection

The MAX25432 requires no external system-level ESD protection. All ADI devices incorporate ESD protection structures to protect against electrostatic discharges encountered during handling and assembly. After an ESD event, the MAX25432 continues to work without latch-up, while competing solutions can latch up and require the power to be cycled. When used with the configurations shown in the *Typical Application Circuits*, the MAX25432 is characterized for protection to the following limits:

- ±15kV IEC 61000-4-2 (150pF, 330Ω) Air-Gap Discharge
- ±8kV IEC 61000-4-2 (150pF, 330Ω) Contact Discharge
- ±15kV ISO 10605 (330pF, 2kΩ) Air-Gap Discharge
- ±8kV ISO 10605 (330pF, 2kΩ) Contact Discharge

Note: All application-level ESD testing is performed on the standard EV kit.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Analog Devices for test setup, test methodology, and test results.

Human Body ESD

Figure 44 shows the Human Body Model, and *Figure 45* shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

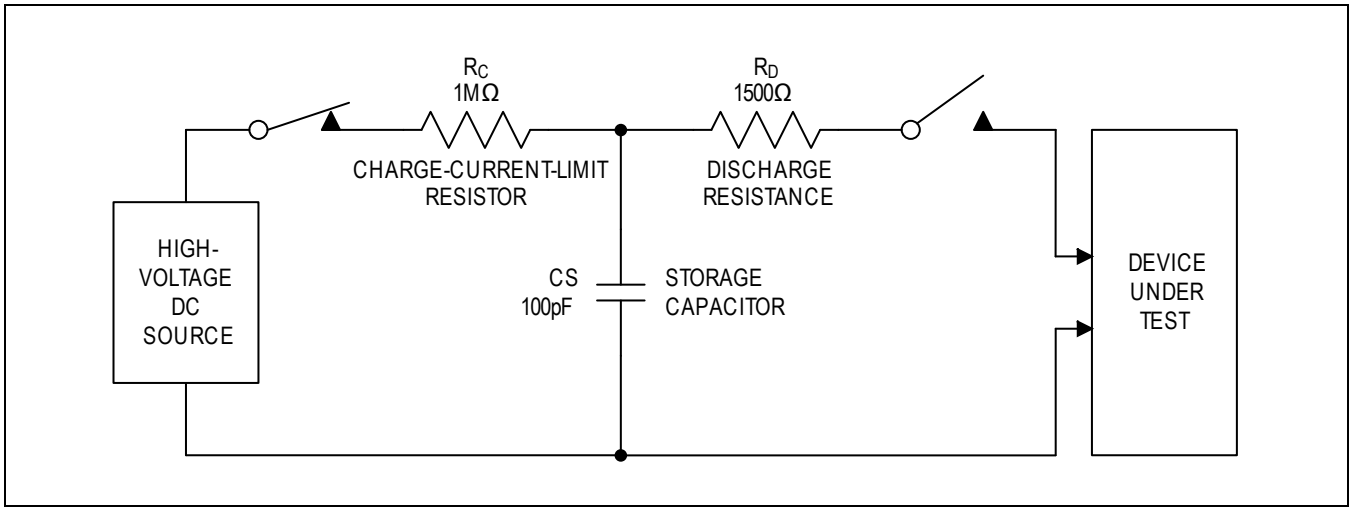


Figure 44. Human Body ESD Test Model

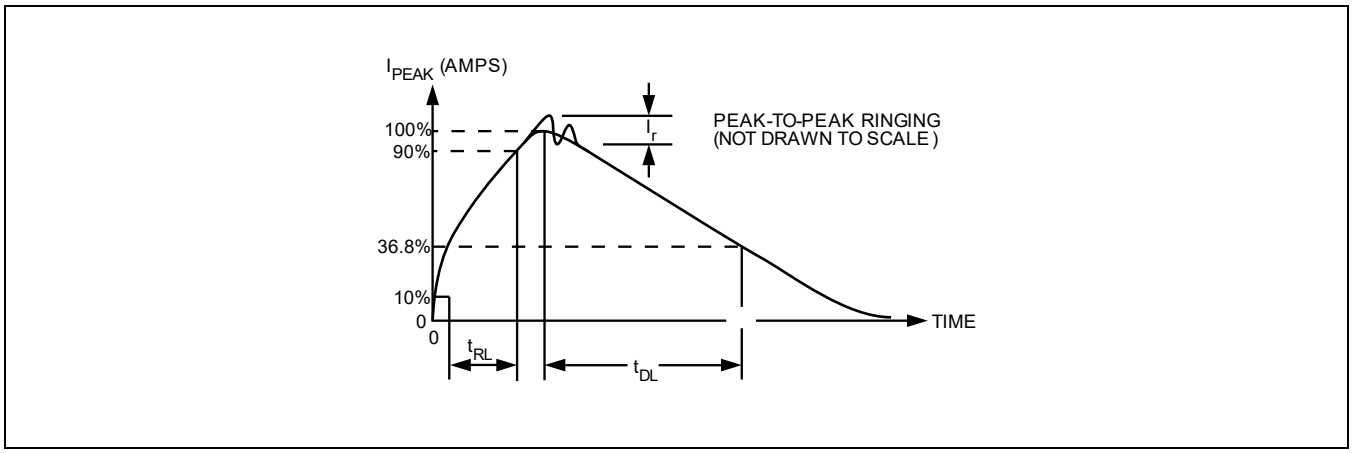


Figure 45. Human Body Current Waveform

IEC 61000-4-2 ESD

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX25432 helps users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. Because the series resistance is lower in the IEC 61000-4-2 ESD test model *Figure 46*, the ESD withstand-voltage measured to this standard is generally lower than that measured using the Human Body Model. *Figure 47* shows the current waveform for the 8kV, IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

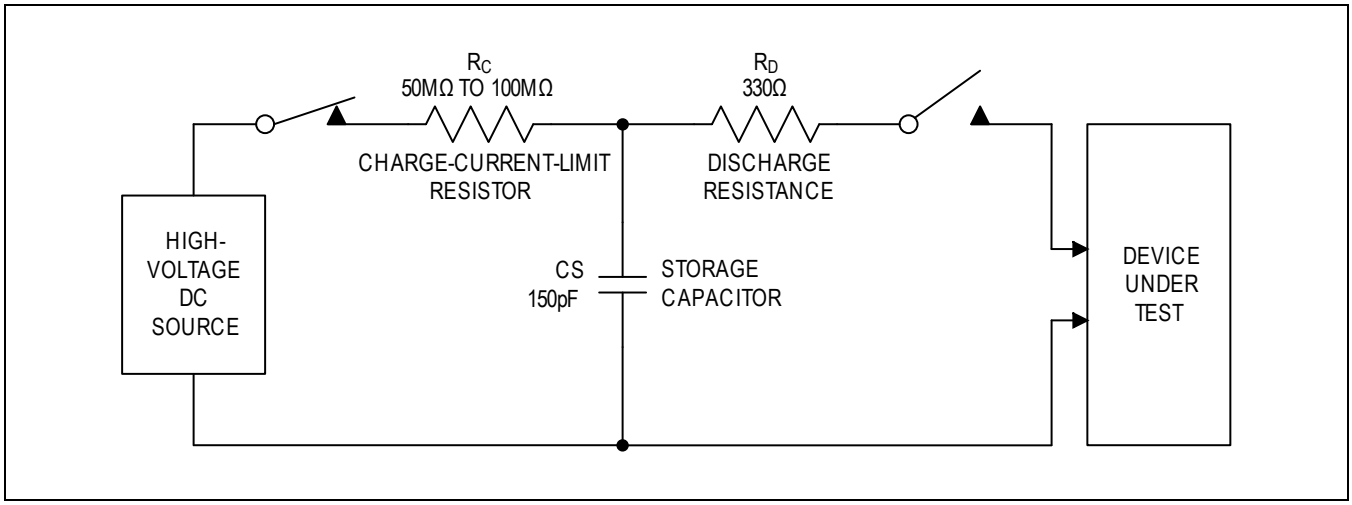


Figure 46. IEC 61000-4-2 ESD Test Model

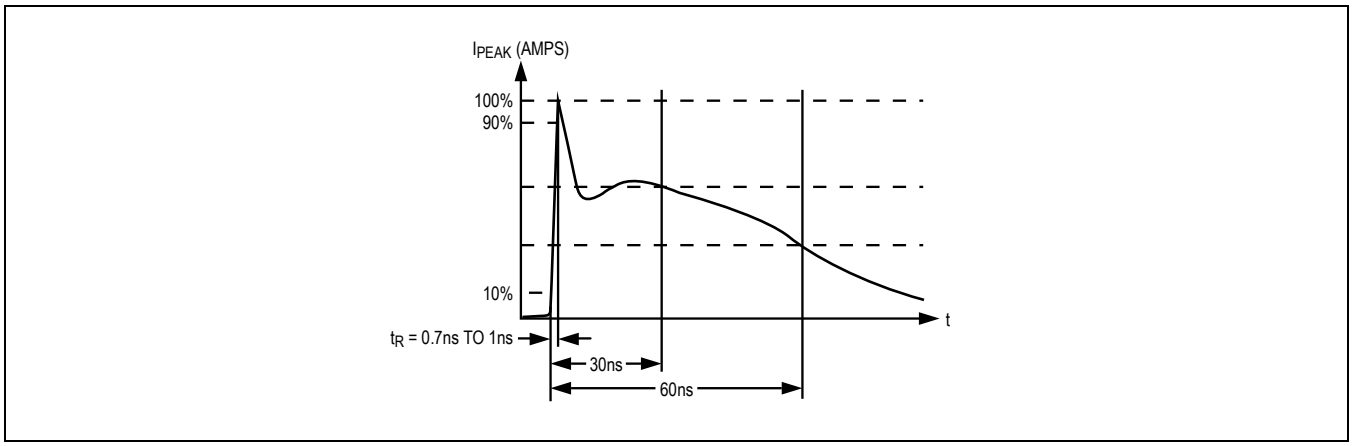
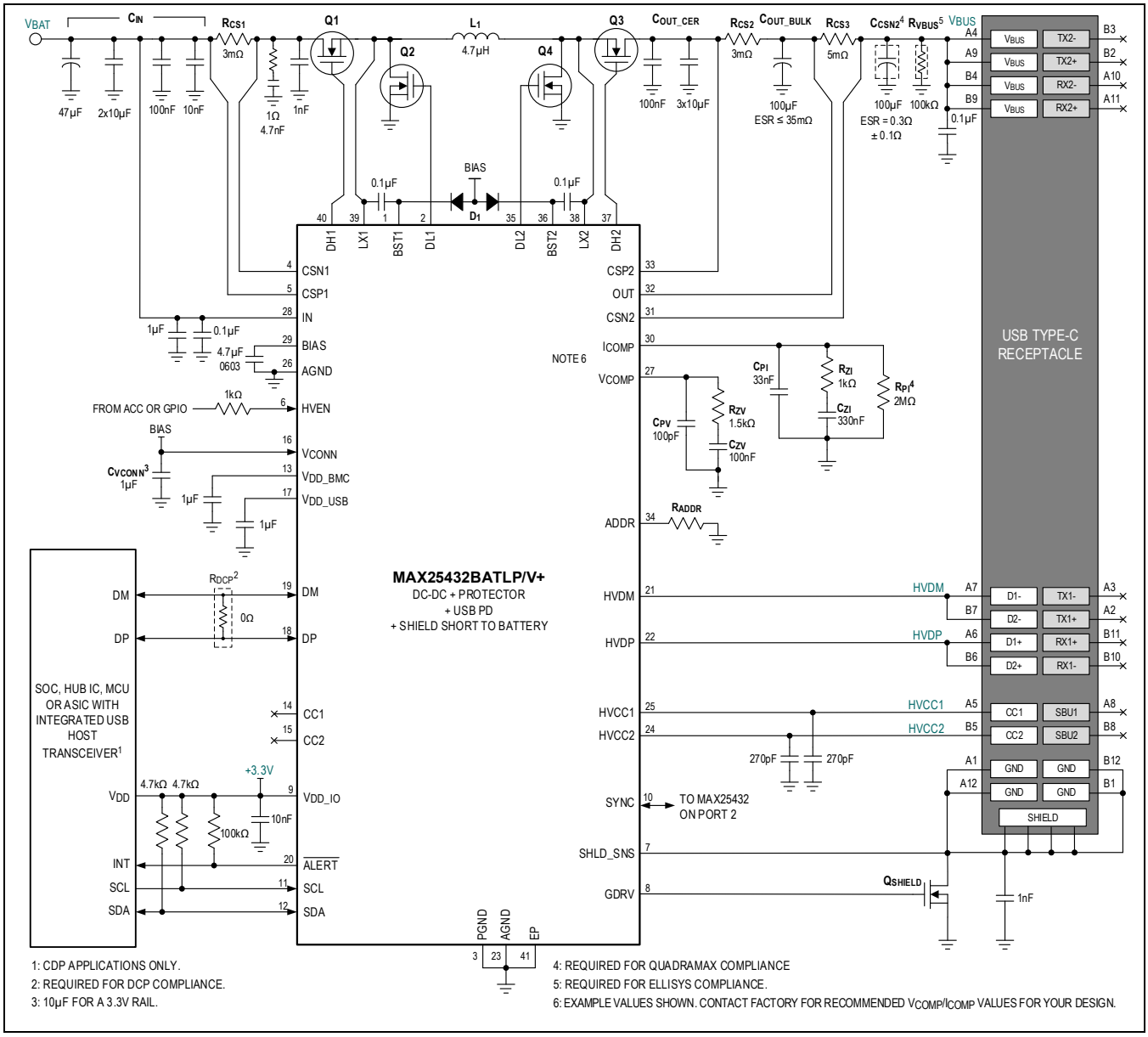


Figure 47. IEC 61000-4-2 Current Waveform

Typical Application Circuits

MAX25432B Application Diagram

This figure shows the MAX25432BATLP/V+ with an external TCPM in a 100W single-port USB PD PPS application operating at 400kHz.



Ordering Information

PART NUMBER	TEMP RANGE	USB PD ARCHITECT.	SHIELD SHORT-TO-BATTERY PROTECTION (SSTB)	NORMALLY OPEN GROUND[2]	USB PD PHY GROUND OFFSET COMPENSATION[3]	ADVANCED MONITORING ALGORITHMS	PIN-PACKAGE
MAX25432BATLP/V+	-40°C to +125°C	Integrated[1]	Yes	Yes	130mV (max)	Yes	40-pin TQFN-EP
MAX25432BATLG/V+		Integrated[1]	Yes	Yes	130mV (max)	No	
MAX25432BATLM/V+		Integrated[1]	No	Yes	800mV (max)	No	

For variants with different options, contact factory.

/V+ Denotes automotive-qualified parts.

For tape-and-reel versions, add the suffix 'T' to the end of the part number (i.e., MAX25432BATLP/V+T).

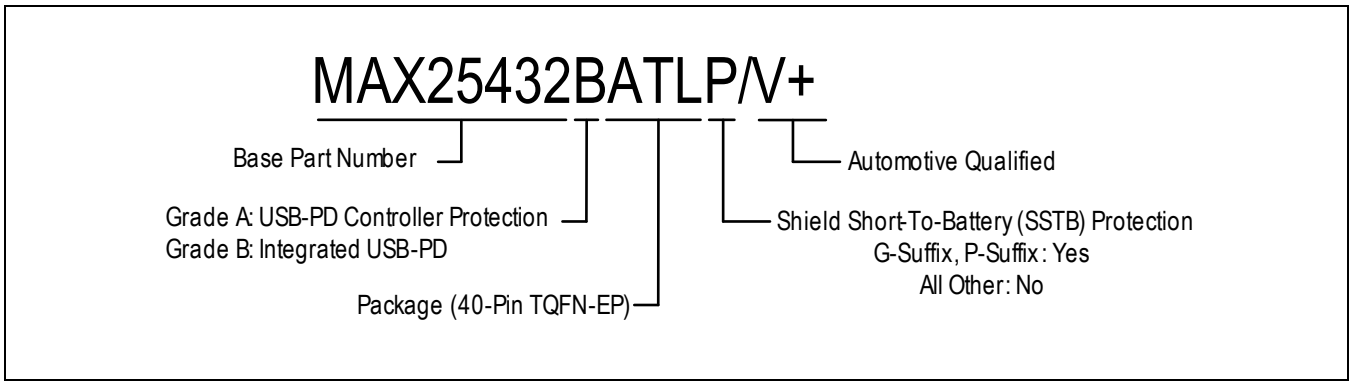
+ Denotes a lead(Pb)-free/RoHS compliant package.

1 Variant with integrated USB PD BMC analog front-end (TCPC) for use with an external I^2C controller which contains the USB PD FW stack (TCPM).

2 Downstream connector ground is automatically opened or closed based on Table 6.

3 Features a BMC Tx/Rx GND compensation circuit that lifts the BMC driver ground reference to reduce offset due to charging current.

Part Number Breakdown



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	09/21	Initial release	—
1	12/23	Added MAX25432BATLP/V+; updated front page, various block diagrams, registers description, I2C terminology, fault table, Updated Register Map descriptions, layout guidelines	All

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