19-4822; Rev 0; 7/09

EVALUATION KIT AVAILABLE

TMDS Digital Video Equalizer for HDMI/DVI Cables

MAX3815A

General Description

The MAX3815A cable equalizer automatically provides compensation for DVI™ and HDMI™ v1.3 cables. It extends the usable cable distance up to 40 meters (1.65Gbps) and 35 meters (2.25Gbps). The MAX3815A is designed to equalize signals encoded in the transition-minimized differential signaling (TMDS®) format.

The MAX3815A features four CML-differential inputs and outputs (three data and one clock). It provides a loss-of-signal (LOS) output that indicates loss-of-clock signal. The outputs include a disable function. Upon LOS, the chip is powered down. For direct chip-to-chip communication, the output drivers can be switched to one-half the DVI output specification to conserve power and reduce EMI. The output drive current can also be increased to allow the use of back termination resistors for improved signal integrity. Equalization can be automatic or set to manual control for specific in-cable applications.

The MAX3815A is available in a 7mm x 7mm, 48-pin TQFP-EP package and operates over a 0°C to +70°C temperature range.

Applications

Front-Projector HDMI/DVI Inputs

High-Definition Televisions and Displays

HDMI/DVI-D Cable-Extender Modules and Active Cable Assemblies

LCD Computer Monitors

HDMI 1.3 Deep Color Systems

Features

- **Guaranteed Performance to 2.25Gbps (HDMI 1.3), Improved Jitter Performance at Low Source Amplitude, and Enhanced Output Driver**
- **Extends 2.25Gbps TMDS Interface Length**
  0 to 35 Meters Over HDMI Cable, 24 AWG
  0 to 22 Meters Over HDMI Cable, 28 AWG
- **Extends 1.65Gbps TMDS Interface Length**
  0 to 40 Meters Over HDMI Cable, 24 AWG
  0 to 28 Meters Over HDMI Cable, 28 AWG
- **Compatible with HDTV Resolutions 720p, 1080i, 1080p, and 1080p with 36-Bit Color**
- **Compatible with Computer Resolutions VGA, SVGA, XGA, SXGA, UXGA, and WUXGA**
- **Fully Automatic Equalization, No System Control Required**
- **3.3V Power Supply**
- **Power Dissipation of 0.6W (typ)**
- **7mm x 7mm, 48-Pin TQFP Lead-Free Package**

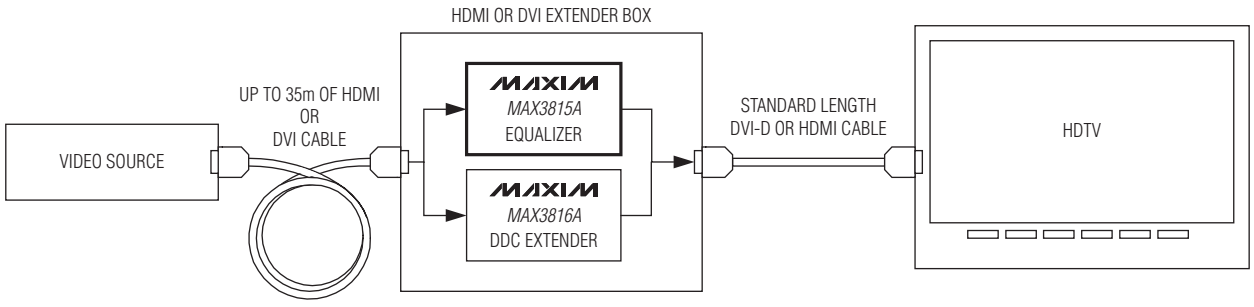
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3815ACCM+	0°C to +70°C	48 TQFP-EP*

+Denotes a lead(Pb)-free/RoHS compliant package.
**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

DVI is a trademark of Digital Display Working Group.
HDMI is a trademark of HDMI Licensing, LLC.
TMDS is a registered trademark of Silicon Image, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

TMDS Digital Video Equalizer for HDMI/DVI Cables

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC} ..... -0.5V to +4.0V
Voltage Range at Output CML Pins ..... -0.5V to +4.0V
Voltage Range at Input CML Pins, RES, VCC_T, and GND_T ..... -0.5V to (V_{CC} + 0.7V)
Voltage Between Input CML Complementary Pair ..... ±3.3V
Voltage Between Output CML Complementary Pair ..... ±1.4V

Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 36.2mW/°C above +70°C) 2896mW
Operating Junction Temperature Range ..... -55°C to +150°C
Storage Temperature Range ..... -55°C to +150°C
Die Attach Temperature ..... +400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.5V, T_A = 0°C to +70°C. Typical values are at V_{CC} = +3.3V, external terminations = 50Ω ±1%, MAX3815A in automatic equalization mode (EQCONTROL = GND), TMDS rate = 250Mbps to 2.25Gbps, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Current	I_{CC}	Clock present ($\overline{CLKLOS}$ = HIGH)			210	270	mA
		Clock and data absent ($\overline{CLKLOS}$ = LOW)			12		
Supply-Noise Tolerance		DC to 500kHz			200		mV_{P-P}
EQUALIZER PERFORMANCE							
Residual Output Jitter (Cables Only) 0.25Gbps to 1.65Gbps (Notes 1, 2, and 3)		1dB skin-effect loss at 825MHz			0.05		UI
		24dB skin-effect loss at 825MHz			0.13	0.21	
Residual Output Jitter (Cables Only) 1.65Gbps to 2.25Gbps (Notes 1, 2, and 3)		1dB skin-effect loss at 825MHz			0.1		UI
		24dB skin-effect loss at 825MHz			0.14	0.28	
CID Tolerance				20			Bits
CONTROL AND STATUS							
$\overline{CLKLOS}$ Assert Level		Differential peak-to-peak at EQ input with max 225MHz clock (see the *Typical Operating Characteristics* for more information)			50		mV_{P-P}
CML INPUTS (CABLE SIDE)							
Differential Input-Voltage Swing	V_{ID}	At cable input		800	1000	1200	mV_{P-P}
Common-Mode Input Voltage	V_{CM}			V_{CC} - 0.4		V_{CC} + 0.1	V
Input Resistance	R_{IN}	Single-ended		45	50	55	Ω
CML OUTPUTS (ASIC SIDE)							
Differential Output-Voltage Swing	V_{OD}	50Ω load, each side to V_{CC}	OUTLEVEL = HIGH	800	1000	1200	mV_{P-P}
			OUTLEVEL = LOW		500		
		With back termination as shown in Figure 4, OUTLEVEL = OPEN			910		
Output-Voltage High		Single-ended, OUTLEVEL = HIGH			V_{CC}		mV
Output-Voltage Low		Single-ended, OUTLEVEL = HIGH		V_{CC} - 600		V_{CC} - 400	mV
Output Voltage During Clock Absence ($\overline{CLKLOS}$ = LOW)		Single-ended		V_{CC} - 10		V_{CC} + 10	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.5V, T_A = 0°C to +70°C. Typical values are at V_{CC} = +3.3V, external terminations = 50Ω ±1%, MAX3815A in automatic equalization mode (EQCONTROL = GND), TMDS rate = 250Mbps to 2.25Gbps, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Output Voltage		50Ω load, each side to V_{CC}, OUTLEVEL = HIGH		V_{CC} - 0.25		V
Rise/Fall Time (Note 1)		20% to 80%	80	160		ps
LVTTL CONTROL AND STATUS INTERFACE						
LVTTL Input High Voltage	V_{IH}		2.0			V
LVTTL Input Low Voltage	V_{IL}				0.8	V
LVTTL Input High Current		$V_{IH(MIN)} < V_{IN} < V_{CC}$			±50	µA
LVTTL Input Low Current		$GND < V_{IN} < V_{IL(MAX)}$			-100	µA
Open-Collector Output High Voltage		$R_{LOAD} \geq 10k\Omega$ to V_{CC}	2.4			V
Open-Collector Output Low Voltage		$R_{LOAD} \geq 2k\Omega$ to V_{CC}			0.4	V
Open-Collector Output Sink Current					5	mA
OUTLEVEL Input Open-State Current Tolerance				±5		µA

Note 1: AC specifications are guaranteed by design and characterization.

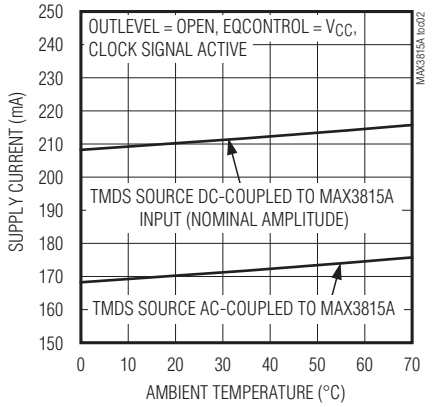
Note 2: Cable input swing is 800mV to 1200mV differential peak-to-peak. Residual output jitter is defined as peak-to-peak jitter, both deterministic plus random, as measured using an oscilloscope histogram with 5000 hits. Source jitter subtracted.

Note 3: Test pattern is a 2^7 - 1 PRBS + 20 ones + 2^7 - 1 PRBS (inverted) + 20 zeros.

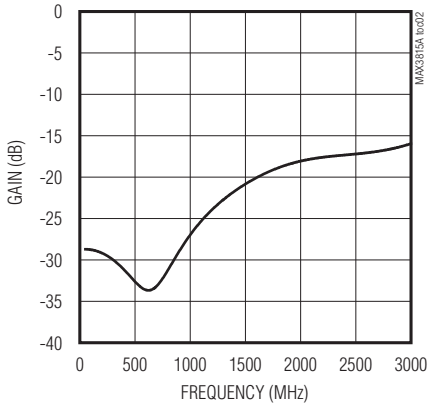
Typical Operating Characteristics

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 20 ones + 2^7 - 1 PRBS (inverted) + 20 zeros, equalizer in automatic mode, cable launch amplitude $1V_{P-P}$ differential, unless otherwise noted.)

SUPPLY CURRENT vs. AMBIENT TEMPERATURE



INPUT RETURN LOSS vs. FREQUENCY

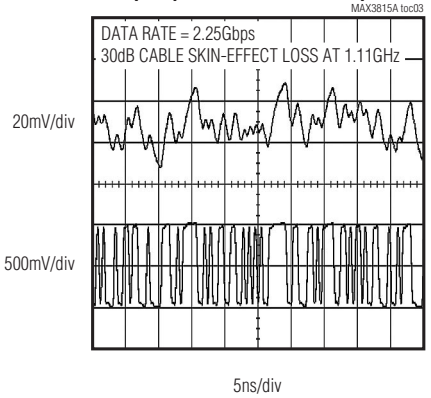


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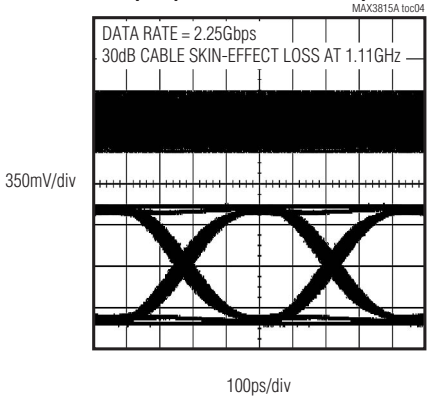
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 20 ones + 2^7 - 1 PRBS (inverted) + 20 zeros, equalizer in automatic mode, cable launch amplitude 1V_{P-P} differential, unless otherwise noted.)

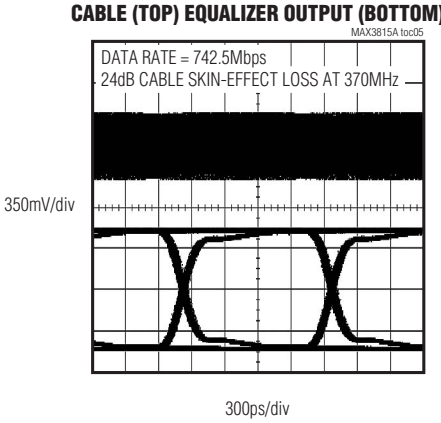
EQUALIZER INPUT AFTER 100ft OF 26 AWG CABLE (TOP) EQUALIZER OUTPUT (BOTTOM)



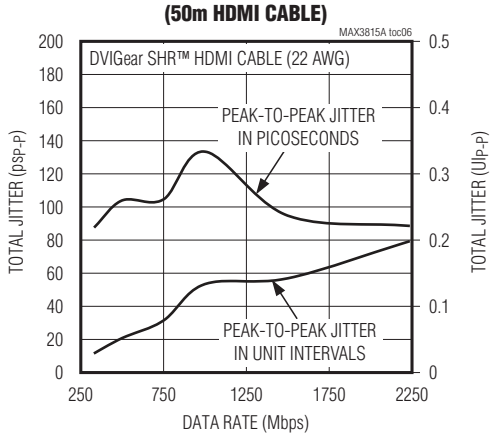
EQUALIZER INPUT EYE AFTER 100ft OF 26 AWG CABLE (TOP) EQUALIZER OUTPUT (BOTTOM)



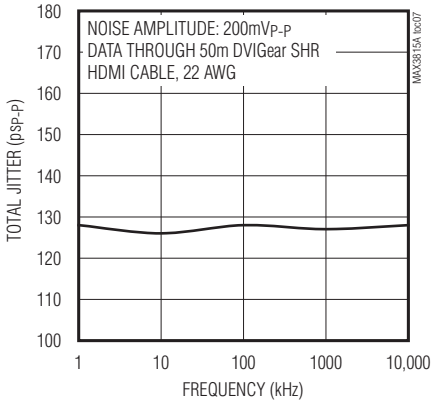
EQUALIZER INPUT EYE AFTER 150ft OF 26 AWG CABLE (TOP) EQUALIZER OUTPUT (BOTTOM)



TOTAL JITTER vs. DATA RATE (50m HDMI CABLE)



TOTAL JITTER vs. POWER-SUPPLY NOISE FREQUENCY (DATA RATE = 2.25Gbps)

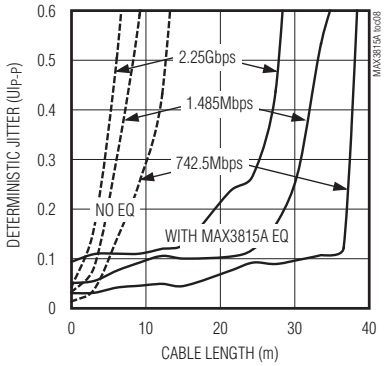


SHR is a trademark of DVIGear, Inc.

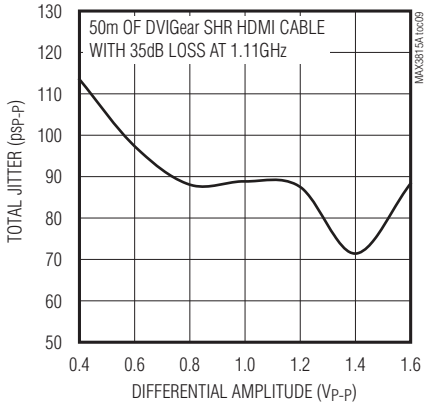
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 20 ones + 2^7 - 1 PRBS (inverted) + 20 zeros, equalizer in automatic mode, cable launch amplitude 1V_{P-P} differential, unless otherwise noted.)

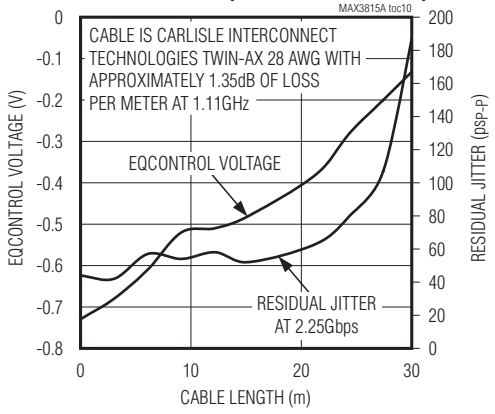
TOTAL JITTER vs. CABLE LENGTH (CARLISLE INTERCONNECT TECHNOLOGIES TWIN-AX 28 AWG)



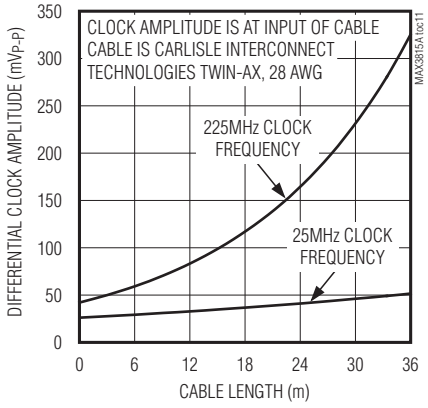
TOTAL JITTER vs. SIGNAL AMPLITUDE INPUT TO CABLE (DATA RATE 2.25Gbps)



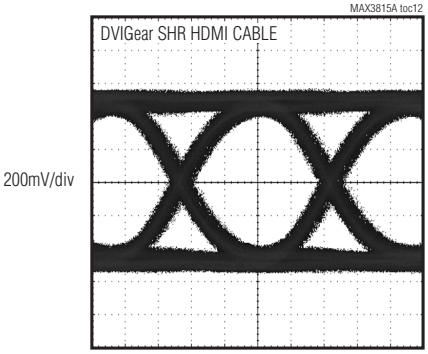
EQCONTROL VOLTAGE (RELATIVE TO V_{CC}) vs. CABLE LENGTH (MANUAL EQ CONTROL)



LOSS-OF-CLOCK ASSERT THRESHOLD vs. CABLE LENGTH



EQUALIZER OUTPUT EYE AFTER 50m OF 22 AWG HDMI CABLE (DATA RATE = 2.25Gbps)



TMDS Digital Video Equalizer for HDMI/DVI Cables

Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 8, 9, 12, 13, 16, 38	V_{CC}	Supply Voltage. All pins must be connected to V_{CC}.
2	RX0_IN-	Negative Data Input, CML
3	RX0_IN+	Positive Data Input, CML
6	RX1_IN-	Negative Data Input, CML
7	RX1_IN+	Positive Data Input, CML
10	RX2_IN-	Negative Data Input, CML
11	RX2_IN+	Positive Data Input, CML
14	RXC_IN+	Positive Clock Input, CML
15	RXC_IN-	Negative Clock Input, CML
17	EQCONTROL	Equalizer Control. This pin allows the user to control the equalization level of the MAX3815A. Connect the pin to GND for automatic operation. Set the voltage to V_{CC} - 1V for minimum equalization, or set the voltage between V_{CC} - 1V and V_{CC} for manual equalization. See the *Applications Information* section for more information.
18	$\overline{CLKLOS}$	Loss-of-Clock Signal Output, LVTTL Open Collector. This pin asserts low upon loss of the input TMDS clock from the cable. Connect pin to V_{CC} through a 4.7kΩ resistor.
19	N.C.	Not Connected. This pin is not internally connected.
20, 23, 24, 25, 28, 29, 32, 33, 36, 37	GND	Ground
21	RXC_OUT-	Negative Clock Output, CML
22	RXC_OUT+	Positive Clock Output, CML
26	RX2_OUT+	Positive Data Output, CML
27	RX2_OUT-	Negative Data Output, CML
30	RX1_OUT+	Positive Data Output, CML
31	RX1_OUT-	Negative Data Output, CML
34	RX0_OUT+	Positive Data Output, CML
35	RX0_OUT-	Negative Data Output, CML
39	OUTLEVEL	Output-Level Control Input • HIGH: Standard swing (1000mV$_{P-P}$ differential) • OPEN: Standard swing (900mV$_{P-P}$ differential) with external 267Ω back termination resistor (see Figure 4) • LOW: One-half standard swing (500mV$_{P-P}$ differential)
40	$\overline{OUTON}$	Output-Enable Control Input, LVTTL. This input enables the CML outputs when forced low and sets a differential logic zero when forced high.
41, 43, 44	VCC_T	Reserved. Must be connected to V_{CC} for normal operation.
42	GND_T	Reserved. Must be connected to GND for normal operation.
45–48	RES	Reserved. Must be left open for normal operation.
—	EP	Exposed Pad. The exposed pad must be soldered to the circuit-board ground for proper thermal and electrical operation.

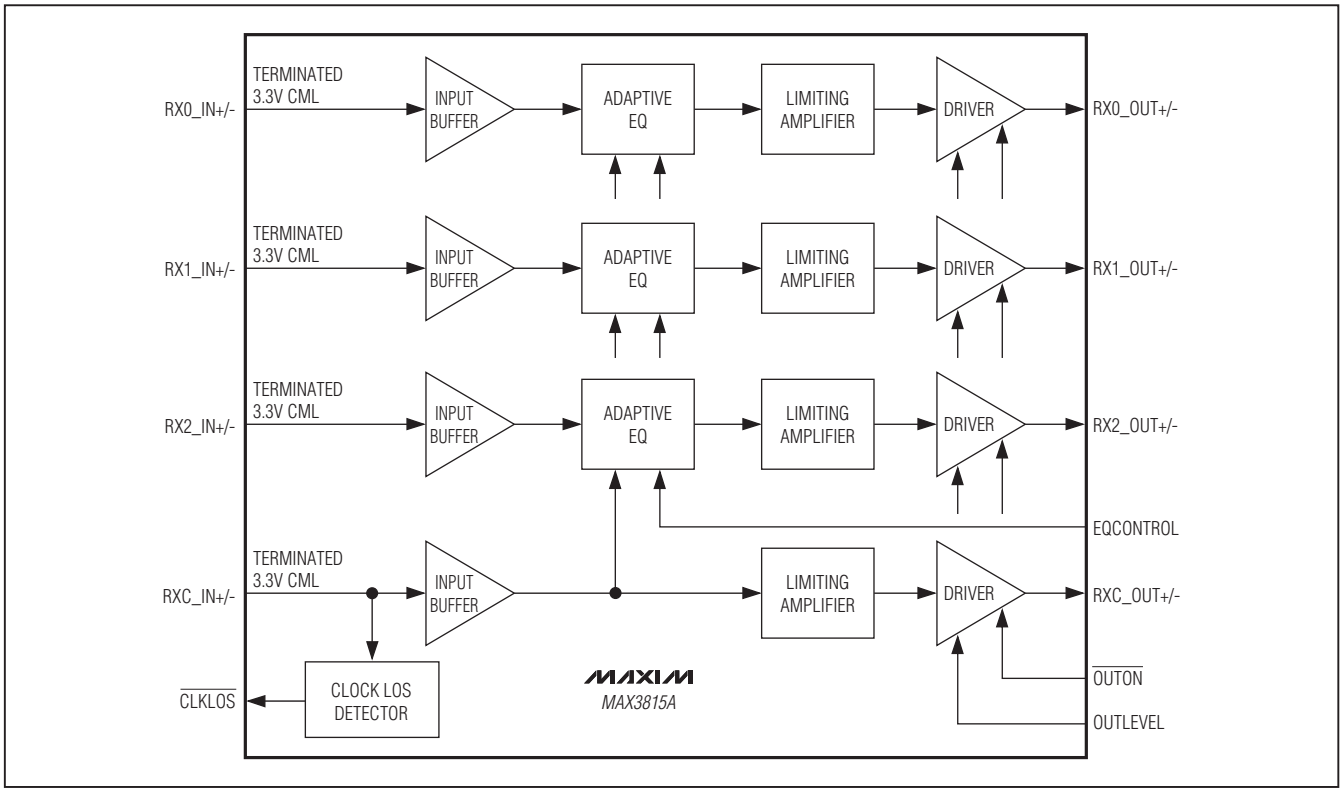


Figure 1. Functional Diagram

Detailed Description

The MAX3815A TMDS equalizer accepts differential CML input data at rates of 250Mbps up to 2.25Gbps (individual channel data rate). It automatically adjusts to skin-effect losses in copper cable. It consists of four CML input buffers, a loss-of-clock signal detector, three independent adaptive equalizers, four limiting amplifiers, and four output buffers (Figure 1).

CML Input Buffers and Output Drivers

The input buffers and the output drivers are implemented using current-mode logic (CML) (see Figures 4 and 5). The output drivers are open-collector and can be turned off with the $\overline{\text{OUTON}}$ pin. The OUTLEVEL pin sets the output drive current to one of three levels; see the *Applications Information* and *Pin Description* sections for more information. For details on interfacing with CML, refer to Application Note 291: *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

Loss-of-Clock Signal Detector

The loss-of-clock signal detector indicates a loss-of-clock signal at the $\overline{\text{CLKLOS}}$ pin. This is an open-collector output that must be connected to V_{CC} through a 4.7kΩ external pullup. This resistor is required whether or not the LOS output is used.

Adaptive Equalizer

The three data channels each contain an independent adaptive equalizer. Each channel analyzes the incoming signal and determines the amount of equalization to apply.

Limiting Amplifier

The limiting amplifier amplifies the signal from the adaptive equalizer and truncates the top and bottom of the waveform to provide a clean high- and low-level signal to the output drivers.

TMDS Digital Video Equalizer for HDMI/DVI Cables

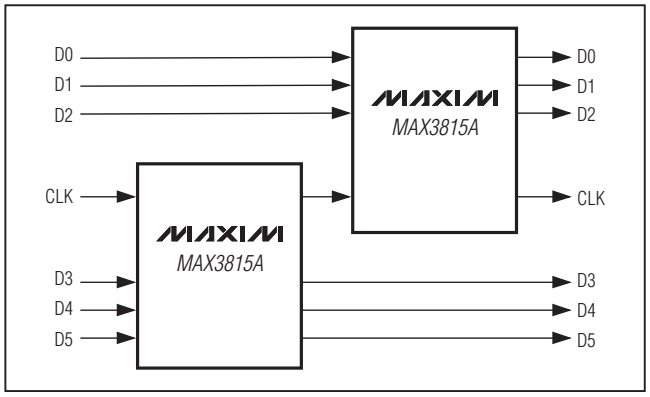


Figure 2. Connection Scheme for MAX3815A in Dual Link Application

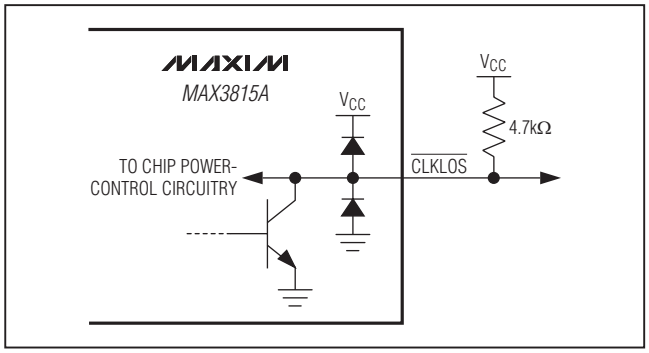


Figure 3. Simplified $\overline{CLKLOS}$ Output Circuit Schematic

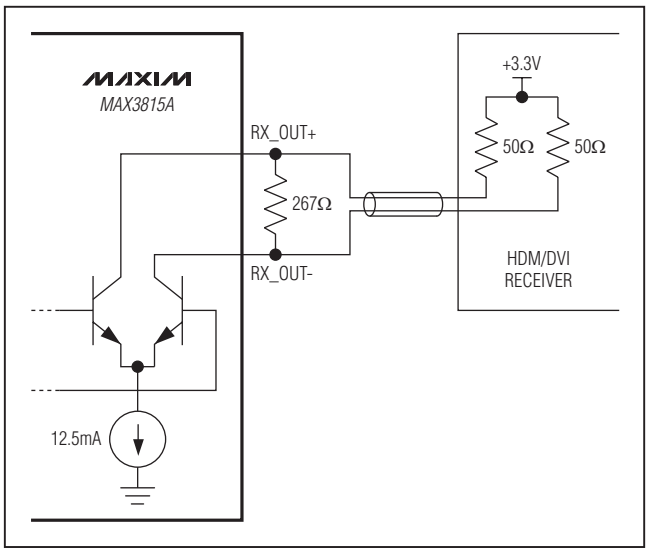


Figure 4. Back Termination Circuit

Applications Information

Typical shielded twisted pair (STP), unshielded twisted pair (UTP), and twin-ax cables exhibit skin-effect losses, which attenuate the high-frequency spectrum of a TMDS signal, eventually causing data errors or even closing the signal eye altogether given a long enough cable. The MAX3815A recovers the data and opens the signal eye through compensating equalization.

The basic TMDS interface is composed of four differential serial links: three links carry serial data up to 2.25Gbps each, and the fourth is a one-tenth-rate (0.1x) clock that operates up to 225MHz. TMDS, as with analog nVGA links, must handle a variety of resolutions and screen update rates. The actual range of digital serial rates is roughly 250Mbps to 2.25Gbps. For applications requiring ultra-high resolutions (e.g., QXGA), a "dual-link" DVI interface is used and is composed of six data links plus the clock, requiring two MAX3815A ICs with the clock going to both ICs. See Figure 2.

The MAX3815A can be used to extend any TMDS interface as used under the following trademarked names: DVI (digital visual interface), DFP™ (digital flat-panel), PanelLink, ADC™ (Apple display connector), and HDMI (high-definition multimedia interface).

Loss-of-Clock Signal ($\overline{CLKLOS}$) Output

A loss-of-clock signal is indicated by the $\overline{CLKLOS}$ output. A low level on $\overline{CLKLOS}$ indicates that the signal power on the RXC_IN pins has dropped below a threshold. When there is sufficient input voltage to the channel (typically greater than 100mV$_{P-P}$ differential), $\overline{CLKLOS}$ is high. The $\overline{CLKLOS}$ output is suitable for indicating problems with the transmission link caused by, for example, a broken cable, a defective driver, or a lost connection to the equalizer. Note that the loss-of-clock circuitry is sensitive to a DC or AC voltage between the RXC_IN pins. A DC or AC voltage greater than ±30mV (typical) is sensed as an active clock signal.

DFP is a trademark of Video Electronics Standards Association (VESA).

ADC is a trademark of Apple Computer, Inc.

The loss-of-clock circuitry powers down the part whenever there is an absence of a clock signal. This mutes the output and reduces power consumption to 83mW whenever the input signal is removed. During power-down, the MAX3815A's TMDS output pins go to a high-impedance state.

The $\overline{CLKLOS}$ is an open-collector output that requires a resistive pullup to V_{CC} for operation. The pullup resistor range is 1kΩ to 10kΩ (see Figure 3).

Output Level Control (OUTLEVEL) Input

The OUTLEVEL pin is a three-state input that allows the user to select between three output settings. Forcing this pin high results in the standard output signal level with no back terminations; leaving the pin open results in a standard output swing with 267Ω differential back termination resistors. Forcing this pin low results in one-half standard output signal level.

Using Back Termination

Using back termination resistance improves signal integrity through absorption of reflections. It also shifts the single-ended output voltage high (V_H) and low (V_L). Table 1 shows the output voltages when using the MAX3815A in each of its three output configurations.

Equalizer Control (EQCONTROL) Input

The EQCONTROL pin allows the user to control the equalization in one of two ways: forcing the pin to ground sets the equalizer in automatic equalization mode, and forcing a voltage between V_{CC} - 1V to V_{CC} allows manual control of the equalization level. Set to V_{CC} for maximum boost (long cable). Set to V_{CC} - 1V for minimum boost (short cable).

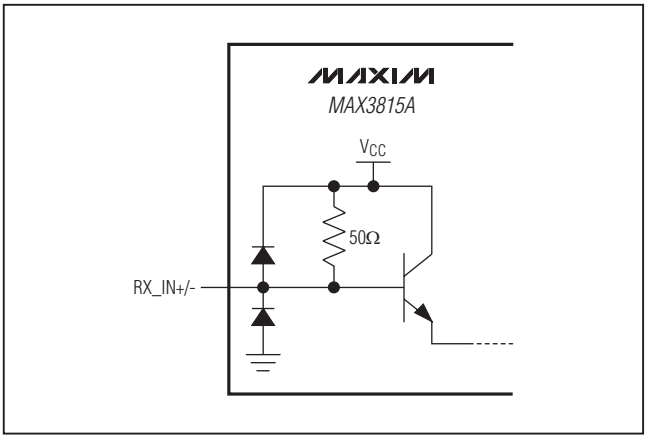


Figure 5. Simplified Input Circuit Schematic

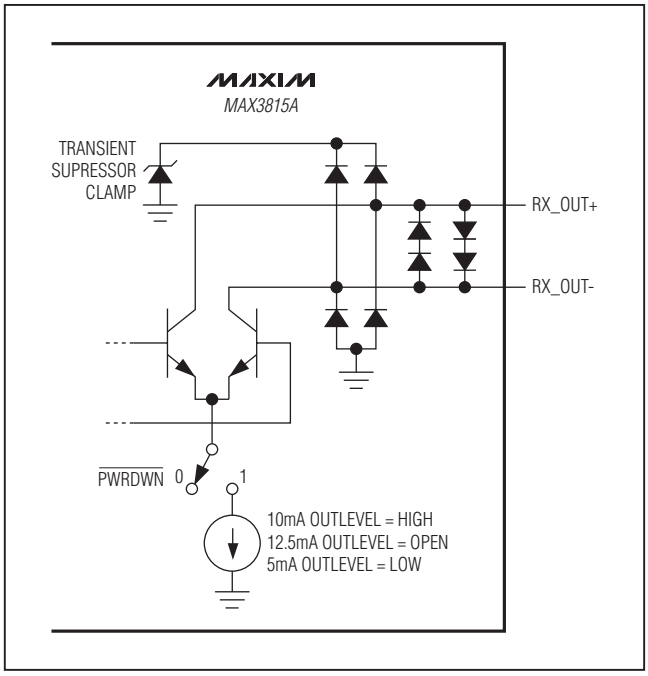


Figure 6. Simplified Output Circuit Schematic

Table 1. Output Settings and Swings

OUTLEVEL	BACK TERMINATION	DIFFERENTIAL SWING (mV_{P-P})	SINGLE-ENDED HIGH (V_H)	SINGLE-ENDED LOW (V_L)
High	Open	1000	V_{CC}	V_{CC} - 500mV
Open	267Ω	910	V_{CC} - 85mV	V_{CC} - 540mV
Low	Open	500	V_{CC}	V_{CC} - 250mV

TMDS Digital Video Equalizer for HDMI/DVI Cables

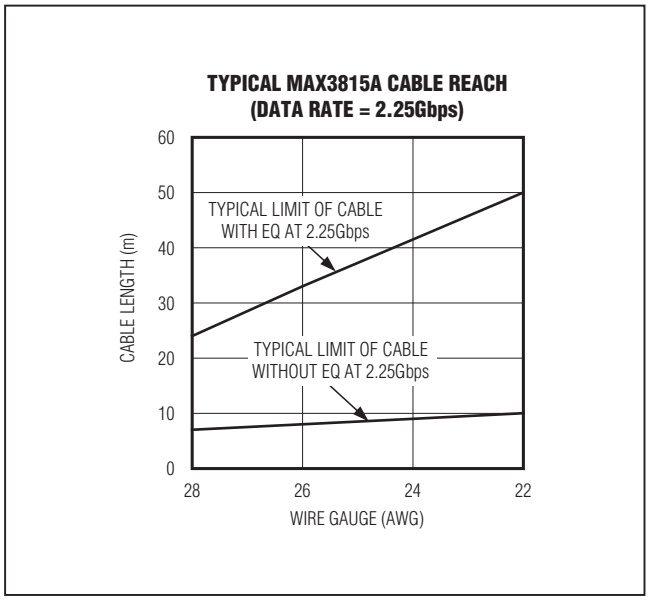


Figure 7. Cable Reach

Output On ($\overline{OUTON}$) Input

The $\overline{OUTON}$ pin is an LVTTL input. Force the pin low to enable the outputs. Force the pin high to set a differential zero on the outputs, irrespective of the signal at the inputs.

Cable Selection

TMDS performance is heavily dependent on cable quality. Deterministic jitter (DJ) can be caused by differential-to-common-mode conversion (or vice versa) within a twisted pair (STP or UTP), usually a result of cable twist or dielectric imbalance. Refer to Application Note 3353: *HFAN-04.5.4: 'Jitter Happens' when a Twisted Pair is Unbalanced* and Application Note 4218: *Unbalanced Twisted Pairs Can Give You the Jitters!* for more information.

Layout Considerations

The data and clock inputs are the most critical paths for the MAX3815A and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. Here are some suggestions for maximizing the performance of the MAX3815A:

- The data and clock inputs should be wired directly between the cable connector and IC without stubs.
- Place supply filter capacitors close to the MAX3815A inputs to provide a low inductance path for supply return currents.
- Input and output data channel designations are only a guide. Polarity assignments can be swapped and channel paths can be interchanged.
- An uninterrupted ground plane should be positioned beneath the high-speed I/Os.
- Ground-path vias should be placed close to the input/output connectors to allow a low inductance return current path.
- Maintain 100Ω differential transmission line impedance into and out of the MAX3815A.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk. Refer to Application Note 3854: *MAX3815: Interfacing to the MAX3815 DVI/HDMI Cable Equalizer* and the EV kit data sheet, MAX3815AEVKIT-HDMI.

Exposed-Pad Package

The exposed pad on the 48-pin TQFP-EP provides a very low thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3815A and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Maxim Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

Chip Information

PROCESS: SiGe BiPOLAR

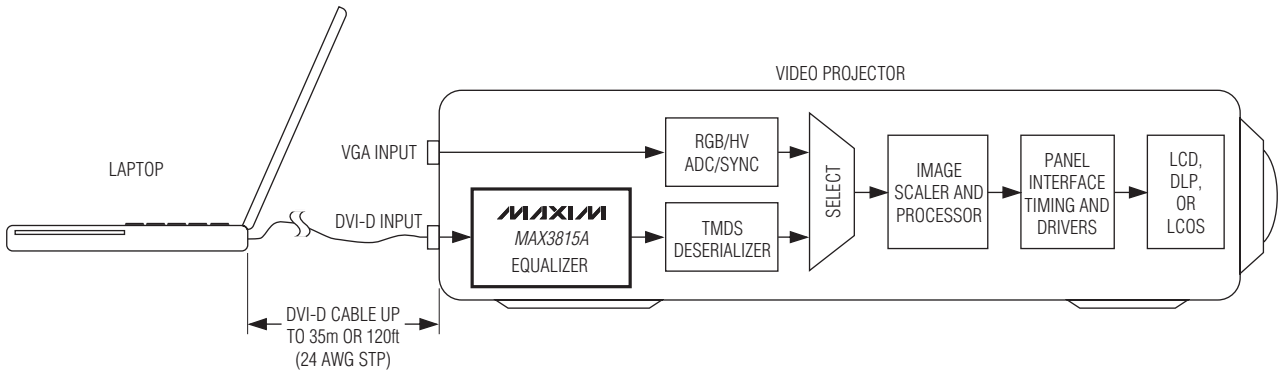
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

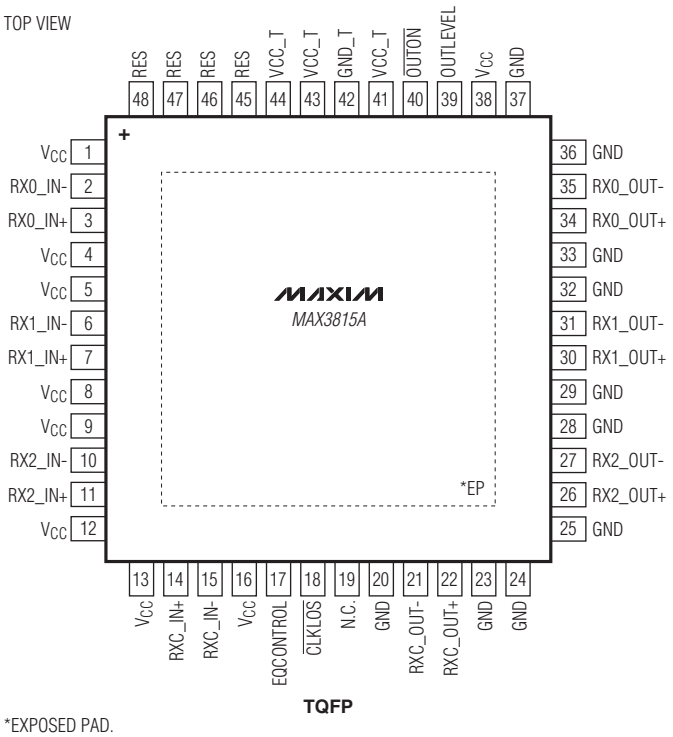
PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFP-EP	C48E+8	21-0065

TMDS Digital Video Equalizer for HDMI/DVI Cables

Typical Operating Circuits (continued)



Pin Configuration



TQFP

*EXPOSED PAD.

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