19-5122; Rev 2; 11/10

EVALUATION KIT AVAILABLE

# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer



## General Description

The MAX5392 dual, 256-tap, volatile, low-voltage, linear taper digital potentiometer offers three end-to-end resistance values of 10kΩ, 50kΩ, and 100kΩ. Operating from a single +1.7V to +5.5V power supply, the device provides a low 35ppm/°C end-to-end temperature coefficient. The device features an I²C interface.

The small package size, low supply operating voltage, low supply current, and automotive temperature range of the MAX5392 makes the device uniquely suited for the portable consumer market, battery-backup industrial applications, and the automotive market.

The MAX5392 is specified over the automotive -40°C to +125°C temperature range and is available in a 16-pin TSSOP package.

## Applications

Low-Voltage Battery Applications

Portable Electronics

Mechanical Potentiometer Replacement

Offset and Gain Control

Adjustable Voltage References/Linear Regulators

Automotive Electronics

## Features

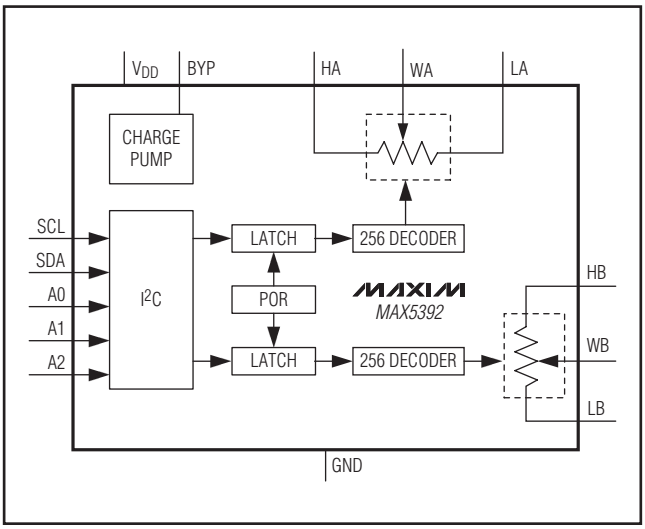
- **Dual, 256-Tap Linear Taper Positions**
- **Single +1.7V to +5.5V Supply Operation**
- **Low 12µA Quiescent Supply Current**
- **10kΩ, 50kΩ, 100kΩ End-to-End Resistance Values**
- **I²C-Compatible Interface**
- **Wiper Set to Midscale on Power-Up**
- **-40°C to +125°C Operating Temperature Range**

## Ordering Information

| PART | PIN-PACKAGE | END-TO-END RESISTANCE (kΩ) |
|---|---|---|
| MAX5392LAUE+ | 16 TSSOP | 10 |
| MAX5392MAUE+ | 16 TSSOP | 50 |
| MAX5392NAUE+ | 16 TSSOP | 100 |

***Note:*** *All devices are specified over the -40°C to +125°C operating temperature range.*
*+Denotes a lead(Pb)-free/RoHS-compliant package.*

## Functional Diagram






***For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.***

# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND .....-0.3V to +6V
H_, W_, L_ to GND .....-0.3V to the lower of ($V_{DD}$ + 0.3V) and +6V
All Other Pins to GND .....-0.3V to +6V
Continuous Current in to H_, W_, and L_
MAX5392L ..... ±5mA
MAX5392M ..... ±2mA
MAX5392N..... ±1mA

Continuous Power Dissipation ($T_A$ = +70°C)
16-Pin TSSOP (derate 11.1mW/°C above +70°C) ...888.9mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +1.7V to +5.5V, $V_{H_}$ = $V_{DD}$, $V_{L_}$ = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{DD}$ = +1.8V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Resolution | N | | | 256 | | | Tap |
| **DC PERFORMANCE (Voltage Divider Mode)** | | | | | | | |
| Integral Nonlinearity | INL | (Note 2) | | -0.5 | | +0.5 | LSB |
| Differential Nonlinearity | DNL | (Note 2) | | -0.5 | | +0.5 | LSB |
| Dual Code Matching | | Register A = Register B | | -0.5 | | +0.5 | LSB |
| Ratiometric Resistor Tempco | | ($\Delta V_W/V_W$)/$\Delta$T, no load | | | 5 | | ppm/°C |
| Full-Scale Error | | Code = FFh | MAX5392L | -3 | -2.2 | | LSB |
| | | | MAX5392M | -1 | -0.6 | | |
| | | | MAX5392N | -0.5 | -0.3 | | |
| Zero-Scale Error | | Code = 00h | MAX5392L | | 2.2 | 3 | LSB |
| | | | MAX5392M | | 0.6 | 1.0 | |
| | | | MAX5392N | | 0.3 | 0.5 | |
| **DC PERFORMANCE (Variable Resistor Mode)** | | | | | | | |
| Integral Nonlinearity | R-INL | MAX5392L (Note 3) | | -1.5 | | +1.5 | LSB |
| | | MAX5392M (Note 3) | | -0.75 | | +0.75 | |
| | | MAX5392N (Note 3) | | -0.5 | | +0.5 | |
| Differential Nonlinearity | R-DNL | (Note 3) | | -0.5 | | +0.5 | LSB |
| **DC PERFORMANCE (Resistor Characteristics)** | | | | | | | |
| Wiper Resistance | $R_{WL}$ | (Note 4) | | | | 200 | Ω |
| Terminal Capacitance | $C_{H_}$, $C_{L_}$ | Measured to GND | | | 10 | | pF |
| Wiper Capacitance | $C_{W_}$ | Measured to GND | | | 50 | | pF |
| End-to-End Resistor Tempco | $TC_R$ | No load | | | 35 | | ppm/°C |
| End-to-End Resistor Tolerance | $\Delta R_{HL}$ | Wiper not connected | | -25 | | +25 | % |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +1.7V to +5.5V, $V_{H_}$ = $V_{DD}$, $V_{L_}$ = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{DD}$ = +1.8V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | | |
| Crosstalk | | (Note 5) | | | -90 | | dB |
| -3dB Bandwidth | BW | Code = 80H, 10pF load, $V_{DD}$ = 1.8V | MAX5392L | | 600 | | kHz |
| | | | MAX5392M | | 100 | | |
| | | | MAX5392N | | 50 | | |
| Total Harmonic Distortion Plus Noise | THD+N | Measured at W, $V_{H_}$ = $1V_{RMS}$ at 1kHz | | | 0.02 | | % |
| Wiper Settling Time | $t_S$ | (Note 6) | MAX5392L | | 400 | | ns |
| | | | MAX5392M | | 1200 | | |
| | | | MAX5392N | | 2200 | | |
| Charge-Pump Feedthrough at W_ | $V_{RW}$ | $f_{CLK}$ = 600kHz, $C_{BYP}$ = 0nF | | | | 600 | $nV_{P-P}$ |
| **POWER SUPPLIES** | | | | | | | |
| Supply Voltage Range | $V_{DD}$ | | | 1.7 | | 5.5 | V |
| Standby Current | | $V_{DD}$ = 5.5V | | | 27 | | µA |
| | | $V_{DD}$ = 1.7V | | | 12 | | |
| **DIGITAL INPUTS** | | | | | | | |
| Minimum Input High Voltage | $V_{IH}$ | $V_{DD}$ = 2.6V to 5.5V | | 70 | | | % x $V_{DD}$ |
| | | $V_{DD}$ = 1.7V to 2.6V | | 75 | | | |
| Maximum Input Low Voltage | $V_{IL}$ | $V_{DD}$ = 2.6V to 5.5V | | | | 30 | % x $V_{DD}$ |
| | | $V_{DD}$ = 1.7V to 2.6V | | | | 25 | |
| Input Leakage Current | | | | -1 | | +1 | µA |
| Input Capacitance | | | | | 5 | | pF |
| **TIMING CHARACTERISTICS—$I^2C$ (Notes 7 and 8)** | | | | | | | |
| Maximum SCL Frequency | $f_{SCL}$ | | | | | 400 | kHz |
| Setup Time for START Condition | $t_{SU:STA}$ | | | 0.6 | | | µs |
| Hold Time for START Condition | $t_{HD:STA}$ | | | 0.6 | | | µs |
| SCL High Time | $t_{HIGH}$ | | | 0.6 | | | µs |
| SCL Low Time | $t_{LOW}$ | | | 1.3 | | | µs |

# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +1.7V to +5.5V, $V_{H_}$ = $V_{DD}$, $V_{L_}$ = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{DD}$ = +1.8V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Data Setup Time | $t_{SU:DAT}$ | | 100 | | | ns |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | | | µs |
| SDA, SCL Rise Time | $t_R$ | | | | 0.3 | µs |
| SDA, SCL Fall | $t_F$ | | | | 0.3 | µs |
| Setup Time for STOP Condition | $t_{SU:STO}$ | | 0.6 | | | µs |
| Bus Free Time Between STOP and START Condition | $t_{BUF}$ | Minimum power-up rate = 0.2V/µs | 1.3 | | | µs |
| Pulse Suppressed Spike Width | $t_{SP}$ | | | | 50 | ns |
| Capacitive Load for Each Bus | $C_B$ | (Note 9) | | | 400 | pF |

**Note 1:** All devices are 100% production tested at $T_A$ = +25°C. Specifications over temperature limits are guaranteed by design and characterization.

**Note 2:** DNL and INL are measured with the potentiometer configured as a voltage-divider (Figure 1) with H_ = $V_{DD}$ and L_ = GND. The wiper terminal is unloaded and measured with a high-input-impedance voltmeter.

**Note 3:** R-DNL and R-INL are measured with the potentiometer configured as a variable resistor (Figure 1). DNL and INL are measured with the potentiometer configured as a variable resistor. H_ is unconnected and L_ = GND. For $V_{DD}$ = +5V, the wiper terminal is driven with a source current of 400µA for the 10kΩ configuration, 80µA for the 50kΩ configuration, and 40µA for the 100kΩ configuration. For $V_{DD}$ = +1.7V, the wiper terminal is driven with a source current of 150µA for the 10kΩ configuration, 30µA for the 50kΩ configuration, and 15µA for the 100kΩ configuration.

**Note 4:** The wiper resistance is the worst value measured by injecting the currents given in Note 3 to W_ with L_ = GND. $R_{W_}$ = ($V_{W_}$ - $V_{H_}$)/$I_{W_}$.

**Note 5:** Drive HA with a 1kHz GND to $V_{DD}$ amplitude tone. LA = LB = GND. No load. WB is at midscale with a 10pF load. Measure WB.

**Note 6:** The wiper-settling time is the worst-case 0 to 50% rise time, measured between tap 0 and tap 127. H_ = $V_{DD}$, L_ = GND, and the wiper terminal is loaded with 10pF capacitance to ground.

**Note 7:** Digital timing is guaranteed by design and characterization, not production tested.

**Note 8:** The SCL clock period includes rise and fall times ($t_R$ = $t_F$). All digital input signals are specified with $t_R$ = $t_F$ = 2ns and timed from a voltage level of ($V_{IL}$ + $V_{IH}$)/2.

**Note 9:** An appropriate bus pullup resistance must be selected depending on board capacitance. For I²C-bus specification information from NXP Semiconductor (formerly Philips Semiconductor), refer to the UM10204: I²C-Bus Specification and User Manual.

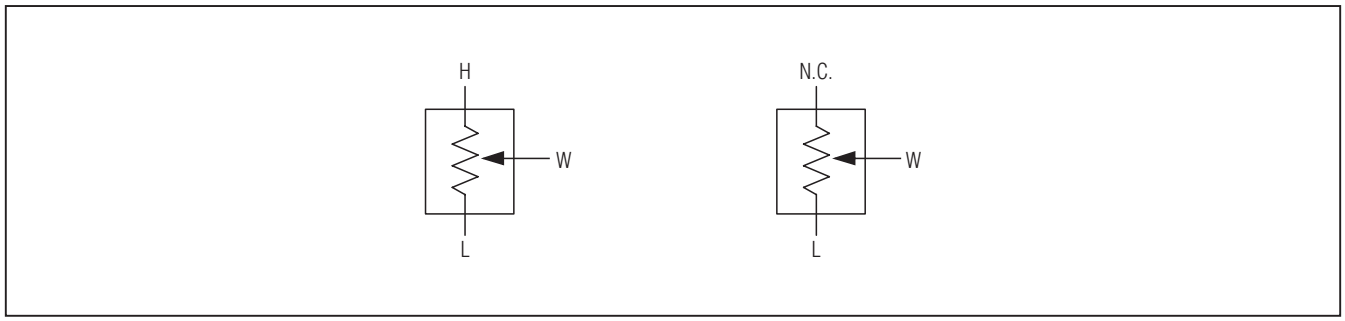


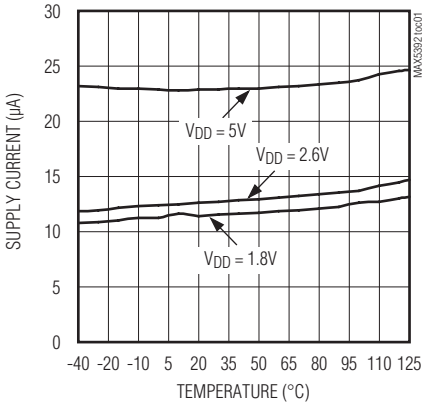

*Figure 1. Voltage-Divider and Variable Resistor Configurations*

# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

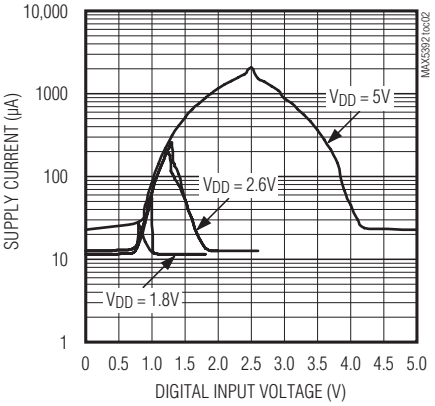
## Typical Operating Characteristics

($V_{DD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.)

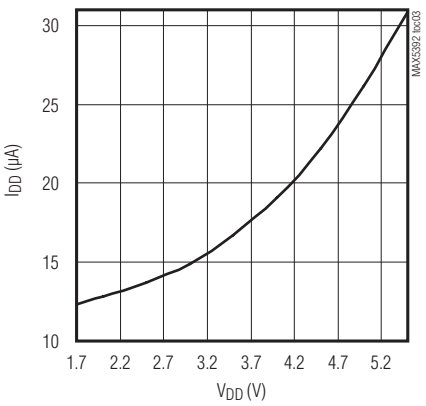
**SUPPLY CURRENT vs. TEMPERATURE**



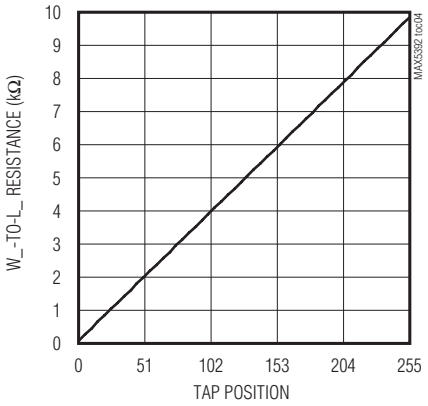

**SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE**



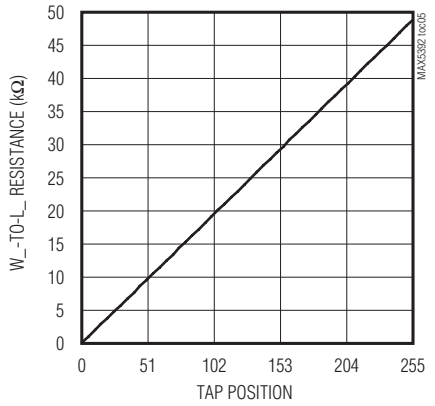

**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



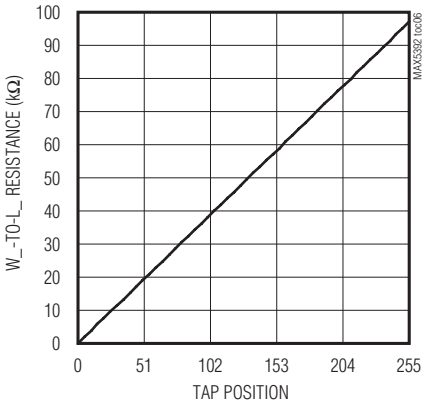

**RESISTANCE (W_-TO-L_) vs. TAP POSITION (10kΩ)**



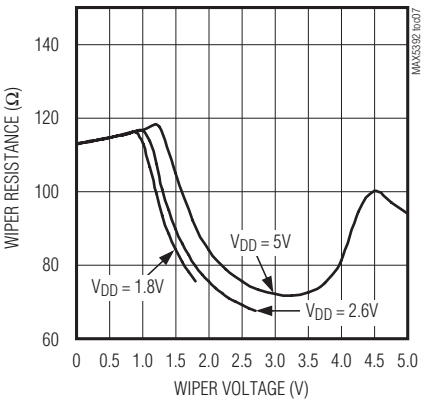

**RESISTANCE (W_-TO-L_) vs. TAP POSITION (50kΩ)**



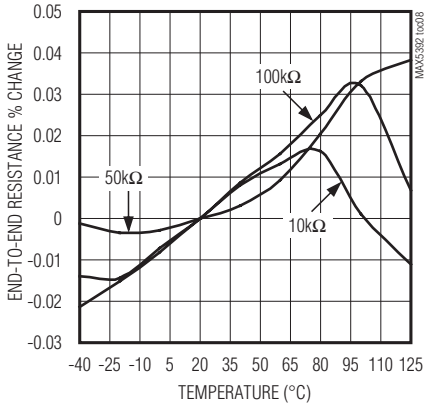

**RESISTANCE (W_-TO-L_) vs. TAP POSITION (100kΩ)**



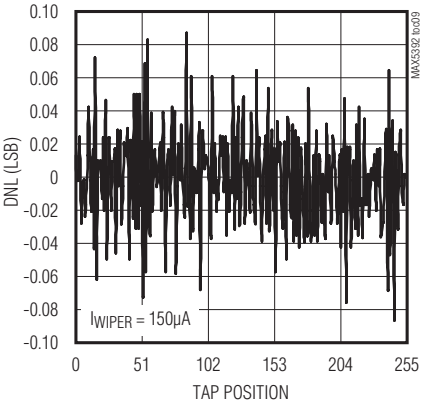

**WIPER RESISTANCE vs. WIPER VOLTAGE (10kΩ)**




**END-TO-END RESISTANCE PERCENTAGE CHANGE vs. TEMPERATURE**




**VARIABLE RESISTOR DNL vs. TAP POSITION (10kΩ)**

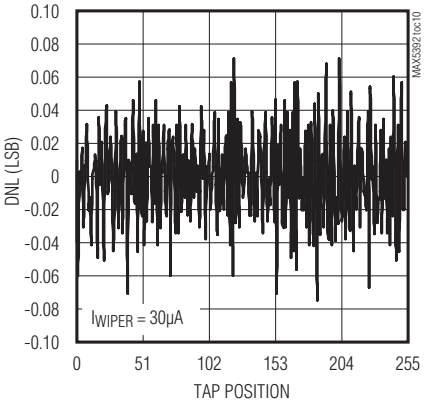


# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

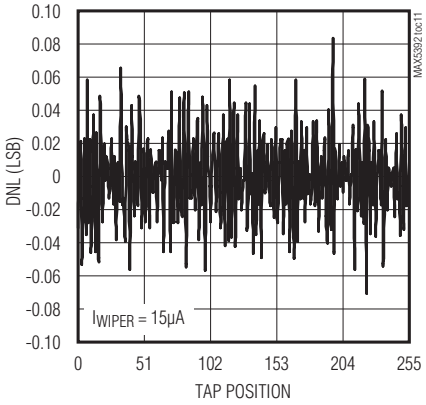
## Typical Operating Characteristics (continued)

($V_{DD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.)

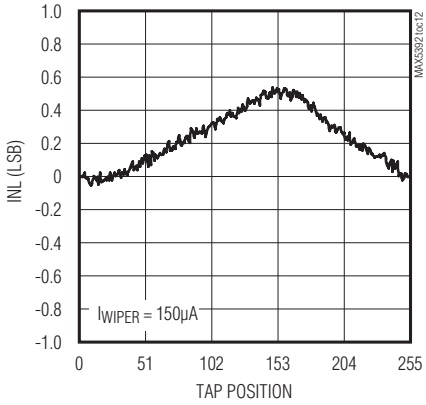
**VARIABLE RESISTOR DNL vs. TAP POSITION (50kΩ)**



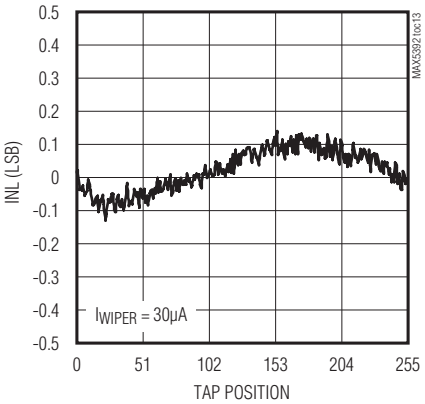

**VARIABLE RESISTOR DNL vs. TAP POSITION (100kΩ)**



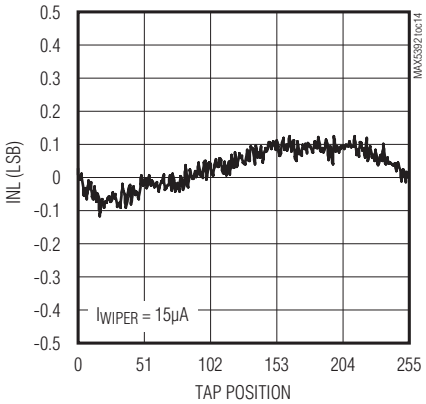

**VARIABLE RESISTOR INL vs. TAP POSITION (10kΩ)**



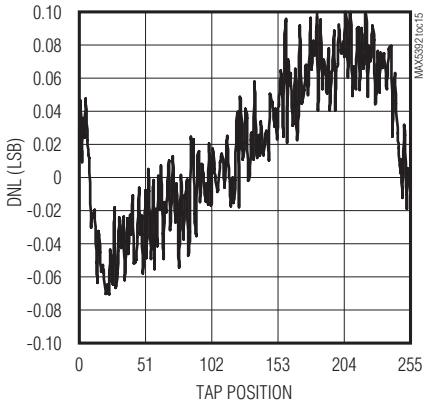

**VARIABLE RESISTOR INL vs. TAP POSITION (50kΩ)**



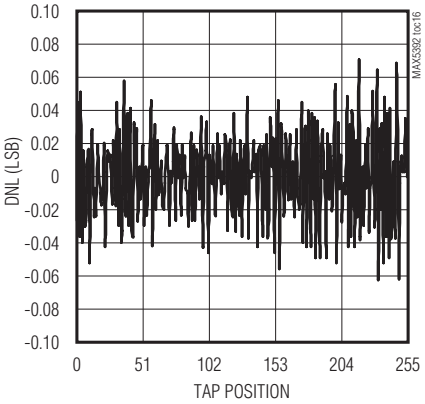

**VARIABLE RESISTOR INL vs. TAP POSITION (100kΩ)**



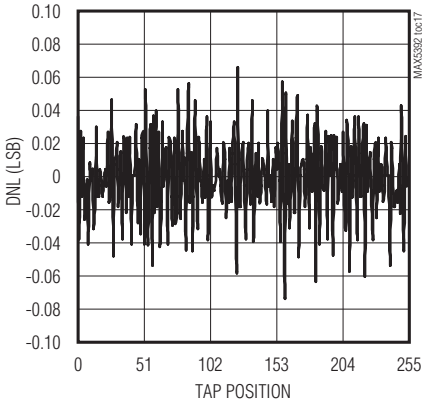

**VOLTAGE-DIVIDER DNL vs. TAP POSITION (10kΩ)**



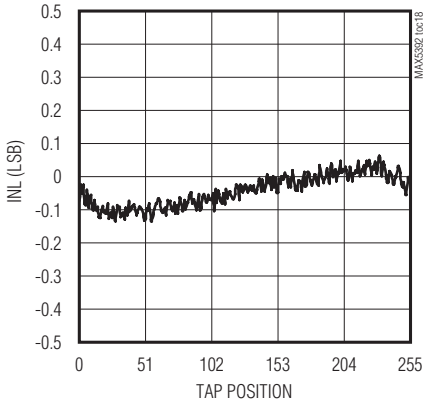

**VOLTAGE-DIVIDER DNL vs. TAP POSITION (50kΩ)**




**VOLTAGE-DIVIDER DNL vs. TAP POSITION (100kΩ)**



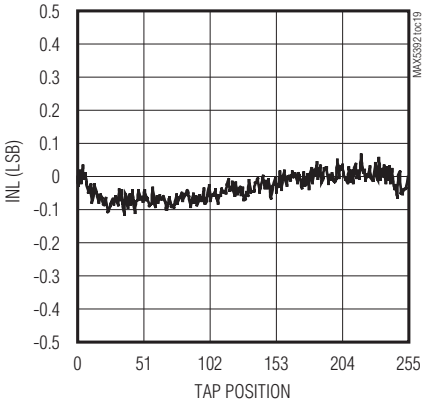

**VOLTAGE-DIVIDER INL vs. TAP POSITION (10kΩ)**



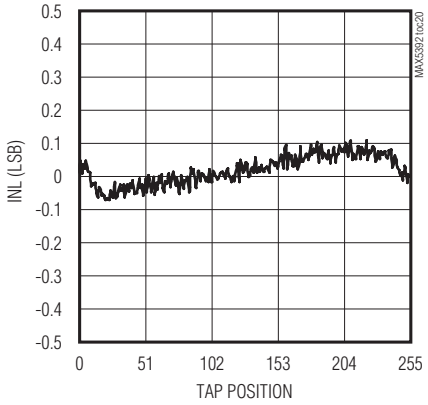
## Typical Operating Characteristics (continued)

($V_{DD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.)

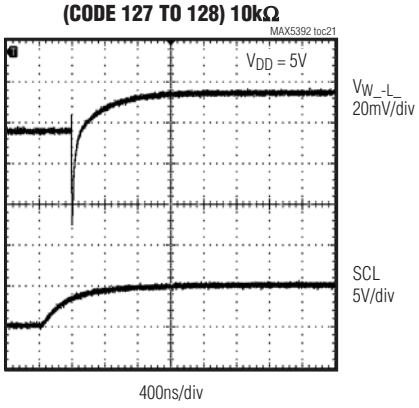
**VOLTAGE-DIVIDER INL vs. TAP POSITION (50kΩ)**



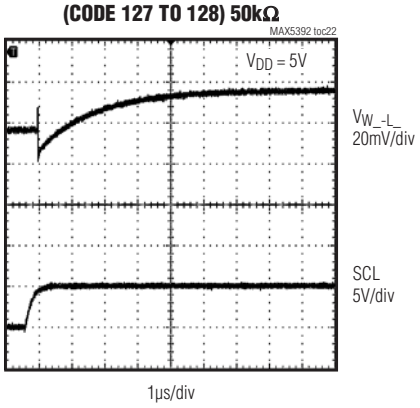

**VOLTAGE-DIVIDER INL vs. TAP POSITION (100kΩ)**



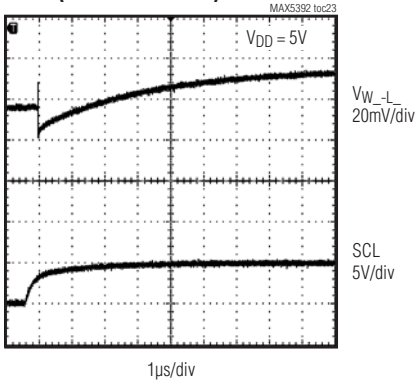

**TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128) 10kΩ**



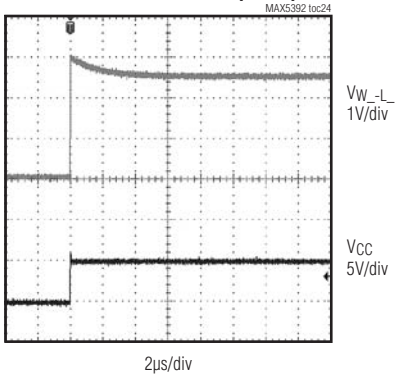

**TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128) 50kΩ**




**TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128) 100kΩ**




**POWER-ON TRANSIENT (50kΩ)**

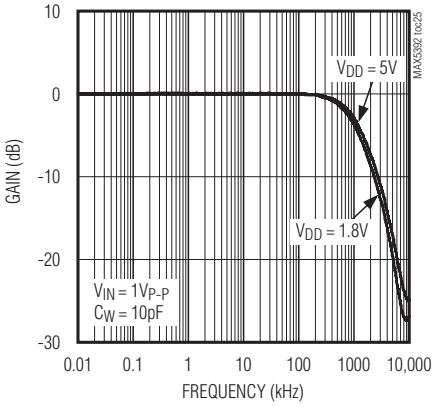


# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

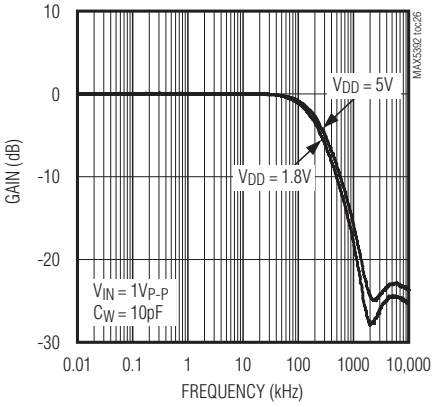
## Typical Operating Characteristics (continued)

($V_{DD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.)

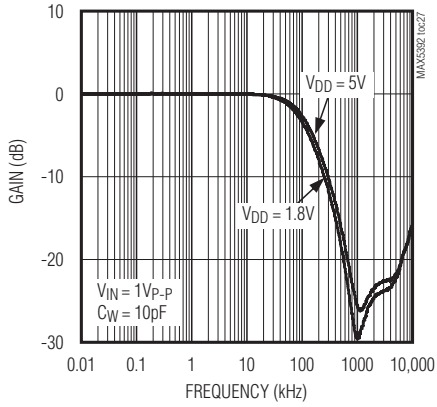
**MIDSCALE FREQUENCY RESPONSE (10kΩ)**



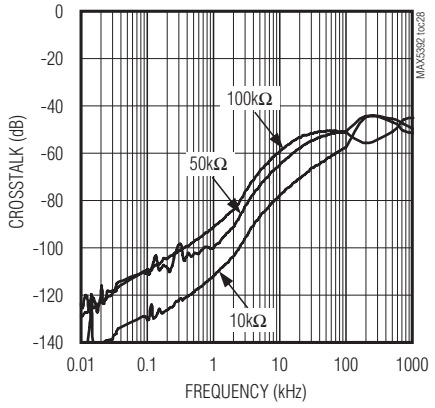

**MIDSCALE FREQUENCY RESPONSE (50kΩ)**



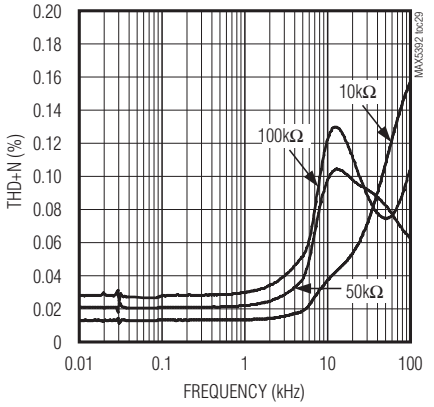

**MIDSCALE FREQUENCY RESPONSE (100kΩ)**



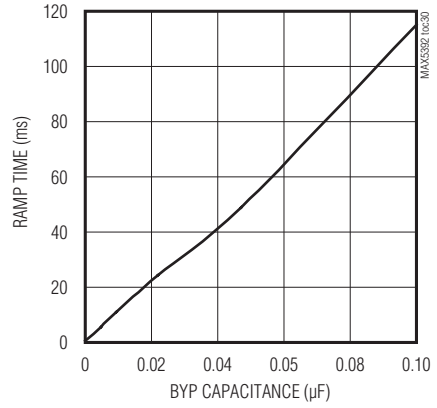

**CROSSTALK vs. FREQUENCY**



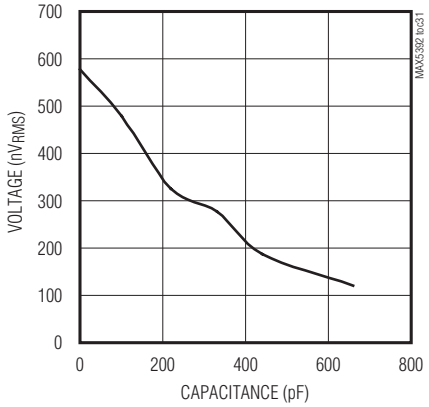

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



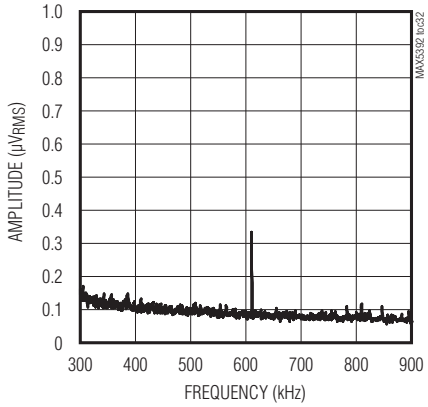

**BYP RAMP TIME vs. $C_{BYP}$**




**CHARGE-PUMP FEEDTHROUGH AT W_ vs. $C_{BYP}$**

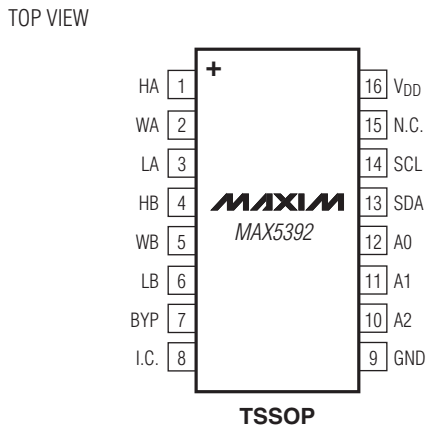



**CHARGE-PUMP FEEDTHROUGH AT W_ vs. FREQUENCY**



# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

## Pin Configuration




## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | HA | Resistor A High Terminal. The voltage at HA can be higher or lower than the voltage at LA. Current can flow into or out of HA. |
| 2 | WA | Resistor A Wiper Terminal |
| 3 | LA | Resistor A Low Terminal. The voltage at LA can be higher or lower than the voltage at HA. Current can flow into or out of LA. |
| 4 | HB | Resistor B High Terminal. The voltage at HB can be higher or lower than the voltage at LB. Current can flow into or out of HB. |
| 5 | WB | Resistor B Wiper Terminal |
| 6 | LB | Resistor B Low Terminal. The voltage at LB can be higher or lower than the voltage at HB. Current can flow into or out of LB. |
| 7 | BYP | Internal Power-Supply Bypass. For additional charge-pump filtering, bypass to GND with a capacitor close to the device. |
| 8 | I.C. | Internally Connected. Connect to GND. |
| 9 | GND | Ground |
| 10 | A2 | Address Input 2. Connect to $V_{DD}$ or GND. |
| 11 | A1 | Address Input 1. Connect to $V_{DD}$ or GND. |
| 12 | A0 | Address Input 0. Connect to $V_{DD}$ or GND. |
| 13 | SDA | $I^2C$-Compatible Serial-Data Input/Output. A pullup resistor is required. |
| 14 | SCL | $I^2C$-Compatible Serial-Clock Input. A pullup resistor is required. |
| 15 | N.C. | No Connection. Not internally connected. |
| 16 | $V_{DD}$ | Power-Supply Input. Bypass $V_{DD}$ to GND with a 0.1µF capacitor close to the device. |

# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

## Detailed Description

The MAX5392 dual, 256-tap, volatile, low-voltage linear taper digital potentiometer offers three end-to-end resistance values of 10kΩ, 50kΩ, and 100kΩ. The potentiometer consists of 255 fixed resistors in series between terminals H_ and L_. The potentiometer wiper, W_, is programmable to access any one of the 256 tap points on the resistor string.

The potentiometers are programmable independently of each other. The MAX5392 features an I²C interface.

### Charge Pump

TThe MAX5392 contains an internal charge pump that guarantees the maximum wiper resistance, $R_{WL}$, to be less than 200Ω for supply voltages down to 1.7V. Pins H_, W_, and L_ are still required to be less than $V_{DD}$ + 0.3V. A bypass input, BYP, is provided to allow additional filtering of the charge-pump output, further reducing clock feedthrough that can occur on H_, W_, or L_. The nominal clock rate of the charge pump is 600kHz. BYP should remain resistively unloaded as any additional load would increase clock feedthrough. See the Charge-Pump Feedthrough at W_ vs. $C_{BYP}$ graph in the *Typical Operating Characteristics* for $C_{BYP}$ sizing guidelines with respect to clock feedthrough to the wiper. The value of $C_{BYP}$ does affect the startup time of the charge pump; however, $C_{BYP}$ does not impact the ability to communicate with the device, nor is there a minimum $C_{BYP}$ requirement. The maximum wiper impedance specification is not guaranteed until the charge pump is fully settled. See the BYP Ramp Time vs. $C_{BYP}$ graph in the *Typical Operating Characteristics* for $C_{BYP}$ impact on charge-pump settling time.

### I²C Digital Interface

The I²C interface contains a shift register that decodes the command and address bytes, routing the data to the appropriate control registers. Data written to a control register immediately updates the wiper position. The wipers A and B power up in midposition, D[7:0] = 80h.

#### Serial Addressing

The MAX5392 operates as a slave device that receives data through an I²C/SMBus™-compatible 2-wire serial interface. The interface uses a serial-data access line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master, typically a microcontroller, initiates all data transfers to the port and generates the SCL clock that synchronizes the data transfer. See Figure 2. Connect a pullup resistor, typically 4.7kΩ, between each of the SDA and SCL lines to a voltage between $V_{DD}$ and 5.5V.

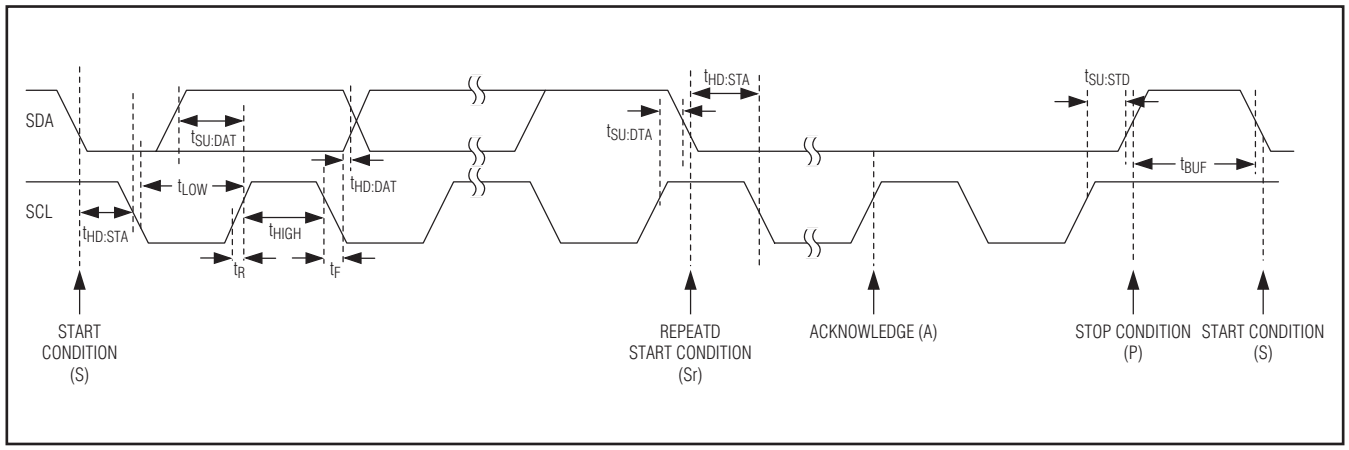



*Figure 2. I²C Serial-Interface Timing Diagram*

*SMBus is a trademark of Intel Corp.*

Each transmission consists of a START (S) condition sent by a master, followed by a 7-bit slave address plus a NOP/$\overline{W}$ bit. See Figures 3, 4, and 7.

### START and STOP Conditions

SCL and SDA remain high when the interface is inactive. A master controller signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. The master controller issues a STOP condition by transitioning the SDA from low to high while SCL is high, after finishing communicating with the slave. The bus is then free for another transmission. See Figure 2.

### Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high. See Figure 5.

### Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data. See Figure 6. Each byte transferred requires a total of 9 bits. The master controller generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line remains stable low during the high period of the clock pulse.

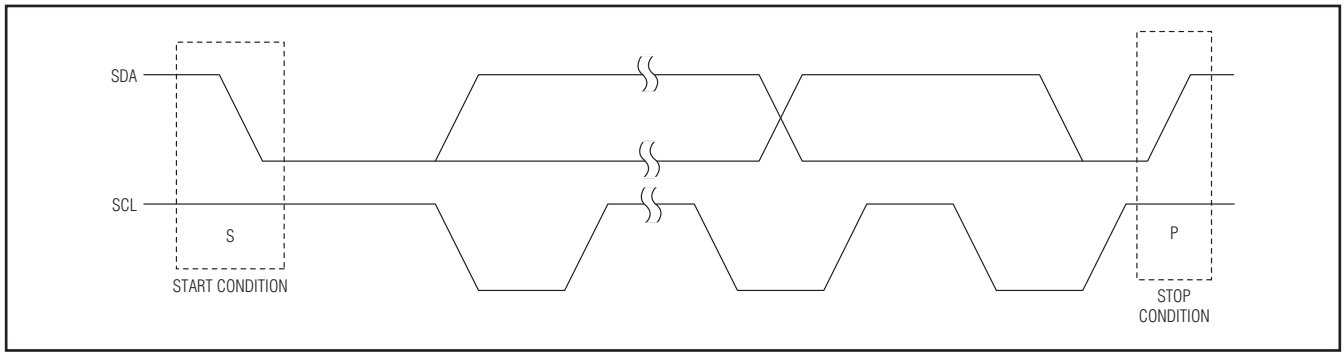



*Figure 3. START and STOP Conditions*

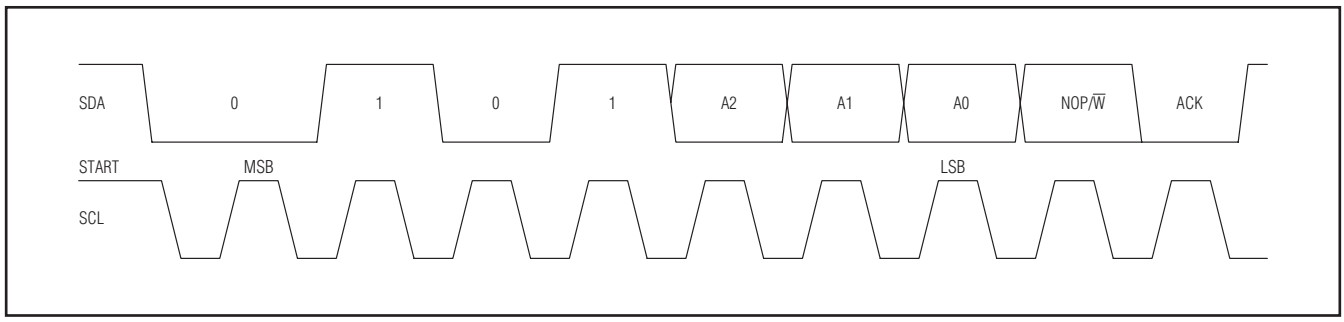



*Figure 4. Slave Address*

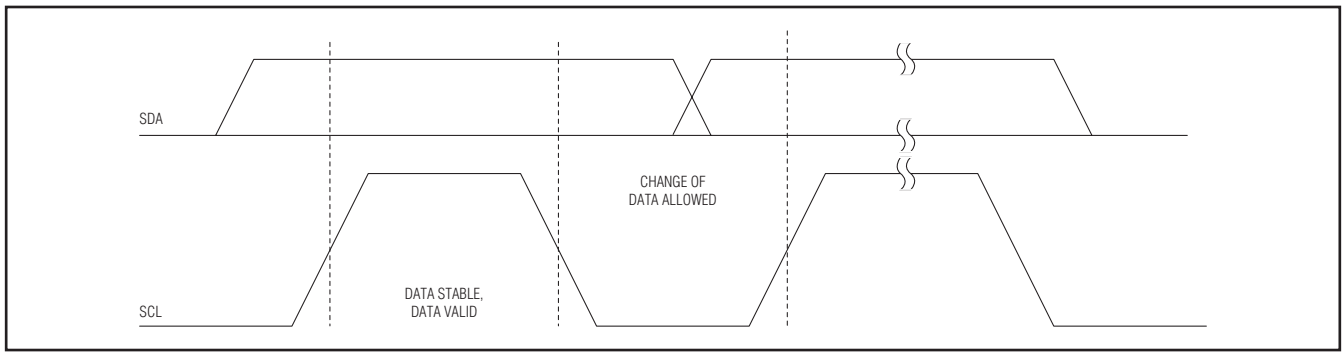



*Figure 5. Bit Transfer*

# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

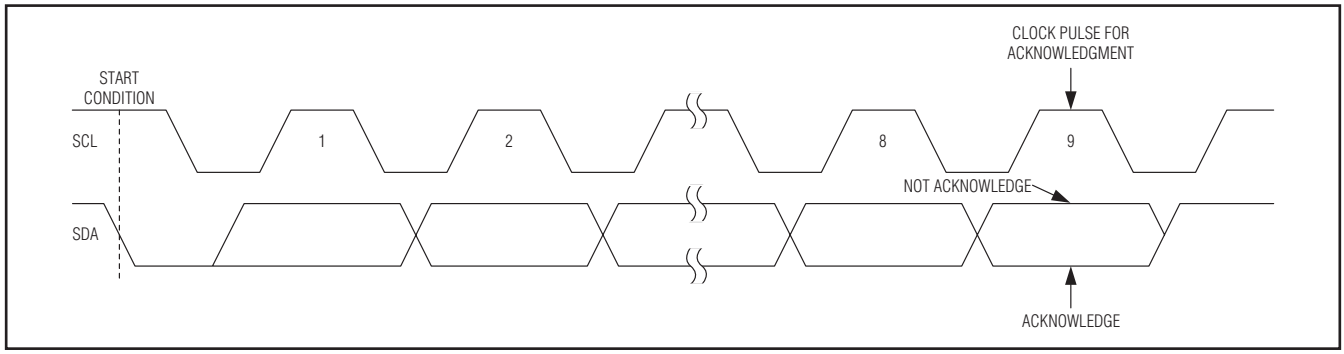



*Figure 6. Acknowledge*

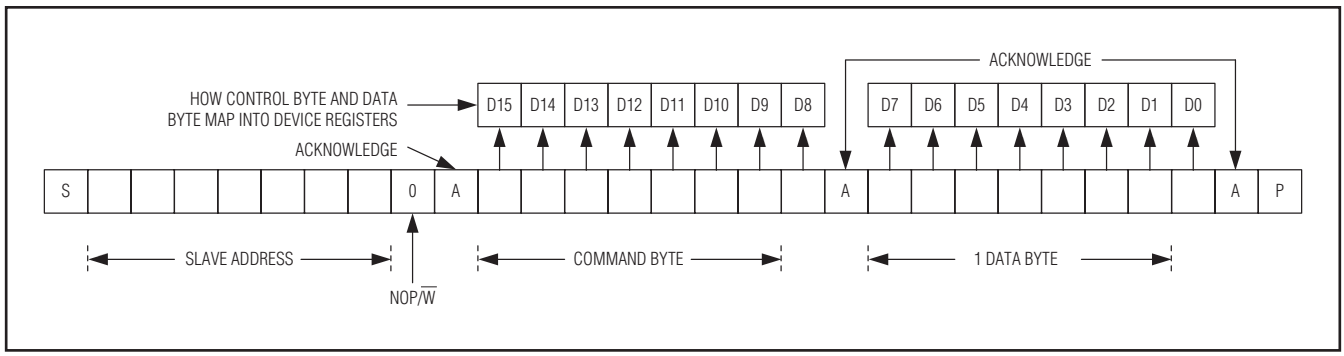



*Figure 7. Command and Single Data Byte Received*

### *Slave Address*

The MAX5392 includes a 7-bit slave address (Figure 4). The 8th bit following the 7th bit of the slave address is the NOP/$\overline{W}$ bit. Set the NOP/$\overline{W}$ bit low for a write command and high for a no-operation command. The device does not support readback.

The device provides three address inputs (A0, A1, and A2), allowing up to eight devices to share a common bus (Table 1). The first 4 bits (MSBs) of the factory-set slave addresses are always 0101. A2, A1, and A0 set the next 3 bits of the slave address. Connect each address input to $V_{DD}$ or GND. Each device must have a unique address to share a common bus.

### *Message Format for Writing*

Write to the devices by transmitting the device's slave address with NOP/$\overline{W}$ (8th bit) set to zero, followed by at least 2 bytes of information. The first byte of information is the command byte. The second byte is the data byte. The data byte goes into the internal register of the device as selected by the command byte (Figure 7 and Table 2).

## Table 1. Slave Addresses

| ADDRESS INPUTS | | | SLAVE ADDRESS |
|---|---|---|---|
| A2 | A1 | A0 | |
| GND | GND | GND | 0101000 |
| GND | GND | $V_{DD}$ | 0101001 |
| GND | $V_{DD}$ | GND | 0101010 |
| GND | $V_{DD}$ | $V_{DD}$ | 0101011 |
| $V_{DD}$ | GND | GND | 0101100 |
| $V_{DD}$ | GND | $V_{DD}$ | 0101101 |
| $V_{DD}$ | $V_{DD}$ | GND | 0101110 |
| $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | 0101111 |

## Table 2. I²C Command Byte Summary

| | | ADDRESS BYTE | | | | | | | | | COMMAND BYTE | | | | | | | | | | DATA BYTE | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SCL CYCLE NUMBER | START (S) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | STOP (P) |
| | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | $\overline{W}$ | ACK (A) | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | ACK (A) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK (A) | |
| REG A | | 0 | 1 | 0 | 1 | A2 | A1 | A0 | 0 | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| REG B | | 0 | 1 | 0 | 1 | A2 | A1 | A0 | 0 | | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| REG A AND B | | 0 | 1 | 0 | 1 | A2 | A1 | A0 | 0 | | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |

### *Command Byte*

Use the command byte to select the destination of the wiper data. See Table 2.

### *Command Descriptions*

**REG A:** The data byte writes to register A and the wiper of potentiometer A moves to the appropriate position. D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wiper to the position closest to LA. D[7:0] = FFh moves the wiper closest to HA. D[7:0] is 80h following power-on.

**REG B:** The data byte writes to register B and the wiper of potentiometer B moves to the appropriate position. D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wiper to the position closest to LB. D[7:0] = FFh moves the wiper to the position closest to HB. D[7:0] is 80h following power-on.

**REG A and B:** The data byte writes to registers A and B and the wipers of potentiometers A and B move to the appropriate position. D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wipers to the position closest to L_. D[7:0] = FFh moves the wipers to the position closest to H_. D[7:0] is 80h following power-on.

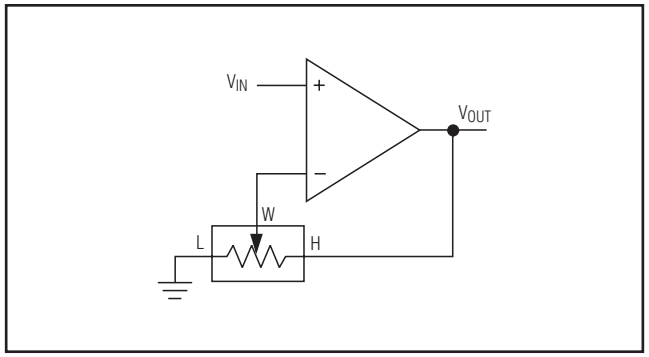



*Figure 8. Variable Gain Noninverting Amplifier*

## Applications Information

### *Variable Gain Amplifier*

Figure 8 shows a potentiometer adjusting the gain of a noninverting amplifier. Figure 9 shows a potentiometer adjusting the gain of an inverting amplifier.

### *Adjustable Dual Regulator*

Figure 10 shows an adjustable dual linear regulator using a dual potentiometer as two variable resistors.

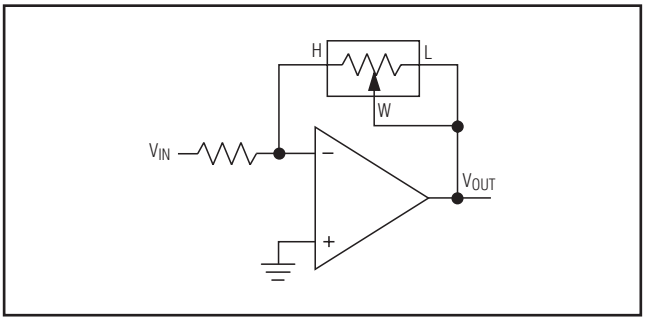



*Figure 9. Variable Gain Inverting Amplifier*

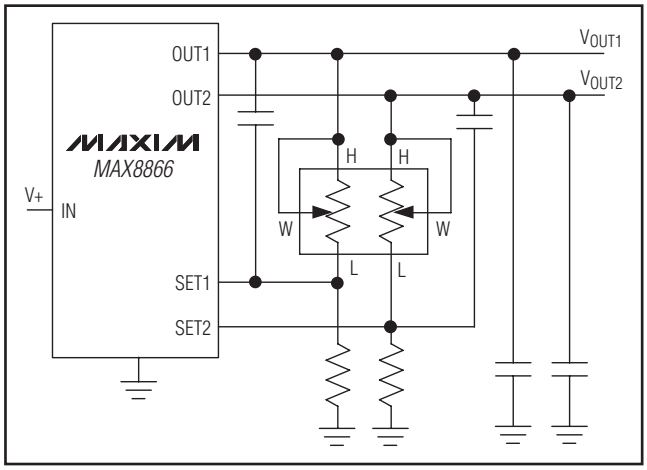



*Figure 10. Adjustable Dual Linear Regulator*

# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

### Adjustable Voltage Reference

Figure 11 shows an adjustable voltage reference circuit using a potentiometer as a voltage-divider.

### Variable Gain Current to Voltage Converter

Figure 12 shows a variable gain current to voltage converter using a potentiometer as a variable resistor.

### LCD Bias Control

Figure 13 shows a positive LCD bias control circuit using a potentiometer as a voltage-divider.

Figure 14 shows a positive LCD bias control circuit using a potentiometer as a variable resistor.

### Programmable Filter

Figure 15 shows a programmable filter using a dual potentiometer.

### Offset Voltage Adjustment Circuit

Figure 16 shows an offset voltage adjustment circuit using a dual potentiometer.

## Chip Information

PROCESS: BiCMOS

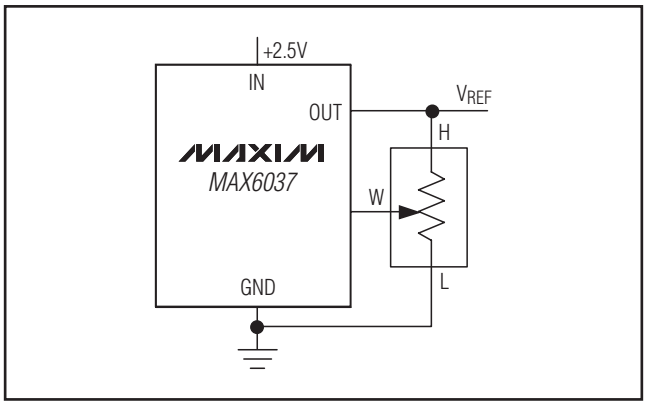



*Figure 11. Adjustable Voltage Reference*

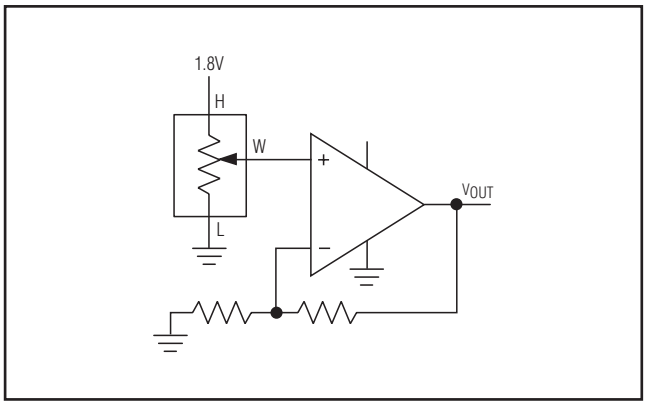



*Figure 13. Positive LCD Bias Control Using a Voltage Divider*

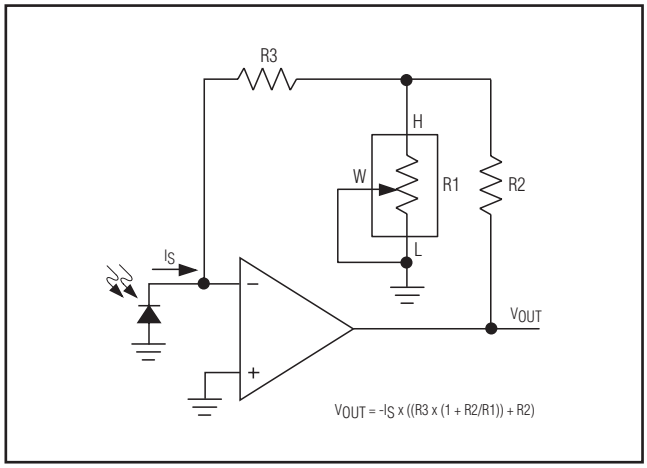



*Figure 12. Variable Gain I-to-V Converter*

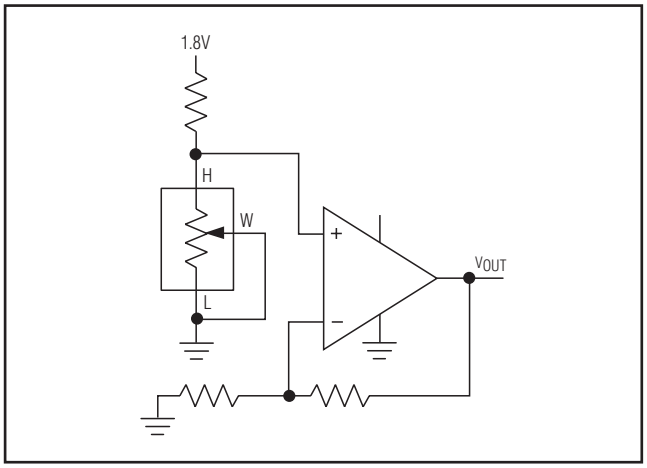



*Figure 14. Positive LCD Bias Control Using a Variable Resistor*

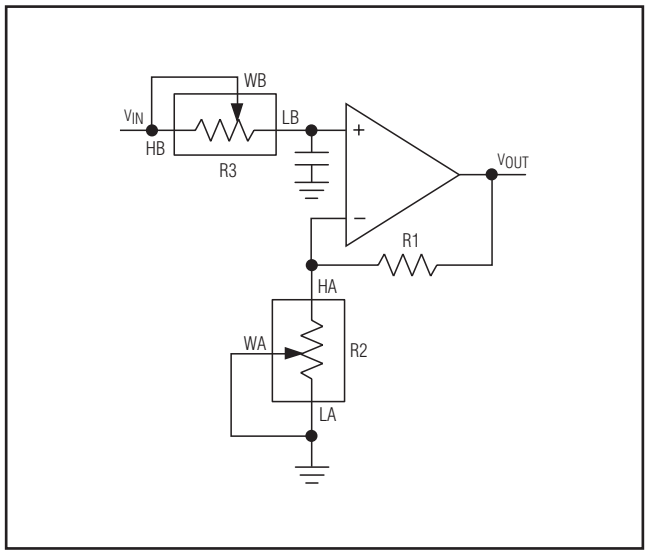



*Figure 15. Programmable Filter*

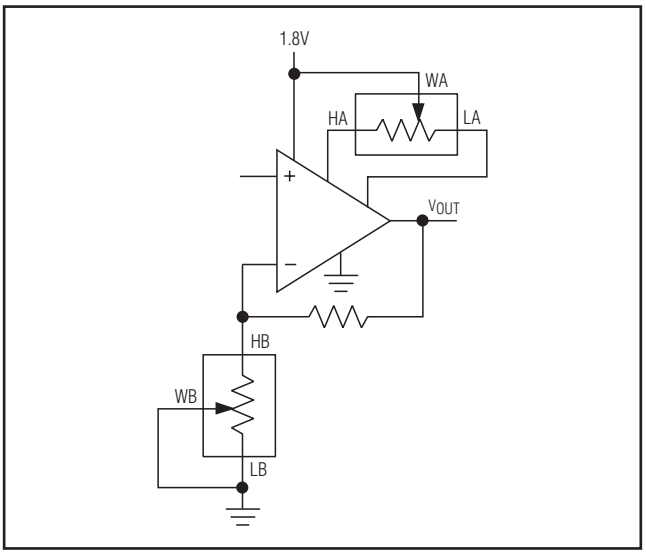



*Figure 16. Offset Voltage Adjustment Circuit*

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 16 TSSOP | U16+2 | 21-0066 | 90-0117 |

# Dual, 256-Tap, Volatile, Low-Voltage, Linear Taper Digital Potentiometer

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 1/10 | Initial release | — |
| 1 | 4/10 | Added Soldering Temperature in *Absolute Maximum Ratings*; corrected code in Conditions of -3dB Bandwidth specification in *Electrical Characteristics* | 2, 3 |
| 2 | 11/10 | Changed *Electrical Characteristics* heading and corrected Figures 9, 12, 14, 15, 16 | 2, 3, 4, 13, 14, 15 |

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