Click here to ask about the production status of specific part numbers.

MAX77533

14V Input, 1.5A High-Efficiency Buck Converter with 9µA I_{SUP}

General Description

The MAX77533 is a synchronous 1.5A step-down DC-DC converter optimized for portable 2-cell and 3-cell battery-operated and USB-C applications. The converter operates on an input supply between 3V and 14V. Output voltage is adjustable between 0.8V and 5V in 50mV steps through an I^2C serial interface (internal feedback) or 0.8V to 99% of the supply voltage with external feedback resistors. Factory-programmed default voltages of 1.2V, 1.8V, and 3.3V with internal feedback are offered to reduce component count for common rails. The device features a low-I_Q SKIP mode which allows excellent efficiency at light loads.

Dedicated enable and power-OK (POK) pins allow simple hardware control. An I^2C serial interface is optionally used for full configuration and control for dynamic voltage scaling and system power optimization.

Built-in undervoltage lockout (UVLO), output active discharge, cycle-by-cycle current limit, thermal shutdown, and short-circuit protection ensure safe operation under abnormal operating conditions.

The MAX77533 is available in a 12-bump, 0.4mm pitch wafer-level package (WLP).

Applications

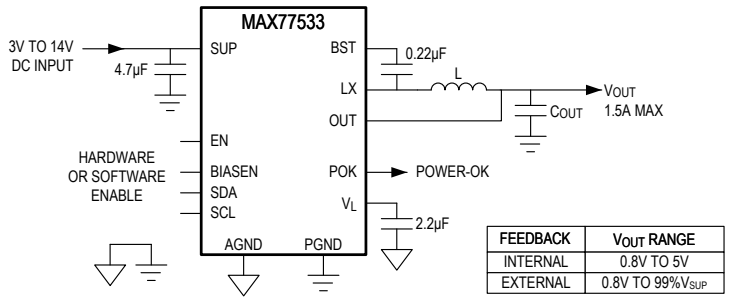
- 2-cell/3-cell High Power Density Supplies
- Portable Li+/Li-ion Battery Powered Devices
- Drones, HD Cameras, and Notebook Computers
- Space-Constrained Portable Electronics

Benefits and Features

- 1.5A Single Channel Buck Regulator
- 3V to 14V Input Voltage Range
- Output Voltage Range
  - 0.8V to 5V I^2C Programmable in 50mV Steps Internal Feedback
  - 1.2V, 1.8V, or 3.3V Factory Preset Options Internal Feedback
  - 0.8V to 99%V_{SUP} with External Feedback Resistors
- High-Efficiency, Low Supply Current Extends Battery Life
  - 94% Peak Efficiency at 7.4V_{SUP}, 3.3V_{OUT} (2520 Inductor)
  - 9µA I_{SUP} (12V_{SUP}, 1.8V_{OUT} Internal Feedback Version)
  - Selectable Light-Load SKIP and Forced-PWM Modes
- 1MHz or 550kHz Fixed-Frequency Switching
- Hardware or Software Control
  - Enable Input and Power-OK Output Pins
  - Optional I^2C Full Control Interface
- Protection Features
  - Cycle-by-Cycle Inductor Peak Current Limit
  - Short-Circuit Hiccup Mode, UVLO, and Thermal Shutdown Protections
  - 1ms Default Soft-Start
- Small Size
  - 1.85mm x 1.4mm (0.7mm max. height) WLP
  - 12-Bump, 0.4mm Pitch, 3 x 4 Array

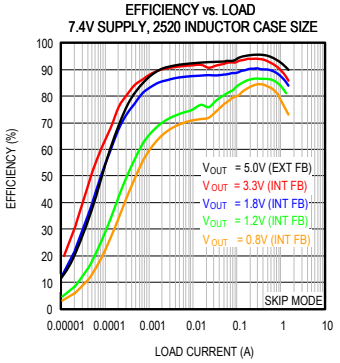
***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



FEEDBACK	V_{OUT} RANGE
INTERNAL	0.8V TO 5V
EXTERNAL	0.8V TO 99%V_{SUP}

14V, 1.5A HIGH-EFFICIENCY BUCK CONVERTER OPTIMIZED FOR 2 OR 3 CELL BATTERY APPLICATIONS



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Absolute Maximum Ratings

SUP to PGND ..... -0.3V to +16V
EN to PGND ..... -0.3V to V_{SUP} + 0.3V
BST to LX ..... -0.3V to +2.2V
BST to PGND ..... -0.3V to +17.8V
SDA, SCL to PGND ..... -0.3V to +6V
V_L to PGND ..... -0.3V to +2.2V
BIASEN, POK to PGND ..... -0.3V to MIN(V_{SUP}+0.3V, +6V)
OUT/FB to PGND ..... -0.3V to +6V
AGND to PGND ..... -0.3V to +0.3V
OUT/FB Short-Circuit Duration ..... Continuous
LX Continuous Current (Note 1) ..... 1.6A_{RMS}
Continuous Power Dissipation (Multilayer Board, T_A = +70°C) (derate 13.73mW/°C above +70°C) (Note 2) 1099mW
Operating Ambient Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: LX has internal clamp diodes to PGND and SUP. Applications that forward bias these diodes should not exceed the ICs package power dissipation limits.

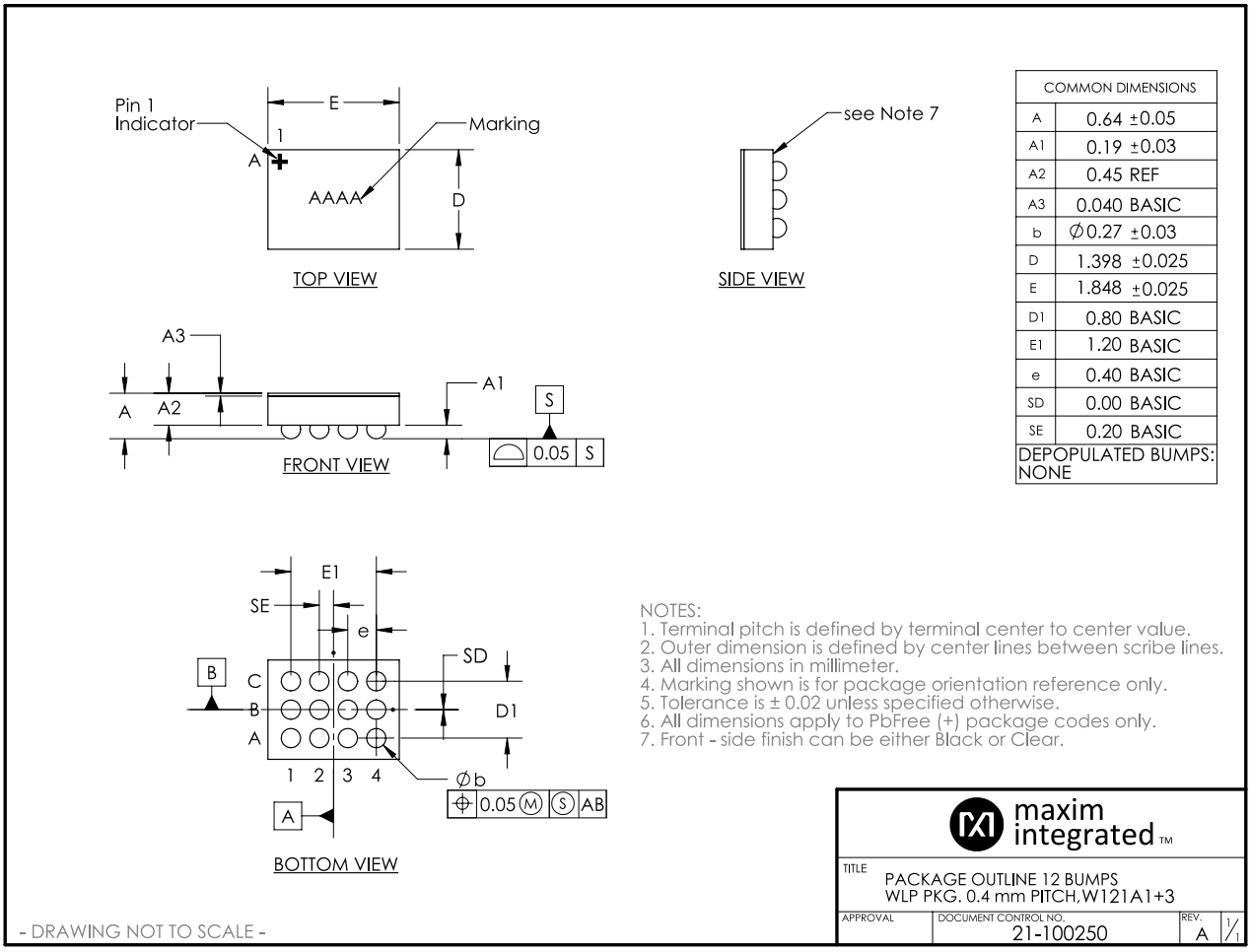
Note 2: Package thermal measurements were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 WLP

Package Code	W121A1+3
Outline Number	21-100250
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	72.82°C/W



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.040 BASIC
b	Ø0.27 ±0.03
D	1.398 ±0.025
E	1.848 ±0.025
D1	0.80 BASIC
E1	1.20 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP} = V_{EN} = 12V, SKIP mode, V_L = 1.8V, configuration registers in reset, T_A = T_J = -40ºC to +85ºC, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 3.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-DOWN CONVERTER							
SUP Valid Voltage Range	V_{SUP}			3		14	V
SUP Undervoltage Lockout	$V_{SUP-UVLO}$	V_{SUP} rising		2.8	2.9	3.0	V
SUP Undervoltage-Lockout Hysteresis					300		mV
SUP Shutdown Current	$I_{SUP-SHDN}$	V_{EN} = V_{BIASEN} = 0V (device disabled)			1.2	3	µA
SUP Standby Current	$I_{SUP-STNBY}$	V_{EN} = 0V, V_{BIASEN} = 1.8V (V_L regulator and internal logic enabled, buck converter output disabled)			40	60	µA
SUP Quiescent Current	I_{SUP-Q}	I_{LOAD} = 0mA, no switching	V_{OUT} = 3.3V, internal feedback version		14	30	µA
			External feedback version		40	60	
			All versions, FPWM mode		1	1.5	mA
V_L Regulator Voltage	V_L	V_{SUP} = 3V to 14V			1.8		V
OUT Voltage Accuracy	V_{OUT}	1.2V factory-default version ($V_{OUT-REG}$ = 1.2V), FPWM mode	V_{SUP} = 12V, I_{LOAD} = 250mA, T_A = +25°C	1.188	1.2	1.212	V
			V_{SUP} = 3V to 14V, I_{LOAD} = 0mA to 1.5A, T_A = -40°C to +85°C	1.176	1.2	1.224	
		3.3V factory-default version ($V_{OUT-REG}$ = 3.3V), FPWM mode	V_{SUP} = 12V, I_{LOAD} = 250mA, T_J = +25°C	3.267	3.3	3.333	
			V_{SUP} = 4.5V to 14V, I_{LOAD} = 0mA to 1.5A, T_J = -40°C to +85°C	3.234	3.3	3.366	
FB Voltage Accuracy	V_{FB}	External feedback version, FPWM mode	V_{SUP} = 12V, I_{LOAD} = 250mA, T_J = +25°C	0.792	0.8	0.808	V
			V_{SUP} = 3.0V to 14V, I_{LOAD} = 0mA to 1.5A, T_J = -40°C to +85°C	0.784	0.8	0.816	
FB Input Current	I_{FB}	V_{FB} = 0.8V, external feedback version			0.02		µA
OUT/FB Load Regulation		FPWM mode, 0A to 1.5A load, all versions			0.1		%
OUT/FB Line Regulation		V_{SUP} = 3V to 14V, V_{OUT} = 1.8V, FPWM mode, I_{OUT} = 0A to 1.5A			0.02		%/V_{SUP}

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 12V, SKIP mode, V_L = 1.8V, configuration registers in reset, T_A = T_J = -40ºC to +85ºC, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 3.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT/FB Soft-Start Ramp Time	t_{SS}	SFT_STRT[1:0] = 0b00			1		ms
		SFT_STRT[1:0] = 0b01			2		
		SFT_STRT[1:0] = 0b10			4		
		SFT_STRT[1:0] = 0b11			8		
High-Side DMOS On-Resistance	R_{ON-HS}	V_L = 1.8V, I_{LX} = 90mA			90	180	mΩ
Low-Side DMOS On-Resistance	R_{ON-LS}	V_L = 1.8V, I_{LX} = 90mA			55	110	mΩ
High-Side DMOS Peak Current Limit	$I_{LX-PLIM}$	$I_{LX-PLIM}$ = 500mA (I_PEAK = 0)		350	500	600	mA
		$I_{LX-PLIM}$ = 2000mA (I_PEAK = 1)		1800	2000	2200	
Low-Side DMOS Valley Current Threshold	$I_{LX-VALLEY}$	Output overloaded (V_{OUT} < 25% of target), threshold below where on-times are allowed to start.	$I_{LX-PLIM}$ = 500mA (I_PEAK = 0)		250		mA
			$I_{LX-PLIM}$ = 2000mA (I_PEAK = 1)		1000		
High-Side DMOS Minimum Current Threshold	$I_{LX-PK-MIN}$	Inductor current ramps to at least $I_{LX-PK-MIN}$ in SKIP mode			200		mA
Low-Side DMOS Zero-Crossing Threshold	I_{ZX}	SKIP mode			40		mA
Low-Side DMOS Negative Current-Limit Threshold	I_{NEG}	FPWM Mode			-700		mA
Minimum On-Time	t_{ON-MIN}				100		ns
Maximum Duty Cycle	D_{MAX}	Dropout condition (V_{SUP} < V_{OUT} target). On-times extend for 16 clocks before LX drives low for 200ns to refresh C_{BST}.			99		%
Switching Frequency	F_{SW}	FPWM mode	External feedback version	0.9	1	1.1	MHz
			Internal feedback version, $V_{OUT-REG}$ ≥ 1.55V	0.9	1	1.1	
			Internal feedback version, $V_{OUT-REG}$ ≤ 1.5V		0.55		
Minimum Switching Frequency	F_{SW-MIN}	SKIP mode			1.43		kHz
Soft-Short Output Voltage Monitor Threshold	$V_{OUT-OVRLD}$				0.25 x $V_{OUT-REG}$		V

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 12V, SKIP mode, V_L = 1.8V, configuration registers in reset, T_A = T_J = -40ºC to +85ºC, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 3.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output-Overloaded Retry (Hiccup) Timer	t_{RETRY}	Switching stopped due to output overload (Note 4)	External feedback version		12		ms
			Internal feedback version, $V_{OUT-REG}$ ≥ 1.55V		12		
			Internal feedback version, $V_{OUT-REG}$ ≤ 1.5V		21.8		
Active Discharge Resistor	R_{AD}	Between OUT and PGND, buck output disabled, active discharge resistor enabled (ADEN = 1), internal feedback versions only			100		Ω
POWER-OK OUTPUT (POK)							
POK Threshold	$V_{POK-RISE}$	V_{OUT} rising, expressed as a percentage of $V_{OUT-REG}$		90	92	94	%
	$V_{POK-FALL}$	V_{OUT} falling, expressed as a percentage of $V_{OUT-REG}$		88	90	92	
POK Debounce Timer	t_{POK-DB}	V_{OUT} rising or falling, 1MHz clock frequency			20		µs
POK Leakage Current	I_{POK}	POK = high (high-Z), V_{POK} = 5V, T_A = +25°C				1	µA
POK Low Voltage	V_{POK}	POK = low, sinking 1mA				0.4	V
ENABLE INPUTS (EN, BIASEN)							
EN Logic High Threshold	V_{EN_HI}			1.1			V
EN Logic Low Threshold	V_{EN_LO}					0.4	V
EN Leakage Current	I_{EN}	V_{EN} = V_{SUP} = 12V			0.1		µA
BIASEN Logic High Threshold	V_{BIASEN_HI}			1.1			V
BIASEN Logic Low Threshold	V_{BIASEN_LO}					0.4	V
SERIAL INTERFACE / I/O STAGE							
SCL, SDA Input High Voltage	V_{IH}			1.44			V
SCL, SDA Input Low Voltage	V_{IL}					0.54	V
SCL, SDA Input Hysteresis	V_{HYS}				0.3		V
SCL, SDA Input Leakage Current	I_I	V_{SCL} = V_{SDA} = 0V or 1.8V		-1		+1	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA				0.4	V
SCL, SDA Pin Capacitance		(Note 5)			10		pF

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 12V, SKIP mode, V_L = 1.8V, configuration registers in reset, T_A = T_J = -40ºC to +85ºC, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 3.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Filter Suppressed Spike Maximum Pulse Width	t_{SP}	(Note 5)		50		ns
SERIAL INTERFACE / TIMING						
Clock Frequency	f_{SCL}				1	MHz
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Setup Time REPEATED START Condition	$t_{SU;STA}$		260			ns
Hold Time REPEATED START Condition	$t_{HD;STA}$		260			ns
SCL Low Period	t_{LOW}		500			ns
SCL High Period	t_{HIGH}		260			ns
Data Setup Time	$t_{SU;DAT}$		50			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Setup Time for STOP Condition	$t_{SU;STO}$		260			ns
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	Junction temperature rising		+165		°C
Thermal-Shutdown Hysteresis				+15		°C

Note 3: The MAX77533 is tested under pulsed load conditions such that $T_A \approx T_J$. Min/Max limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization using statistical quality control methods. Note that the maximum ambient temperature consistent with this specification is determined by specific operating conditions, board layout, rated package thermal impedance, and other environmental factors.

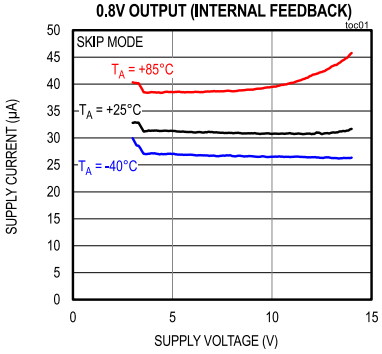
Note 4: See the *Short-Circuit Protection and Hiccup Mode* section.

Note 5: Design guidance only. Not production tested.

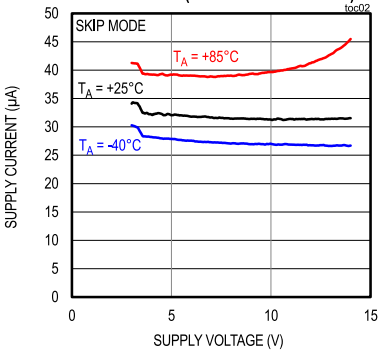
Typical Operating Characteristics

(V_{SUP} = 12V, V_{OUT} = 1.8V, L = 2.2µH (MURATA 2520 case size), SKIP Mode, $I_{LX-PLIM}$ = 2A, T_A = +25ºC, internal feedback version (unless otherwise noted).)

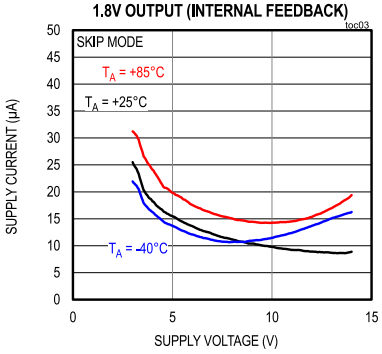
SUPPLY CURRENT vs. SUPPLY VOLTAGE
0.8V OUTPUT (INTERNAL FEEDBACK)



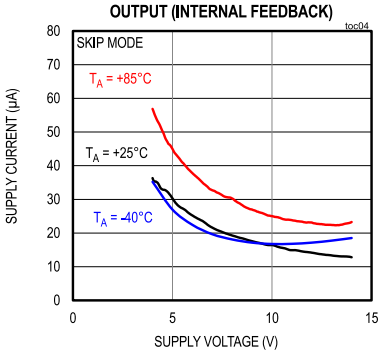
SUPPLY CURRENT vs. SUPPLY VOLTAGE
1.2V OUTPUT (INTERNAL FEEDBACK)



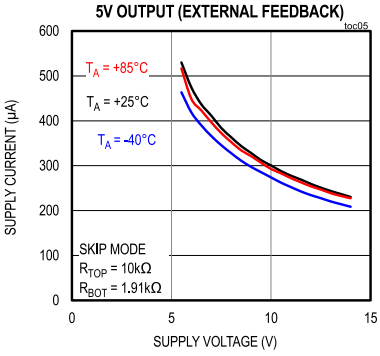
SUPPLY CURRENT vs. SUPPLY VOLTAGE
1.8V OUTPUT (INTERNAL FEEDBACK)



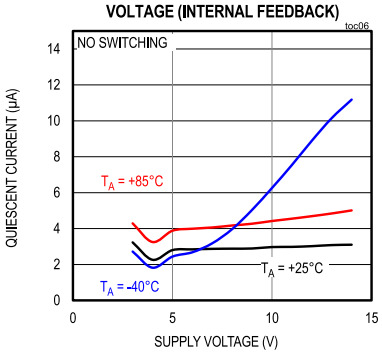
SUPPLY CURRENT vs. SUPPLY VOLTAGE 3.3V
OUTPUT (INTERNAL FEEDBACK)



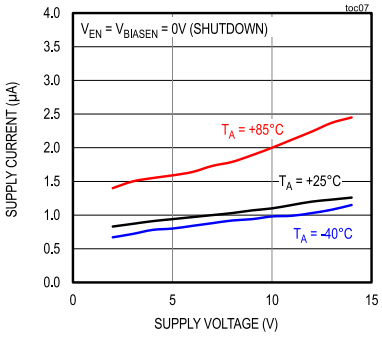
SUPPLY CURRENT vs. SUPPLY VOLTAGE
5V OUTPUT (EXTERNAL FEEDBACK)



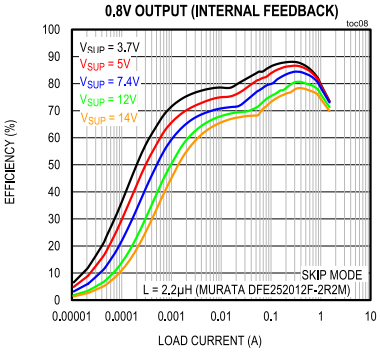
QUIESCENT CURRENT vs. SUPPLY
VOLTAGE (INTERNAL FEEDBACK)



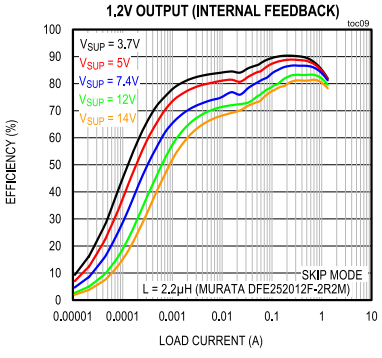
SHUTDOWN CURRENT vs. SUPPLY
VOLTAGE



EFFICIENCY vs. LOAD
0.8V OUTPUT (INTERNAL FEEDBACK)



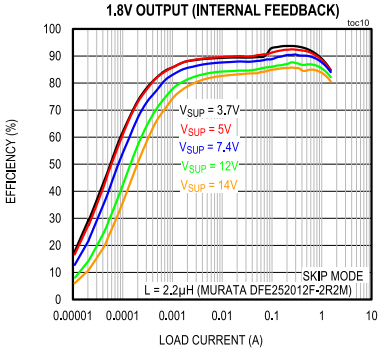
EFFICIENCY vs. LOAD
1.2V OUTPUT (INTERNAL FEEDBACK)



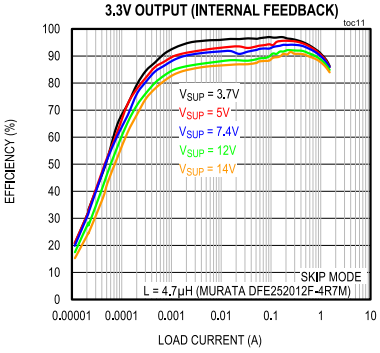
Typical Operating Characteristics (continued)

(V_{SUP} = 12V, V_{OUT} = 1.8V, L = 2.2µH (MURATA 2520 case size), SKIP Mode, $I_{LX-PLIM}$ = 2A, T_A = +25ºC, internal feedback version (unless otherwise noted).)

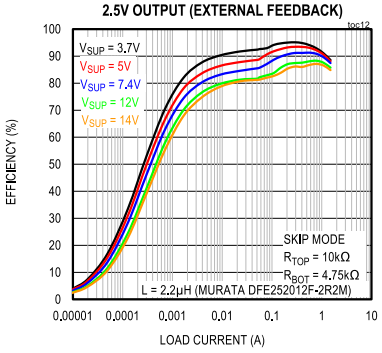
EFFICIENCY vs. LOAD
1.8V OUTPUT (INTERNAL FEEDBACK)



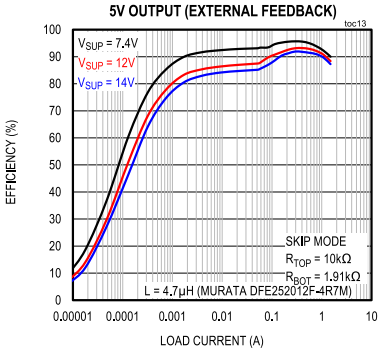
EFFICIENCY vs. LOAD
3.3V OUTPUT (INTERNAL FEEDBACK)



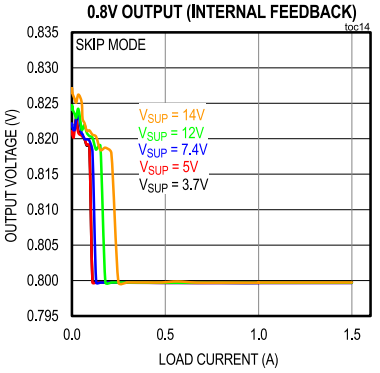
EFFICIENCY vs. LOAD
2.5V OUTPUT (EXTERNAL FEEDBACK)



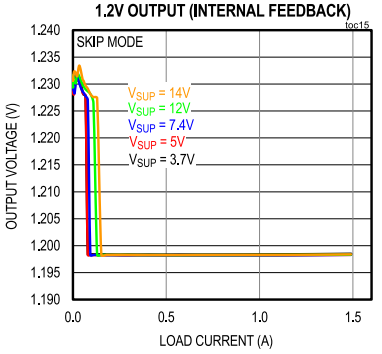
EFFICIENCY vs. LOAD
5V OUTPUT (EXTERNAL FEEDBACK)



LOAD REGULATION
0.8V OUTPUT (INTERNAL FEEDBACK)



LOAD REGULATION
1.2V OUTPUT (INTERNAL FEEDBACK)



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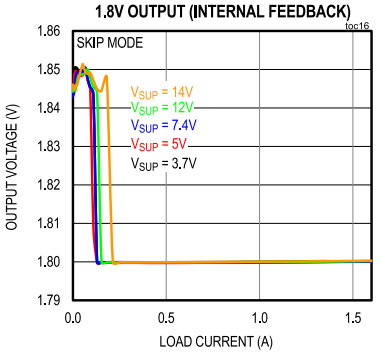

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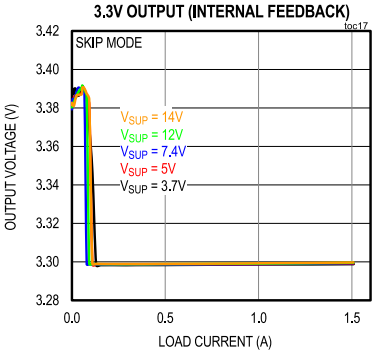

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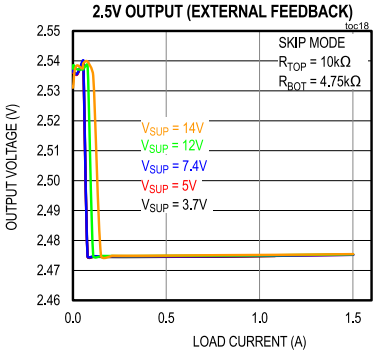
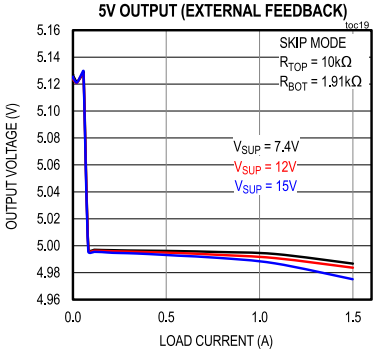


Typical Operating Characteristics (continued)

(V_{SUP} = 12V, V_{OUT} = 1.8V, L = 2.2µH (MURATA 2520 case size), SKIP Mode, $I_{LX-PLIM}$ = 2A, T_A = +25ºC, internal feedback version (unless otherwise noted).)

LOAD REGULATION
5V OUTPUT (EXTERNAL FEEDBACK)



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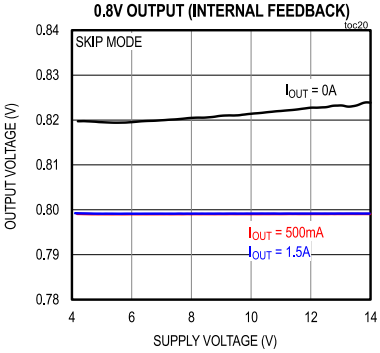
0.8V OUTPUT (INTERNAL FEEDBACK)



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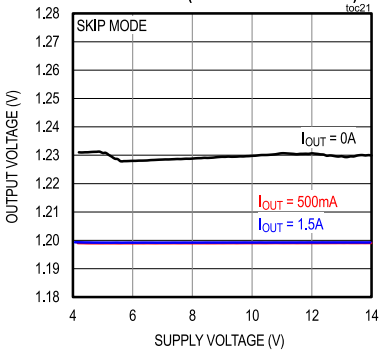

LINE REGULATION
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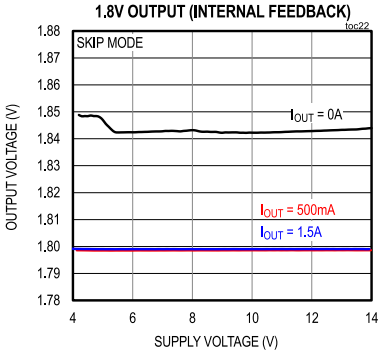

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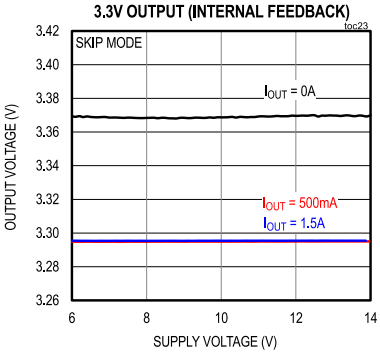

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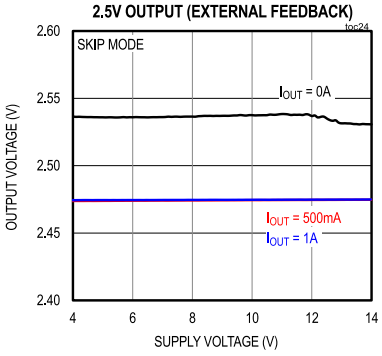
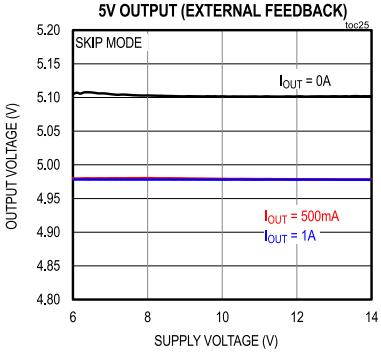


LINE REGULATION
5V OUTPUT (EXTERNAL FEEDBACK)



LOAD TRANSIENT RESPONSE
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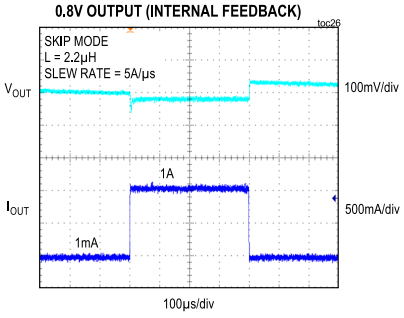

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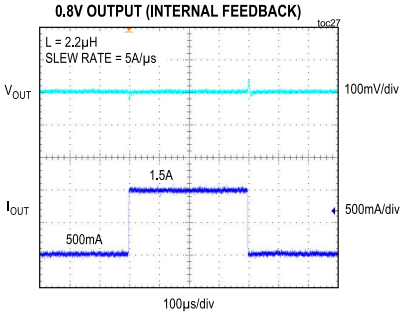
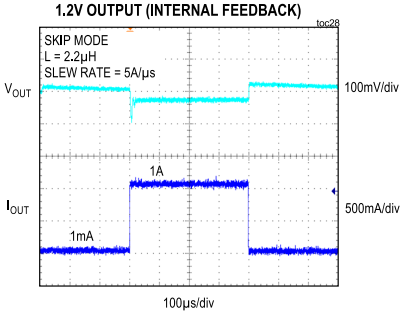


Typical Operating Characteristics (continued)

(V_{SUP} = 12V, V_{OUT} = 1.8V, L = 2.2µH (MURATA 2520 case size), SKIP Mode, $I_{LX-PLIM}$ = 2A, T_A = +25ºC, internal feedback version (unless otherwise noted).)

LOAD TRANSIENT RESPONSE
1.2V OUTPUT (INTERNAL FEEDBACK)



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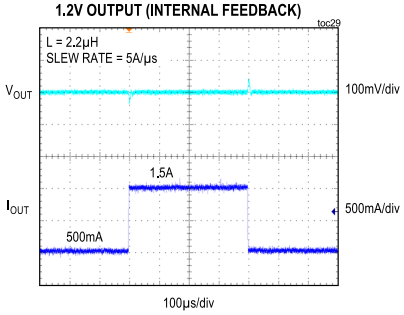

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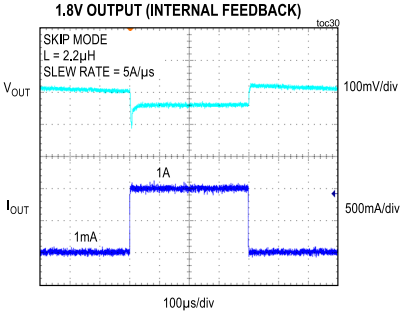

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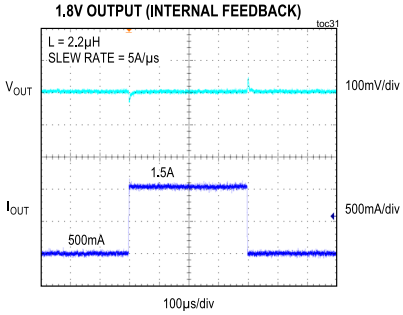
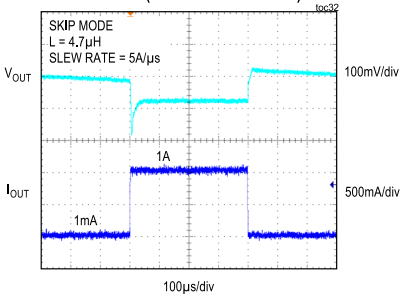
1.8V OUTPUT (INTERNAL FEEDBACK)



LOAD TRANSIENT RESPONSE
3.3V OUTPUT (INTERNAL FEEDBACK)



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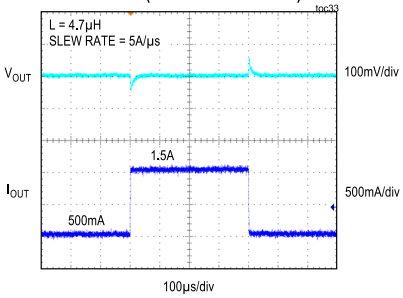
3.3V OUTPUT (INTERNAL FEEDBACK)



LOAD TRANSIENT RESPONSE
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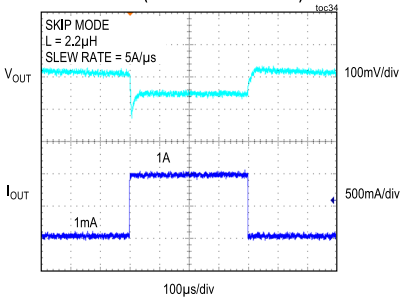

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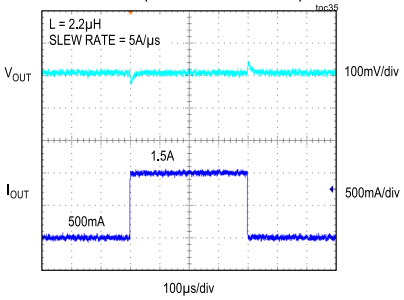

LINE TRANSIENT RESPONSE
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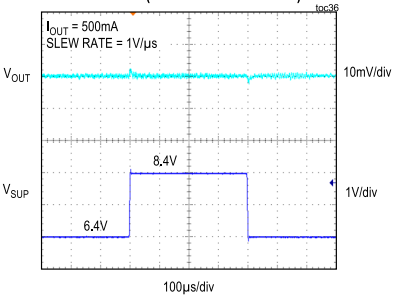
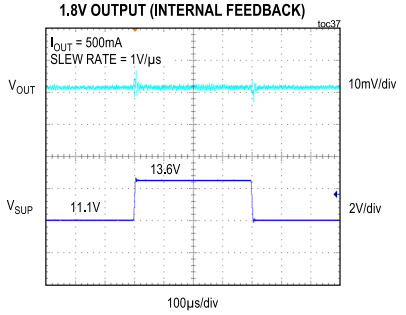


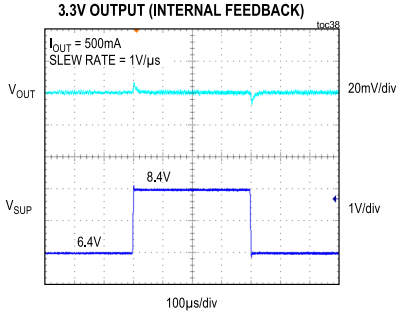
Typical Operating Characteristics (continued)

(V_{SUP} = 12V, V_{OUT} = 1.8V, L = 2.2µH (MURATA 2520 case size), SKIP Mode, $I_{LX-PLIM}$ = 2A, T_A = +25ºC, internal feedback version (unless otherwise noted).)

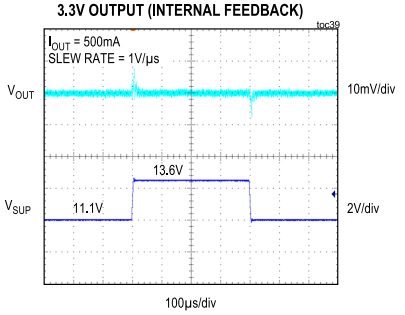
LINE TRANSIENT RESPONSE
1.8V OUTPUT (INTERNAL FEEDBACK)



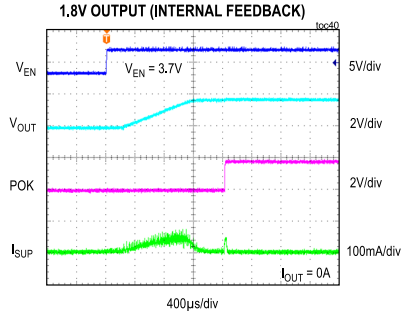
LINE TRANSIENT RESPONSE
3.3V OUTPUT (INTERNAL FEEDBACK)



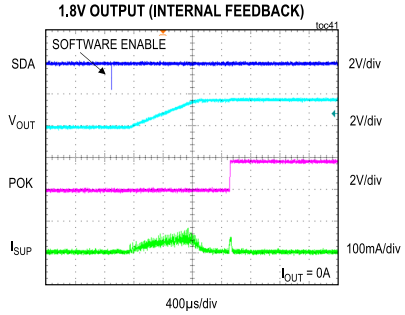
LINE TRANSIENT RESPONSE
3.3V OUTPUT (INTERNAL FEEDBACK)



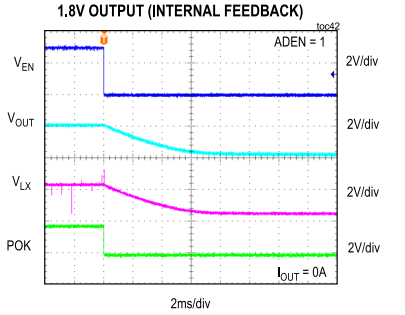
HARDWARE STARTUP WAVEFORM
1.8V OUTPUT (INTERNAL FEEDBACK)



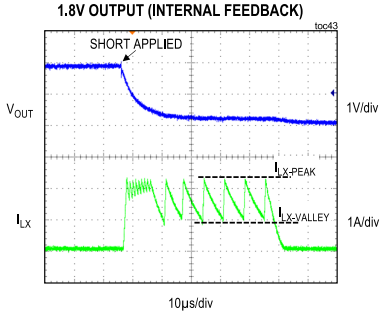
SOFTWARE STARTUP WAVEFORM
1.8V OUTPUT (INTERNAL FEEDBACK)



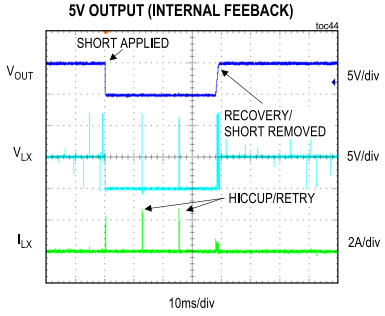
SHUTDOWN WAVEFORM
1.8V OUTPUT (INTERNAL FEEDBACK)



SHORT-CIRCUIT RESPONSE
1.8V OUTPUT (INTERNAL FEEDBACK)

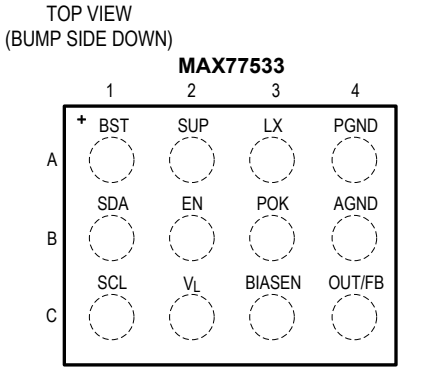


SHORT-CIRCUIT HICCUP AND RECOVERY
5V OUTPUT (INTERNAL FEEBACK)



Bump Configuration

12 WLP



12 WLP
(1.85mm x 1.4mm x 0.7mm, 0.4mm PITCH)

Bump Descriptions

PIN	NAME	FUNCTION
A1	BST	High-Side FET Driver Supply. Connect a 0.22µF ceramic capacitor between BST and LX.
A2	SUP	Buck Supply Input. Bypass to PGND with a 4.7µF ceramic capacitor as close to the IC as possible.
A3	LX	Switching Node. LX is high-impedance when the converter is disabled.
A4	PGND	Power Ground. Connect to AGND on the PCB.
B4	AGND	Quiet Ground. Connect to PGND on the PCB.
C4	OUT/FB	**Internal Feedback Versions:** Output Voltage Sense Input. Connect to the positive voltage side of the output capacitors to regulate the buck output voltage. **External Feedback Version:** Feedback Sense Input. Connect a resistor voltage divider between the converter's output and AGND to set the output voltage. Connect a 100pF feed-forward capacitor between the converter's output and FB. Do not route FB close to sources of EMI or noise.
C2	V_L	Low-Voltage Internal IC Supply Output. Bypass to AGND with a 2.2µF ceramic capacitor. Do not load this pin externally.
B3	POK	Open-Drain Power-OK Output. An external pullup resistor (10kΩ to 100kΩ) is required to use this pin. Leave this pin unconnected if unused.
B2	EN	Enable Input. Drive EN above V_{EN_HI} to enable the buck output. Drive EN to PGND to disable. EN is compatible with the SUP voltage domain. If using I^2C to control the buck, the enable bit (EN_BIT) interacts with the EN pin. See the *Buck Enable Control (EN)* section.
C3	BIASEN	Bias Enable Input. Enables the I^2C interface without enabling the buck output. Drive BIASEN above V_{BIASEN_HI} to enable the I^2C interface. Drive to ground to disable. See the *Bias Enable Control (BIASEN)* section for more information.
B1	SDA	I^2C Serial Interface Data. Connect to ground if not used.
C1	SCL	I^2C Serial Interface Clock. Connect to ground if not used.

Detailed Description

The MAX77533 is a small, high-efficiency 1.5A step-down (buck) DC-DC converter. The step-down converter uses synchronous rectification and internal current-mode compensation. The buck operates on a supply voltage between 3V and 14V. Output voltage is configurable through I^2C from 0.8V to 5V or external programming resistors between 0.8V and 99% of V_{SUP}. Factory-default voltage options of 1.2V, 1.8V, and 3.3V are available (see the *Ordering Information* table). The buck utilizes an ultra-low supply current (I_{SUP}) SKIP mode (9µA typ for 1.8V_{OUT}) that maintains very high-efficiency at light loads.

Buck Regulator Control Scheme

The step-down converter uses a PWM peak current-mode control scheme with a high-gain architecture. Peak current-mode control provides precise control of the inductor current on a cycle-by-cycle basis and inherent compensation for supply voltage variation.

On-times (MOSFET Q1 on) are started by a fixed-frequency clock and terminated by a PWM comparator. See Figure 1. When an on-time ends (starting an off-time) current conducts through the low-side MOSFET (Q2 on). Shoot-through current from SUP to PGND is avoided by introducing a brief period of dead time between switching events when neither MOSFET is on. Inductor current conducts through the MOSFETs' intrinsic body diode during dead time.

The PWM comparator regulates V_{OUT} by controlling duty cycle. The negative input of the PWM comparator is a voltage proportional to the actual output voltage error. The positive input is the sum of the current-sense signal through MOSFET Q1 and a slope-compensation ramp. The PWM comparator ends an on-time when the error voltage becomes less than the slope-compensated current-sense signal. On-times begin again due to a fixed-frequency clock pulse. The controller's compensation components and current-sense circuits are integrated. This reduces the risk of routing sensitive control signals on the PCB.

A high-gain architecture is present in the controller design. The feedback uses an integrator to eliminate steady-state output voltage error while the converter is conducting heavy loads. See the *Typical Operating Characteristics* section for information about the converter's typical voltage regulation behavior versus load.

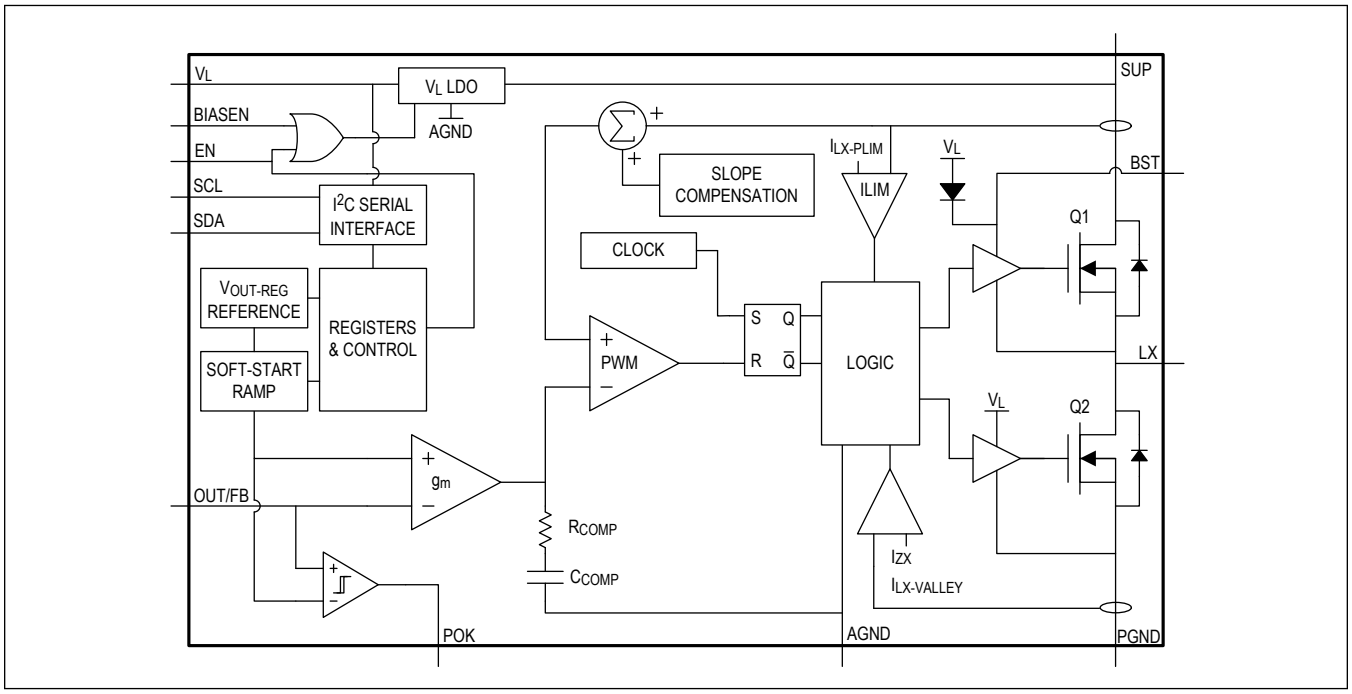


Figure 1. Buck Control Scheme Diagram

Mode Control

Write the MODE bit to 0 to enable SKIP mode. Write MODE to 1 to enable forced-PWM (FPWM) mode. The default value of MODE is 0 (SKIP).

SKIP Mode

SKIP mode causes discontinuous inductor current at light loads by forcing the low-side MOSFET (Q2) off if inductor current falls below I_{ZX} (40mA typ) during an off-time. This prevents inductor current from sourcing back to the input (SUP) and enables high-efficiency by reducing the total number of switching cycles required to regulate the output voltage.

When the load is very light and the output voltage is in regulation, then the converter automatically transitions to standby mode. In this mode, the LX node is high-impedance and the converter's internal circuit blocks are deactivated to reduce I_Q consumption. Output voltage typically rests 2.5% above the regulation target in standby mode. A low-power comparator monitors the output voltage during standby. The converter reactivates and starts switching again when V_{OUT} drops below 102% of regulation target.

FPWM Mode

The low-side MOSFET (Q2) current-limit threshold is I_{NEG} (-700mA typ) in FPWM mode, which allows the converter to switch at constant frequency at light loads. The buck has the best possible load-transient response in this mode at the cost of higher I_Q consumption. Use FPWM for applications that do not require low-I_Q and/or when heavy load transients are expected. Switching frequency is fixed by an internal oscillator in FPWM mode. See Table 1.

Table 1. Buck Switching Frequency

FEEDBACK	OUTPUT VOLTAGE	SWITCHING FREQUENCY (F_{SW})
External (V_{OUT} set by resistors)	0.8V to 99%V_{SUP}	1MHz
Internal (V_{OUT} set by serial interface)	1.55V to 5V	1MHz
Internal (V_{OUT} set by serial interface)	0.8V to 1.5V	550kHz

Buck Enable Control (EN)

Raise the EN pin voltage above V_{EN_HI} (or tie to SUP) to enable the buck output. Lower EN to PGND to disable.

When using I^2C to control the device, the EN pin interacts with the enable bit (EN_BIT). The logical relationship between the EN pin and EN_BIT is by default an OR. Use the EN_LOGIC bit to change this relationship to a logical AND. See Table 2.

Table 2. Buck Enable Truth Table

EN_LOGIC (BIT)	EN (PIN)	EN_BIT (BIT)	BUCK OUTPUT
0 (logical OR)	0	0	OFF
	0	1	ON
	1	0	ON
	1	1	ON
1 (logical AND)	0	0	OFF
	0	1	OFF
	1	0	OFF
	1	1	ON

The reset state (default state) of EN_BIT and EN_LOGIC is 0. This means that the default relationship between the enable pin and the enable bit is a logical OR.

Bias Enable Control (BIASEN)

BIASEN is an active-high digital input that enables the device's V_L regulator and I^2C serial interface. Raise BIASEN above V_{BIASEN_HI} to activate the serial interface. Lower BIASEN to PGND to deactivate.

Serial I^2C reads and writes may happen while SUP is valid and BIASEN is high regardless of whether the buck output is on or off. This allows the host controller to change the device's configuration registers before enabling the buck output.

When the device is enabled through the EN pin, the BIASEN signal is a *don't care*. See Table 3.

Table 3. V_L Enable Truth Table

EN (PIN)	BIASEN (PIN)	V_L AND I^2C SERIAL INTERFACE
0	0	OFF
0	1	ON
1	X	ON

V_L Regulator

An integrated 1.8V linear regulator (V_L) provides power to low-voltage internal circuit blocks and switching FET gate drivers. V_L activates according to Table 3.

SUP powers V_L for the internal feedback versions of the device when $V_{OUT-REG}$ is < 1.8V. If $V_{OUT-REG}$ is ≥ 1.8V, then the V_L regulator power input switches from SUP to OUT after the buck soft-start ramp finishes and POK = 1. Switching V_L's input to OUT utilizes the buck's high-efficiency to power the linear regulator (as opposed to SUP) and improves the device's total power efficiency. SUP permanently powers V_L for the external feedback version of the device.

Do not load V_L externally for any MAX77533 version. The V_L regulator activates whenever EN or BIASEN is high. Connect a 2.2µF ceramic capacitor from V_L to ground on the PCB.

Soft-Start

The device has an internal soft-start timer (t_{SS}) that controls the ramp time of the output as the converter is starting. Soft-start limits inrush current during buck startup. SFT_STRT[1:0] programs t_{SS} to 1ms/2ms/4ms/8ms. The default value of SFT_STRT[1:0] can be programmed at the factory. The converter soft-starts every time the buck enables, exits a UVLO condition, and/or retries from an overcurrent (hiccup) or overtemperature condition.

Power-OK (POK) Output

The device features an active-high, open-drain POK output to monitor the output voltage. POK requires an external pullup resistor (typically 10kΩ to 100kΩ). POK goes high (high-impedance) after the buck converter output increases above 92% ($V_{POK-RISE}$) of the target regulation voltage ($V_{OUT-REG}$) and the soft-start ramp is done. POK goes low when the output drops below 90% ($V_{POK-FALL}$) of target or when the buck is disabled.

Peak Inductor Current Limit

The buck converter's high-side MOSFET peak current limit ($I_{LX-PLIM}$) is register programmable. Applications can use $I_{LX-PLIM}$ programmability to ensure that the converter never exceeds the saturation current rating of the inductor on the PCB.

Program the I_PEAK bit to 0 to set $I_{LX-PLIM}$ to 500mA. Program I_PEAK to 1 to set $I_{LX-PLIM}$ to 2000mA. The default value is 1 (2000mA).

Active Discharge Resistor

The device integrates a 100Ω active discharge resistor (R_{AD}) between OUT and PGND that discharges the output capacitor when the buck is disabled. Write ADEN = 1 through I^2C to enable the active discharge resistor function. The default value of ADEN can be programmed at the factory. The active discharge function is permanently disabled for the external feedback version of the device.

R_{AD} discharges the output capacitor for 16383 clock periods when ADEN = 1 and the buck is disabled.

- For $V_{OUT-REG} \geq 1.55V$, this is approximately 16ms.
- For $V_{OUT-REG} \leq 1.5V$, this is approximately 30ms.

The OUT pin returns to a high-impedance state after this time.

Short-Circuit Protection and Hiccup Mode

The device has fault protection designed to protect itself from abnormal conditions. If the output is overloaded, cycle-by-cycle current limit prevents inductor current from increasing beyond $I_{LX-PLIM}$.

The buck stops switching if V_{OUT} falls to less than 25% of programmed $V_{OUT-REG}$ and 15 consecutive on-times are ended by current limit. After switching stops, the buck waits for t_{RETRY} before attempting to soft-start again (hiccup mode). While V_{OUT} is less than 25% of target, the converter prevents new on-times if the inductor current has not fallen below $I_{LX-VALLEY}$. This prevents inductor current from increasing uncontrollably due to the short-circuited output.

Thermal Shutdown

The device has an internal thermal protection circuit which monitors die temperature. The temperature monitor disables the buck if the die temperature exceeds T_{SHDN} (165°C typ). The buck soft-starts again after the die temperature cools by approximately 15°C.

Register Reset Condition

The device's internal configuration registers reset to their default values if V_{SUP} falls below the UVLO falling threshold ($V_{SUP-UVLO}$ minus UVLO hysteresis, 2.6V typ). Contact the factory to request a version of the device that holds configuration registers in reset if BIASEN is low.

I²C Serial Interface

All MAX77533 versions feature a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77533 is a slave-only device that relies on an external bus master to generate SCL. SCL clock rates from 0Hz to 3.4MHz are supported. I²C is an open-drain bus, and therefore, SDA and SCL require pullups.

The device's I²C-communication controller implements 7-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. The slave address is factory-programmable to one of four options (see Table 4). All slave addresses not mentioned in Table 4 are not acknowledged.

The device uses 8-bit registers with 8-bit register addressing. They support standard communication protocols: (1) Writing to a single register (2) Writing to multiple sequential registers with an automatically incrementing data pointer (3) Reading from a single register (4) Reading from multiple sequential registers with an automatically incrementing data pointer. For additional information on the I²C protocols, refer to the *MAX77503 I²C Implementer's Guide* and/or the I²C specification that is freely available on the internet.

Table 4. I²C Slave Address Options

7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
0x1E 0b 001 1110	0x3C 0b 0011 1100	0x3D 0b 0011 1101
0x24 0b 010 0100	0x48 0b 0100 1000	0x49 0b 0100 1001
0x37 0b 011 0111	0x6E 0b 0110 1110	0x6F 0b 0110 1111
0x77 0b 111 0111	0xEE 0b 1110 1110	0xEF 0b 1110 1111
See the *Ordering Information* table for the slave address associated with each part number.		

Register Map

MAX77533

ADDRESS	NAME	MSB							LSB
Configuration Registers									
0x00	CONFIG_A[7:0]	RSVD	ADEN	SFT_STRT[1:0]		I_PEAK	MODE	EN_LOGIC	EN_BIT
0x01	CONFIG_B[7:0]	RSVD	V_OUTREG[6:0]						

Register Details

CONFIG_A (0x00)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	ADEN	SFT_STRT[1:0]		I_PEAK	MODE	EN_LOGIC	EN_BIT
Reset	0b0	OTP	OTP		0b1	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
ADEN	6	Active discharge resistor enable. This function is only available in the internal feedback versions of the device. This function is permanently disabled in the external feedback version (bit is a *don't care*).	0 = disabled 1 = enabled
SFT_STRT	5:4	Soft-start control. Sets the buck converter's startup ramp time (t_{SS}).	00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms
I_PEAK	3	High-side DMOS peak current-limit threshold control. Sets peak LX current limit ($I_{LX-PLIM}$).	0 = 500mA 1 = 2000mA
MODE	2	Buck converter mode control.	0 = SKIP mode 1 = FPWM mode
EN_LOGIC	1	Enable logic control bit. Determines the logical relationship between EN_BIT (enable bit) and EN (enable pin).	0 = logical *OR* relationship 1 = logical *AND* relationship
EN_BIT	0	Buck enable bit.	0 = disabled 1 = enabled

CONFIG_B (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	V_OUTREG[6:0]						
Reset	0b0	0x08 / 0x14 / 0x32 (See the Ordering Information table)						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A

BITFIELD	BITS	DESCRIPTION	DECODE
V_OUTREG	6:0	Output Voltage Control (internal feedback versions only). Sets $V_{OUT-REG}$. Programmable in 50mV per LSB from 0x00 (0.8V) to 0x54 (5V). The default value of this register is preset for internal feedback versions of the device. See the Ordering Information section. Overwriting the default value sets a new target output voltage. This register is a *don't care* for the external feedback version of the device. Avoid changing this bitfield while the converter is both enabled and loaded. Increasing the V_{OUT} target while the buck is supplying load may cause the converter to enter hiccup mode.	0x00 = 0.80V 0x01 = 0.85V 0x02 = 0.90V ... 0x08 = 1.20V .... 0x14 = 1.80V ... 0x32 = 3.30V ... 0x53 = 4.95V 0x54-0x7F = 5.0V

Applications Information

Buck Enable Options

The MAX77533 offers a high degree of control flexibility. See Figure 2 for suggested methods of controlling the buck converter.

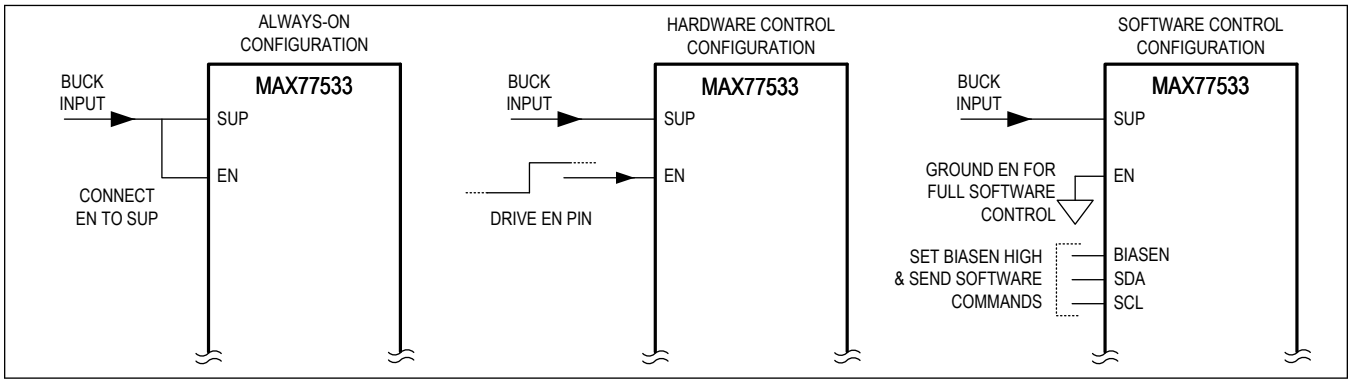


Figure 2. Buck Enable Options

Always-On

Strap the EN pin to SUP to configure the device in an *always-on* configuration. See Figure 2 (left). The buck converter activates whenever V_{SUP} is valid and $T_J < T_{SHDN}$.

Hardware Control

Drive the EN pin externally to control the buck. See Figure 2 (center). The buck converter activates whenever $V_{EN} > V_{EN_HI}$ (1.1V min), $T_J < T_{SHDN}$, and V_{SUP} is valid.

The default relationship between the EN pin and the EN_BIT is a logic OR. See Table 2 for more details.

Software Control

Use the I^2C serial interface to control the buck by connecting SDA and SCL to a serial host. See Figure 2 (right).

Assert BIASEN logic high to first activate the I^2C serial interface. The serial host can now do the following:

- Set the target output voltage, $V_{OUT-REG}$ (internal feedback versions only).
- Set the desired soft-start time, t_{SS}.
- Set the peak inductor current limit, $I_{LX-PLIM}$.
- Enable the buck output using EN_BIT.
- Change the converter mode (SKIP/FPWM) dynamically.
- Control the active discharge resistor (internal feedback versions only).

See the *I^2C Serial Interface* and *Register Map* sections for more information. Configuration registers reset if V_{SUP} falls below $V_{SUP-UVLO}$ (2.6V typ). Contact the factory to request a version of the device that holds configuration registers in reset if BIASEN is low.

SUP Capacitor Selection

Choose the input capacitor (C_{SUP}) to be a 4.7µF nominal capacitor that maintains 1µF effective capacitance at its working voltage. Larger values improve the decoupling of the buck converter, but increase inrush current from the voltage supply when connected. C_{SUP} reduces the current peaks drawn from the input power source during buck operation and reduces switching noise in the system. The ESR/ESL of C_{SUP} and its series PCB trace should be very low (i.e., <15mΩ + <2nH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required for stable operation of the buck. Choose the effective C_{OUT} to be 30µF minimum.

Effective C_{OUT} is the actual capacitance value seen by the buck output during operation. Choose effective C_{OUT} carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias. Refer to *Tutorial 5527* for more information.

Larger values of C_{OUT} (above the required effective minimum) improve load transient performance, but increase the input surge currents during soft-start and output voltage changes. The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor’s ESR dominates the output voltage ripple in continuous conduction mode. Therefore, the size of the output capacitor depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD} \times LIR$$

where LIR is the inductor's ripple current to average current ratio. Compute LIR with Equation 1.

Equation 1:

$$LIR = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{V_{IN} \times F_{SW} \times I_{LOAD} \times L}$$

where I_{LOAD} is the buck's output current in the particular application (1.5A max), V_{IN} is the application's input voltage, and F_{SW} is the switching frequency (see Table 1).

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Inductor Selection

Choose an inductor with a saturation current greater than or equal to the maximum peak current limit setting ($I_{LX-PLIM}$). Inductors with lower saturation current and higher DCR ratings tend to be physically small. Higher values of DCR reduce buck efficiency. Choose the RMS current rating of the inductor (the current at which temperature rises appreciably) based on the system's expected load current.

Choose an inductor value based on the V_{OUT} setting. See Table 5.

Table 5. Inductor Value vs. Output Voltage

V_{OUT} RANGE	INDUCTOR VALUE (µH)
$V_{OUT} \le 2.5V$	2.2
$2.5V < V_{OUT} \le 5.6V$	4.7
$5.6V < V_{OUT} \le 7.75V$	6.8
$7.75V < V_{OUT} \le 12V$	10
$V_{OUT} > 12V$	15

The chosen inductor value (L) should ensure that the peak inductor ripple current (I_{PEAK}) is below the high-side MOSFET peak current limit ($I_{LX-PLIM}$) so that the buck can maintain voltage regulation over load.

Use Equation 2 and Equation 3 to compute I_{PEAK}. If I_{PEAK} is greater than $I_{LX-PLIM}$ then increase the inductor value.

Equation 2:

$$I_{P-P} = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{V_{IN} \times F_{SW} \times L}$$

Equation 3:

$$I_{PEAK} = I_{LOAD} + \frac{I_{P-P}}{2}$$

where I_{LOAD} is the buck's output current in the particular application (1.5A max), V_{IN} is the application's largest expected input voltage (14V max), and F_{SW} is the switching frequency (see Table 1).

Setting V_{OUT} and Choosing C_{FF} (MAX77533AEWC)

The external feedback version of the device (MAX77533AEWC) uses resistors to set the output voltage between 0.8V and 99% of the input voltage. Connect a resistor divider between V_{OUT}, FB, and AGND as shown in Figure 3. One percent tolerance resistors (or better) are recommended to maintain high output accuracy. Choose R_{TOP} (V_{OUT} to FB) to be 10kΩ. Calculate the value of R_{BOT} (FB to AGND) for a desired output voltage with Equation 4.

Equation 4:

$$R_{BOT} = \frac{R_{TOP}}{\left[\frac{V_{OUT}}{V_{FB}} - 1\right]}$$

where V_{FB} is 0.8V and V_{OUT} is the desired output voltage.

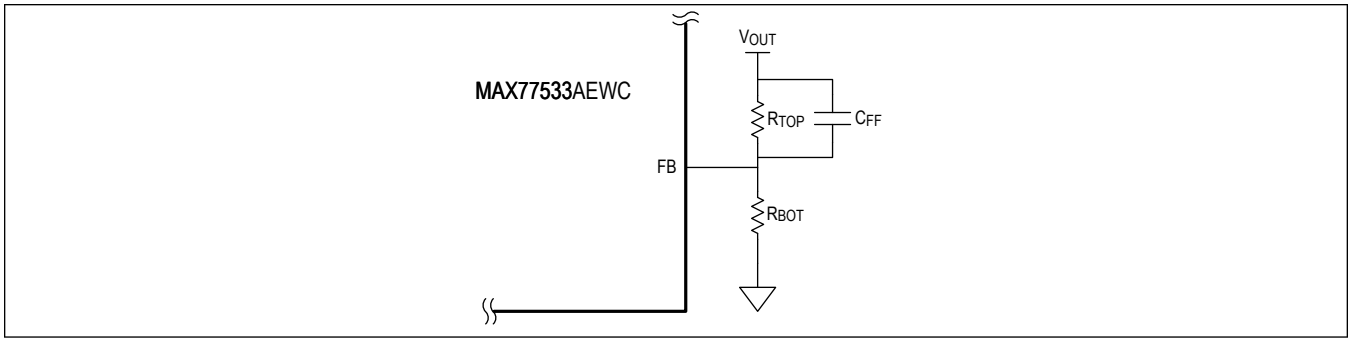


Figure 3. External Feedback Network

Choose the feed-forward capacitor (C_{FF}) value to be 100pF. C_{FF} is required to compensate the feedback network and maintain stability. Table 6 lists common feedback network combinations for various output voltages.

Table 6. Common Feedback Network Values

OUTPUT VOLTAGE TARGET (V)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	C_{FF} (pF)
0.8	0	OPEN	OPEN
0.82	10	402	100
0.85	10	160	100
0.9	10	81.6	100
1.0	10	40.7	100
1.05	10	32	100
1.1	10	26.7	100
1.2	10	20	100
1.25	10	17.8	100
1.35	10	14.5	100
1.5	10	11.4	100
1.55	10	10.7	100
1.8	10	8.06	100
1.85	10	7.68	100
2.05	10	6.34	100
2.5	10	4.75	100
2.8	10	4.17	100
3.0	10	3.65	100
3.3	10	3.24	100
3.5	10	2.94	100
5	10	1.91	100
5.6	10	1.65	100

No external feedback network is required for the internal feedback versions (MAX77533BEWCxx) of the device. For these versions, change the bits in V_OUTREG[6:0] to program the output voltage between 0.8V and 5V in 50mV steps per LSB.

Considerations for Output Voltages Below 1.55V

Carefully consider the input voltage range when choosing output voltages below 1.55V. The minimum on-time for this device is 100ns, so limiting the input voltage is required for stable operation at 1MHz switching frequency. See the following example when considering an output voltage of 0.9V and a maximum input voltage of 8V.

Minimum Duty = (100ns) x (1MHz) = 0.10

Minimum Achievable V_{OUT} = (Maximum Desired V_{IN}) x (Minimum Duty) = (8V) x (0.10) = 0.80V

Therefore, 0.9V can be considered for this input voltage range with a minimum achievable output voltage of 0.80V.

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. Figure 4 shows an example PCB top-metal layout for the internal feedback version of the device.

Follow these guidelines when designing the PCB:

1. Place the SUP capacitor immediately next to the SUP pin of the device. Since the device operates at 1MHz switching frequency, this placement is critical for effective decoupling of high-frequency noise from the SUP pin.
2. Place the inductor and output capacitor close to the device and keep the loop area of switching current small.
3. Make the trace between LX and the inductor short and wide. Do not take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.
4. The trace between BST and C_{BST} should be as short as possible.
5. Connect PGND and AGND together at the return terminal of the output capacitor. Do not connect them anywhere else.
6. Keep the power traces and load connections short and wide. This practice is essential for high-efficiency.
7. Place the V_L capacitor ground next to the AGND pin and connect with a short and wide trace.

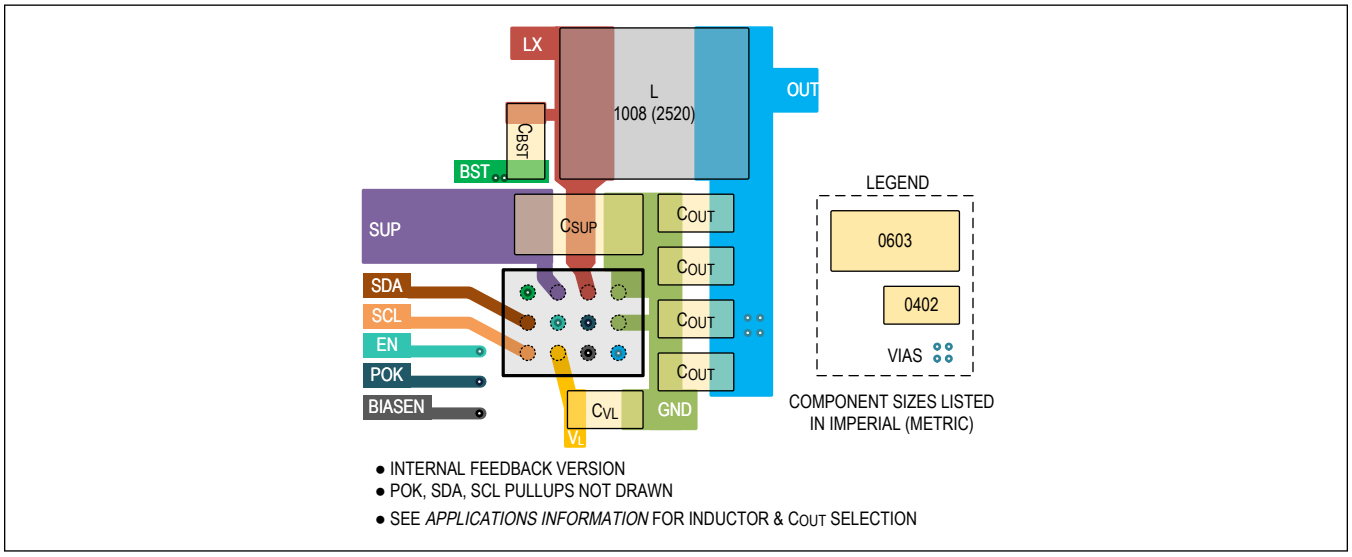
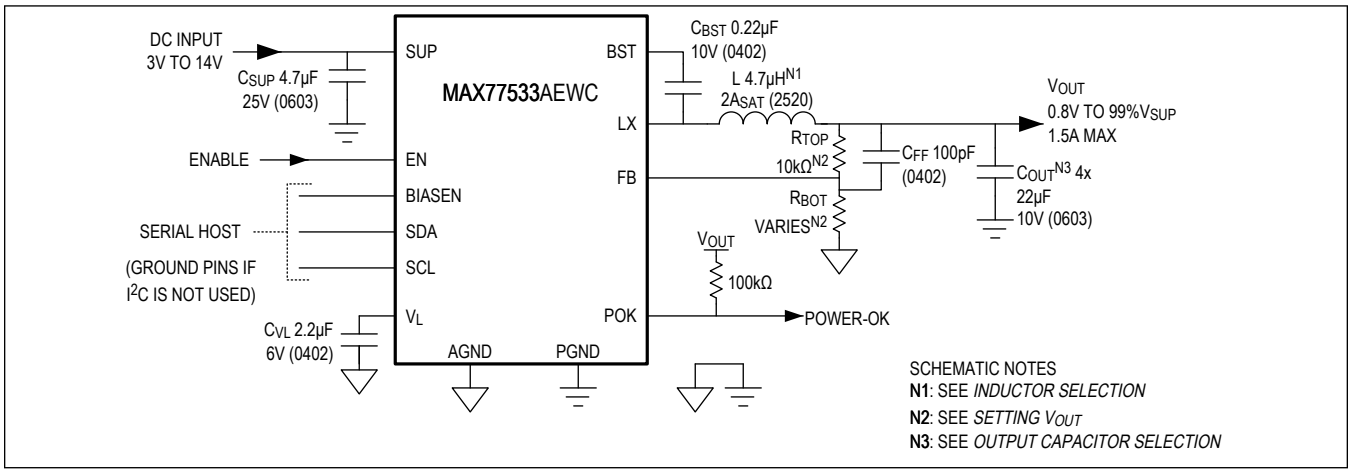


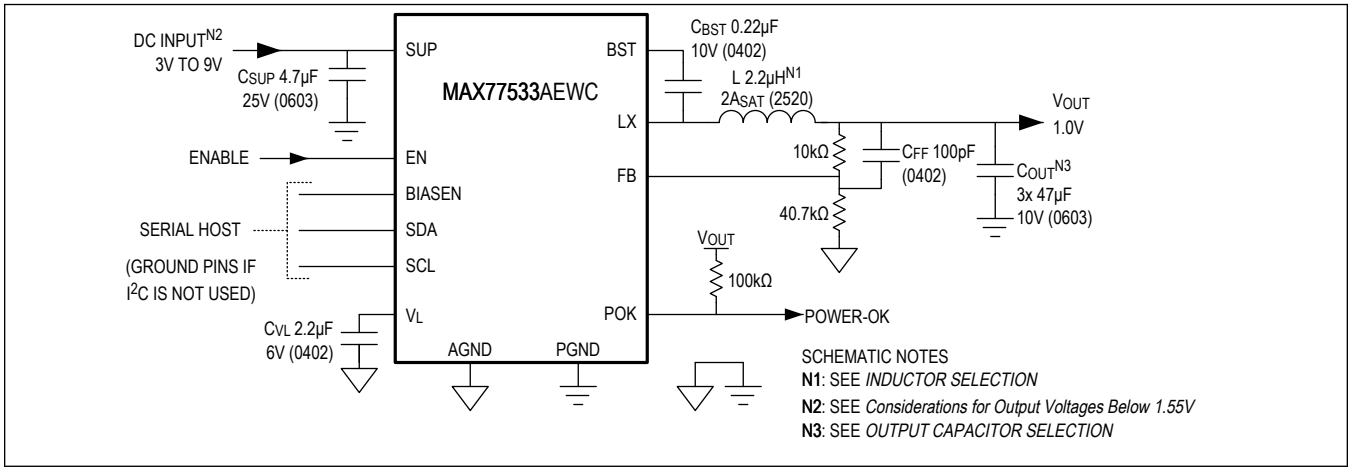
Figure 4. PCB Top-Metal and Component Layout Example

Typical Application Circuit(s)

External Feedback

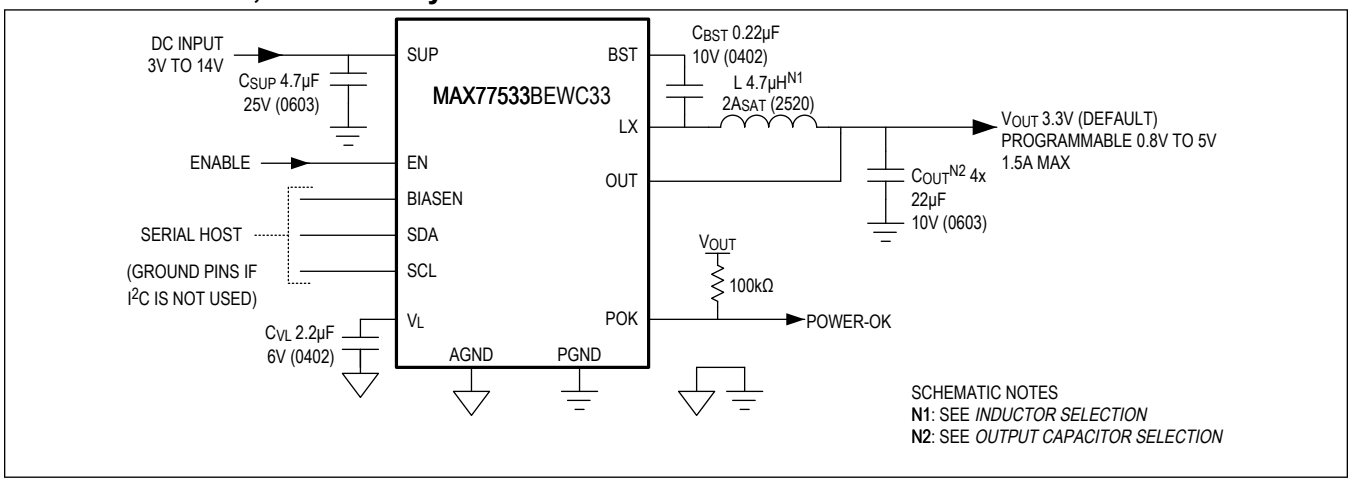


External Feedback, 1.0V Output

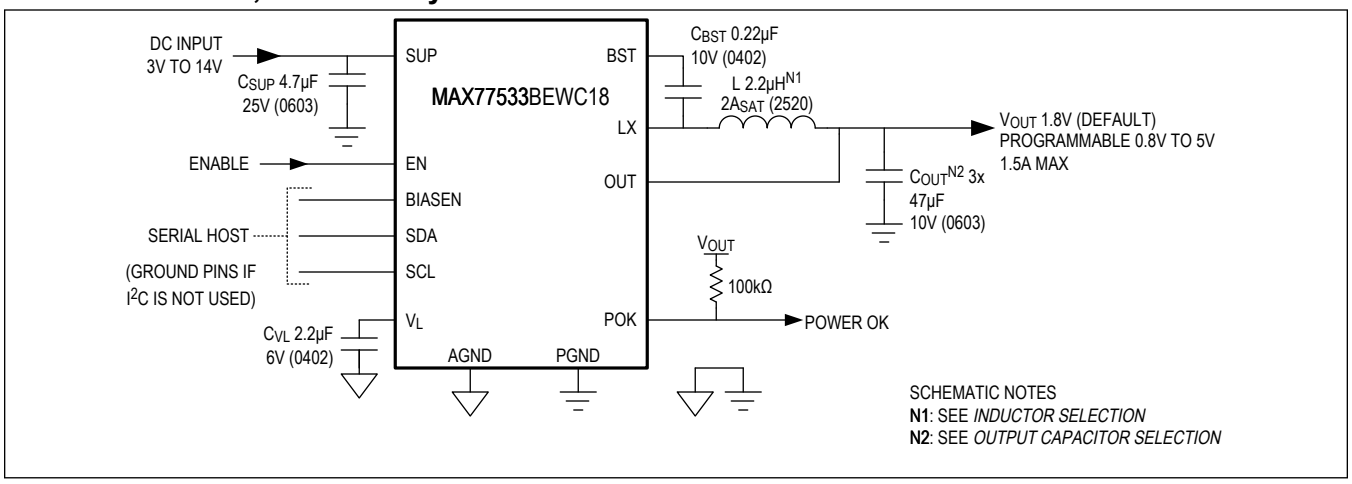


Typical Application Circuit(s) (continued)

Internal Feedback, 3.3V Factory Default

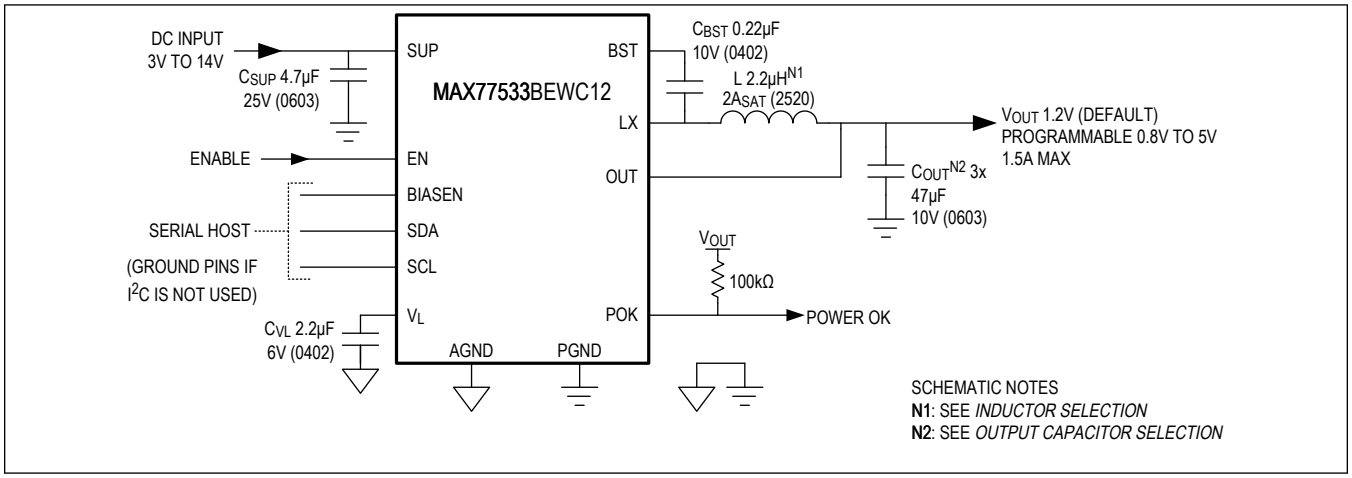


Internal Feedback, 1.8V Factory Default



Typical Application Circuit(s) (continued)

Internal Feedback, 1.2V Factory Default



Ordering Information

PART NUMBER	VOLTAGE FEEDBACK	DEFAULT OUTPUT VOLTAGE ($V_{OUT-REG}$)	DEFAULT SOFT-START TIME (t_{SS})	DEFAULT ACTIVE DISCHARGE (ADEN)	I^2C ADDRESS (7-BIT)
MAX77533AEWC+	External	N/A (external resistors)	1ms	N/A (permanently disabled)	0x1E
MAX77533BEWC33+	Internal	3.3V	1ms	enabled	0x1E
MAX77533BEWC18+*	Internal	1.8V	1ms	enabled	0x24
MAX77533BEWC12+	Internal	1.2V	1ms	enabled	0x37

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/20	Initial release	—
1	4/21	Updated *General Description, Benefits and Features, Simplified Applications Circuit*; added Note 2 to *Absolute Maximum Ratings* section; renumbered notes in *Electrical Characteristics* tables; updated TOCs 1-5, 11, 12, 17, 25-40, and added TOC 6; updated *Bump Descriptions* table; updated *Detailed Description, Buck Regulator Control Scheme*, and *FPWM Mode* sections; updated Table 1, *Setting V_{OUT} and Choosing CFF (MAX77533AEWC)* section, Table 6, *Typical Application Circuit(s)*, and *Ordering Information* table; added *Considerations for Output Voltages Below 1.55V* section	1, 6, 9-19, 26-30, 32
2	5/21	Added OUT Voltage Accuracy section to the *Electrical Characteristics* table	8

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