19-2616; Rev 0; 10/02

MAXIM

4-Port LVDS and LVTTL-to-LVDS Repeaters

General Description

The MAX9169/MAX9170 low-jitter, low-voltage differential signaling LVDS/LVTTL-to-LVDS repeaters are ideal for applications that require high-speed data or clock distribution while minimizing power, space, and noise. The devices accept a single LVDS (MAX9169) or LVTTL (MAX9170) input and repeat the input at four LVDS outputs. Each differential output drives 100Ω, allowing point-to-point distribution of signals on transmission lines with 100Ω termination at the receiver input. The MAX9169 and MAX9170 are pin compatible with the SN65LVDS104 and SN65LVDS105, respectively, and offer improved pulse-skew performance.

Ultra-low 150ps (max) pulse skew and 200ps$_{P-P}$ (max) added deterministic jitter ensure reliable communication in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery or serializers and deserializers. The high-speed switching performance guarantees 630Mbps data rate and less than 120ps channel-to-channel skew over the 3.0V to 3.6V operating supply range.

Supply current is 30mA (max) for the MAX9169, and 25mA (max) for the MAX9170. LVDS inputs and outputs conform to the ANSI EIA/TIA-644 standard. A fail-safe feature on the MAX9169 sets the output high when the input is undriven and open, terminated, or shorted. The MAX9169/MAX9170 are offered in 16-pin TSSOP and SO packages, and operate over an extended -40°C to +85°C temperature range.

Refer to the MAX9130 data sheet for an LVDS line receiver in an SC70 package.

Applications

Point-to-Point Baseband Data Transmission

Cellular Phone Base Stations

Add/Drop Muxes

Digital Cross-Connects

Network Switches/Routers

Backplane Interconnect

Clock Distribution

Pin Configurations appear at end of data sheet.

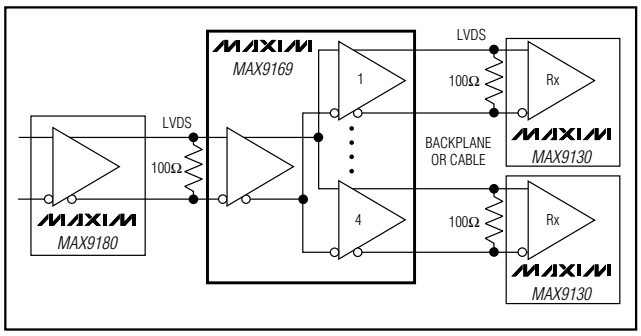
Features

- **150ps (max) Pulse Skew**
- **200ps$_{P-P}$ (max) Added Deterministic Jitter at 630Mbps (2^{23} - 1) PRBS Pattern**
- **8ps$_{RMS}$ (max) Added Random Jitter**
- **120ps (max) Channel-to-Channel Skew**
- **630Mbps Data Rate**
- **Conforms to ANSI EIA/TIA-644 LVDS Standard**
- **30mA (max) (MAX9169), 25mA (max) (MAX9170) Supply Current, a 15% Improvement vs. Competition**
- **LVDS (MAX9169) or +5V Tolerant LVTTL/LVCMOS (MAX9170) Input Versions**
- **Fail-Safe Circuit Sets Output High for Undriven Differential Input**
- **Output Rated for 10pF Load**
- **Individual Output Enables**
- **Single 3.3V Supply**
- **Improved Second Source of the SN65LVDS104 (MAX9169)/SN65LVDS105 (MAX9170)**
- **16-Pin SO and TSSOP Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INPUT
MAX9169ESE	-40°C to +85°C	16 SO	LVDS
MAX9169EUE	-40°C to +85°C	16 TSSOP	LVDS
MAX9170ESE	-40°C to +85°C	16 SO	LVTTL
MAX9170EUE	-40°C to +85°C	16 TSSOP	LVTTL

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

4-Port LVDS and LVTTL-to-LVDS Repeaters

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to +4V
Inputs
IN+, IN- to GND .....-0.5V to +4V
IN, EN_ to GND .....-0.5V to +6V
Outputs
OUT_+, OUT_- to GND .....-0.5V to +4V
Continuous Power Dissipation (T_A = +70°C)
16-Pin SO (derate 8.7mW/°C above +70°C) 696mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
ESD Protection
Human Body Model (MAX9169)
(IN+, IN-, OUT_+, OUT_-) .....≥16kV
Human Body Model (MAX9170)
(OUT_+, OUT_-) .....≥10kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, R_L = 100Ω ±1%, EN_ = high, MAX9169 differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, LVDS input common-mode voltage $V_{CM} = |V_{ID}/2|$ to +2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = +25°C for MAX9169. Typical values are at V_{CC} = 3.3V, V_{IN} = 0 or V_{CC}, T_A = +25°C for MAX9170.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS INPUTS (IN+, IN-) (MAX9169)						
Differential Input High Threshold	V_{TH}			5	50	mV
Differential Input Low Threshold	V_{TL}		-50	-5		mV
Input Current (IN+ or IN-, Single Ended)	I_{IN+}, I_{IN-}	V_{IN} = 0V, other input open, Figure 1	-2	-11.8	-20	µA
		V_{IN} = +2.4V, other input open, Figure 1	-1.2	-3.2		
Power-Off Input Current (IN+ or IN-, Single Ended)	I_{INO+}, I_{INO-}	V_{CC} = +1.5V, V_{IN} = +2.4V, other input open, Figure 1		3.2	20	µA
Input Current	I_{IN+}, I_{IN-}	0.05V ≤ $\|V_{ID}\|$ ≤ 0.6V, Figure 1	-15		+15	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.2V, Figure 1	-20		+20	
Power-Off Input Current	I_{INO+}, I_{INO-}	0.05V ≤ $\|V_{ID}\|$ ≤ 0.6V, V_{CC} = 1.5V, Figure 1	-15		+15	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.2V, V_{CC} = 1.5V, Figure 1	-20		+20	
Fail-Safe Input Resistor	R_{IN1}	V_{CC} = 3.6V, 0 or open, Figure 1	103	138	190	kΩ
	R_{IN2}	V_{CC} = 3.6V, 0 or open, Figure 1	154	210	260	
Input Capacitance	C_{IN}	IN+ or IN- to GND (Note 3)		2.2		pF
+5V TOLERANT LVTTL/LVCMOS INPUTS (IN, EN_)						
Input High Voltage	V_{IH}		2.0		5.5	V
Input Low Voltage	V_{IL}		0		0.8	V
Input Current	I_{IH}	V_{IN} = 2V to 5.5V			20	µA
	I_{IL}	V_{IN} = 0 to 0.8V			10	
Input Capacitance (MAX9170)	C_{IN}	IN to GND (Note 3)		2.2		pF
LVDS OUTPUTS (OUT_+, OUT_-)						
Differential Output Voltage	V_{OD}	Figures 3, 4, 6, 7	250	350	450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Figures 3, 4, 6, 7		1.5	25	mV
Steady-State Output Offset Voltage	V_{OS}	Figures 2, 4, 5, 7, 8, 9	1.125	1.26	1.375	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, R_L = 100Ω ±1%, EN_ = high, MAX9169 differential input voltage | V_{ID} | = 0.05V to 1.2V, LVDS input common-mode voltage V_{CM} = | V_{ID}/2 | to +2.4V - | V_{ID}/2 |, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, | V_{ID} | = 0.2V, V_{CM} = 1.25V, T_A = +25°C for MAX9169. Typical values are at V_{CC} = 3.3V, V_{IN} = 0 or V_{CC}, T_A = +25°C for MAX9170.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	Figures 2, 4, 5, 7, 8, 9			1.5	25	mV
Peak-to-Peak Output Offset Voltage	$V_{OS(P-P)}$	Figures 8, 9 (Note 4)			40	150	mV
Output Voltage	V_{OH}	Figures 3, 4, 6, 7				1.65	V
	V_{OL}	Figures 3, 4, 6, 7		0.9			
Fail-Safe Differential Output Voltage (MAX9169)	V_{OD+}	IN+, IN- open, undriven and shorted, or undriven and parallel terminated		+250	+350	+450	mV
High-Impedance Output Current	I_{OZ}	EN_ = low, V_{OUT_+} = +3.6V or 0, V_{OUT_-} = +3.6V or 0		-0.5	0.01	+0.5	µA
Power-Off Output Current	I_{OFF}	V_{CC} = +1.5V, V_{OUT_+} = +3.6V or 0, V_{OUT_-} = +3.6V or 0		-0.5	0.01	+0.5	µA
Output Short-Circuit Current	I_{OS}	V_{ID} = +50mV or -50mV, V_{OUT+} = 0 or V_{CC}, V_{OUT-} = 0 or V_{CC}		-10	±5.8	+10	mA
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{ID} = +50mV or -50mV, V_{OD} = 0 (Note 5)			5.8	10	mA
Output Capacitance	C_O	OUT_+ or OUT_- to GND (Note 6)			3.6		pF
POWER SUPPLY							
Supply Current	I_{CC}	DC, R_L = 100Ω, Figures 10, 13	MAX9169		22	30	mA
			MAX9170		18	25	
		315MHz (630Mbps), R_L = 100Ω, Figures 10, 13	MAX9169		43	60	
			MAX9170		41	55	
Disabled Supply Current	I_{CCZ}	EN_ = low	MAX9169		6.8	8.0	mA
			MAX9170		4.3	6.4	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, R_L = 100Ω ±1%, C_L = 10pF, EN_ = high, MAX9169 differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, LVDS input common-mode voltage V_{CM} = $|V_{ID}/2|$ to +2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, V_{CC} = 3.3V, T_A = +25°C for MAX9169. Typical values are at V_{IN} = 0 or V_{CC}, V_{CC} = 3.3V, T_A = +25°C for MAX9170.) (Notes 5, 7, and 8)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Rise Time	t_R	Figures 10–15		0.6	0.8	1.2	ns
Fall Time	t_F	Figures 10–15		0.6	0.8	1.2	ns
Added Deterministic Jitter	t_{DJ}	(Note 9)			110	200	ps
Added Random Jitter	t_{RJ}	(Note 10)			6	8	ps
Differential Propagation Delay High to Low	t_{PHL}	Figures 10, 11, 13, 14	MAX9169	2.2	3.5	4.2	ns
			MAX9170	1.5	2.6	3.2	
Differential Propagation Delay Low to High	t_{PLH}	Figures 10, 11, 13, 14	MAX9169	2.2	3.5	4.2	ns
			MAX9170	1.5	2.6	3.2	
Pulse Skew $\|t_{PLH} - t_{PHL}\|$	t_{SKEW}	Figures 10, 11, 13, 14			40	250	ps
Pulse Skew $\|t_{PLH} - t_{PHL}\|$	$t_{SK(P)}$	Figures 10, 12, 13, 15 (Note 11)			40	150	ps
Channel-to-Channel Skew (Note 12)	$t_{SK(0)}$	MAX9169, Figures 10, 11, 12			25	120	ps
		MAX9170, Figures 13, 14, 15			15	100	
Differential Part-to-Part Skew (Note 13)	$t_{SK(PP)}$	MAX9169, Figures 10, 11, 12			0.28	1.2	ns
		MAX9170, Figures 13, 14, 15			0.19	1.2	
Disable Time	t_{PHZ}	High to high-Z, Figures 16–19			11	15	ns
	t_{PLZ}	Low to high-Z, Figures 16–19			11.8	15	
Enable Time	t_{PZH}	High-Z to high, Figures 16–19			2.3	10	ns
	t_{PZL}	High-Z to low, Figures 16–19			5.8	10	

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH}, V_{TL}, V_{ID}, V_{OD}, and ΔV_{OD}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 3: Signal generator output for IN+, IN-, or single-ended IN: $V_{IN} = 0.4 \sin(4E6\pi t) + 0.5$.

Note 4: All input pulses are supplied by a generator having the following characteristics: t_R or $t_F \le 1$ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10ns.

Note 5: Guaranteed by design and characterization.

Note 6: Signal generator output for OUT+ or OUT-: $V_{IN} = 0.4 \sin(4E6\pi t) + 0.5$, EN_ = low.

Note 7: C_L includes scope probe and test jig capacitance.

Note 8: Signal generator output for differential inputs IN+, IN- (unless otherwise noted): frequency = 50MHz, 49% to 51% duty cycle, R_O = 50Ω, t_R = 1.0ns, and t_F = 1.0ns (0% to 100%). Signal generator output for single-ended input IN (unless otherwise noted): frequency = 50MHz, 49% to 51% duty cycle, R_O = 50Ω, $V_{IH} = V_{CC}$, V_{IL} = 0V, t_R = 1.0ns, and t_F = 1.0ns (0% to 100%).

Note 9: Signal generator output for MAX9169 t_{DJ}: V_{OH} = +1.3V, V_{OL} = +1.1V, data rate = 630Mbps, 2^{23} -1 PRBS, R_O = 50Ω, t_R = 1.0ns and t_F = 1.0ns (0% to 100%). Signal generator output for MAX9170 t_{DJ}: $V_{OH} = V_{CC}$, V_{OL} = 0V, data rate = 630Mbps, 2^{23} -1 PRBS, R_O = 50Ω, t_R = 1.0ns, and t_F = 1.0ns (0% to 100%).

Note 10: Signal generator output for MAX9169 t_{RJ}: V_{OH} = +1.3V, V_{OL} = +1.1V, frequency = 315MHz, 50% duty cycle, R_O = 50Ω, t_R = 1.0ns, and t_F = 1.0ns (0% to 100%). Signal generator output for MAX9170 t_{RJ}: $V_{OH} = V_{CC}$, V_{OL} = 0V, frequency = 315MHz, 50% duty cycle, R_O = 50Ω, t_R = 1.0ns, and t_F = 1.0ns (0% to 100%).

Note 11: Signal generator output for MAX9169 $t_{SK(P)}$: V_{OH} = +1.4V, V_{OL} = +1.0V, R_O = 50Ω, t_R = 1.0ns, and t_F = 1.0ns (0% to 100%). Signal generator output for MAX9170 $t_{SK(P)}$: V_{OH} = +3.0, V_{OL} = 0V, R_O = 50Ω, t_R = 1.0ns, and t_F = 1.0ns (0% to 100%).

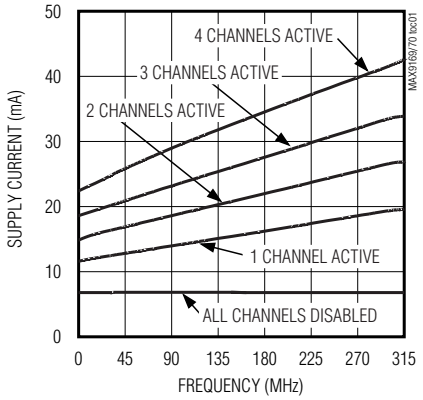
Note 12: $t_{SK(0)}$ is the magnitude of the time difference between t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.

Note 13: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

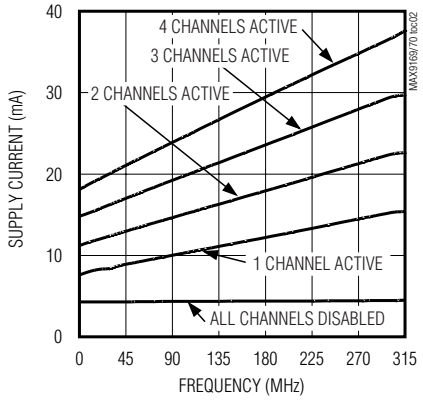
Typical Operating Characteristics

(V_{CC} = 3.3V, R_L = 100Ω, C_L = 10pF, | V_{ID} | = 150mV, V_{CM} = 1.25V, f_{IN} = 50MHz, T_A = +25°C, unless otherwise noted.)

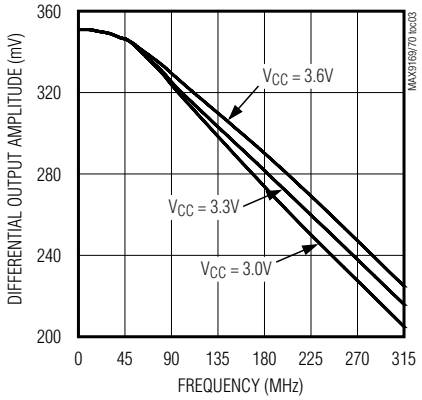
MAX9169 SUPPLY CURRENT vs. FREQUENCY



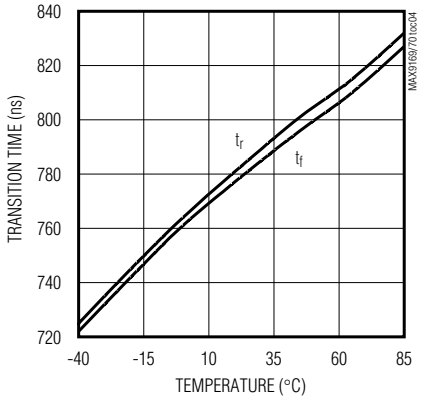
MAX9170 SUPPLY CURRENT vs. FREQUENCY



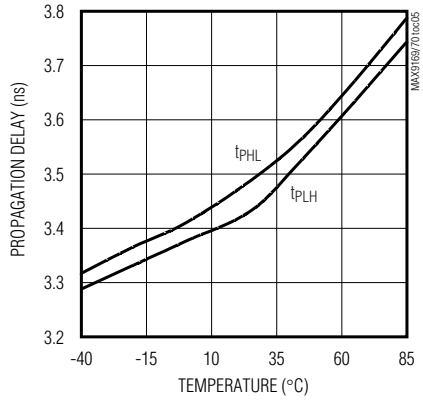
DIFFERENTIAL OUTPUT AMPLITUDE vs. FREQUENCY



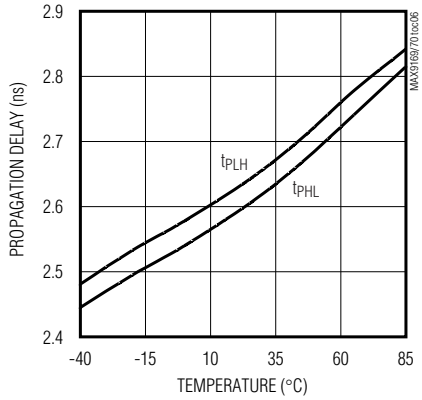
TRANSITION TIME vs. TEMPERATURE



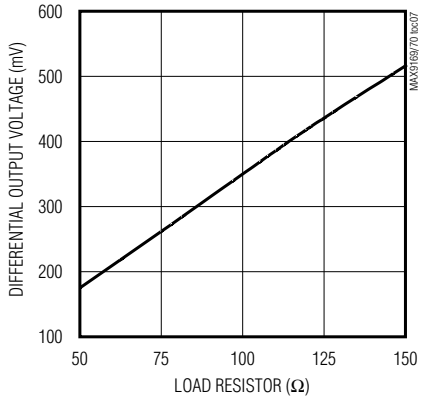
MAX9169 PROPAGATION DELAY vs. TEMPERATURE



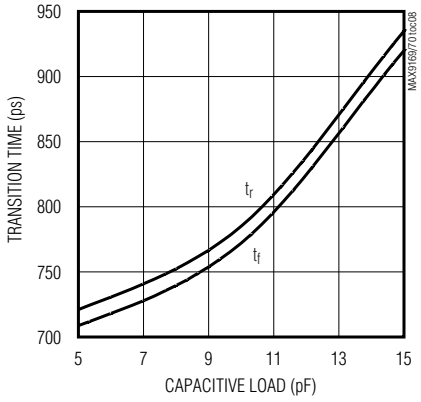
MAX9170 PROPAGATION DELAY vs. TEMPERATURE



DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD RESISTOR



TRANSITION TIME vs. CAPACITIVE LOAD



Pin Description

PIN		NAME	FUNCTION
MAX9169	MAX9170		
1	1	EN1	OUT1+/OUT1- Enable. +5V tolerant LVTTL/LVCMOS input. Set EN1 high to enable OUT1+/OUT1-. Set EN1 low to disable OUT1+/OUT1- (high-impedance mode). Integrated pulldown to GND.
2	2	EN2	OUT2+/OUT2- Enable. +5V tolerant LVTTL/LVCMOS input. Set EN2 high to enable OUT2+/OUT2-. Set EN2 low to disable OUT2+/OUT2- (high-impedance mode). Integrated pulldown to GND.
3	3	EN3	OUT3+/OUT3- Enable. +5V tolerant LVTTL/LVCMOS input. Set EN3 high to enable OUT3+/OUT3-. Set EN3 low to disable OUT3+/OUT3- (high-impedance mode). Integrated pulldown to GND.
4	4	V_{CC}	Power-Supply Voltage. Bypass with 0.1µF and 0.001µF capacitors to ground.
5	5	GND	Ground
6	—	IN+	Noninverting Differential LVDS Input
7	—	IN-	Inverting Differential LVDS Input
8	8	EN4	OUT4+/OUT4- Enable. +5V tolerant LVTTL/LVCMOS input. Set EN4 high to enable OUT4+/OUT4-. Set EN4 low to disable OUT4+/OUT4- (high-impedance mode). Integrated pulldown to GND.
9	9	OUT4-	Inverting Differential LVDS Output
10	10	OUT4+	Noninverting Differential LVDS Output
11	11	OUT3-	Inverting Differential LVDS Output
12	12	OUT3+	Noninverting Differential LVDS Output
13	13	OUT2-	Inverting Differential LVDS Output
14	14	OUT2+	Noninverting Differential LVDS Output
15	15	OUT1-	Inverting Differential LVDS Output
16	16	OUT1+	Noninverting Differential LVDS Output
—	6	IN	Data Input, 5V Tolerant LVTTL/LVCMOS. Integrated pulldown to GND.
—	7	N.C.	No Connection

Table 1. MAX9169 Input/Output Functions

INPUT		OUTPUT
$V_{ID} = V_{IN+} - V_{IN-}$	EN_	V_{OD}
X	Low or open	High-Z
+50mV	High	High
-50mV	High	Low
Open	High	High
Undriven short	High	High
Undriven parallel terminated	High	High

Table 2. MAX9170 Input/Output Functions

INPUT		OUTPUT
V_{IN}	EN_	V_{OD}
X	Low or open	High-Z
High	High	High
Low	High	Low
Open	High	Low

Detailed Description

LVDS is a signaling method for point-to-point and multidrop data communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 and IEEE 1596.3 standards. LVDS uses a lower voltage swing than other common standards, achieving higher data rates with reduced power consumption, while reducing EMI emissions and system susceptibility to noise.

The MAX9169/MAX9170 are 630Mbps, four-port repeaters for high-speed, low-power applications. The MAX9169 accepts an LVDS input and has a fail-safe input circuit. The MAX9170 features a +5V tolerant single-ended LVTTL/LVCMOS input. Both devices repeat the input at four LVDS outputs. The MAX9169 detects differential signals as low as 50mV and as high as 1.2V over a $|V_{ID}|/2$ to 2.4V - $|V_{ID}|/2$ common-mode range. The MAX9170's +5V tolerant LVTTL/LVCMOS input includes circuitry to hold the decision threshold constant at +1.5V over temperature and supply voltage.

The MAX9169/MAX9170 outputs use a current-steering configuration to generate a 2.5mA to 4.5mA output current. This current-steering approach induces less ground bounce and shoot-through current, enhancing noise margin and system speed performance. The outputs are short-circuit current limited and are high impedance when disabled or when the device is not powered.

The MAX9169/MAX9170 current-steering output requires a resistive load to terminate the signal and complete the transmission loop. Because the devices switch the direction of current flow and not voltage levels, the output voltage swing is determined by the value of the termination resistor multiplied by the output current. With a typical 3.5mA output current, the MAX9169/MAX9170 produce a 350mV output voltage when driving a transmission line terminated with a 100Ω resistor (3.5mA × 100Ω = 350mV). Logic states are determined by the direction of current flow through the termination resistor.

Fail-Safe Circuitry

The fail-safe feature of the MAX9169 sets the outputs high when the differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without a fail-safe circuit, when the input is undriven, noise at the input may switch the outputs and it may appear to the system that data is being sent. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when an LVDS driver output is in high impedance. A shorted input can occur because of cable failure.

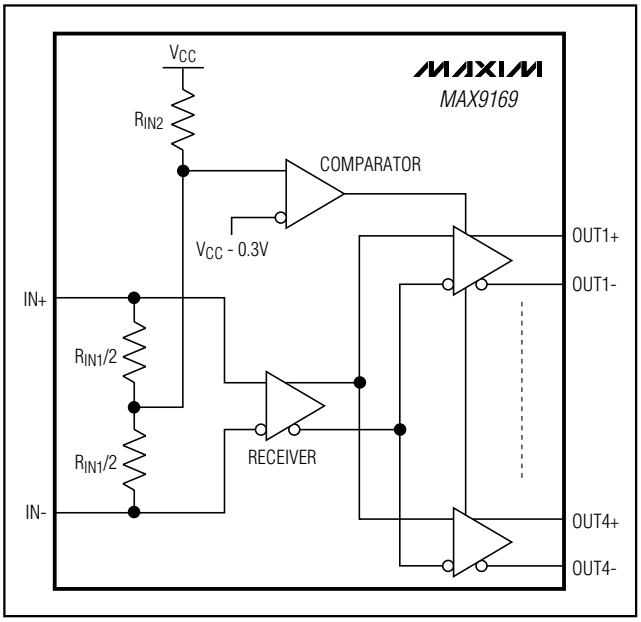


Figure 1. MAX9169 Input Fail-Safe Circuit

When the input is driven with signals meeting the LVDS standard, the input common-mode voltage is less than V_{CC} - 0.3V and the fail-safe circuit is not activated (Figure 1). If the input is open, undriven and shorted, or undriven and parallel terminated, an internal resistor in the fail-safe circuit pulls both the inputs above V_{CC} - 0.3V, activating the fail-safe circuit and forcing the outputs high.

Applications Information

Supply Bypassing

Bypass V_{CC} with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller value capacitor closest to the V_{CC} pin. Use multiple parallel vias to minimize parasitic inductance.

Traces, Cables, and Connectors

The characteristics of differential input and output connections affect the performance of the MAX9169/MAX9170. Use controlled-impedance traces, cables, and connectors with matched characteristic impedance.

Ensure that noise couples as common mode by running the traces of a differential pair close together. Reduce within-pair skew by matching the electrical length of the traces of a differential pair. Excessive skew can result in a degradation of magnetic field cancellation. Maintain a constant distance between traces of a differential pair to avoid discontinuities in differen-

tial impedance. Minimize the number of vias to further prevent impedance discontinuities.

Avoid the use of unbalanced cables, such as ribbon cable. Balanced cables, such as twisted pair, offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

The MAX9169/MAX9170 LVDS outputs are specified for a 100Ω load but can drive 90Ω to 132Ω to accommodate various types of interconnect. The termination resistor at the driven receiver should match the differential characteristic impedance of the interconnect and be located close to the receiver input. Use a ±1% surface-mount termination resistor.

Board Layout

A four-layer PC board with separate layers for power, ground, and LVDS signals is recommended. Keep LVTTL/LVCMOS signals separated from the LVDS signals to prevent crosstalk to the LVDS lines.

Test Circuits and Timing Diagrams

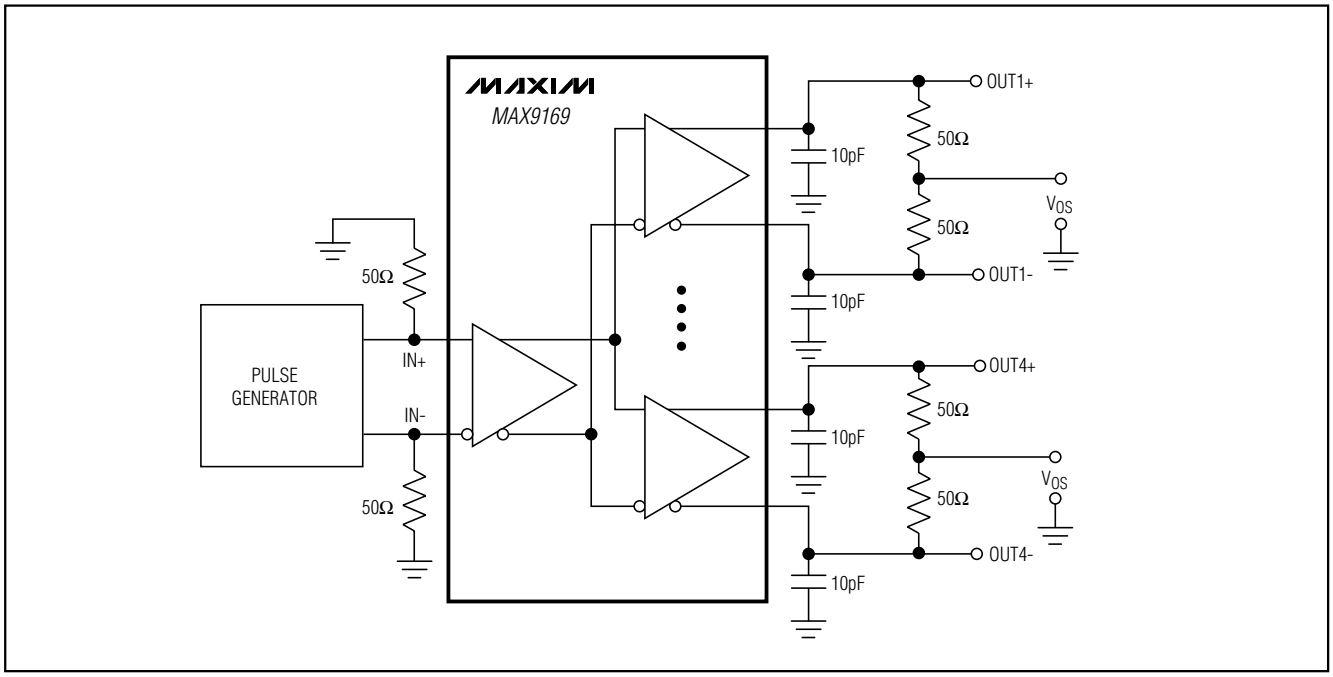


Figure 2. MAX9169 Output Offset Voltage Test Circuit

Test Circuits and Timing Diagrams (continued)

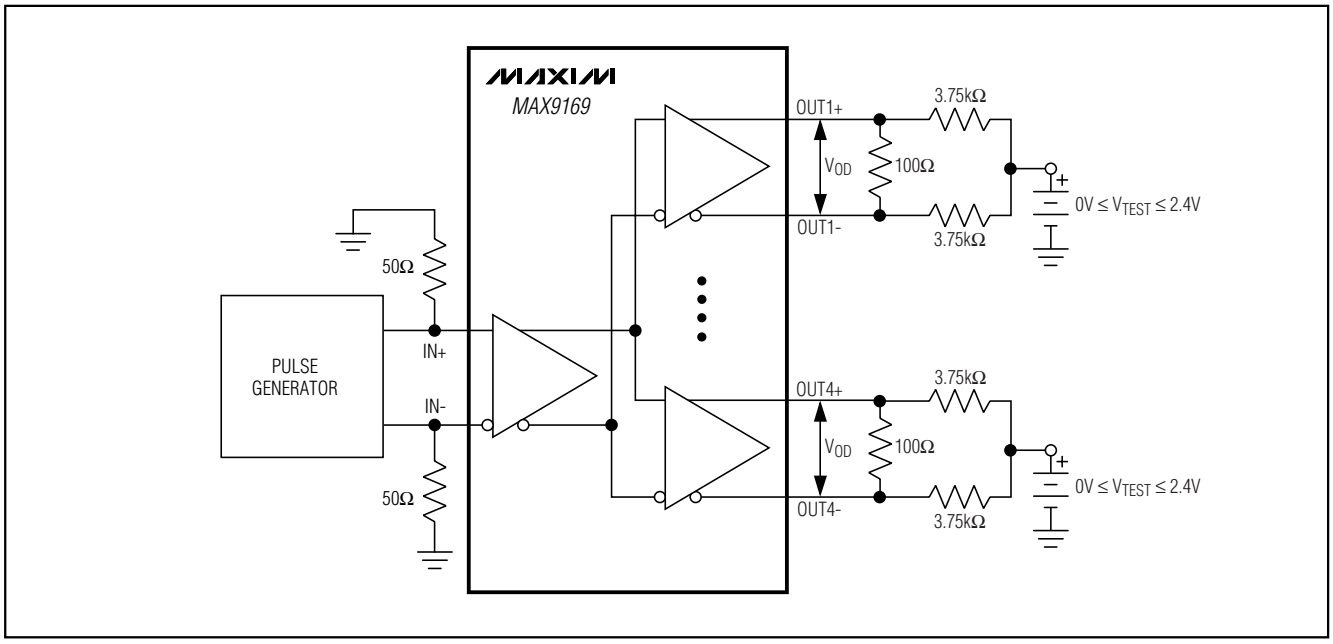


Figure 3. MAX9169 Differential Output Voltage Test Circuit

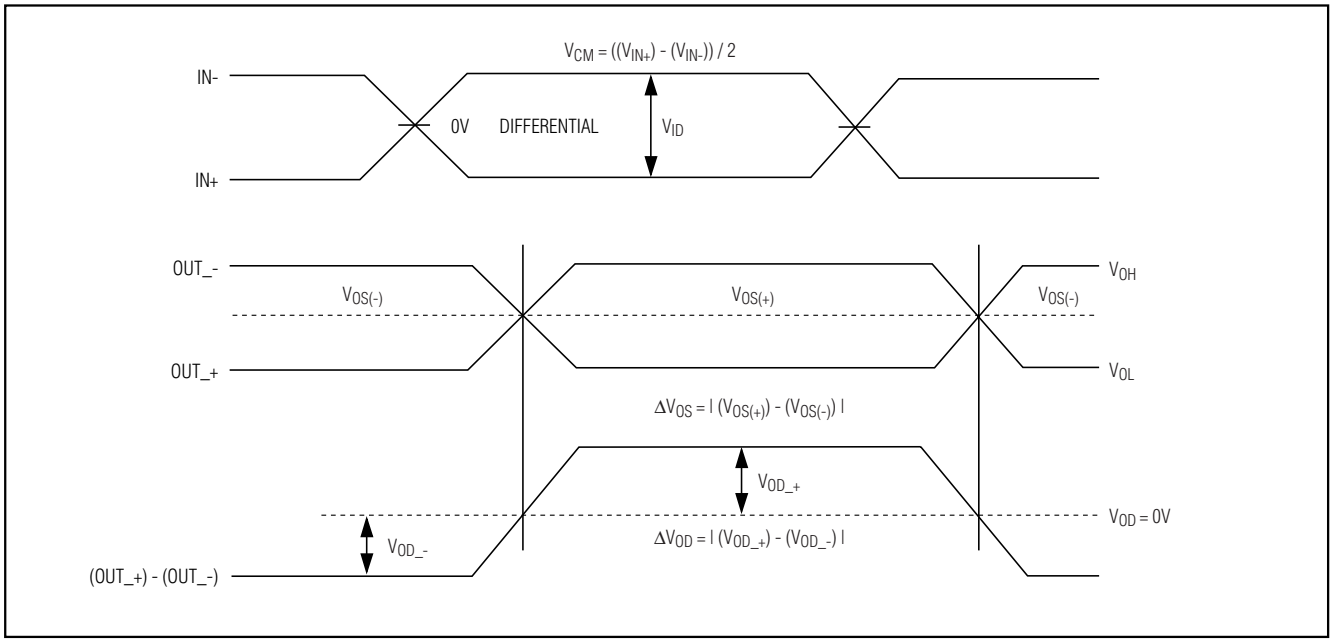


Figure 4. MAX9169 Output DC Parameters

4-Port LVDS and LVTTL-to-LVDS Repeaters

Test Circuits and Timing Diagrams (continued)

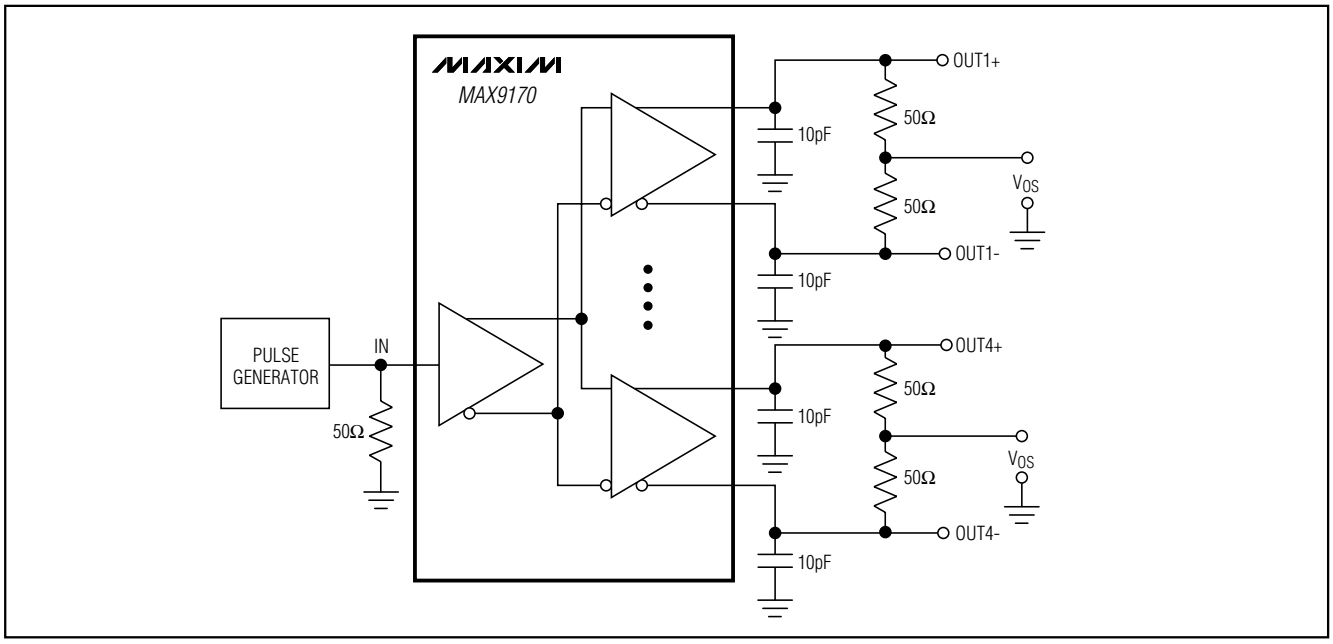


Figure 5. MAX9170 Output Offset Voltage Test Circuit

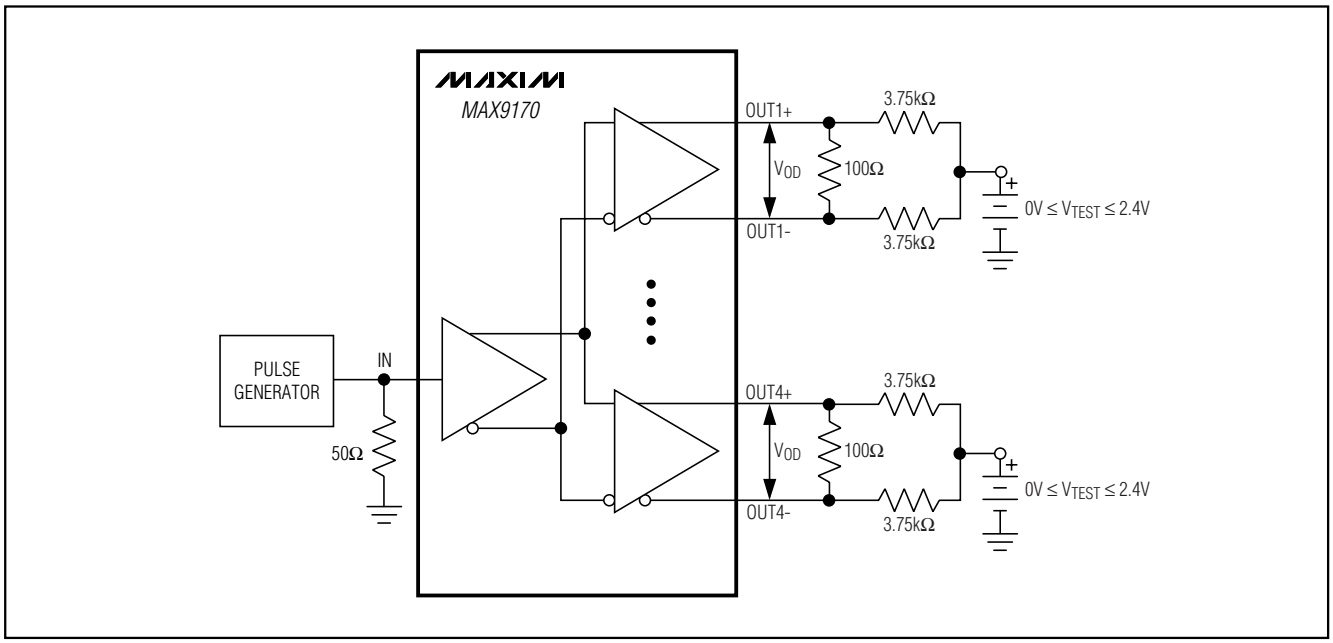


Figure 6. MAX9170 Differential Output Voltage Test Circuit

Test Circuits and Timing Diagrams (continued)

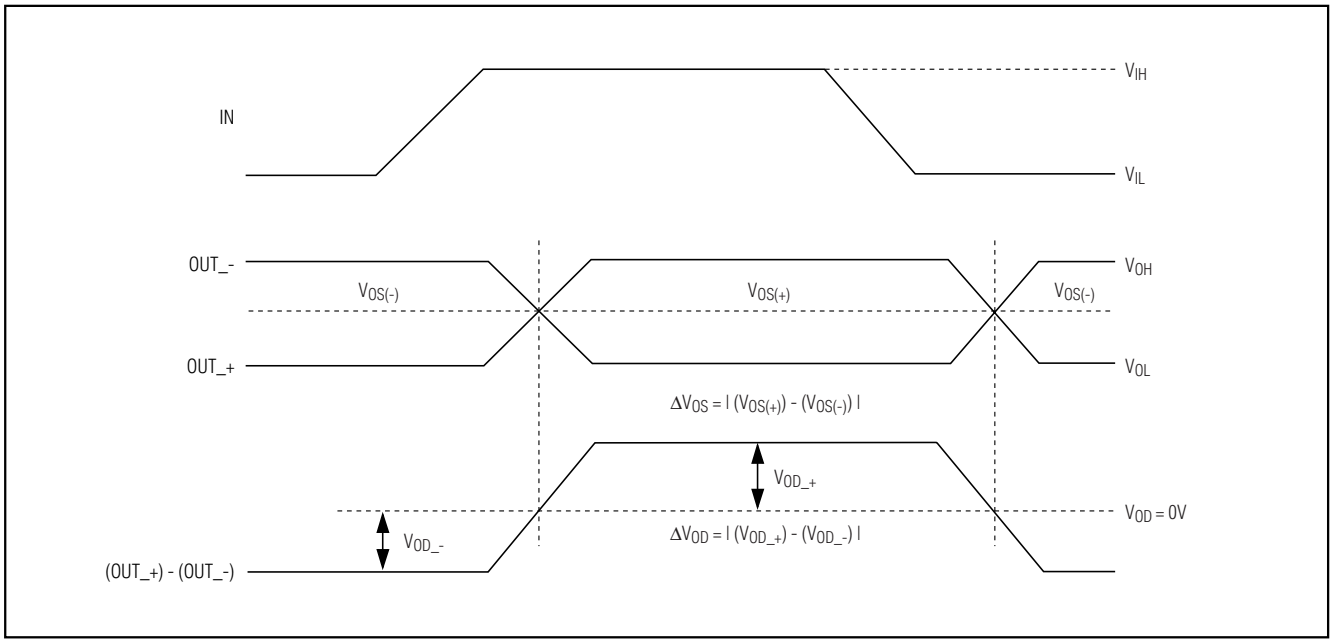


Figure 7. MAX9170 LVDS Output DC Parameters

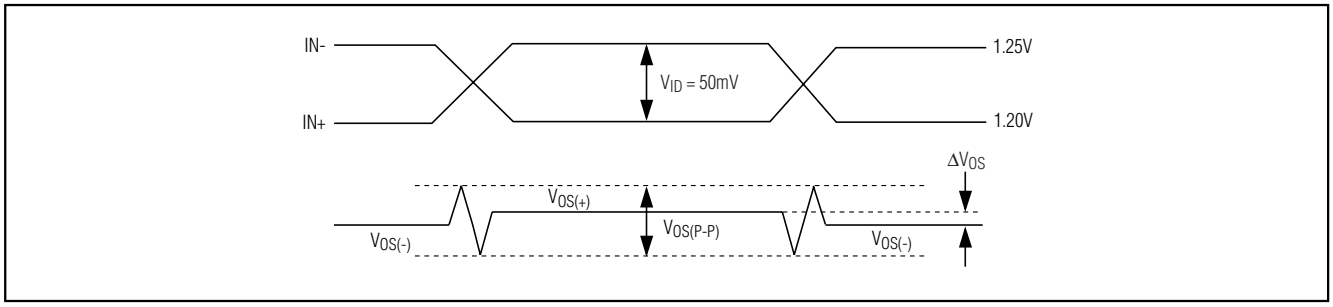


Figure 8. MAX9169 Output Offset Voltage Waveforms

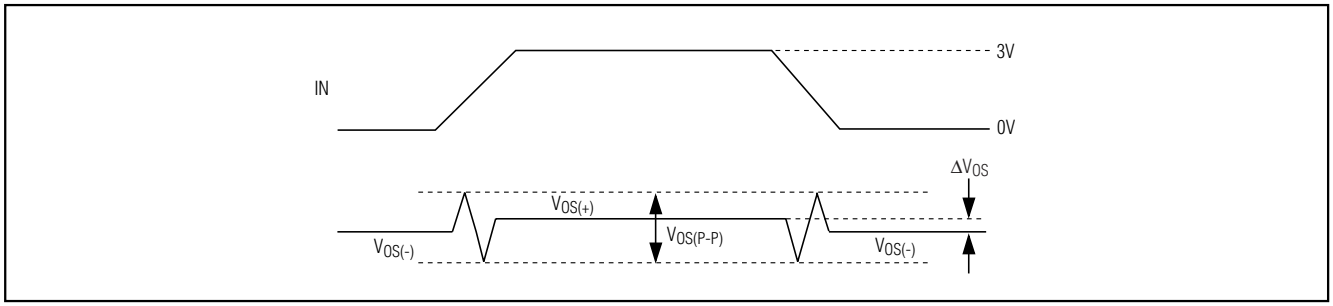


Figure 9. MAX9170 Output Offset Voltage Waveforms

Test Circuits and Timing Diagrams (continued)

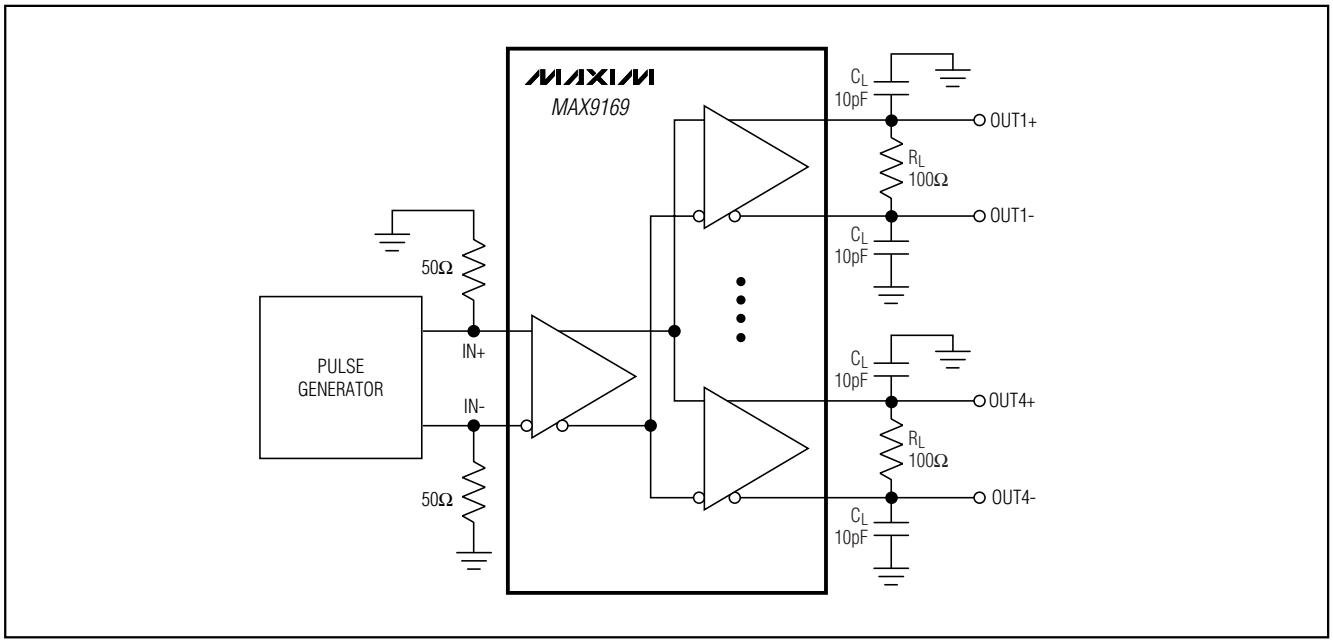


Figure 10. MAX9169 Propagation Delay and Transition Time Test Circuit

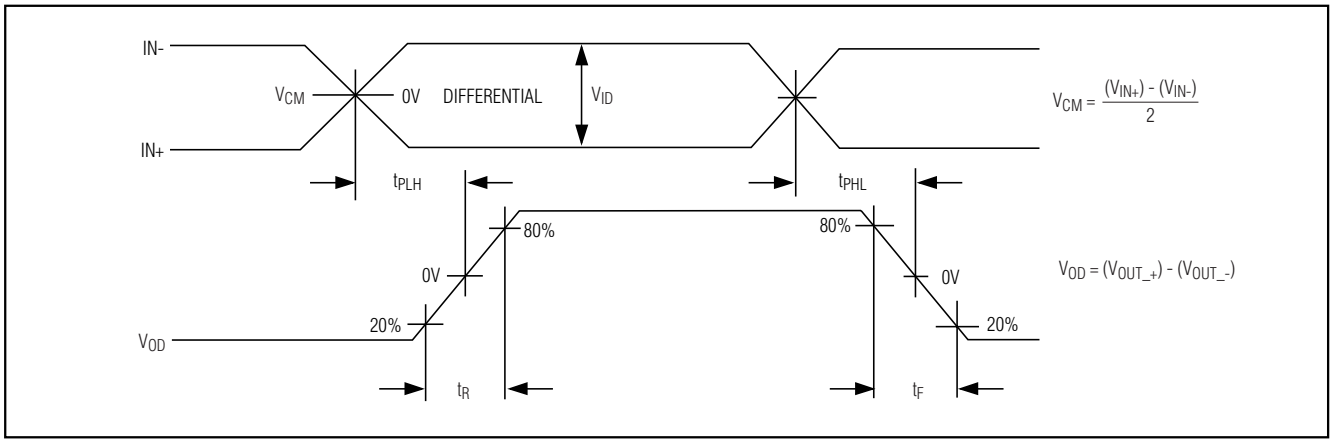


Figure 11. MAX9169 Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Diagrams (continued)

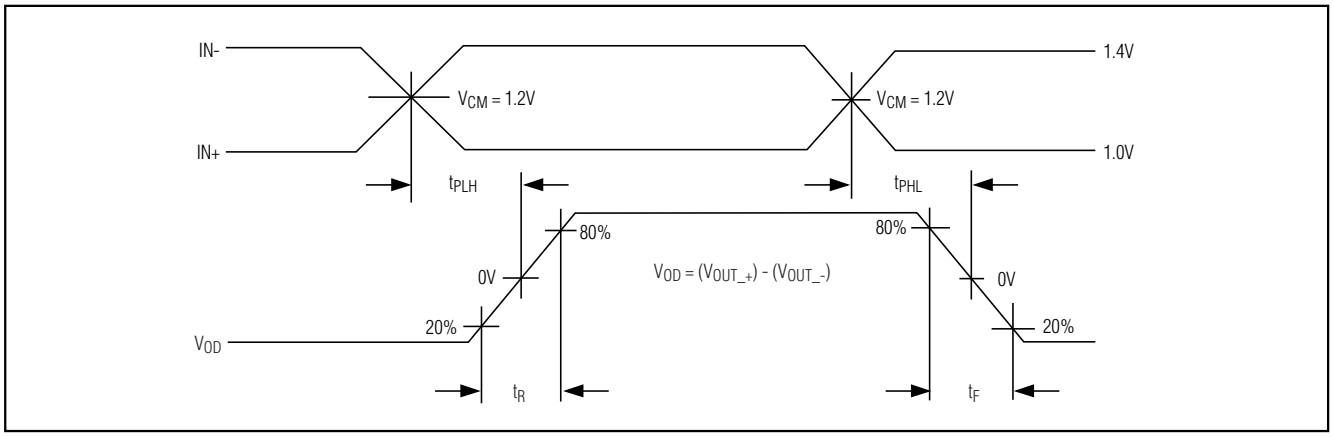


Figure 12. MAX9169 Propagation Delay and Transition Time Waveforms, $t_{SK(p)}$

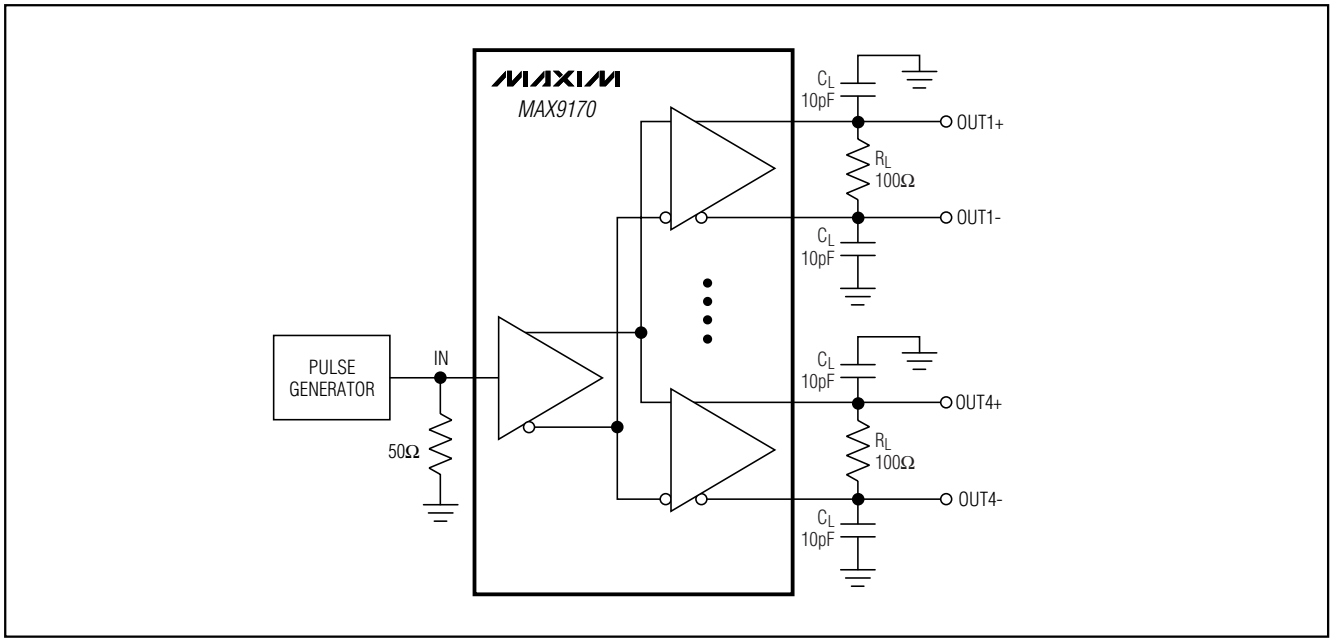


Figure 13. MAX9170 Propagation Delay and Transition Time Test Circuit

Test Circuits and Timing Diagrams (continued)

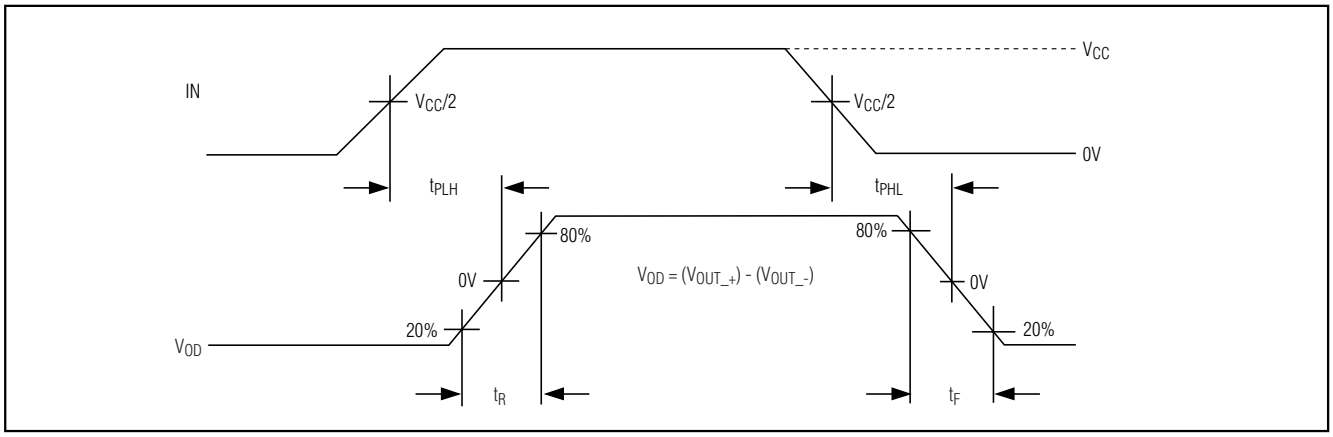


Figure 14. MAX9170 Propagation Delay and Transition Time Waveforms

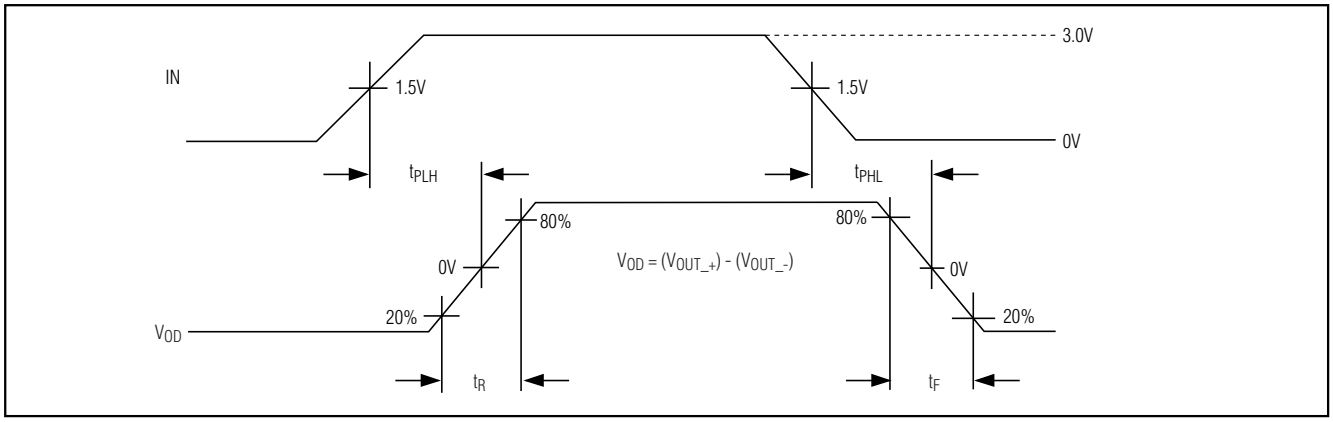


Figure 15. MAX9170 Propagation Delay and Transition Time Waveforms, $t_{SK(p)}$

Test Circuits and Timing Diagrams (continued)

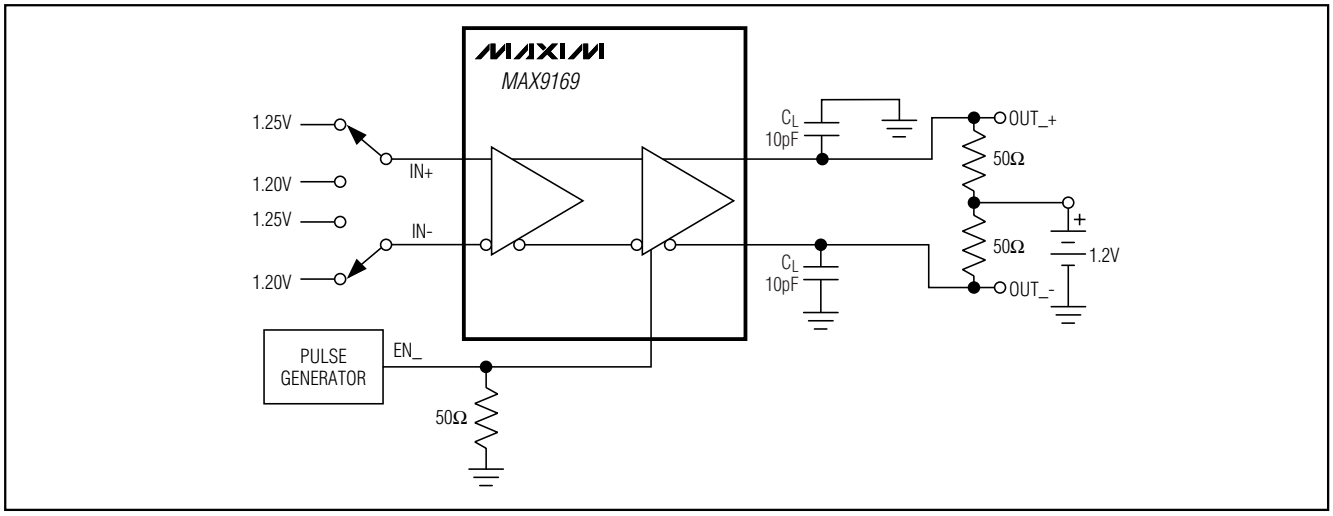


Figure 16. MAX9169 Enable and Disable Time Test Circuit

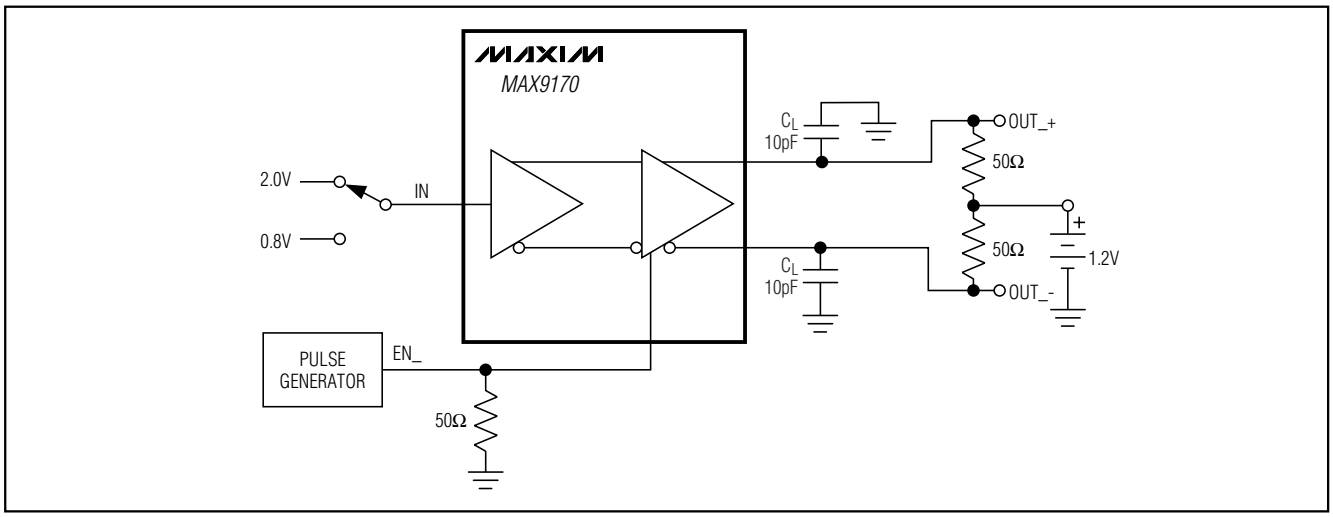


Figure 17. MAX9170 Enable and Disable Time Test Circuit

4-Port LVDS and LVTTL-to-LVDS Repeaters

Test Circuits and Timing Diagrams (continued)

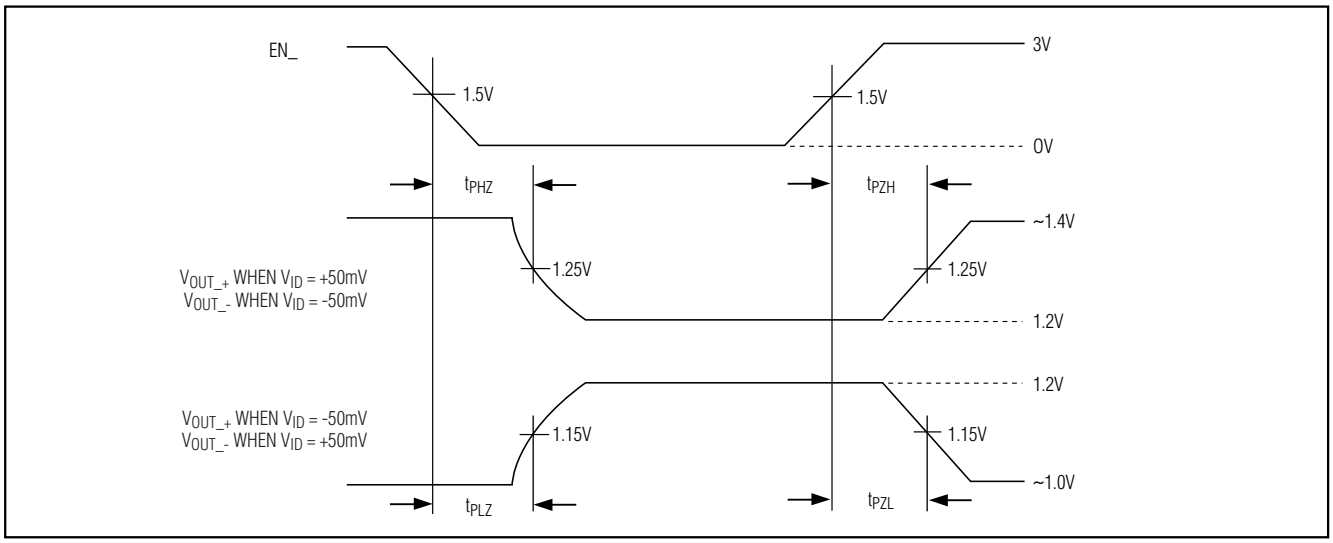


Figure 18. MAX9169 Enable and Disable Time Waveforms

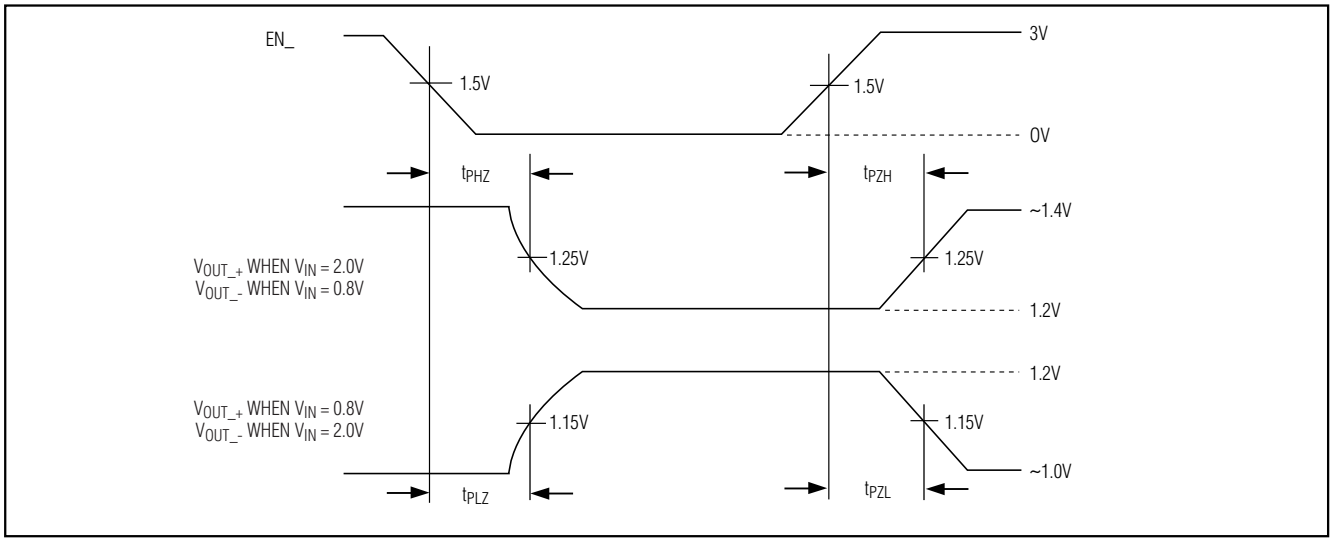
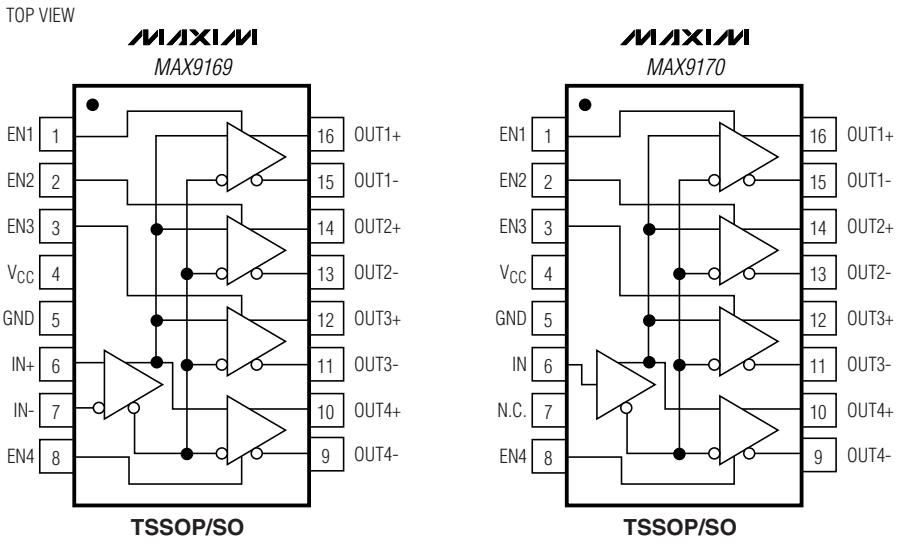


Figure 19. MAX9170 Enable and Disable Time Waveforms

Pin Configurations



Chip Information

TRANSISTOR COUNT: 1187

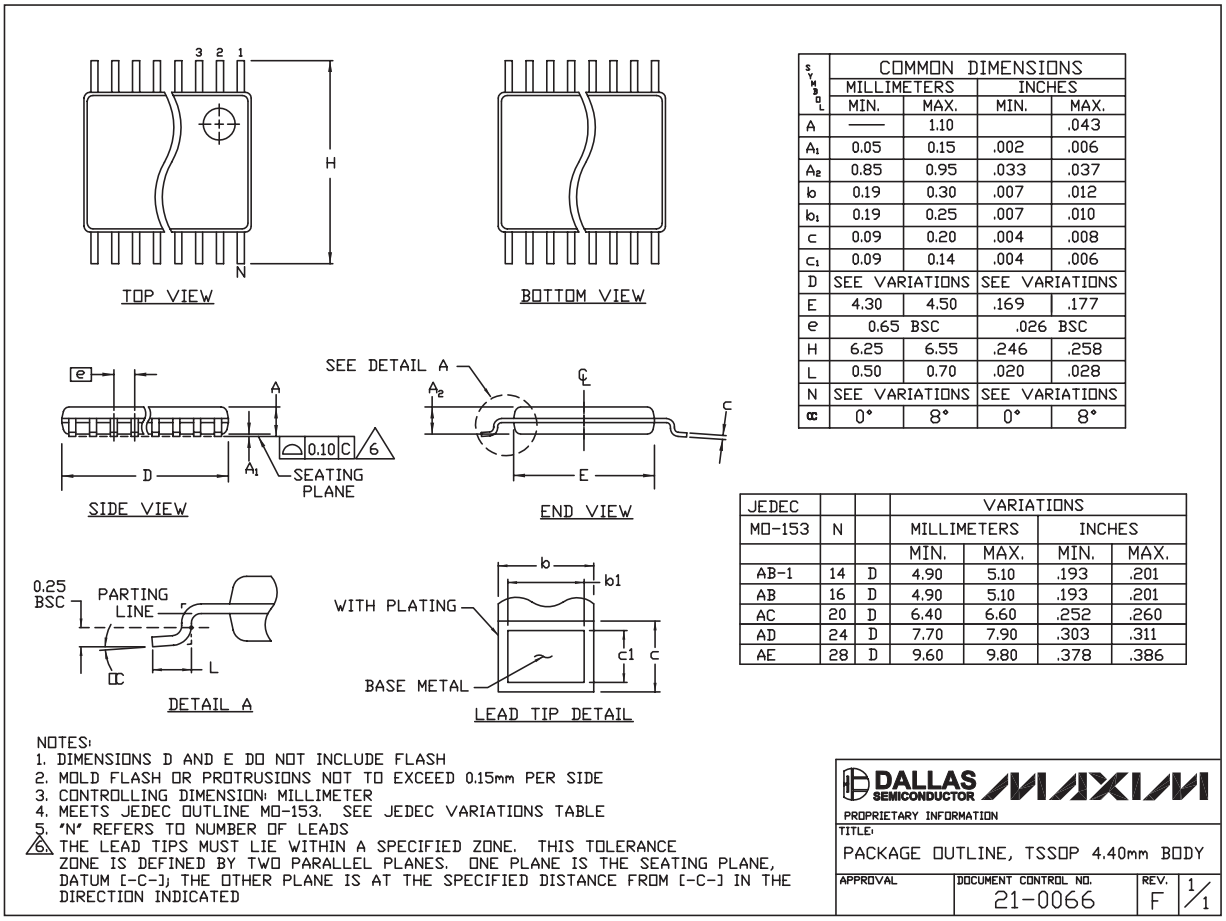
PROCESS: CMOS

4-Port LVDS and LVTTL-to-LVDS Repeaters

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

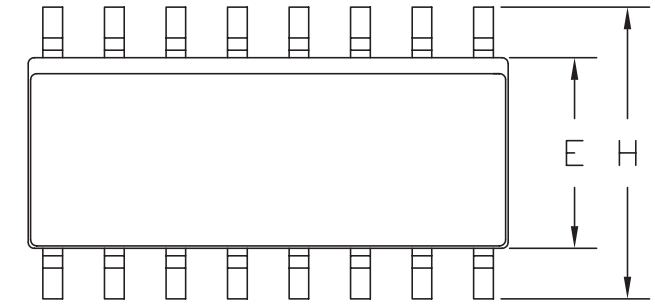
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1

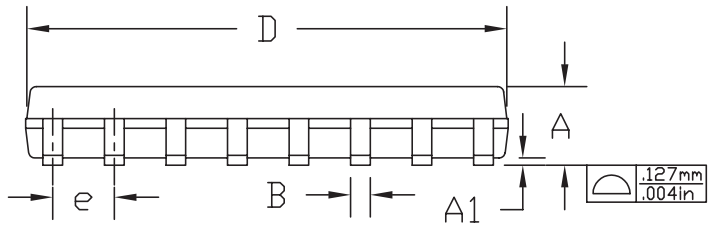
Package Information (continued)

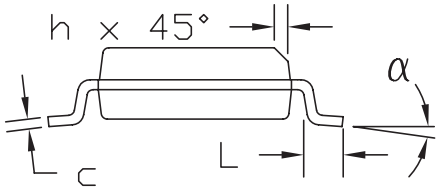
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

16L SOIC.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0?	8?	0?	8?





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AC.

MAXIM
PROPRIETARY INFORMATION

TITLE			
16L (N) SOIC OUTLINE			
APPROVAL	DWG 21-0588	REV B	1/1

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