19-2152; Rev 2; 11/02

Differential LVPECL/LVECL/HSTL Receiver/Drivers

General Description

The MAX9321/MAX9321A are low-skew differential receiver/drivers designed for clock and data distribution. The differential input can be adapted to accept a single-ended input by connecting the on-chip V_{BB} supply to an input as a reference voltage.

The MAX9321/MAX9321A feature ultra-low propagation delay (172ps) and part-to-part skew (20ps) with 24mA maximum supply current, making these devices ideal for clock buffering or repeating. For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock and data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply. Multiple pinouts are provided to simplify routing across a backplane to either side of a double-sided board.

Both devices are offered in space-saving 8-pin SOT23, SO, and µMAX packages.

Applications

Precision Clock Buffers

Low-Jitter Data Repeaters

Features

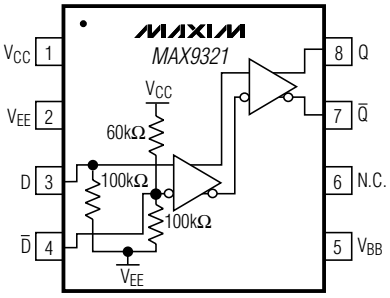
- **Improved Second Source of the MC10LVEP16 (MAX9321)**
- **+2.25V to +3.8V Differential HSTL/LVPECL Operation**
- **-2.25V to -3.8V Differential LVECL Operation**
- **Low 17mA Supply Current**
- **20ps Part-to-Part Skew**
- **172ps Propagation Delay**
- **Minimum 300mV Output at 3GHz**
- **Output Low for Open Input**
- **ESD Protection >2kV (Human Body Model)**
- **On-Chip Reference for Single-Ended Input**
- **Available in Thermally Enhanced Exposed-Pad SO Package**

Ordering Information

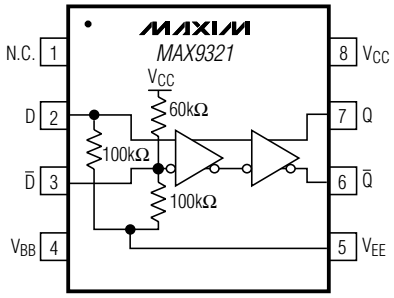
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9321EKA-T	-40°C to +85°C	8 SOT23-8	AALK
MAX9321EUA*	-40°C to +85°C	8 µMAX	—
MAX9321ESA	-40°C to +85°C	8 SO	—
MAX9321AEKA-T	-40°C to +85°C	8 SOT23-8	AAIX
MAX9321AEUA*	-40°C to +85°C	8 µMAX	—
MAX9321AESA	-40°C to +85°C	8 SO-EP**	—

**Future product—contact factory for availability.*
***EP = Exposed pad.*

Pin Configurations



SOT23



µMAX/SO

Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Differential LVPECL/LVECL/HSTL Receiver/Drivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to V_{EE} .....+4.1V
D or $\overline{D}$ ..... V_{EE} - 0.3V to V_{CC} + 0.3V
D to $\overline{D}$ .....±3.0V
Continuous Output Current.....50mA
Surge Output Current.....100mA
V_{BB} Sink/Source Current .....±0.6mA
Junction-to-Ambient Thermal Resistance in Still Air
8-Pin SOT23.....+112°C/W
8-Pin µMAX.....+221°C/W
8-Pin SO-EP .....+53°C/W
Junction-to-Ambient Thermal Resistance with 500 LFPM Airflow
8-Pin SOT23.....+78°C/W
8-Pin µMAX.....+155°C/W
8-Pin SO.....+99°C/W
Junction-to-Case Thermal Resistance
8-Pin SOT23.....+80°C/W
8-Pin µMAX.....+39°C/W
8-Pin SO.....+40°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (D, $\overline{D}$, Q, $\overline{Q}$, V_{BB}).....>2kV
Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2.0V. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1–5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL INPUT (D, $\overline{D}$)												
Single-Ended Input High Voltage	V_{IH}	V_{BB} connected to $\overline{D}$ (V_{IL} for V_{BB} connected to D), Figure 1	V_{CC} - 1.210		V_{CC}	V_{CC} - 1.145		V_{CC}	V_{CC} - 1.085		V_{CC}	V
Single-Ended Input Low Voltage	V_{IL}	V_{BB} connected to $\overline{D}$ (V_{IH} for V_{BB} connected to D), Figure 1	V_{EE}		V_{CC} - 1.65	V_{EE}		V_{CC} - 1.545	V_{EE}		V_{CC} - 1.485	V
High Voltage of Differential Input	V_{IHD}		V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V
Low Voltage of Differential Input	V_{ILD}		V_{EE}		V_{CC} - 0.1	V_{EE}		V_{CC} - 0.1	V_{EE}		V_{CC} - 0.1	V
Differential Input Voltage	V_{IHD} - V_{ILD}	For V_{CC} - V_{EE} < 3.0V	0.1		V_{CC} - V_{EE}	0.1		V_{CC} - V_{EE}	0.1		V_{CC} - V_{EE}	V
		For V_{CC} - V_{EE} ≥ 3.0V	0.1		3.0	0.1		3.0	0.1		3.0	
Input High Current	I_{IH}				150			150			150	µA
D Input Low Current	I_{ILD}		-10		100	-10		100	-10		100	µA
$\overline{D}$ Input Low Current	$I_{IL\overline{D}}$		-150		+150	-150		+150	-150		+150	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2.0V. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1–5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL OUTPUT (Q, $\overline{Q}$)												
Single-Ended Output High Voltage	V_{OH}	Figure 1	V_{CC} - 1.135		V_{CC} - 0.885	V_{CC} - 1.07		V_{CC} - 0.82	V_{CC} - 1.01		V_{CC} - 0.76	V
Single-Ended Output Low Voltage	V_{OL}	Figure 1	V_{CC} - 1.935		V_{CC} - 1.685	V_{CC} - 1.87		V_{CC} - 1.62	V_{CC} - 1.81		V_{CC} - 1.56	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 1	550			550			550			mV
REFERENCE (V_{BB})												
Reference Voltage Output (Note 6)	V_{BB}	I_{BB} = ±0.5mA	V_{CC} - 1.55		V_{CC} - 1.31	V_{CC} - 1.445		V_{CC} - 1.245	V_{CC} - 1.385		V_{CC} - 1.185	V
POWER SUPPLY												
Supply Current (Note 7)	I_{EE}			16	24		17	24		18	24	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, input frequency = 1.5GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{EE} + 1.2V to V_{CC}, V_{ILD} = V_{EE} to V_{CC} - 0.15V, V_{IHD} - V_{ILD} = 0.15V to the smaller of 3V or V_{CC} - V_{EE}. Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 8, 11)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD}, t_{PHLD}	Figure 2	145	184	235	145	172	245	130	167	230	ps
Part-to-Part Skew (Note 9)	t_{SKPP}			25	90		20	100		20	100	ps
Added Random Jitter (Note 10)	t_{RJ}	f_{IN} = 1.5GHz, Clock pattern		1.7	2.8		1.7	2.8		1.7	2.8	ps (RMS)
		f_{IN} = 3.0GHz, Clock pattern		0.6	1.5		0.6	1.5		0.6	1.5	

Differential LVPECL/LVECL/HSTL Receiver/Drivers

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, input frequency = 1.5GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{EE} + 1.2V to V_{CC}, V_{ILD} = V_{EE} to V_{CC} - 0.15V, V_{IHD} - V_{ILD} = 0.15V to the smaller of 3V or V_{CC} - V_{EE}. Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 8, 11)

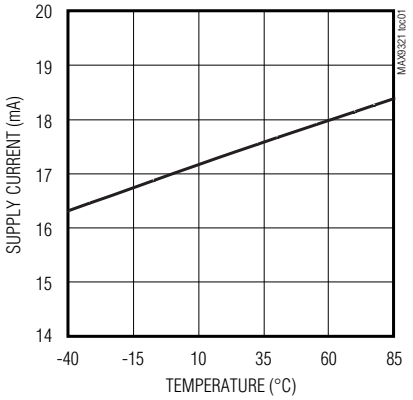
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Added Deterministic Jitter (Note 10)	t_{DJ}	3.0Gbps 2^{23} -1 PRBS pattern		57	80		57	80		57	80	ps (p-p)
Switching Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 300mV, Clock pattern, Figure 2	3.0			3.0			3.0			GHz
		V_{OH} - V_{OL} ≥ 550mV, Clock pattern, Figure 2	2.0			2.0			2.0			
Output Rise/ Fall Time (20% to 80%)	t_R, t_F	Figure 2	50	88	120	50	89	120	50	90	120	ps

Note 1: Guaranteed by design and characterization.
Note 2: Measurements are made with the device in thermal equilibrium.
Note 3: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 4: DC parameters production tested at T_A = +25°C. Guaranteed by design and characterization over the full operating temperature range.
Note 5: Single-ended input operation is limited to V_{CC} - V_{EE} ≥ 3.0V.
Note 6: Use V_{BB} as a reference for inputs on the same device only.
Note 7: All pins open except V_{CC} and V_{EE}.
Note 8: Guaranteed by design and characterization. Limits are set at ±6 sigma.
Note 9: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 10: Device jitter added to the input signal.

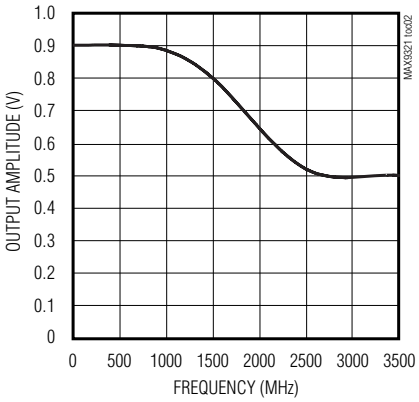
Typical Operating Characteristics

(SO packages) (V_{CC} = +3.3V, V_{EE} = 0, input transition time = 125ps (20% to 80%), V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, f_{IN} = 1.5GHz, outputs loaded with 50Ω to V_{CC} - 2V, T_A = +25°C, unless otherwise noted.)

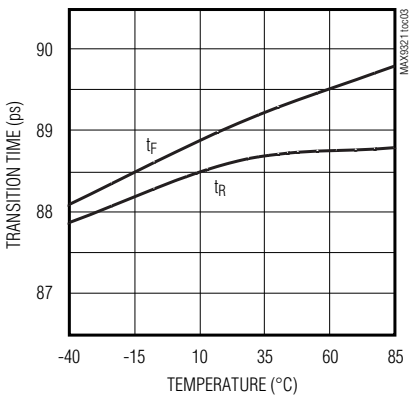
SUPPLY CURRENT, I_{EE} vs. TEMPERATURE



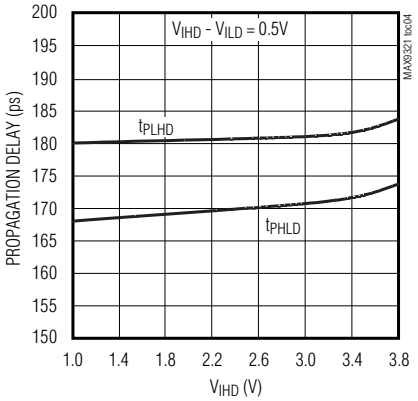
OUTPUT AMPLITUDE, V_{OH} - V_{OL} vs. FREQUENCY



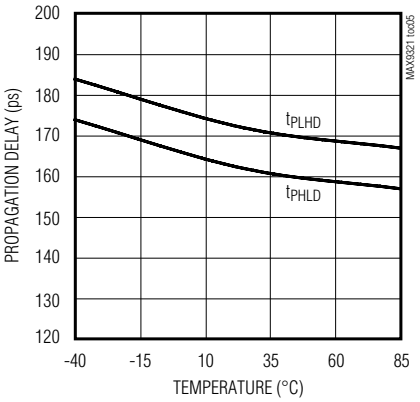
TRANSITION TIME vs. TEMPERATURE



PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT, V_{IHD}



PROPAGATION DELAY vs. TEMPERATURE



Differential LVPECL/LVECL/HSTL Receiver/Drivers

Pin Description (MAX9321)

PIN		NAME	FUNCTION
µMAX/SO	SOT23		
1	6	N.C.	No Connection
2	3	D	Noninverting Differential Input. 100kΩ pulldown to V_{EE}.
3	4	$\overline{D}$	Inverting Differential Input. 60kΩ pullup to V_{CC} and 100kΩ pulldown to V_{EE}.
4	5	V_{BB}	Reference Output Voltage. Connect to the inverting or noninverting input to provide a reference for single-ended operation. When used, bypass with a 0.01µF ceramic capacitor to V_{CC}; otherwise leave open.
5	2	V_{EE}	Negative Supply Voltage
6	7	$\overline{Q}$	Inverting Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
7	8	Q	Noninverting Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
8	1	V_{CC}	Positive Supply Voltage. Bypass from V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

Pin Description (MAX9321A)

PIN		NAME	FUNCTION
µMAX/SO	SOT23		
1	6	N.C.	No Connection
2	3	$\overline{D}$	Inverting Differential Input. 60kΩ pullup to V_{CC} and 100kΩ pulldown to V_{EE}.
3	4	D	Noninverting Differential Input. 100kΩ pulldown to V_{EE}.
4	5	V_{BB}	Reference Output Voltage. Connect to the inverting or noninverting input to provide a reference for single-ended operation. When used, bypass with a 0.01µF ceramic capacitor to V_{CC}; otherwise leave open.
5	2	V_{EE}	Negative Supply Voltage
6	8	Q	Noninverting Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
7	7	$\overline{Q}$	Inverting Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
8	1	V_{CC}	Positive Supply Voltage. Bypass from V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

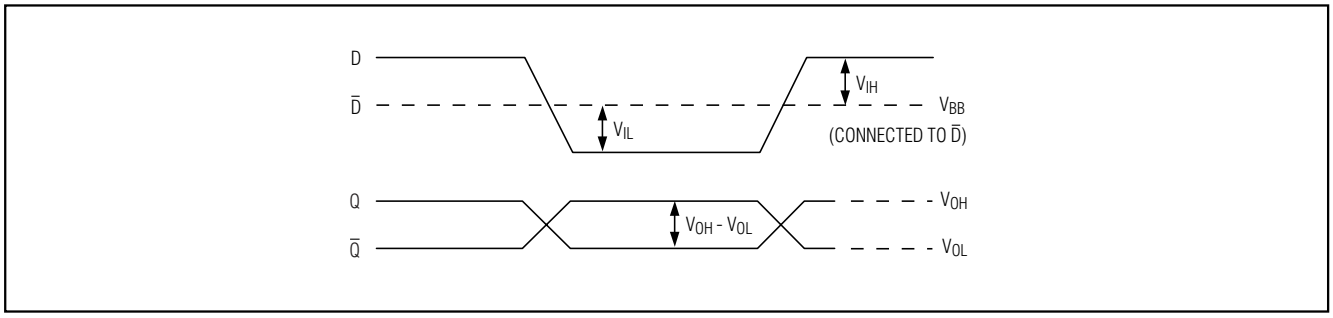


Figure 1. Switching with Single-Ended Input

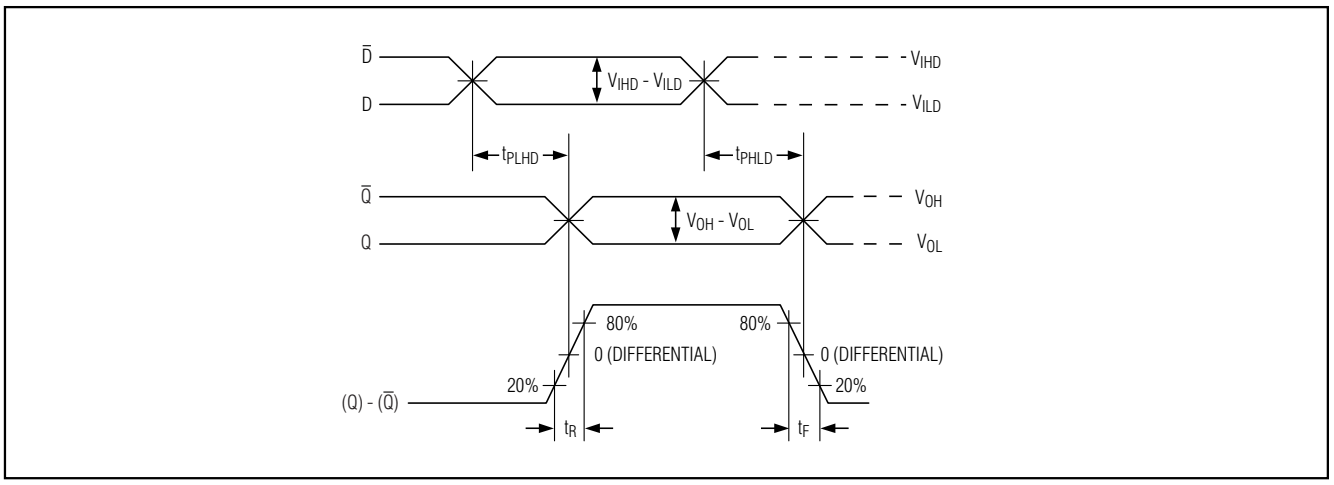


Figure 2. Differential Transition Time and Propagation Delay Timing Diagram

Detailed Description

The MAX9321/MAX9321A are low-skew differential receiver/drivers designed for clock and data distribution. For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock and data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

Inputs

The differential input can be configured to accept a single-ended input when operating at approximately V_{CC} - V_{EE} = 3.0V to 3.8V. This is accomplished by connecting the on-chip reference voltage, V_{BB}, to an input as a reference. For example, the differential D, $\overline{D}$ input is converted to a noninverting, single-ended input by connecting V_{BB} to $\overline{D}$ and connecting the single-ended input to D. An inverting input is obtained by connecting V_{BB} to D and connecting the single-ended input to $\overline{D}$. With the differential input configured as single ended (using V_{BB}), the single-ended input can be driven to V_{CC} and V_{EE} or with a single-ended LVPECL/LVECL signal.

When the differential input is configured as a single-ended input (using V_{BB}), the approximate supply range is V_{CC} - V_{EE} = 3.0V to 3.8V. This is because one of the inputs must be V_{EE} + 1.2V or higher for proper operation of the input stage. V_{BB} must be at least V_{EE} + 1.2V because it becomes the high-level input when the other (single-ended) input swings below it. Therefore, minimum V_{BB} = V_{EE} + 1.2V.

The minimum V_{BB} output is V_{CC} - 1.510V. Substituting the minimum V_{BB} into V_{BB} = V_{EE} + 1.2V results in a minimum supply of 2.71V. Rounding up to a standard supply gives the single-ended operating supply range of V_{CC} - V_{EE} = 3.0V to 3.8V.

Differential LVPECL/LVECL/HSTL Receiver/Drivers

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB} reference is not used, it can be left open. The V_{BB} reference can source or sink 0.5mA. Use V_{BB} only for an input on the same device as the V_{BB} reference.

The maximum magnitude of the differential input from D to $\overline{D}$ is 3.0V or V_{CC} - V_{EE}, whichever is less. This limit also applies to the difference between any reference voltage input and a single-ended input.

The differential input has bias resistors that drive the output to a differential low when the inputs are open. The inverting input is biased with a 60kΩ pullup to V_{CC} and a 100kΩ pulldown to V_{EE}. The noninverting input is biased with a 100kΩ pulldown to V_{EE}.

Specifications for the high and low voltage of the differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously (V_{ILD} cannot be higher than V_{IHD}).

Outputs

Output levels are referenced to V_{CC} and are considered LVPECL or LVECL, depending on the level of the V_{CC} supply. With V_{CC} connected to a positive supply and V_{EE} connected to GND, the output is LVPECL. The output is LVECL when V_{CC} is connected to GND and V_{EE} is connected to a negative supply.

A single-ended input of at least V_{BB} ±100mV or a differential input of at least ±100mV switches the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table.

Applications Information

Supply Bypassing

Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the 0.01µF value capacitor closest to the device. Use multiple parallel vias for low inductance. When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC} (if the V_{BB} reference is not used, it can be left open).

Traces

Input and output trace characteristics affect the performance of the MAX9321/MAX9321A. Connect each signal of a differential input or output to a 50Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Reduce skew within a differential pair by matching the electrical length of the traces.

The exposed-pad (EP) SO package can be soldered to the PC board for enhanced thermal performance. If the EP is not soldered to the PC board, the thermal resistance is the same as the regular SO package. The EP is connected to the chip V_{EE} supply. Be sure that the pad does not touch signal lines or other supplies.

Contact Maxim's Packaging department for guidelines on the use of EP packages.

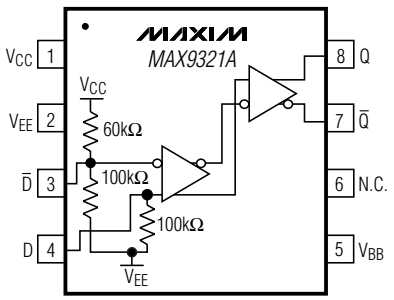
Output Termination

Terminate outputs through 50Ω to V_{CC} - 2V or use an equivalent Thevenin termination. When a single-ended signal is taken from the differential output, terminate both outputs. For example, when Q is used as a single-ended output, terminate both Q and $\overline{Q}$.

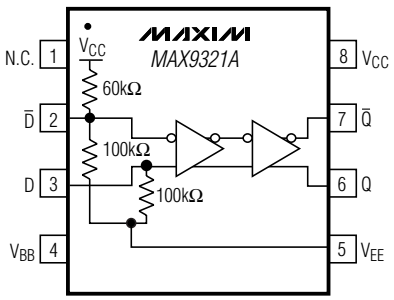
Chip Information

TRANSISTOR COUNT: 162

Pin Configurations (continued)



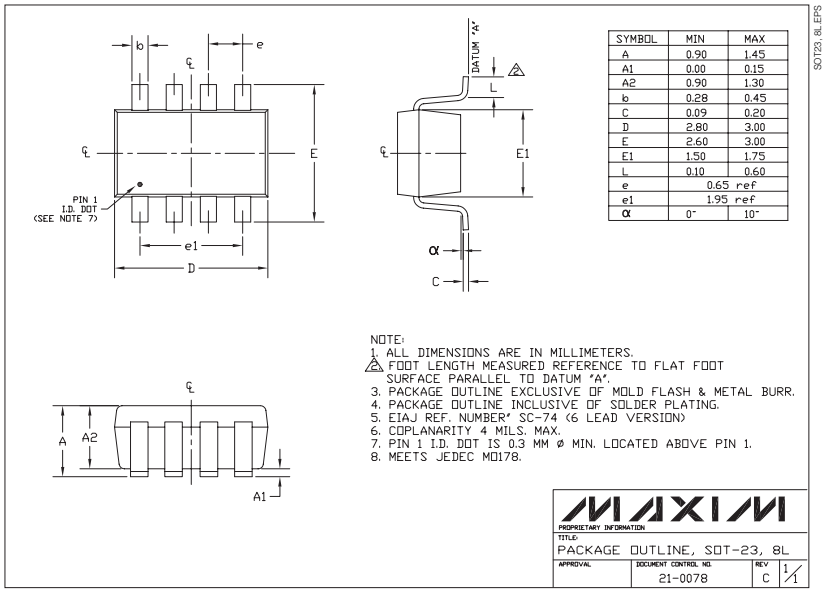
SOT23



µMAX/SO

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



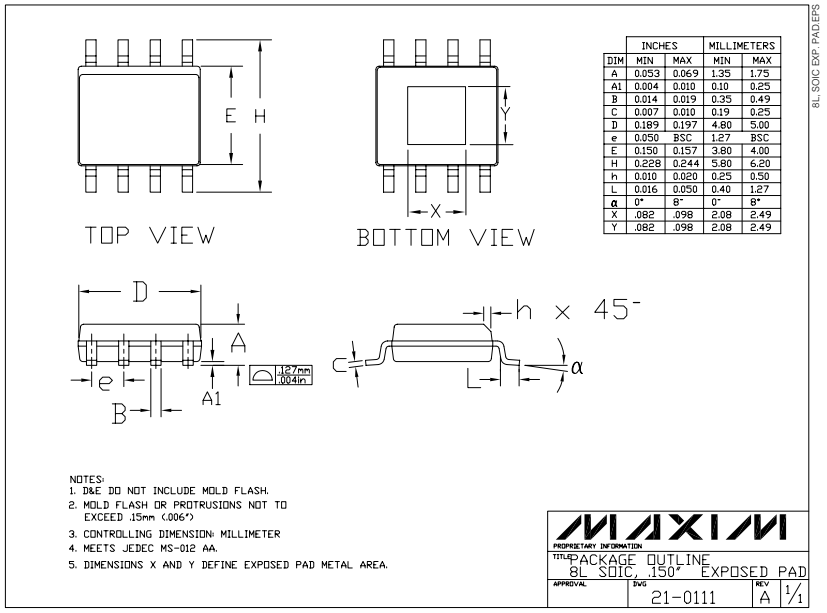
SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
8. MEETS JEDEC MO178.

MAXIM PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 8L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0078	C	1/1



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°
X	.082	.098	2.08	2.49
Y	.082	.098	2.08	2.49

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AA.
5. DIMENSIONS X AND Y DEFINE EXPOSED PAD METAL AREA.

MAXIM PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 8L SOIC, .150" EXPOSED PAD

APPROVAL	DWG	REV	
	21-0111	A	1/1

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