SC2200 Dual RF Power Amplifier Linearizer (RFPAL)

General Description

The SC2200 belongs to the 4th-generation family of RF PA linearizers (RFPAL) that provides increased integration and functionality over the previous generations. The device is a dual-path linearizer that is a fully-adaptive, RFIN/RFOUT predistortion linearization solution optimized for a wide range of amplifiers, power levels, and communication protocols. It supports 2G to 4G standards (FDD and TDD) from 698MHz to 2700MHz as well as an expanded range of signal bandwidths from 60MHz down to 1.2MHz. The SC2200 accepts single-ended RF signals to eliminate baluns and features a mirrored pinout facilitating design of both paths. The device uses the PA output and input signals to adaptively generate an optimized correction function to minimize the PA's distortion. Using RF-domain analog signal processing enables the SC2200 to operate over wide bandwidths and with very low power consumption. The dual linearizer is optimized for high-performance MIMO applications, including small cells, active antenna, and distributed antenna systems.

Applications

- Cellular Infrastructure
  - Single/Multicarrier, Multistandard: CDMA/EVDO, TD-SCDMA, WiMAX, WCDMA/HSDPA, LTE, and TD-LTE
  - BTS Amplifiers, RRH, Booster Amplifiers, Repeaters, Small Cells, Microcells, Picocells, DAS, AAS and MIMO Systems
- Wide Range of PAs and Output Power
  - Amplifier: Class A/AB, Doherty
  - Average PA Output Power Examples:
    Cellular Infrastructure: 27dBm to 40dBm
  - PA Process: LDMOS, GaN, HBT, GaAs and InGaP

Benefits

- Ease of Use
  - Integrated RFIN/RFOUT Solution
- Smaller Total System Form Factor (24mm x 26mm)
- Reduces System Power Consumption and OPEX
- Reduces BOM Costs and Total Volume
  - Smaller Power Supply, Heat Sink, and Enclosure
  - Lower Back-Off Reduces Transistor Costs

Features

- Frequency Range: 698MHz–2700MHz
- Integrated Preamp and Single-Ended RF I/Os
- Single +1.8V Supply Voltage
- External Reference Clock Support:
  - 10, 13, 15.36, 19.2, 20, 26, and 30.72MHz
- Packaged in 11mm x 11mm SAWN QFN Package
- Operating Case Temperature: -40°C to +100°C
- RoHS, Green, REACH, and ISO9001 Compliant
- Dual-Path RFIN/RFOUT Linearizer in CMOS SoC
- Fully Adaptive Correction
- Up to 28dB ACLR and 38dB IMD Improvement (1)
- 1.2MHz < BWSIG ≤ 60MHz
- Power Consumption:
  - Duty-Cycled (10%) Feedback: 1500mW (Dual-Path)
  - 100% Adaptation: 1.95W (Dual-Path)

***Ordering Information* and *Block Diagram* appears at end of data sheet.**

19-7748; Rev 1; 6/16

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Absolute Maximum Ratings

Supply Voltage (AVDD18 to GND) ..... -0.2V to +2.2V
Supply Voltage (DVDD18 to GND) ..... -0.2V to +2.2V
Supply Voltage (V_{DDIO} to GND) ..... -0.2V to +2.2V
Input Voltage (1.8V pins) ..... -0.2V to V_{DD18} + 0.2V
Input Voltage (V_{DDIO} pins) ..... -0.2V to V_{DDIO} + 0.2V
Input to RF Inputs (RMS) ..... +0dBm
Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C
Operating Case Temperature ..... -40°C to +100°C

Warning: Any stress beyond the ranges indicated may damage the device permanently. The specified stress ratings do not imply functional performance in these ranges. Exposure of the device to the absolute maximum ratings for extended periods of time is likely to degrade the reliability of this product

DC Characteristics

PARAMETER (Note 1)	MIN	TYP	MAX	UNITS
Supply Voltage (DVDDIO to GND)	1.7	1.8	1.9	V
Supply Voltage (AVDD18 to GND)	1.7	1.8	1.9	V
Supply Voltage (DVDD18 to GND)	1.7	1.8	1.9	V
Supply Peak Current (DVDDIO to GND) (Notes 2, 3, 5, 6)			50	mA
Supply Peak Current (AVDD18 to GND) (Notes 1, 2, 3, 5)			1300	mA
Supply Peak Current (DVDD18 to GND) (Notes 1, 2, 3, 5)			400	
Average Power Dissipation: Full-Speed Adaptation (Notes 3, 4, 6)		1950		mW
Average Power Dissipation: Duty-Cycled Feedback (Notes 3, 5, 6)		1500		mW

Note 1: All specifications in this table apply to both paths being enabled.
Note 2: Peak current includes supply decoupling network. Refer to the *Hardware Design Guide* for sizing of the voltage regulators.
Note 3: Characterized at over operating voltages, case temperature with 20MHz input signal BW, and V_{DVDDIO} = 1.8V.
Note 4: Continuous adaptation, tracking (100% duty cycled feedback), and advanced features active or inactive.
Note 5: Duty-cycled feedback power dissipations averaged over on time of 100ms (9%) and off time of 1.0s (91%).
Note 6: Power dissipation can be FW dependent. Refer to the FW release notes for any changes to values listed above.

Radio Frequency Signals

(Operation at T_A = +25°C, V_{AVDD18} = 1.8V, V_{DVDDIO} = 1.8V, V_{DVDD18} = 1.8V and 20MHz external clock, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency (Note 7)	f		698		2700	MHz
Input Signal Bandwidth (Note 8)	BW_{SIG}		1.2		60	MHz
Noise Power		Relative to -3dBm at RFOUT		-137		dBm/Hz
RFINDLY-RFOUT Preamp Gain	G	When set to default FW settings		10		dB
RFINDLY-RFOUT Preamp Gain Deviation from T_C = +25°C	$G_{TEMPDEV}$	T_C = -40°C to +100°C at 2140MHz		+1		dB
		T_C = -40°C to +100°C at 2700MHz		-2		
Path A/B Isolation	ISO	At 2700MHz		43		dB

Note 7: See the *Operating Frequency Range* table for frequency limits of each defined band.
Note 8: Correction performance across range of input signal BWs also depends on PA output power and carrier configuration.

RF Range for Maximum Correction—698MHz to 2700MHz

(Operation at T_A = +25°C, V_{AVDD18} = 1.8V, V_{DVDDIO} = 1.8V, V_{DVDD18} = 1.8V and 20MHz external clock, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RFIN Peak Power (Note 9)	P_{RFIN_PKL}	698MHz–2200MHz (Note 10)	-3	0	3	dBm
	P_{RFIN_PKH}	2200MHz–2700MHz (Note 10)	-3	0	3	
	P_{RFINRG_PKL}	Operating range, 698MHz–2200MHz	-32		3	
	P_{RFINRG_PKH}	Operating range, 2200MHz–2700MHz	-32		3	
RFINDLY Peak Power (Notes 9, 11)	$P_{RFINDLY_PK}$	PA operated at maximum power	-11	-8	-5	dBm
	$P_{RFINDLYRG_PK}$	Operating range	-40		-5	
RFFB Peak Power (Note 9)	P_{RFFB_PK}	PA operated at maximum power	-8	-4	-2	dBm
	P_{RFFBRG_PK}	Operating range	-37		-2	
RFOUT Peak Power (Note 9)	P_{RFOUT_PKL}	PA operated at maximum power (Note 12) 698MHz–2200MHz (Note 10)	-1	2	5	dBm
	P_{RFOUT_PKH}	PA operated at maximum power (Note 12) 2200MHz–2700MHz (Note 10)	-1	2	5	

Note 9: Peak power is defined as the 10^{-4} point on the CCDF (complementary cumulative distribution function) of the signal.
Note 10: PA operated at maximum power.
Note 11: PRFOUT_PK must be below +7dBm pk under all conditions.
Note 12: Only when the internal through path is enabled.
Note 13: IO type (input/output, pull up/down, push pull, open drain…) is programmable for DIO* pins. Refer to the *Programming Guide and HW Design Guide* for more information.
Note 14: User can configure the SC2200 to accept the following external clock frequencies: 10, 13, 15.36, 19.2, 20, 26 and 30.72MHz. External clock frequency other than 20MHz requires programming through the SPI bus. Refer to the *Programming Guide and Hardware Design Guide* for more information.

Digital I/O—DC Characteristics

(Guaranteed performance across worst-case supply voltage and temperature range, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS Input Logic-Low	V_{IL}		-0.2		0.2 x V_{DD}	V
CMOS Input Logic-High	V_{IH}	V_{DD} = DVDDIO	V_{DD} x 0.8		V_{DD} x 1.1	V
CMOS Output Logic-High	V_{OH}	V_{DD} = DVDDIO	V_{DD} x 0.9		V_{DD}	V
CMOS Output Logic-Low	V_{OL}		0.0		0.1 x V_{DD}	V
CMOS Output Current (Note 13)	I_{OL18}/I_{OH18}	V_{DVDDIO} = 1.8V	-4.0		+4.0	mA

Note 13: IO type (input/output, pull up/down, push pull, open drain…) is programmable for DIO* pins. Refer to the *Programming Guide and HW Design Guide* for more information.

Digital I/O—External Clock (XTALI)

(Guaranteed performance across worst-case supply voltage and temperature range, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
User Programmable External Clock (Note 14)	f_{CLK}		10	20	30.72	MHz
External Clock Frequency Accuracy					1	%
External Clock Frequency Drift		Including aging and temperature			100	ppm
Duty Cycle		Square wave	45		55	%
External Clock Amplitude	V_{CLK}	Sine or square wave	500		1500	mV_{P-P}
External Clock Phase Noise	P_{NCLK}	At 100kHz offset			-130	dBc/Hz

Note 14: User can configure the SC2200 to accept the following external clock frequencies: 10, 13, 15.36, 19.2, 20, 26 and 30.72MHz. External clock frequency other than 20MHz requires programming through the SPI bus. Refer to the *Programming Guide and Hardware Design Guide* for more information.

Crystal Requirements (XTALI/XTALO)

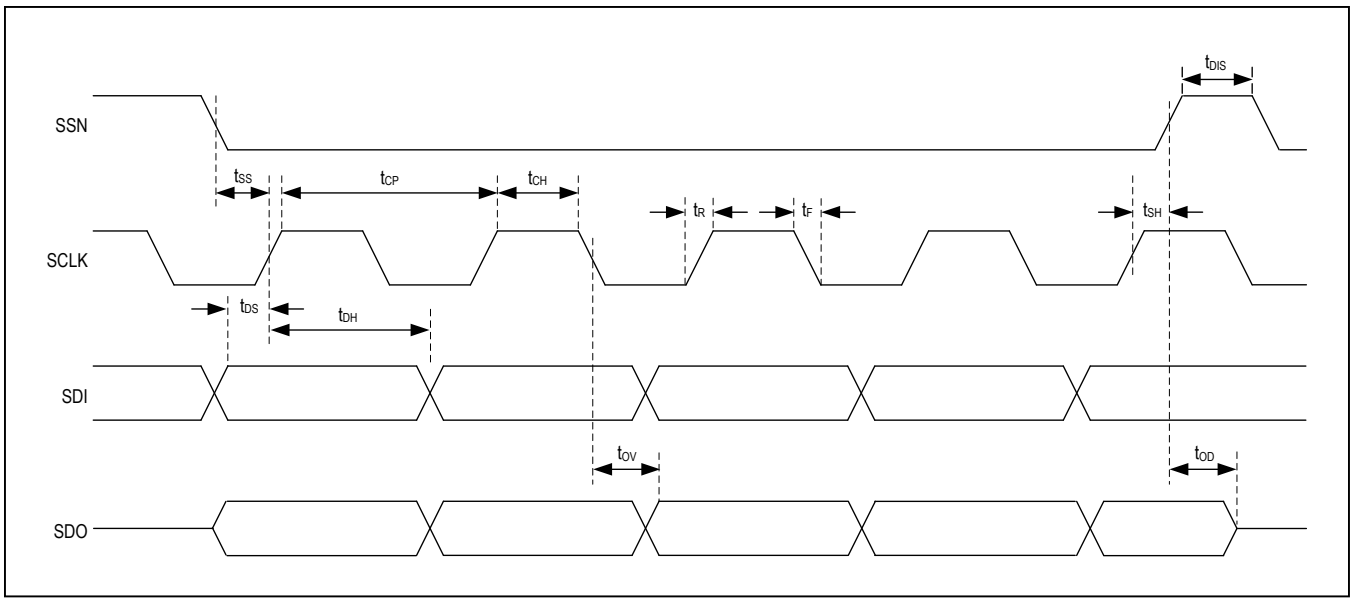
(Guaranteed performance across worst-case supply voltage and temperature range, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ESR				50	Ω
Capacitive Load to Ground			10	12	pF
Frequency Accuracy				250	ppm
Frequency Drift	Including aging and temperature			100	ppm

Serial Peripheral Interface (SPI) Bus Specifications

(Guaranteed performance across worst-case supply voltage and temperature range, unless otherwise specified.)

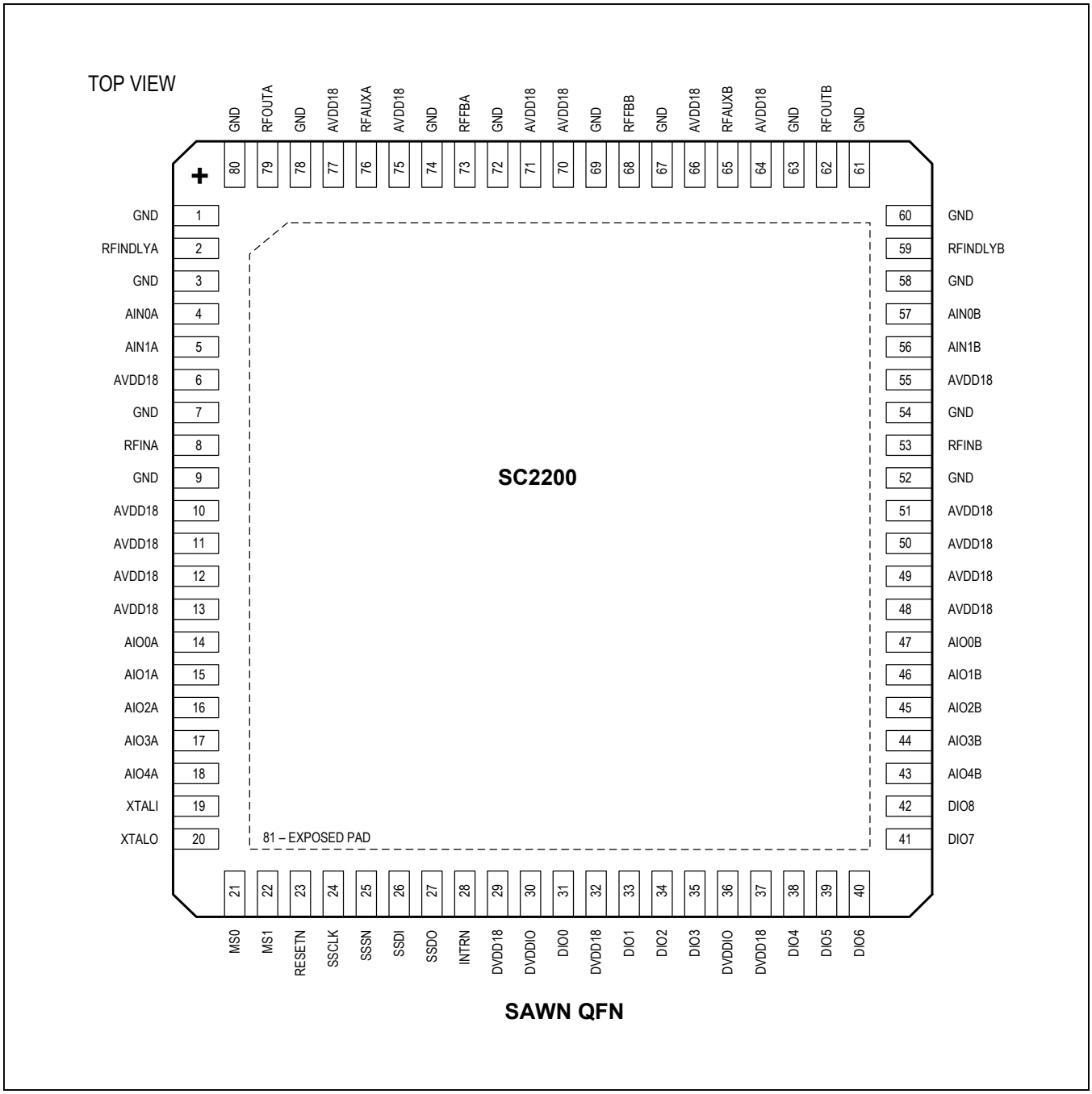
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Select Setup Time	t_{SS}		100			ns
Select Hold Time	t_{SH}		100			ns
Select Disable Time	t_{DIS}		100			ns
Data Setup Time	t_{DS}		25			ns
Data Hold Time	t_{DH}		45			ns
Rise Time	t_R				25	ns
Fall Time	t_F				25	ns
Clock Period	t_{CP}		250			ns
Clock High Time	t_{CH}		100			ns
Time to Output Valid	t_{OV}				100	ns
Output Data Disable	t_{OD}				0	ns



CAS25512DWFL EEPROM Endurance

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write/Erase Cycles	C_{EEPROM}	Page mode, T_A = +25°C	1M			E/W cycles

Pin Configuration



SAWN QFN

Pin Description

PIN	NAME	TYPE	FUNCTION
1, 3, 7, 9, 52, 54, 58, 60, 61, 63, 67, 69, 72, 74, 78, 80	GND	RF Shield	Ground for Shield of RF Signal
2	RFINDLYA	Analog In	Delayed RF Single-Ended Input Signal for Tx Path A
4, 5	AIN0A, AIN1A	Analog In	Do not connect. Reserved for internal use.
6, 10–13, 48–51, 55, 64, 66, 70, 71, 75, 77	AVDD18	Supply	+1.8V DC Supply Voltage for Analog Circuits
8	RFINA	Analog In	RF 50Ω Input Signal for Tx Path A
14–18	AIO0A–AIO4A	Analog In/Out	Do not connect. Reserved for internal use.
19	XTALI	Analog In	Oscillator or External Clock Input. For the oscillator, connect a 20MHz crystal across XTALI to XTALO. For the external clock, connect clock source operating at 10, 13, 15.36, 19.2, 20, 26, 30.72MHz. Refer to the *Hardware Design Guide* for details.
20	XTALO	Analog Out	Crystal Output. Excitation driver for crystal or ceramic resonator.
21	MS0	Digital In	Load Enable. Required to program FW upgrades to internal EEPROM. Has internal pulldown to GND.
22	MS1	Digital In	Do not connect. Reserved for internal use. Has internal pulldown to GND.
23	RESETN	Digital In	Reset when Low. Has internal pullup to DVDDIO.
24	SSCLK	Digital In	Slave SPI Clock. Has internal pulldown to GND.
25	SSSN	Digital In	Slave SPI Select Enabled Low. Has internal pullup to DVDDIO.
26	SSDI	Digital In	Slave SPI Data Input to RFPAL. Has internal pulldown to GND.
27	SSDO	Digital Out	Slave SPI Data Output from RFPAL. Three-state. DVDDIO logic levels.
28	INTRN	Digital Out	General-Purpose Digital Output Controlled by FW. Notifies or interrupts the SPI host when low that (e.g., alarm) information is available to be collected. Open-drain output with internal pullup to DVDDIO.
29, 32, 37	DVDD18	Supply	+1.8V DC Supply Voltage for Digital Circuits
30, 36	DVDDIO	Supply	+1.8V DC Supply Voltage for Digital I/O Interface Circuits
31, 33–35, 38–42	DIO0–DI08	Digital In/Out	Do not connect. Reserved for internal use.
43–47	AIO4B–AIO0B	Analog In/Out	Do not connect. Reserved for internal use.
53	RFINB	Analog In	RF Single-Ended Input Signal for Tx Path B
56, 57	AIN1B, AIN0B	Analog In	Do not connect. Reserved for internal use.
59	RFINDLYB	Analog In	Delayed RF Single-Ended Input Signal for Tx Path B
62	RFOUTB	Analog Out	RF Single-Ended Output Signal for Tx Path B
65	RFAUXB	Analog Out	Do not connect. Reserved for internal use.
68	RFFBB	Analog In	RF Single-Ended Feedback Signal for Tx Path B
73	RFFBA	Analog In	RF Single-Ended Feedback Signal for Tx Path A
76	RFAUXA	Analog Out	Do not connect. Reserved for internal use.
79	RFOUTA	Analog Out	RF Single-Ended Output Signal for Tx Path A
81	GND	Supply	Exposed Pad. Serves as supply ground and thermal interface.

Detailed Description

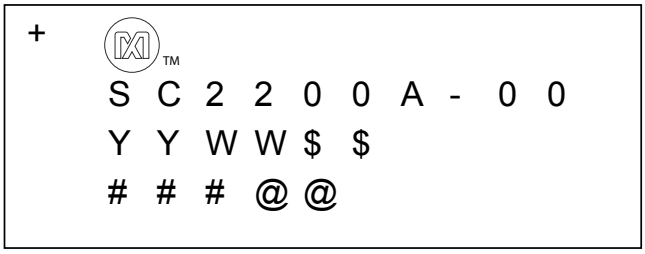
Introduction to Predistortion Using the SC2200

Wideband signals in today's telecommunications systems have high peak-to-average ratios and stringent spectral regrowth specifications. These specifications place high linearity demands on power amplifiers. Linearity can be achieved by backing off output power at the price of reducing efficiency. However, this increases the component and operating costs of the power amplifier. Better linearity can be achieved through the use of digital predistortion and other linearization techniques, but many of these methods are time consuming and costly to implement.

The SC2200 is a true RFIN and RFOUT solution where the complex signal processing is done in the RF domain, supporting modular power amplifier designs that are independent of the baseband and transceiver subsystems. This simple system-on-chip offers wide signal bandwidth, broad frequency of operation, and very low power consumption. It reduces development costs and speeds time to market. Applicable across a broad range of signals—including 2G, 3G, 4G wireless, and other modulation types—the powerful analog signal processing engine is capable of linearizing the most efficient power amplifier topologies. The SC2200 delivers the required efficiency and performance demanded by today's wireless systems.

Wireless service providers are deploying networks with wider coverage, greater subscriber density, and higher data rates. These networks require more efficient power amplifiers. Additionally, the emergence of MIMO, distributed architectures, and active antenna systems is driving the increased need to support smaller, more-efficient power amplifier implementations. Furthermore, a strong push continues toward reducing the total capital and operating costs of base stations.

Top Mark



OPTIONAL NOTES:

MAXIM INTEGRATED MARKING STANDARDS SPECIFICATION REFERENCE: 20-0400.

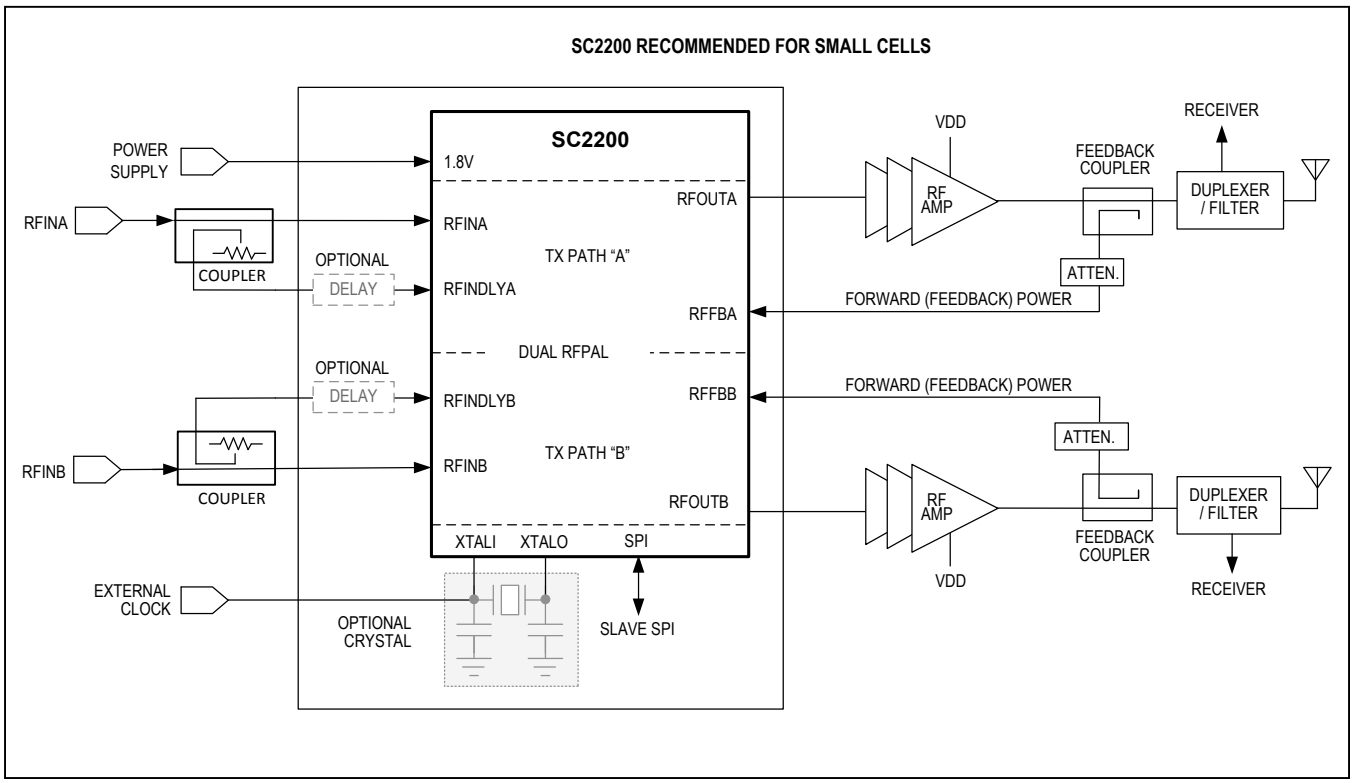
LINE	TOP MARK	DESCRIPTION
1	+	Indicates the part is lead (Pb)-free and designates location of pin one/ball A1Pb-free laser mark
2	SC2200	Product part number
2	A	Product revision
2	-00	Product configuration: -00 = Dual-RFPAL Base Configuration
3	YY	Date code—year
3	WW	Date code—work week
3	$$	Indicates the package revision code from the reliability database
4	###	Indicates the last 3 numeric characters from the lot number
4	@@	Indicates the first 2 alpha characters after the numeric characters from the lot number

ESD

ESD (Electro-Static Discharge) sensitive device. Although this product incorporates ESD protection circuitry, permanent damage may occur on devices subjected to electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or device failure.

TEST METHODOLOGY	CLASS	VOLTAGE	UNIT
Human Body Model (per JS-001-2012)	1C	1000	V
Charge Device Model (per JESD22-C101)	II	250	V

Block Diagram



Ordering Information

PART	DESCRIPTION
SC2200A-00A00	IC, dual-RFPAL, 698-2700 MHz, FW5.0.09.04

PON = Part ordering number.

Shipping designator:

E = 7in tape and reel. Append shipping designator (E) at end of part number. If left blank, designates bulk shipping option.

Evaluation Kit Ordering Information

PART NUMBER	DESCRIPTION
SC2200-EVK900	Evaluation kit, dual-RFPAL, 698MHz–960MHz
SC2200-EVK1900	Evaluation kit, dual-RFPAL, 1800MHz–2200MHz
SC2200-EVK2400	Evaluation kit, dual-RFPAL, 2300MHz–2700MHz
SC-USB-SPI2*	Adapter, SPI-USB Interface/Controller

EV kits ship with most recent release of FW.

**Not required for operating evaluation kits. Only recommended for prototypes debug and/or programming linearizer during manufacturing (if no other means are available, such as on-board controller, etc.).*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
SAWN QFN	K8011MK+1B	21-0766	90-0606

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/15	Initial release	—
1	6/16	Updated *General Description*	1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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