Apacer

RoHS Compliant

Serial ATA Flash Drive

SV240-25 Product Specifications



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Specifications Overview:

- **Compliance with SATA Revision 3.2**
  - SATA 6 Gb/s interface
  - Backward compatible with SATA 1.5 and 3 Gb/s interfaces
  - ATA command set-4 (ACS-4)
- **Capacity**
  - 120, 240, 480, 960, 1920 GB
- **Performance**[1]
  - Burst read/write: 600 MB/sec
  - Sequential read: Up to 560 MB/sec
  - Sequential write: Up to 495 MB/sec
  - Random read (4K): Up to 95,000 IOPS
  - Random write (4K): Up to 85,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - DataDefender™
  - ATA Secure Erase
  - Device Sleep
  - TRIM
  - Hyper Cache Technology
  - Over-provisioning
  - DataRAID™
  - SMART Read Refresh™
- **DRAM Cache for Enhanced Random Performance**
- **Endurance (in drive writes per day: DWPD)**
  - 120 GB: 2.28 DWPD
  - 240 GB: 2.2 DWPD
  - 480 GB: 2.27 DWPD
  - 960 GB: 2.28 DWPD
  - 1920 GB: 2.28 DWPD
- **Temperature Range**
  - Operating:
    - Standard: 0°C to 70°C
    - Wide: -40°C to 85°C
  - Storage: -55°C to 100°C
- **Supply Voltage**
  - 5.0 V ± 10%
- **Power Consumption**[1]
  - Active mode: 430 mA
  - Idle mode: 60 mA
- **SATA Power Management Modes**
- **Connector Type**
  - 7-pin SATA signal connector
  - 15-pin SATA power connector
- **Form Factor**
  - 2.5”
  - Dimensions: 100.00 x 69.85 x 6.90, unit: mm
  - Net weight: 63g ± 5%
- **NAND Flash Type:** 3D TLC (BiCS3)
- **MTBF:** >3,000,000 hours
- **Security**
  - AES 256-bit hardware encryption
  - Trusted Computing Group (TCG) Opal 2.0 (optional)
- **Reliability**
  - Thermal Sensor
  - End-to-End Data Protection
- **RoHS Compliant**

Note:
1. Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings. The term idle refers to the standby state of the device.

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1. General Description

Apacer's SV240-25, utilizing 3D NAND for higher capacity up to 1920GB and providing more power efficiency than 2D NAND, is a well-balanced solid-state disk (SSD) drive with standard form factor and great performance. Designed with SATA-based connector pinouts and in SATA 6 Gb/s interface, SV240-25 provides full compliance with the latest SATA Revision 3.2 interface specifications and delivers exceptional read/write speed, making it the ideal companion for heavy-loading industrial or server operations.

Regarding reliability, SV240-25 is built with a powerful SATA controller that supports on-the-module ECC as well as efficient wear leveling scheme and implemented with LDPC (Low Density Parity Check) ECC engine to extend SSD endurance and increase data reliability. Furthermore, SV240-25 is equipped with a built-in thermal sensor to monitor the temperature of the SSD via S.M.A.R.T commands to prevent overheating. Operating under 6 Gb/s interface, SV240-25 is provided with Apacer latest S.M.A.R.T. that is primarily oriented for the latest SATA interface SSD, for drive lifetime monitoring and analysis. For highly-intensive applications, End-to-End Data Protection ensures that data integrity can be assured at multiple points in the path to enable reliable delivery of data transfers.

Security-wise, Advanced Encryption Standard (AES) and Trusted Computing Group (TCG) Opal (optional) ensure data security and provide users with peace of mind knowing their data is safeguarded against unauthorized use at all times. SV240-25 also adopts the latest page mapping file translation layer and comes with various implementations including power saving modes, wear leveling, flash block management, S.M.A.R.T., TRIM, Hyper Cache technology, over-provisioning, DataDefender™, DataRAID™ and SMART Read Refresh™.

2. Functional Block

Apacer SV240-25 includes a single-chip controller designed with a DRAM and flash media. The controller integrates the flash management unit to support multi-channel, multi-bank flash arrays. Figure 2-1 shows the functional block diagram.

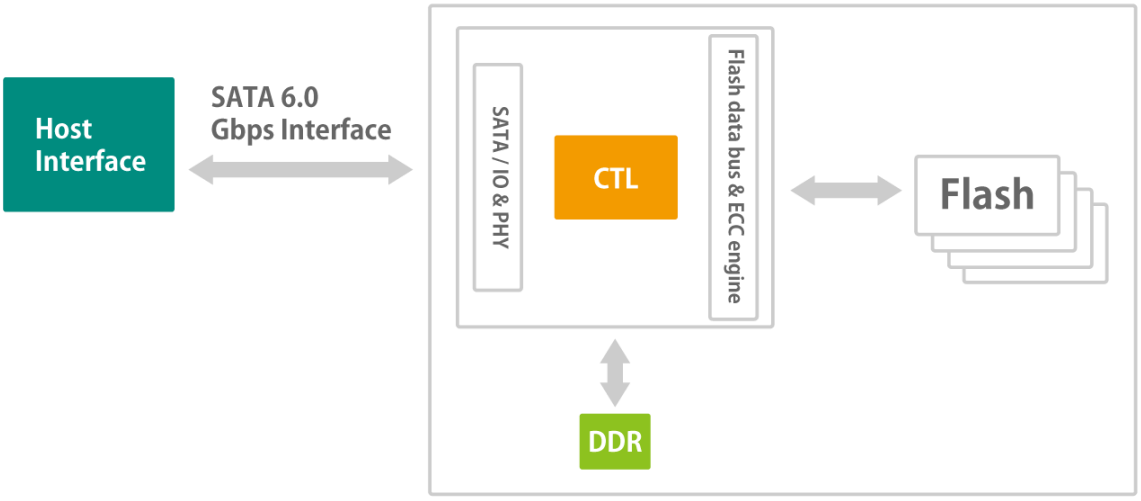

Figure 2-1 Functional Block Diagram

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3. Pin Assignments

Table 3-1 describes the SFD signal segment, and Table 3-2, power segment.

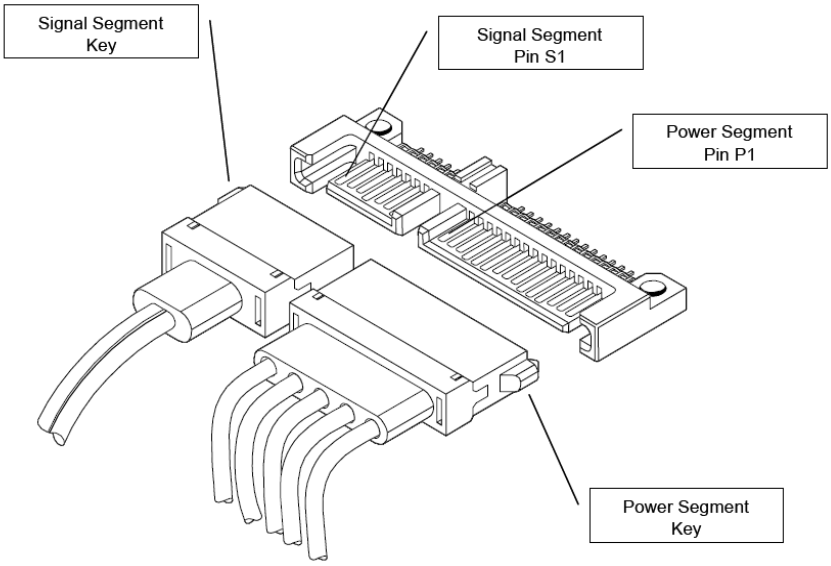

Figure 3-1 SATA Connectors

Table 3-1 Signal Segment

Pin	Type	Description
S1	GND	
S2	RxP	+ Differential Receive Signal
S3	RxN	- Differential Receive Signal
S4	GND	
S5	TxN	- Differential Transmit Signal
S6	TxP	+ Differential Transmit Signal
S7	GND	

Table 3-2 Power Segment

Pin	Signal/Description
P1	Unused (3.3V)
P2	Unused (3.3V)
P3	Device Sleep
P4	Reserved for Apacer use only[1]
P5	Ground
P6	Ground
P7	5V
P8	5V
P9	5V
P10	Ground
P11	Reserved for Apacer use only[1]
P12	Ground
P13	Unused (12V)
P14	Unused (12V)
P15	Unused (12V)

Note:
1. Reserved by Apacer, please do not connect to a host.

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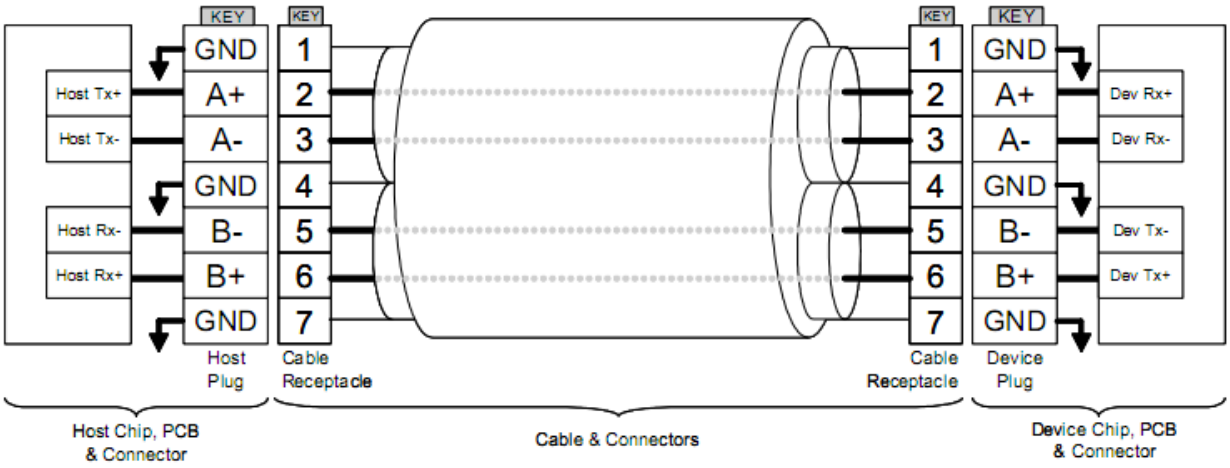

Figure 3-2 SATA Cable/Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable. The connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

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4. Product Specifications

4.1 Capacity

Capacity specifications of SV240-25 are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes	Cylinders	Heads	Sectors	Total LBA
120 GB	120,034,123,776	16,383	16	63	234,441,648
240 GB	240,057,409,536	16,383	16	63	468,862,128
480 GB	480,103,981,056	16,383	16	63	937,703,088
960 GB	960,197,124,096	16,383	16	63	1,875,385,008
1920 GB	1,920,383,410,176	16,383	16	63	3,750,748,848

Notes:
- Display of total bytes varies from operating systems.
- 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
- LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of SV240-25 is listed below in Table 4-2.

Table 4-2 Performance Specifications

Capacity / Performance	120 GB	240 GB	480 GB	960 GB	1920 GB
Sequential Read (MB/s)	560	560	560	560	560
Sequential Write (MB/s)	455	480	495	490	485
Random Read IOPS (4K)	66,000	95,000	96,000	95,000	95,000
Random Write IOPS (4K)	81,000	85,000	85,000	84,000	80,000

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 32.

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4.3 Environmental

Environmental specifications of SV240-25 product are shown in Table 4-3.

Table 4-3 Environmental Specifications

Environment	Specifications
Temperature	0°C to 70°C (Standard); -40°C to 85°C (Wide)
	-55°C to 100°C (Non-operation)
Vibration	Operation: 7.69(Grms), 20~2000(Hz)/random (compliant with MIL-STD-810G) Non-operation: 4.02(Grms), 15~2000(Hz)/random (compliant with MIL-STD-810G)
Shock	Operation: Acceleration, 50(G)/11(ms)/half sine (compliant with MIL-STD-202G) Non-operation: Acceleration,1,500(G)/0.5(ms)/half sine (compliant with MIL-STD-883K)

Note: This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SV240-25. The prediction result for SV240-25 is more than 3,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

SV240-25 complies with the following standards:

- CE
- FCC
- RoHS
- MIL-STD-810G

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4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

Capacity	Drive Writes Per Day
120 GB	2.28
240 GB	2.2
480 GB	2.27
960 GB	2.28
1920 GB	2.28

Notes:

- This estimation complies with JEDEC JESD-219, enterprise endurance workload of random data with payload size distribution.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024 GB
- DWPD (Drive Write Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 3 years)

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5. Flash Management

5.1 Error Correction/Detection

SV240-25 implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 DataDefender™

Apacer's DataDefender is an advanced technology of power failure management which combines both firmware and hardware mechanisms to ensure data integrity. When power disruption occurs, the low voltage detector will be triggered. When this happens, the SSD's protection mechanism is activated and cuts off data transmission from the host. Once the power supply is resumed, the firmware protection mechanism will ensure the integrity of the firmware as well as the data already written into the NAND flash media.

Note: The controller unit of this product model is designed with a DRAM as a write cache for improved performance and data efficiency. Though unlikely to happen in most cases, the data cached in the volatile DRAM might be potentially affected if a sudden power loss takes place before the cached data is flushed into non-volatile NAND flash memory.

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5.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

5.6 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

5.7 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.8 Device Sleep (DevSleep or DEVSLP) Mode

Device Sleep is a feature that allows SATA devices to enter a low power mode by designating a particular pin as DEVSLP signal with an aim to reducing power consumption.

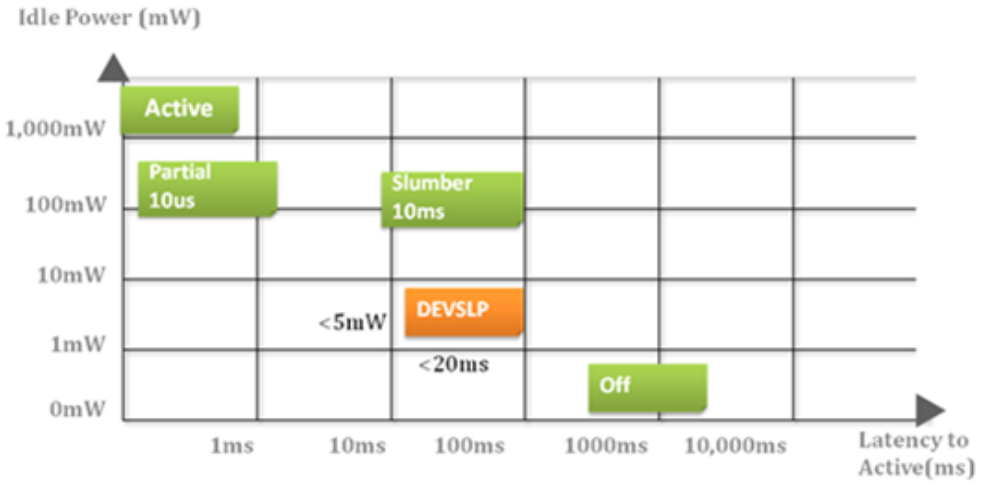

Figure 5-1 Device Sleep

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5.9 SATA Power Management

By complying with SATA 6 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, TX & RX operational
- PARTIAL: Reduces power, resumes in under 10 µs (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.
- Device Sleep (DevSleep or DEVSLP): PHY powered down; power consumption ≦ 5 mW; host assertion time ≦ 10 ms; exit timeout from this state ≦ 20 ms (unless specified otherwise in SATA Identify Device Log).

Note: The behaviors of power management features would depend on host/device settings.

5.10 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

5.11 Over-provisioning

Over-provisioning (OP) is a certain portion of the SSD capacity exclusively for increasing Garbage Collection (GC) efficiency, especially when the SSD is filled to full capacity or performs a heavy mixed-random workload. OP has the advantages of providing extended life expectancy, reliable data integrity, and high sustained write performance.

5.12 DataRAID™

Apacer's DataRAID algorithm applies an additional level of protection and error-checking. Using this algorithm, a certain amount of space is given over to aggregating and resaving the existing parity data used for error checking. So, in the event that data becomes corrupted, the parity data can be compared to the existing uncorrupted data and the content of the corrupted data can be rebuilt.

5.13 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

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6. Security and Reliability Features

6.1 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

6.2 TCG Opal (optional)

Developed by the Trusted Computing Group (TCG), an organization whose members work together to formulate industry standards, Opal is a set of security specifications used for applying hardware-based encryption to storage devices.

Hardware encryption has many advantages. First of all, it transfers the computational load of the encryption process to dedicated processors, reducing the stress on the host system's CPU. In addition, storage devices complying with Opal specifications are self-encryption devices. Opal specifications also feature boot authentication. When the drive is being accessed, the shadow MBR will request the drive password at boot. The drive will only unlock and decrypt if the correct password is supplied. The other feature is LBA-specific permissions. Users are assigned different permissions for LBA ranges created by the device administrator. Each LBA range is password-protected and can only be accessed by users with the correct key to perform permitted actions (read/write/erase).

6.3 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using a designated pin for transmission, storage device owners are able to read temperature data.

6.4 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and ensure data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

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7. Software Interface

7.1 Command Set

This section defines the software requirements and the format of the commands the host sends to SV240-25. Commands are issued to SV240-25 by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

Table 7-1 Command Set

Code	Command	Code	Command
E5h	CHECK POWER MODE	F4h	SECURITY ERASE UNIT
06h	DATA SET MANAGEMENT	F5h	SECURITY FREEZE LOCK
92h	DOWNLOAD MICROCODE	F1h	SECURITY SET PASSWORD
90h	EXECUTE DEVICE DIAGNOSTIC	F2h	SECURITY UNLOCK
E7h	FLUSH CACHE	70h	SEEK
EAh	FLUSH CACHE EXT	EFh	SET FEATURES
ECh	IDENTIFY DEVICE	C6h	SET MULTIPLE MODE
E3h	IDLE	E6h	SLEEP
E1h	IDLE IMMEDIATE	B0h	SMART
91h	INITIALIZE DEVICE PARAMETERS	E2h	STANDBY
E4h	READ BUFFER	E0h	STANDBY IMMEDIATE
C8h	READ DMA	E8h	WRITE BUFFER
25h	READ DMA EXT	CAh	WRITE DMA
60h	READ FPDMA QUEUED	35h	WRITE DMA EXT
C4h	READ MULTIPLE	3Dh	WRITE DMA FUA EXT
29h	READ MULTIPLE EXT	61h	WRITE FPDMA QUEUED
2Fh	READ LOG EXT	3Fh	WRITE LOG EXT
47h	READ LOG DMA EXT	57h	WRITE LOG DMA EXT
20h	READ SECTOR	C5h	WRITE MULTIPLE
24h	READ SECTOR EXT	39h	WRITE MULTIPLE EXT
40h	READ VERIFY SECTORS	CEh	WRITE MULTIPLE FUA EXT
42h	READ VERIFY SECTORS EXT	30h	WRITE SECTOR
10h	RECALIBRATE	34h	WRITE SECTOR EXT
F6h	SECURITY DISABLE PASSWORD	45h	WRITE UNCORRECTABLE EXT
F3h	SECURITY ERASE PREPARE		

Table 7-2 Trusted Computing Feature Set

Code	Command	Code	Command
5Ch	TRUSTED RECEIVE	5Eh	TRUSTED SEND
5Dh	TRUSTED RECEIVE DMA	5Fh	TRUSTED SEND DMA

Note: This feature set is only applicable to products implemented with AES and Opal functions.

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7.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

Table 7-3 SMART Subcommand Set

Code	SMART Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D4h	EXECUTE OFF-LINE IMMEDIATE
D5h	SMART READ LOG
D6h	SMART WRITE LOG
D8h	ENABLE OPERATIONS
D9h	DISABLE OPERATIONS
DAh	RETURN STATUS

Table 7-4 General SMART Attribute Structure

Byte	Description
0	ID (Hex)
1 – 2	Status Flag
3	Value
4	Worst
5*-11	Raw Data

*Byte 5: LSB

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Table 7-5 SMART Attribute ID List

ID (Hex)	Attribute Name
9 (0x09)	Power-on Hours
12 (0x0C)	Power Cycle Count
163 (0xA3)	Maximum Erase Count
164 (0xA4)	Average Erase Count
166 (0xA6)	Total Later Bad Block Count
167 (0xA7)	SSD Protect Mode (Vendor Specific)
168 (0xA8)	SATA PHY Error Count
171 (0xAB)	Program Fail Count
172 (0xAC)	Erase Fail Count
175 (0xAF)	Bad Cluster Table Count
192 (0xC0)	Unexpected Power Loss Count
194 (0xC2)	Temperature
231 (0xE7)	Lifetime Left
241 (0xF1)	Total Sectors of Write

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8. Electrical Specifications

8.1 Operating Voltage

Table 8-1 lists the supply voltage for SV240-25.

Table 8-1 Operating Range

Item	Range
Supply Voltage	5V ± 10%

8.2 Power Consumption

Table 8-2 lists the power consumption for SV240-25.

Table 8-2 Power Consumption

Capacity / Mode	120 GB	240 GB	480 GB	960 GB	1920 GB
Active (mA)	370	395	400	420	430
Idle (mA)	60	60	60	60	60

Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

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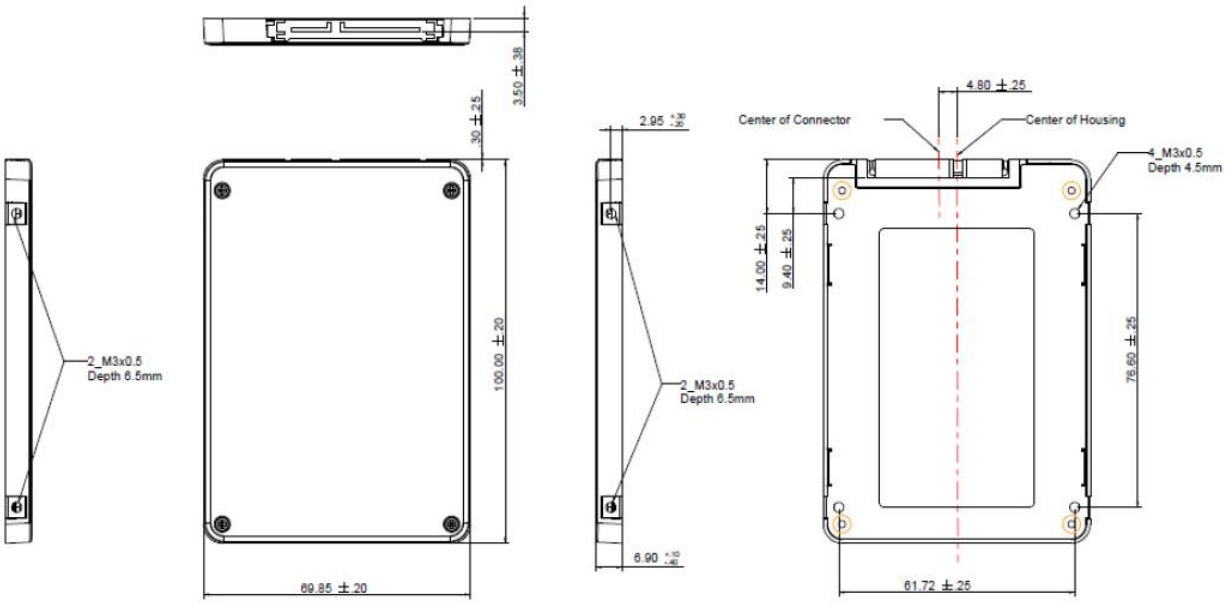
9. Mechanical Specifications

9.1 Dimensions



Unit: mm

Figure 9-1 Physical Dimensions

9.2 Net Weight

Table 9-1 Net Weight

Capacity	Net Weight (g ± 5%)
120GB	59.2
240GB	60.69
480GB	61.89
960GB	62.26
1920GB	63

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10. Product Ordering Information

10.1 Product Code Designations

Apacer's SV240-25 SSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the SV240-25 series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	1	2	.	X	X	5	X	X	C	.	X	X	X	X	X

Code 1-3 (Product Line & Form Factor)	SATA+25
Code 5-6 (Model/Solution)	24: SV240-25 A2 :SV240 with TCG Opal
Code 7-8 (Product Capacity)	5H: 120GB 5J: 240GB 5K: 480GB 5L: 960GB 5M: 1920GB
Code 9 (Flash Type & Product Temp)	G: 3D TLC Standard temperature H: 3D TLC Wide temperature
Code 10 (Product Spec)	2.5" 7mm plastic housing
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	16: Thermal Sensor DEVSLP OP 27: Thermal Sensor with DEVSLP + TCG Opal OP

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10.2 Valid Combinations

The following tables list the available models of the SV240-25 series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

10.2.1 Without TCG Opal

Capacity	Standard Temperature	Wide Temperature
120GB	A12.245HGC.00216	A12.245HHC.00116
240GB	A12.245JGC.00216	A12.245JHC.00116
480GB	A12.245KGC.00216	A12.245KHC.00116
960GB	A12.245LGC.00216	A12.245LHC.00116
1920GB	A12.245MGC.00216	A12.245MHC.00116

10.2.2 With TCG Opal

Capacity	Standard Temperature	Wide Temperature
120GB	A12.A25HGC.00227	A12.A25HHC.00127
240GB	A12.A25JGC.00227	A12.A25JHC.00127
480GB	A12.A25KGC.00227	A12.A25KHC.00127
960GB	A12.A25LGC.00227	A12.A25LHC.00127
1920GB	A12.A25MGC.00227	A12.A25MHC.00127

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Revision History

Revision	Description	Date
1.0	Initial release	1/21/2020
1.1	Modified total bytes at Table 4-1 Capacity Specifications	2/10/2020
1.2	- Updated seq. write speed for 120GB at Table 4-2 Performance Specifications - Updated MTBF from >1,000,000 hours to >3,000,000 hours	3/26/2020
1.3	- Added TCG Opal to the Security section on Specifications Overview page - Updated 1. General Descriptions by adding TCG Opal to the last paragraph - Updated Table 4-1 by changing max LBA to total LBA - Updated the description of 5.2 Bad Block Management - Updated the section title and description for 5.4 Flash Translation Layer – Page Mapping - Updated 7.1 Command Set by adding Table 7-2 - Updated 10. Product Ordering Information	6/30/2020
1.4	- Updated storage temperature from -40-100°C to -55-100°C - Updated Performance, Endurance and Power Consumption on Specifications Overview page - Updated Tables 4-2, 4-4 and 8-5 - Updated 10 Product Ordering Information by changing codes 15-16 for 10.2.1 Without TCG Opal	11/12/2021
1.5	- Updated Performance and Power Consumption on Specifications Overview page - Updated Tables 4-2 and 8-2 - Updated the description of 5.4 DataDefender - Updated 10. Product Ordering Information by adding 10.2.2 With TCG Opal	12/24/2021
1.6	- Updated endurance rating and warranty period at Endurance on Specifications Overview page and 4.4 Endurance - Updated description of pin 4 and pin 11 for Table 3-2 Power Segment	6/15/2022
1.7	Removed UL from 4.5 Certification and Compliance	8/1/2022

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