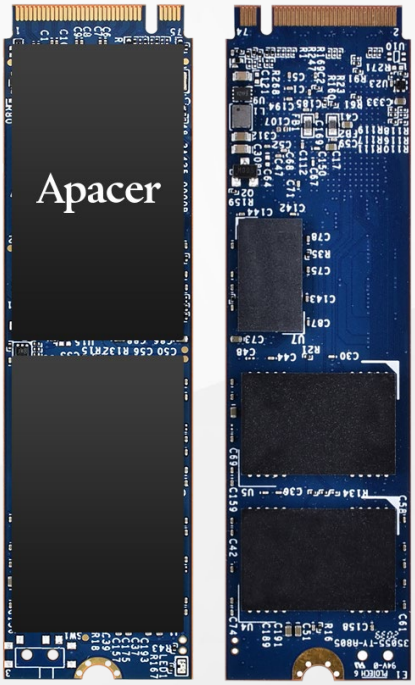
Apacer

RoHS Compliant

PCI Express Flash Drive

Industrial PV210-M280 BiCS5 Product Specifications



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Specifications Overview:

- **PCIe Interface**
  - Compliant with PCI Express 3.1
  - Compliant with NVMe 1.3
  - Compatible with PCIe Gen3 x4 interface
- **Capacity**
  - 120, 240, 480, 960, 1920 GB
- **Performance**[1]
  - Interface burst read/write: 4 GB/sec
  - Sequential read: up to 3,545 MB/sec
  - Sequential write: up to 2,640 MB/sec
  - Random read (4K): up to 631,000 IOPS
  - Random write (4K): up to 531,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - DataDefender™
  - TRIM
  - Hyper Cache Technology
  - Over-provisioning
  - DataRAID™
  - NVMe Secure Erase
- **DRAM Cache for Enhanced Random Performance**
- **NAND Flash Type:** 3D TLC (BiCS5)
- **MTBF:** >3,000,000 hours
- **Endurance (in drive writes per day : DWPD)**
  - 120 GB: 2.06 DWPD
  - 240 GB: 2.12 DWPD
  - 480 GB: 1.89 DWPD
  - 960 GB: 1.85 DWPD
  - 1920 GB: 2 DWPD
- **Temperature Range**
  - Operating (Tc):
    - Standard: 0°C to 70°C
    - Wide: -40°C to 85°C
  - Storage (Ta): -55°C to 100°C
- **Supply Voltage**
  - 3.3V ± 5%
- **Power Consumption**[1]
  - Active mode (Max.): 1,915 mA
  - Idle mode: 250 mA
- **Connector Type**
  - 75-pin M.2 module pinout
- **Power Management**
  - Supports APST
  - Supports ASPM L1.2
- **Security**
  - AES 256-bit hardware encryption
  - Trusted Computing Group (TCG) Opal 2.0 (optional)
- **Reliability**
  - Thermal Sensor
  - Thermal Throttling
  - End-to-End Data Protection
  - CoreGlacier™
  - Sidefill
- **Physical Characteristics**
  - Form factor: Double-sided M.2 2280-D5-M
  - Dimensions: 22.00 x 80.00 x 4.08(max), unit: mm
  - Net weight: 7.48g ± 5%
- **LED Indicators for Drive Behavior**
- **RoHS Compliant**

Note:
1. Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

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1. General Description

Apacer PV210-M280 is the fastest SSD designed as M.2 2280 mechanical dimensions which provides full compliance with PCIe Gen3 x4 interface and NVMe 1.3 specifications, allowing it to operate in power management modes and greatly save on power consumption. Built with a powerful PCIe controller that supports on-the-module ECC as well as efficient wear leveling scheme, PV210-M280 delivers exceptionally low latency and outstanding performance in data transfer. With the compact and high-speed storage, PV210-M280 is the ideal choice for larger, faster hosts deployed in a wide range of applications that require outstanding performance.

Utilizing 3D NAND technology to offer higher capacities of up to 1920GB and providing superior power efficiency compared to 2D NAND, PV210-M280 is equipped with an LDPC (Low Density Parity Check) ECC engine to extend SSD endurance and increase data reliability. Additionally, it features a built-in thermal sensor to monitor SSD temperature via S.M.A.R.T commands and is configured with thermal throttling to dynamically adjust frequency scaling, enhancing data reliability and providing sustained performance under overheating conditions. To ensure normal operation in high-vibration environments and under extreme conditions, PV210-M280 provides Sidefill technology to increase product reliability and resistance to thermal and mechanical stress. The CoreGlacier feature is also available to maintain low temperatures while still enabling high-speed performance. For highly-intensive applications, End-to-End Data Protection ensures data integrity at multiple points in the data transfer path, enabling reliable data delivery.

Security-wise, Advanced Encryption Standard (AES) and Trusted Computing Group (TCG) Opal (optional) ensure data security and provide users with a peace of mind knowing their data is safeguarded against unauthorized use at all times. PV210-M280 also adopts the latest page mapping file translation layer and comes with various implementations including flash block management, DataDefender, TRIM, power saving modes, Hyper Cache technology, over-provisioning, DataRAID, and NVMe secure erase.

With exceptional performance, trustable reliability, and enhanced data protection, PV210-M280 is definitely the ideal storage or cache solution for a variety of applications ranging from industrial, imaging, computing to enterprise markets.

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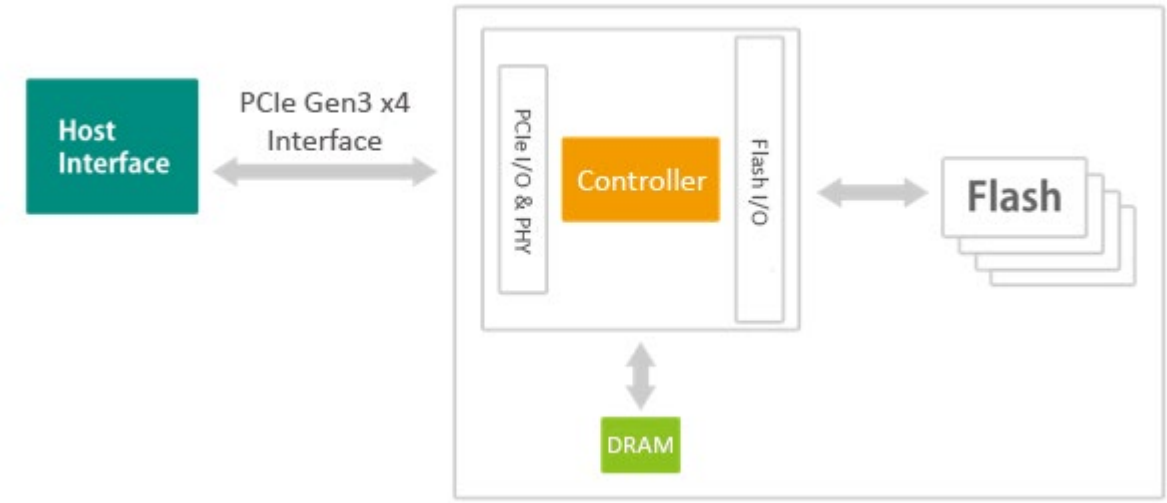
2. Functional Block



Note: The actual number of NAND flash used on Apacer PV210-M280 varies from capacities. The illustration is for reference only.

Figure 2-1 Functional Block Diagram

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3. Pin Assignments

This connector does not support hot plug capability. There are a total of 75 pins. 12 pin locations are used for mechanical key locations; this allows such a module to plug into Key M connectors.

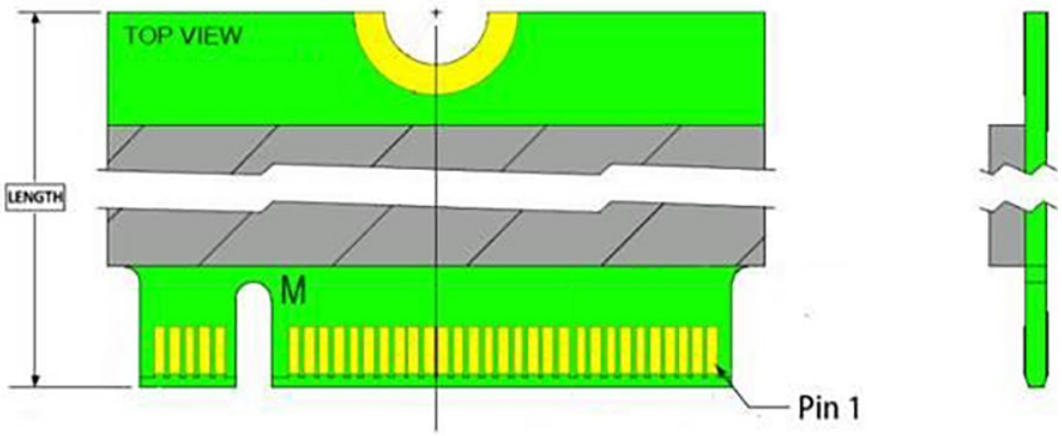

Figure 3-1 Pin Connectors

Table 3-1 Pin Assignments

Pin No.	Type	Description
1	GND	Ground
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	Reserved for Apacer use only[1]
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#(O)	Status indicators via LED devices
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signals defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect

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Table 3-1 Pin Assignments

Pin No.	Type	Description
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	Reserved for Apacer use only[1]
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	Reserved for Apacer use only[1]
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	Reserved for Apacer use only[1]
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK	Reserved for Apacer use only[1]
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA	Reserved for Apacer use only[1]
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#	No connect
45	GND	Ground
46	I2C_CLK	I2C clock; Open Drain with pull up on platform
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	I2C_DATA	I2C Data; Open Drain with pull up on platform
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as specification. defined by the PCIe Mini CEM
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Substates.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) spec. defined by the PCI Express M.2
54	PEWAKE#(I/O)(0/3.3V)	No connect
55	REFCLKp	PCIe Reference Clock signals (100 MHz) spec. defined by the PCI Express M.2
56	Reserved for MFG DATA	Reserved for Apacer use only[1]
57	GND	Ground
58	Reserved for MFG CLOCK	Reserved for Apacer use only[1]
59	Module Key M	Module Key
60	Module Key M	Module Key
61	Module Key M	Module Key

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Table 3-1 Pin Assignments

Pin No.	Type	Description
62	Module Key M	Module Key
63	Module Key M	Module Key
64	Module Key M	Module Key
65	Module Key M	Module Key
66	Module Key M	Module Key
67	N/C	Reserved for Apacer use only[1]
68	SUSCLK(32KHz)(I)(0/3.3V)	No connect
69	PEDET (NC-PCIe)	Host I/F Indication; No connect for PCIe.
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

Note:
1. Reserved by Apacer, please do not connect to a host.

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4. Product Specifications

4.1 Capacity

Capacity specifications of PV210-M280 are available as shown in Table 4-1.

Table 4-1 Capacity Specifications

Capacity	Total bytes	Total LBA
120 GB	120,034,123,776	234,441,648
240 GB	240,057,409,536	468,862,128
480 GB	480,103,981,056	937,703,088
960 GB	960,197,124,096	1,875,385,008
1920 GB	1,920,383,410,176	3,750,748,848

Notes:
- Display of total bytes varies from operating systems.
- 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
- LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of PV210-M280 is listed below in Table 4-2.

Table 4-2 Performance Specifications

Capacity / Performance	120 GB	240 GB	480 GB	960 GB	1920 GB
Sequential Read (MB/s)	1,060	1,240	2,975	3,545	3,505
Sequential Write (MB/s)	525	1,105	2,220	2,500	2,640
4K Random Read (IOPS)	44,000	90,000	179,000	351,000	631,000
4K Random Write (IOPS)	111,000	231,000	435,000	504,000	531,000

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 8.0.4 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 128.

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4.3 Environmental Specifications

Environmental specifications of PV210-M280 are shown in Table 4-3.

Table 4-3 Environmental Specifications

Parameter	Type	Specifications
Temperature	Operating (Tc)	0°C to 70°C (Standard); -40°C to 85°C (Wide)
	Non-operating (Ta)	-55°C to 100°C
Vibration	Operating	7.69 GRMS, 20~2000 Hz/random (compliant with MIL-STD-810G)
	Non-operating	4.02 GRMS, 15~2000 Hz/random (compliant with MIL-STD-810G)
Shock	Operating	Acceleration, 50(G)/11(ms)/half sine (compliant with MIL-STD-202G)
	Non-operating	Acceleration, 1500(G)/0.5(ms)/half sine (compliant with MIL-STD-883K)

Notes:

- This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.
- Tc: case temperature; Ta: ambient temperature. The operating temperature is determined by the case temperature. Adequate airflow is advisable as it enables the device to maintain optimal temperatures, especially in environments with heavy workloads.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in PV210-M280. The prediction result for PV210-M280 is more than 3,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

PV210-M280 complies with the following standards:

- CE
- UKCA
- FCC
- RoHS
- MIL-STD-810G

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4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

Capacity	Drive Writes Per Day
120 GB	2.06
240 GB	2.12
480 GB	1.89
960 GB	1.85
1,920 GB	2

Notes:

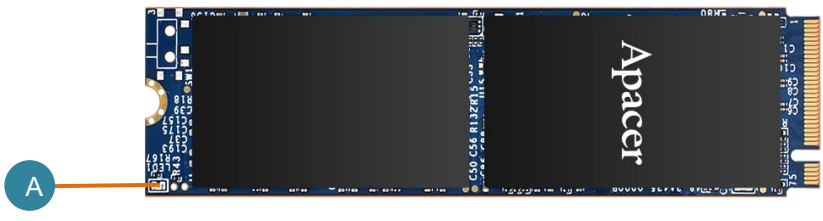
- This estimation complies with JEDEC JESD-219, enterprise endurance workload of random data with payload size distribution.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 3 years)

4.7 LED Indicator Behavior

The behavior of the PV210-M280 LED indicators is described in Table 4-5.

Table 4-5 LED Behavior

Location	LED	Description
LED A	DAS	LED blinks when the drive is being accessed



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5. Flash Management

5.1 Error Correction/Detection

PV210-M280 implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 DataDefender™

Apacer's DataDefender is an advanced technology of power failure management which combines both firmware and hardware mechanisms to ensure data integrity. When power disruption occurs, the low voltage detector will be triggered. When this happens, the SSD's protection mechanism is activated and cuts off data transmission from the host. Once the power supply is resumed, the firmware protection mechanism will ensure the integrity of the firmware as well as the data already written into the NAND flash media.

Note: The controller unit of this product model is designed with a DRAM as a write cache for improved performance and data efficiency. Though unlikely to happen in most cases, the data cached in the volatile DRAM might be potentially affected if a sudden power loss takes place before the cached data is flushed into non-volatile NAND flash memory.

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5.5 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

5.6 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.7 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

5.8 Over-provisioning

Over-provisioning (OP) is a certain portion of the SSD capacity exclusively for increasing Garbage Collection (GC) efficiency, especially when the SSD is filled to full capacity or performs a heavy mixed-random workload. OP has the advantages of providing extended life expectancy, reliable data integrity, and high sustained write performance.

5.9 DataRAID™

Apacer's DataRAID algorithm applies an additional level of protection and error-checking. Using this algorithm, a certain amount of space is given over to aggregating and resaving the existing parity data used for error checking. So, in the event that data becomes corrupted, the parity data can be compared to the existing uncorrupted data and the content of the corrupted data can be rebuilt.

5.10 NVMe Secure Erase

NVMe Secure Erase is an NVMe drive sanitize command currently embedded in most of the storage drives. Defined in NVMe specifications, NVMe Secure Erase is part of Format NVM command that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the NVMe-based storage media currently in the market are built-in with this command. NVMe Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

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6. Security and Reliability Features

6.1 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

6.2 TCG Opal (optional)

Developed by the Trusted Computing Group (TCG), an organization whose members work together to formulate industry standards, Opal is a set of security specifications used for applying hardware-based encryption to storage devices.

Hardware encryption has many advantages. First of all, it transfers the computational load of the encryption process to dedicated processors, reducing the stress on the host system's CPU. In addition, storage devices complying with Opal specifications are self-encryption devices. Opal specifications also feature boot authentication. When the drive is being accessed, the shadow MBR will request the drive password at boot. The drive will only unlock and decrypt if the correct password is supplied. The other feature is LBA-specific permissions. Users are assigned different permissions for LBA ranges created by the device administrator. Each LBA range is password-protected and can only be accessed by users with the correct key to perform permitted actions (read/write/erase).

6.3 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

6.4 Thermal Throttling

Thermal throttling can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device’s temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

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6.5 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and that ensures data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

6.6 CoreGlacier™

In many applications, SSDs are subject to challenging conditions. If the working environment is already hot, and the SSD's operation causes it to increase in temperature as well, the result could be damage to the hardware or corrupted data. In cases like this, leading industrial manufacturers know to turn to Apacer. Apacer developed CoreGlacier, a heatsink that distributes dissipation in isolated components with no thermal diffusion, to prevent heat-related damage from occurring.

6.7 Sidefill

Apacer's sidefill technology strengthens the connections between solder joints and their board, making them more robust and vibration-resistant. It also allows for heat dissipation to offset thermal damage.

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7. Software Interface

7.1 Command Set

Table 7-1 summarizes the commands supported by PV210-M280.

Table 7-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test

Table 7-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

Note: 81h and 82h are only applicable to models with TCG Opal support.

Table 7-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
09h	Dataset Management

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7.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Table 7-4 SMART (02h)

Byte	Length	Description
0	1	Critical Warning
1-2	2	Composite Temperature
3	1	Available Spare
4	1	Available Spare Threshold
5	1	Percentage Used (Average Erase Count / P/E Cycle Count)
6-31	26	Reserved
32-47	16	Data Units Read
48-63	16	Data Units Written
64-79	16	Host Read Commands
80-95	16	Host Write Commands
96-111	16	Controller Busy Time
112-127	16	Power Cycles
128-143	16	Power On Hours
144-159	16	Unsafe Shutdowns
160-175	16	Media and Data Integrity Errors
176-191	16	Number of Error Information Log Entries
192-195	4	Warning Composite Temperature Time
196-199	4	Critical Composite Temperature Time
200-201	2	Temperature Sensor 1: Controller Temperature
202-203	2	Temperature Sensor 2: PCB Temperature
204-205	2	Temperature Sensor 3: NAND Flash Temperature
206-207	2	Temperature Sensor 4
208-209	2	Temperature Sensor 5
210-211	2	Temperature Sensor 6
212-213	2	Temperature Sensor 7
214-215	2	Temperature Sensor 8
216-511	296	Reserved

Note: Temperature display of the Temperature Sensor from 1 to 8 (corresponding bytes from 200 to 215) is not supported if the return value is 0h.

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Table 7-5 SMART (C0h)

Byte	Length	Description
0-255	256	Reserved
256-257	2	SSD Protect Mode
258-261	4	Host Read UNC Count
262-265	4	Reserved
266-269	4	CRC Error Count
270-273	4	Total Early Bad Block Count
274-277	4	Total Later Bad Block Count
278-281	4	Max Erase Count
282-285	4	Average Erase Count
286-289	4	Program Fail Count
290-293	4	Erase Fail Count
294-301	8	Flash Write Sector
302-305	4	Total Spare Block
306-309	4	Current Spare Block
310-313	4	Read Retry Count
314-511	210	Reserved

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8. Electrical Specifications

8.1 Operating Voltage

Table 8-1 lists the supply voltage for PV210-M280.

Table 8-1 Operating Range

Item	Range
Supply Voltage	3.3V ± 5%

8.2 Power Consumption

Table 8-2 lists the power consumption for PV210-M280.

Table 8-2 Power Consumption

Capacity / Mode	Unit	120 GB	240 GB	480 GB	960 GB	1920 GB
Active (Max.)	mA	805	905	1,585	1,700	1,915
Idle		240	240	235	245	250

Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Power consumption is measured using CrystalDiskMark 8.0.4 with file size 1,000MB.

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9. Mechanical Specifications

Table 9-1 Physical Information

Parameter	Unit	120 GB	240 GB	480 GB	960 GB	1920 GB
Length	mm	80.00 ± 0.15				
Width		22.00 ± 0.15				
Height (Max.)		4.08				
Weight	g ± 5%	6.8	7.18	6.9	7.27	7.48

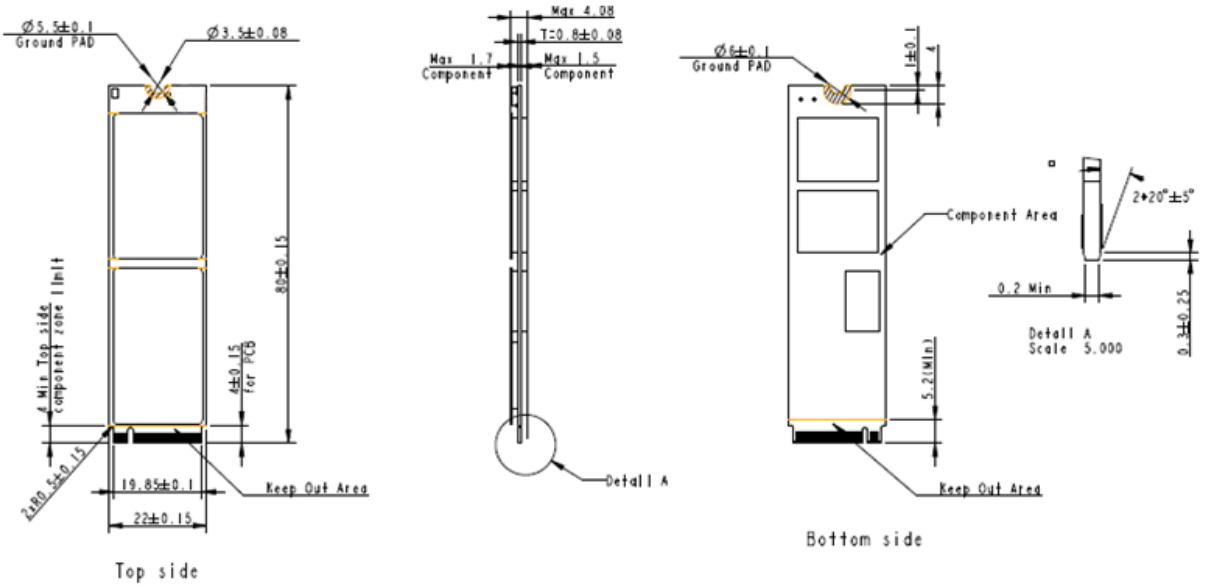

Figure 9-1 Physical Dimensions

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10. Product Ordering Information

10.1 Product Code Designations

Apacer's PV210-M280 SSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the PV210-M280 series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	B	9	2	.	X	3	5	X	X	U	.	X	X	X	X	X

Code 1-3 (Product Line & Form Factor)	PCIe M.2 2280
Code 5-6 (Model/Solution)	93: PV210 A3: PV210 with TCG Opal
Code 7-8 (Product Capacity)	5H: 120GB 5J: 240 GB 5K: 480GB 5L: 960GB 5M: 1920GB
Code 9 (Flash Type & Product Temp)	G: 3D TLC Standard Temperature H: 3D TLC Wide Temperature
Code 10 (Product Spec)	Double-sided M key with graphene
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	15: Thermal Sensor OP 16: Thermal Sensor OP + TCG Opal

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10.2 Valid Combinations

The following tables list the available models of the PV210-M280 series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

10.2.1 Without TCG Opal

Capacity	Standard Temperature	Wide Temperature
120GB	B92.935HGU.00215	B92.935HHU.00315
240GB	B92.935JGU.00415	B92.935JHU.00415
480GB	B92.935KGU.00315	B92.935KHU.00315
960GB	B92.935LGU.00315	B92.935LHU.00315
1920GB	B92.935MGU.00315	B92.935MHU.00315

10.2.2 With TCG Opal

Capacity	Standard Temperature	Wide Temperature
120GB	B92.A35HGU.00116	B92.A35HHU.00116
240GB	B92.A35JGU.00316	B92.A35JHU.00316
480GB	B92.A35KGU.00316	B92.A35KHU.00316
960GB	B92.A35LGU.00316	B92.A35LHU.00316
1920GB	B92.A35MGU.00316	B92.A35MHU.00316

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Revision History

Revision	Description	Date
0.1	Preliminary release	4/19/2022
1.0	Official release	4/26/2022
1.1	- Added DataDefender and TCG Opal support - Updated Table 3-1 by changing the description of pins 30, 56, 58 and 67 - Updated warranty period at the notes for 4.4 Endurance - Updated Table 7-2 by adding opcodes 81h and 82h - Updated 10. Product Ordering Information by adding A3 to code 5-6 and 09 to code 15-16	6/29/2022
1.2	Updated endurance rating on Specifications Overview page and Table 4-4	7/1/2022
1.3	- Added wide temp support - Added a note to Table 7-2 - Modified 9.1 and 9.2 by removing the WP switch - Updated 10. Product Ordering Information due to firmware change	10/27/2022
1.4	- Added rear view of the product to the cover page - Added Sidefill support	9/26/2023
1.5	- Added 120GB and 240GB support - Updated Table 3-1 by changing the description of pins 6, 28, 36, 40, and 42 to “Reserved for Apacer use only” and that of pins 54 and 68 to “No connect” - Updated Performance, Endurance, and Power Consumption on Specifications Overview page and Table 4-2, 4-4, and 8-2 - Removed the Write Zeroes command from Table 7-3 - Updated 10. Product Ordering Information due to firmware change	1/11/2024
1.6	- Removed double-sided dimensions from Physical Characteristics on Specifications Overview page and 9. Mechanical Specifications - Added a note regarding temperature to Table 4-3 - Removed PCB Sensor from the description of byte 1-2 at Table 7-4	3/26/2024

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