ATP NVMe PCIe Gen3x4 pSLC

M.2 2230 SSD

N700Sc Series

Datasheet

Version 1.1

P/N
AF40GSAJB-DBAXX
AF80GSAJB-DBAXX
AF160GSAJB-DBAXX

ATP NVMe Gen3x4 pSLC M.2 2230 SSD

Product Specification

- Capacities:
  - 40GB, 80GB, 160GB
- Form Factors:
  - M.2 2230-S4-M
- Thickness:
  - Up to 2.5mm
- Weight:
  - <10 grams
- PCIe Gen3 x4 performance
  - Sequential Read: Up to 2,000MB/s
  - Sequential Write: Up to 1,600MB/s
- Read and Write IOPS (QD32, HMB)
  - Random 4K Reads: Up to 135,600 IOPS
  - Random 4K Writes: Up to 112,000 IOPS
- LDPC (Low Density Parity Check) ECC algorithm
- End-to-End Data Path Protection
- AES 256-bit Encryption, TCG OPAL 2.0
- Compliant with PCI Express Specification Rev.3.1a
- Compliant with PCIe M.2 Specification V1.1
- Compliant with NVM Express Specification Rev.1.3c
- Configured Full User Capacity in SLC mode
- Support
  - SMART command set support
  - TRIM command
  - Global wear-leveling
  - Thermal throttling mechanism
- GPIO Features
  - Power Loss Protection by Notification (PLN#/PLA#)
  - Hardware Write Protect
  - Hardware Quick Erase[1]
- Support Host Memory Buffer (HMB)
- Power
  - 3.3V Input Power
- Temperature, Case (T_C)
  - Consumer: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Storage (T-ambient): -40°C to 85°C
- Reliability
  - MTBF (Mean Time Between Failure): > 1,500,000 hours
  - Shock (operating): Half Sine 1,500G /0.5ms
  - Vibration (operating): Sine 16.4G /10~2000Hz
  - Data Retention (@30°C): 5 Years (with 10% P/E Cycles)
- Endurance (TBW in Sequential Write)
  - 40GB: 1,070 TB
  - 80GB: 2,140 TB
  - 160GB: 4,280 TB
- Certifications and Declarations
  - CE
  - FCC
  - BSMI
  - UKCA
- Product Ecological Compliance
  - RoHS
  - REACH

Note:

1. Host needs to guarantee power supply until all Erase operations are completed. By project support Secure Sanitize, compliant with USA Airforce AFSSI-5020
2. Case temperature, the device temperature as indicated by SMART temperature attribute (Composite Temperatur

ATP Confidential © ATP Electronics, Inc.

CONTENT

Disclaimer ***1***

Revision History ***2***

1.0 Product Specification ***3***

1.1 Product Image *3*

1.2 Capacity *3*

1.3 Environment Specifications *4*

1.4 Reliability *4*

1.5 Electrical Characteristics *5*

1.6 Drive Performance *6*

1.7 Write/Erase Endurance[1] *6*

2.0 Product Overview ***7***

2.1 Block Diagram *7*

2.2 Auto- Refresh Technology *7*

2.3 Power Loss Notification *8*

2.4 Enhanced Mode (SLC Mode) Pre-Configured to Enhanced Reliability *8*

2.5 End-to-End Data Path Protection Technology *9*

2.6 FFU – Field Firmware Update *9*

2.7 Dynamic Power Management *9*

2.8 Host Memory Buffer (HMB) (Optional) *10*

2.9 Hardware Write Protect *10*

2.10 Hardware Quick Erase *10*

2.11 AES-256 Encryption and TCG-Opal 2.0 ..... *11*

3.0 Mechanical Dimension & NVMe SSD Pin Assignment ***12***

3.1 Mechanical Form Factor (Units in mm) *12*

3.2 Pin Location *12*

3.3 Pin Assignment *13*

4.0 NVMe Command Sets (Preliminary) ***15***

4.1 Opcode Codes for Admin Commands *15*

4.2. Opcode for NVMe Commands *15*

4.3. Advanced of Admin Commands (Get Log Page) *16*

4.4. Advanced of Admin Commands (Get/Set Features) *16*

4.5. SMART/Health Information (Preliminary) *17*

5.0 Part Number Decoder ***19***

6.0 Certification and Declarations ***20***

Disclaimer

ATP Electronics Inc. shall not be liable for any errors or omissions that may appear in this document and disclaims responsibility for any consequences resulting from the use of the information set forth herein.

ATP may make changes to specifications and product descriptions at any time, without notice. The information in this paper is furnished for informational use only so ATP assumes no responsibility or liability for any errors or inaccuracies that may appear in this document.

All parts of the ATP documentation are protected by copyright law and all rights are reserved. This documentation may not, in whole or in part, be copied, photocopied, reproduced, translated, or reduced to any electronic medium or machine-readable form without prior consent, in writing, from ATP Electronics, Inc.

Notwithstanding any clause of this Agreement, Supplier are not warranted and liable for use any Product in developing, or for incorporation into, products or services used in applications or environments requiring failsafe performance, such as in the operation of nuclear facilities, aircraft navigation or air traffic control, life support machines, surgically implanted devices, weapons systems, or other applications, devices or systems in which the failure of Product could lead directly to death, personal injury, or severe physical or environmental damage.

The information set forth in this document is considered to be “Proprietary” and “Confidential” property owned by ATP.

© Copyright ATP all rights reserved.

Revision History

Date	Version	Changes compared to previous issue
April 20th, 2022	1.0	- First Release for 40GB, 80GB, 160GB
May 25th, 2022	1.1	- Update product marketing naming to N700Sc Series

ATP Confidential © ATP Electronics, Inc.

1.0 Product Specification

1.1 Product Image



Figure 1-1: ATP Product Image (For Reference)

1.2 Capacity

Table 1-2: Capacity Settings

Capacity	LBA
40GB	78,161,328
80GB	156,301,488
160GB	312,581,808

Note:

1. Sector size is 512 bytes
2. LBA counts are based on IDEMA (LBA1-03) standard

ATP Confidential © ATP Electronics, Inc.

1.3 Environment Specifications

Table 1-3-1: Environment Specification

Type		Standard
Temperature, Case (T_C)[1]	Operating (XX)	0°C to 70°C
	Operating (IX)	-40°C to 85°C
	Non-Operating	-40°C to 85°C
Airflow[2,3,4]	Operating	600 LFM @ Max. T_C
Rate of Temp. Change	Operating	1~2°C / minute
Relative Humidity	Operating	8% to 95%, noncondensing
	Non-Operating	8% to 93%, noncondensing
Vibration	Operating	Sine 16.4G, 10~2000Hz
Shock	Operating	Half sine 1500G/0.5ms

1. Case temperature, the composite temperature as indicated by SMART temperature attribute. (ID:2)
2. Sufficient airflow is recommended for 100% sequential writes as the SSD approaches the case temperature in effort to maintain best performance. In the case the SSD temperature exceeds the assigned case temp, the SSD will throttle the performance to mitigate thermal challenges.
3. Airflow is measured upstream of the drive and flows parallel to and through any cooling fins.
4. For more information, please contact your local ATP representative.

1.4 Reliability

Table1-4: Reliability

Type	Value
MTBF (@ 25°C) [1]	>1,500,000 hours
Data Retention (@ 30°C)[2]	5 years (with 10% P/E cycle)

Notes:

1. The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Telcordia SR-332, which based on reliability data of the individual components in drive. It assumes nominal voltage, with all other parameters within specified range.
2. Data retention value may vary across different temperature range and is experimental result to be used for reference.

ATP Confidential © ATP Electronics, Inc.

1.5 Electrical Characteristics

Table 1-5-1: Power Consumption (Power Rail Sum)

Condition	Power Consumption [1,4]			Unit
	40 GB	80 GB	160 GB	
NVMe Power State 0				
Active Writes[2]	2150	2150	2200	mW
Active Reads[2]	2100	2150	2150	mW
Idle/Suspend	<100	<135	<615	mW
Slumber/Sleep[3]				
NVMe Power State 1: Light Throttle	<85	<85	<355	mW
NVMe Power State 2: Heavy Throttle	<80	<80	<190	mW
NVMe Power State 3: Slumber	<20	<20	<20	mW
NVMe Power State 4: Sleep	<5	<5	<5	mW

Notes:
1) PWR_1 = 3.3V; PWR_2 = 1.2V; PWR_3 = 0.9V; T_a = +25°C
2) Active powers are measured on sequential write and read
3) Power states 3 and 4, the PCIe state is set to L1.2 link state.
4) Above measurements are average RMS current consumptions over a defined period. Not 100% tested.

ATP Confidential © ATP Electronics, Inc.

1.6 Drive Performance

Table 1-6: Drive Performance

Validation Item	Typical Value (up to)			Unit
	40 GB	80 GB	160 GB	
HMB On/Off - Fresh Out of Box				
Sequential Write	570	1100	1600	MB/s
Sequential Read	1800	2000	2000	MB/s
HMB On/Off – Steady State				
Sequential Write	570	1100	1600	MB/s
Sequential Read	1800	2000	2000	MB/s
HMB On				
Random Write (QD=32, Thread=1)	107K	107K	112K	IOPS
Random Read (QD=32, Thread=1)	107K	135K	135K	IOPS
HMB Off				
Random Write (QD=1, Thread=1)	35K	45K	45K	IOPS
Random Read (QD=1, Thread=1)	10K	10K	10K	IOPS

Notes:
1) Drive write cache enabled.
2) NVMe power state 0.
3) 4KB transfers can be further improved with the support of HMB by the host.
4) Actual performance may vary depending on use conditions, system variations and environment.
5) Sequential performance measured using CDM 5.1.2 on Windows 10 64-bit (128KB data size, QD=32 by Thread=1 (Total QD=32)).
6) Random performance measured using Iometer on Windows 10 64bit (4KB data size. QD=32 by Thread 1 (Total QD=32), QD=1 by Thread 1 (Total QD=1))
7) Airflow 600 LFM @ Max. Tcase

1.7 Write/Erase Endurance[1]

Table 1-7: TBW

Capacity	Random write[2]	Sequential write[3]
40GB	155 TB	1,070 TB
80GB	310 TB	2,140 TB
160GB	620 TB	4,280 TB

1. Endurance can be predicted based on the usage conditions applied to the device, the internal NAND component cycles, the write amplification factor, and the wear leveling efficiency of the drive. TBW may vary depending on application, please contact ATP for TCO evaluation if specific usage type applies.
2. The random endurance calculation is based on JESD219A Enterprise workload. ,
3. The sequential write endurance calculation is based on pure sequential write at 128K transfer size to run in 4K alignment test pattern

ATP Confidential © ATP Electronics, Inc.

2.0 Product Overview

2.1 Block Diagram

ATP SSD consists of below functional blocks. The advanced architecture is optimized to provide highest data reliability and transfer performance.

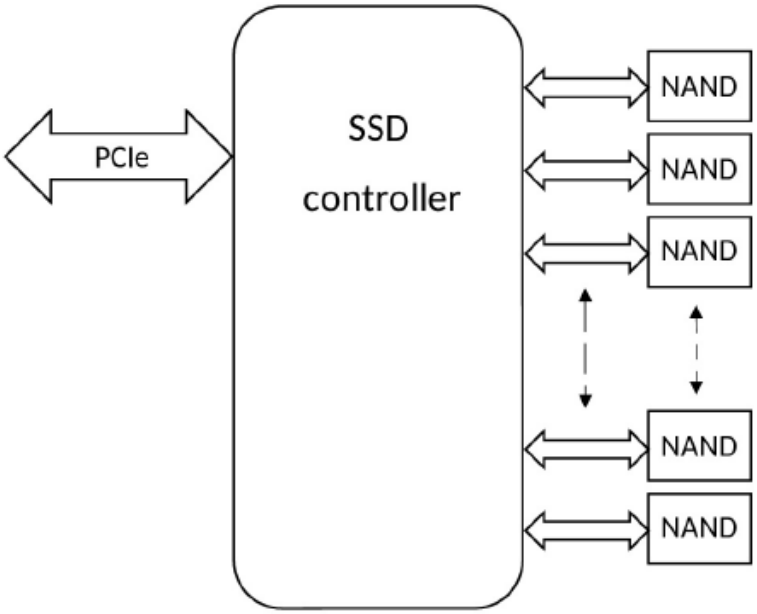


Figure 2-1: Block diagram for ATP NVMe SSD

2.2 Auto- Refresh Technology

AutoRefresh Technology improves the data integrity of read-only areas by monitoring the error bit level and read counts in every read operation.

AutoRefresh Technology detects when the read count is about to exceed the threshold. Before the limit is reached, data in the affected block is copied to a healthy block, thus preventing the controller from reading blocks with too many error bits. With this technology, the ATP NVMe pSLC M.2 2230 SSD performs reliably and prevents uncorrectable data damage.

ATP Confidential © ATP Electronics, Inc.

2.3 Power Loss Notification

For stand-alone applications, managing unstable power is crucial to maintaining data integrity, especially for small form factor storage devices like M.2 SSDs, which have limited space to implement a hardware-based power protection solution.

Following NVMe specifications, ATP pSLC M.2 2230 SSD supports two signals: Power Loss Notification and Power Loss Acknowledge. Power Loss Notification is triggered by the host. When it detects any power loss event, it will inform the device to flush all data in temporary memory to the ATP pSLC M.2 2230 SSD. By completing the flushing process, ATP pSLC M.2 2230 SSD can ensure that data is safely stored even when power is no longer available. After the device completes the process, it will send a response to the host, and the host can then safely shut down or re-boot the system.

2.4 Enhanced Mode (SLC Mode) Pre-Configured to Enhanced Reliability

Single-level cell (SLC) mode, also commonly known as pseudo-SLC (pSLC), is a method of using multi-level cell (MLC), triple-level cell (TLC) and quad-level cell (QLC) NAND flash in a way that reduces the number of bits stored in each cell to one. Reducing the number of stored bits in each cell to one increases the reliability and lifetime of the NAND flash memory, while benefiting from the lower cost of the newer technology.

As a result, although the SLC mode reduces the capacity of MLC memory by 50%, the capacity of TLC by 66.6% and the capacity of QLC flash by 75%, it still achieves a lower cost per bit than SLC because of the higher cell density. It improves the performance, reliability and endurance of the newer technologies to something closer to that of SLC. Implementing the SLC mode effectively requires a high-quality SSD management optimized for the specific flash memory used, in order to provide the highest performance and most reliable data storage.

ATP Confidential © ATP Electronics, Inc.

2.5 End-to-End Data Path Protection Technology

End-to-end data path protection provides error control throughout the entire data transfer path from the host system to the SSD and vice versa, thus ensuring data integrity and reliable data transfers.

ATP's NVMe pSLC M.2 2230 SSD employs a data protection technology called SRAM Soft Error Detector and Recovery mechanism. SRAM soft errors randomly corrupt memory bits and alter stored data but do not cause physical damage to the memory or storage device. These errors can significantly jeopardize data accuracy because they cannot be detected nor solved by ECC engines. The SRAM Soft Error Detector monitors and detects such error risks. As soon as an SRAM error is detected, SRAM Soft Error Recovery then attempts to correct the error according to the SSD's capability. SRAM Soft Error Detector and Recovery can ensure better system stability, high levels of data integrity and optimal device endurance.

The SRAM Soft Error Detector and Recovery mechanism of the ATP NVMe pSLC M.2 2230 SSD is better compared with the previous, as it does not only detect up to 2-bit errors, but it can also correct 1-bit errors.

2.6 FFU – Field Firmware Update

The Field Firmware Update feature offers a simplified and secure method of ensuring the ATP elms is running the latest firmware to address bugs and enable new features when they are available. With this feature, a new version of the firmware may be downloaded and installed to ATP NVMe pSLC M.2 2230 storage product for better performance and stronger reliability.

Please refer to the ATP Application Note for detailed steps on how to use this feature.

2.7 Dynamic Power Management

Reducing energy consumption not only saves cost but also makes the storage device work longer. ATP's Dynamic Power Management (DPM) technology effectively lowers power consumption without significantly degrading performance.

Featuring NVMe Revision 1.3 Power States, and ATP's enhanced DPM technology, the ATP SSD enters different power stages more effectively to balance performance, power consumption compared with other solutions for better cost benefits and longer drive operation.

ATP Confidential © ATP Electronics, Inc.

2.8 Host Memory Buffer (HMB) (Optional)

Host Memory Buffer (HMB) is a key feature of NVMe. It allows the host driver to allocate a portion of the system memory (DRAM) for the exclusive use of the SSD as cache for address mapping information and/or user data. With HMB, SSDs can overcome the limited memory capacity within the storage and thus optimize I/O performance without requiring the SSD to bring up its own DRAM. HMB also helps DRAM-less SSDs improve performance by obtaining DRAM resources as cache. Although accessing the system memory over PCIe is still slower than accessing the onboard DRAM, it is still faster than reading from the flash storage.

2.9 Hardware Write Protect

To protect data that is already stored in the ATP NVMe pSLC M.2 2230 SSD, users can enable the hardware protect feature by putting a jumper on specific pins on the general input/output pin (GPIO). When hardware write protect is enabled, the storage device enters “Read Only” mode and no further data can be written to it.

Please refer to the technical user documentation that came with the ATP NVMe pSLC M.2 2230 SSD for information on the GPIO location and pinout assignments as well as detailed instructions on how to enable the hardware write protect feature.

2.10 Hardware Quick Erase

For specific applications, the host can use the GPIO connector to trigger an “erase data” activity. When this feature is activated, all data in the SSD will be erased automatically and cannot be recovered anymore. This feature is particularly useful if the SSD will be repurposed or disposed of. To make sure that sensitive data is permanently and securely erased, and to ensure that no unauthorized person can retrieve stored data, users can enable the hardware Quick Erase feature. To safely execute this feature and complete the erase process, the host needs to supply enough power to the SSD; otherwise, it might result in an unpredictable status, and cause the drive to re-initialize.

ATP Confidential © ATP Electronics, Inc.

2.11 AES-256 Encryption and TCG-Opal 2.0

Depending on project support, ATP NVMe pSLC M.2 2230 SSD features AES-256 encryption and comply with TCG Opal 2.0.

AES-256

ATP NVMe pSLC M.2 2230 SSD features AES-256 safeguard data against unauthorized access. Advanced Encryption Standard (AES) is the first and only publicly accessible cipher approved by the US National Security Agency (NSA) for protecting top secret information. AES-256, which has a key length of 256 bits, supports the largest bit size and is practically unbreakable by brute force based on current computing power, making it the strongest encryption standard.

TCG Opal 2.0

TCG Opal Security Subsystem Class (SSC) is a set of specifications for self-encrypting drives (SEDs) developed by the Trusted Computing Group (TCG), a non-profit organization that develops, defines, and promotes open standards and specifications for secure computing.

The Opal SSC, currently available in version 2.0, presents a hierarchy of security management standards to secure data from theft and tampering by unauthorized persons who are able to gain access to the storage device or host system where the storage device resides. Storage devices supporting Opal 2.0 use hardware encryption technology to secure data stored in them. By encrypting the entire drive, users do not have to worry about their data being accessed if the drive, laptop or mobile device gets stolen or lost.

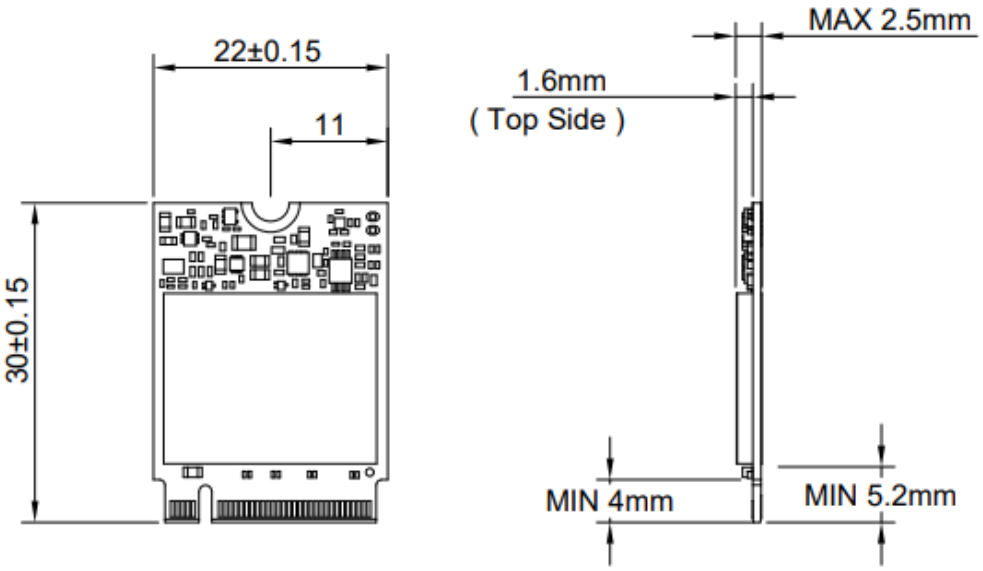
ATP Confidential © ATP Electronics, Inc.

3.0 Mechanical Dimension & NVMe SSD Pin Assignment

3.1 Mechanical Form Factor (Units in mm)

Table 3.1: Mechanical Dimension

Type		Value
M.2 2230-S4-M	Length	30 mm +/- 0.15
	Width	22 mm +/- 0.15
	Thickness	2.5 mm (MAX)

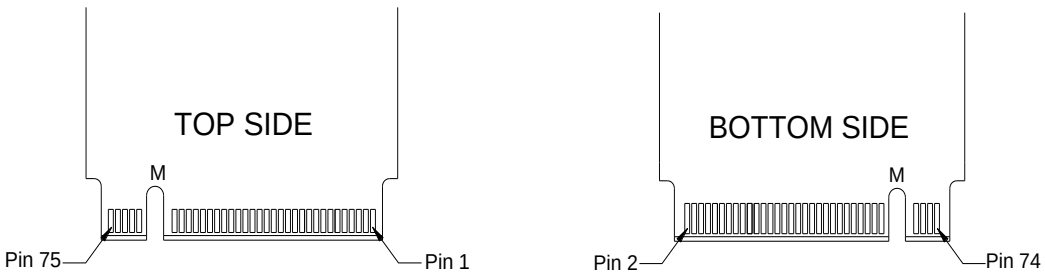


model drawing

3.2 Pin Location

The following figure shows the pin location of the M.2 Embedded SSD, the golden finger is with both signal and power segments.

Figure 3-2



ATP Confidential © ATP Electronics, Inc.

3.3 Pin Assignment

Pin assignment in show in Table 3-1 below.

Table 3-1

Pin No.	Function	Description	Pin No.	Function	Description
1	GND	Ground	2	3.3V	3.3 V Source
3	GND	Ground	4	3.3V	3.3 V Source
5	PETn3	PCIe 3 Transmit(-)	6	N/C	No Connect
7	PETp3	PCIe 3Transmit(+)	8	N/C	No Connect
9	GND	Ground	10	LED1# (O)	LED
11	PERn3	PCIe 3 Receive(-)	12	3.3V	3.3 V Source
13	PERp3	PCIe 3 Receive(+)	14	3.3V	3.3 V Source
15	GND	Ground	16	3.3V	3.3 V Source
17	PETn2	PCIe 2 Transmit(-)	18	3.3V	3.3 V Source
19	PETp2	PCIe 2Transmit(+)	20	N/C	No Connect
21	GND	Ground	22	N/C	No Connect
23	PERn2	PCIe 2 Receive(-)	24	N/C	No Connect
25	PERp2	PCIe 2 Receive(+)	26	N/C	No Connect
27	GND	Ground	28	N/C	Force ROM
29	PETn1	PCIe 1 Transmit(-)	30	N/C	No Connect
31	PETp1	PCIe 1Transmit(+)	32	N/C	No Connect
33	GND	Ground	34	N/C	No Connect
35	PERn1	PCIe 1 Receive(-)	36	N/C	No Connect
37	PERp1	PCIe 1 Receive(+)	38	N/C	No Connect
39	GND	Ground	40	SMB_CLK(I/O)	No Connect
41	PETn0	PCIe 0 Transmit(-)	42	SMB_DATA(I/O)	No Connect
43	PETp0	PCIe 0 Transmit(+)	44	ALERT# (O)	Reserved No Connect
45	GND	Ground	46	N/C	No Connect
47	PERn0	PCIe 0 Receive(-)	48	N/C	No Connect
49	PERp0	PCIe 0 Receive(+)	50	PERST# (I) 3.3V	PCIe Reset
51	GND	Ground	52	CLKREQ# (I/O) (0/3.3V)	Clock Request
53	REFCLKn	REFCLKn	54	PEWAKE# (I/O) (0/3.3V)	Reserved No Connect
55	REFCLKp	REFCLKp	56	Reserved for MFG_DATA	UART_RX
57	GND	Ground	58	Reserved for	UART_TX

ATP Confidential © ATP Electronics, Inc.

Pin No.	Function	Description	Pin No.	Function	Description
				MFG_CLOCK	
Module Key			Module Key		
67	N/C	No Connect	68	SUSCLK(32kHz) (I) (0/3.3V)	No Connect
69	NC-PCIe	Reserved No Connect	70	3.3V	3.3V Source
71	GND	Ground	72	3.3V	3.3V Source
73	GND	Ground	74	3.3V	3.3V Source
75	GND	Ground			

ATP Confidential © ATP Electronics, Inc.

4.0 NVMe Command Sets (Preliminary)

4.1 Opcode Codes for Admin Commands

Table 4-1: Opcode Codes for Admin Commands:

Opcode	Optional/Mandatory	Command
00h	M	Delete I/O Submission Queue
01h	M	Create I/O Submission Queue
02h	M	Get Log Page
04h	M	Delete I/O Completion Queue
05h	M	Create I/O Completion Queue
06h	M	Identify
08h	M	Abort
09h	M	Set Feature
0Ah	M	Get Feature
0Ch	M	Asynchronous Event Request
10h	O	Firmware Commit
11h	O	Firmware Image Download
14h	O	Device Self-test
NVM Command Set Specific		
80h	O	Format NVM
81h	O	Security Send
82h	O	Security Receive
84h	O	Sanitize

4.2. Opcode for NVMe Commands

Table 4-2: Opcode Codes for NVMe Commands:

Opcode	Optional/Mandatory	Command
00h	M	Flush
01h	M	Write
02h	M	Read
04h	O	Write Uncorrectable
05h	O	Compare
08h	O	Write Zeros
09h	O	Dataset Management

ATP Confidential © ATP Electronics, Inc.

4.3. Advanced of Admin Commands (Get Log Page)

Table 4-3: Get Log page

Opcode	Optional/Mandatory	Command
01h	M	Error Information
02h	M	SMART/Health Information
03h	M	Firmware Slot Information
05h	O	Command Effects Log
06h	O	Device Self-test
07h	O	Telemetry Host-Initiated
08h	O	Telemetry Controller-Initiated

4.4. Advanced of Admin Commands (Get/Set Features)

Table 4-4: Get/Set Features

Opcode	Optional/Mandatory	Command
01h	M	Arbitration
02h	M	Power Management
03h	O	LBA Range Type
04h	M	Temperature Threshold
05h	M	Error Recovery
06h	O	Volatile Write Cache
07h	M	Number of Queues
08h	M	Interrupt Coalescing
09h	M	Interrupt Vector Configuration
0Ah	M	Write Atomicity Normal
0Bh	M	Asynchronous Event Configuration
0Ch	O	Autonomous Power State Transition
0Dh	O	Set Host Memory Buffer
10h	O	Host Controlled Thermal Management
11h	O	Non-Operational Power State Configuration
NVM Command Set Specific		
80h	O	Software Progress Marker

ATP Confidential © ATP Electronics, Inc.

4.5. SMART/Health Information (Preliminary)

Table 4-5: SMART Attribute

Byte Address	Length	Attribute Name
0	1	Critical Warning Bit 7:5 – Reserved Bit 4 – 1h: the volatile memory backup device has failed. (only valid if the controller has a volatile memory backup solution) Bit 3 – 1h: the media has been placed in read only mode Bit 2 – 1h: the NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability Bit 1 – 1h: a temperature is above an over temperature threshold or below
2:1	2	Composite Temperature
3	1	Available Spare
4	1	Available Spare Threshold
5	1	Percentage Used
31:6	26	Reserved
47:32	16	Data Units Read
63:48	16	Data Units Written
79:64	16	Host Read Commands
95:80	16	Host Write Commands
111:96	16	Controller Busy Time
127:112	16	Power Cycles
143:128	16	Power On Hours
159:144	16	Unsafe Shutdowns
175:160	16	Media and Data Integrity Errors
191:176	16	Number of Error Information Log Entries
195:192	4	Warning Composite Temperature Time
199:196	4	Critical Composite Temperature Time
201:200	2	Device Temperature
203:202	2	Controller Temperature
219:216	4	Thermal Management Temperature 1 Transition Count
223:220	4	Thermal Management Temperature 2 Transition Count
227:224	4	Total Time for Thermal Management Temperature 1
231:228	4	Total Time for Thermal Management Temperature 2

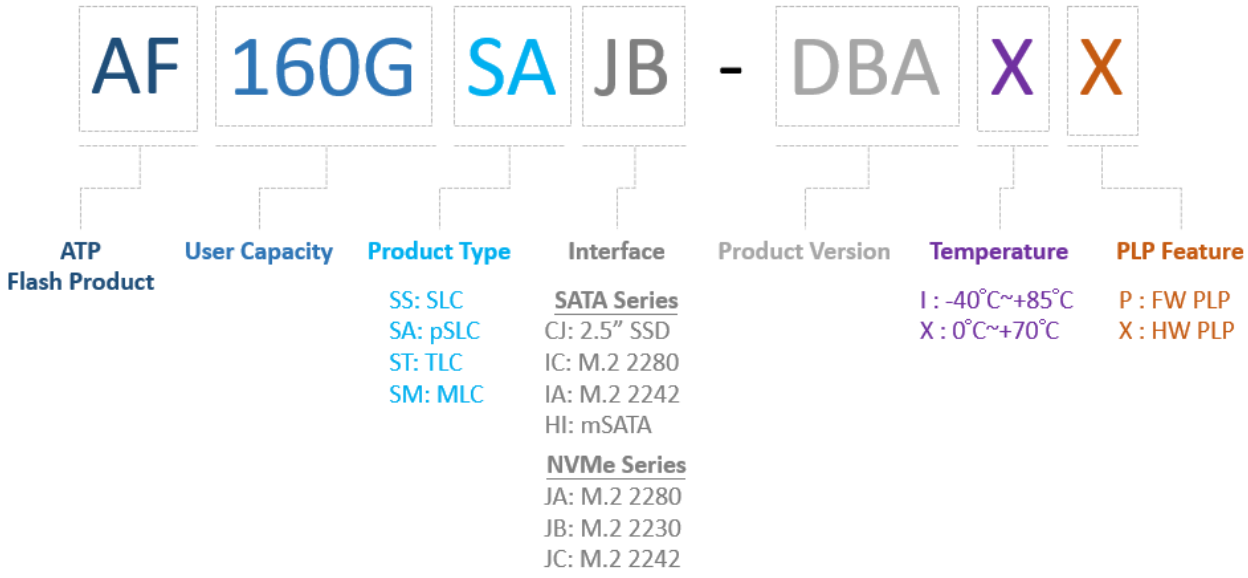
ATP Confidential © ATP Electronics, Inc.

Byte Address	Length	Attribute Name
233:232	2	Reallocated Flash Blocks Count
235:234	2	Initial Spare Blocks
239:236	4	Uncorrectable Sector Count
243:240	4	Total Block Program Failure
247:244	4	Reported Uncorrectable Errors
251:248	4	Hardware ECC Recovered
255:252	4	Current Pending Block Count
259:256	4	Offline Surface Scan
263:260	4	Total Block Erase Failure
267:264	4	Maximum Erase Count
271:268	4	Average Erase Count
279:272	8	Total Erase Count
287:280	8	Total Sectors Read from NAND Flash
295:288	8	Total Host Sectors Written to Device
303:296	8	Total NAND Sectors Written to NAND Flash
311:304	8	Total Host Sectors Read from Device
315:312	4	CRC Error
319:316	4	Raw Read Error Count
320	1	Thermal Throttle Stage

ATP Confidential © ATP Electronics, Inc.

5.0 Part Number Decoder

Standard Part Number



(Only for reference)

OEM Part Number



(Only for reference)

ATP Confidential © ATP Electronics, Inc.

6.0 Certification and Declarations

Certification	Mark	Description
CE compliant		The CE marking (also known as CE mark) is a mandatory conformance mark on many products placed on the single market in the European Economic Area (EEA). The CE marking certifies that a product has met EU consumer safety, health or environmental requirements. CE stands for Conformité Européenne, "European conformity" in French.
FCC		FCC Part 15 Class B was used for Evolution of United States (US) Emission Standards for Commercial Electronic Products, The United States (US) covers all types of unintentional radiators under Subparts A and B (Sections 15.1 through 15.199) of FCC 47 CFR Part 15, usually called just FCC Part 15
BSMI compliant		BSMI logo signifies the product is compliant with Taiwan EMC standard for CNS13438.
UKCA		The UKCA (UK Conformity Assessed) marking is a new UK product mark for the products that conforms to the CE marking and sold in Great Britain, which is effective from 1st of January 2021.
RoHS	-	Compliant with the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EU)
REACH	-	Compliant with REACH (Registration, Evaluation, Authorization and Restriction of Chemicals which is an EU Regulation that came into force on 1 June 2007

ATP TAIWAN (HQ)
TEL: +886-2-2659-6368
FAX: +886-2-2659-4982
sales-apac@atpinc.com

ATP USA
TEL: +1-408-732-5000
FAX: +1-408-732-5055
sales@atpinc.com

ATP JAPAN
TEL: +81-3-6890-8277
FAX: +81-3-6890-8301
sales-japan@atpinc.com

ATP EUROPE
TEL: +49-89-3749999-0
FAX: +49-89-3749999-29
sales-europe@atpinc.com

ATP CHINA
TEL: +86-21-5080-2220
FAX: +86-21-9687-0000-026
sales@cn.atpinc.com

ATP Confidential © ATP Electronics, Inc.