Real-time Clock Module (I2C Bus)

Features

- Using external 32.768kHz quartz crystal
- Supports I²C-Bus's high speed mode (400 kHz)
- Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- Programmable square wave output signal
- 56-byte, battery-backed, nonvolatile (NV) RAM for data storage
- Automatic power-fail detect and switch circuitry of battery backup
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- UL Recognized: E348121

Description

The PT7C433833A serial real-time clock is a low-power clock/calendar with a programmable square-wave output and 56 bytes of nonvolatile RAM.

Address and data are transferred serially via a 2-wire, bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

The PT7C4338 series have a built-in power sense circuit that detects power failures and automatically switches to the battery supply.

Table 1 shows the basic functions of PT7C4338. More details are shown in section: overview of functions.

Table 1. Basic functions of PT7C4338

Item	Function			PT7C4338
1	Oscillator	Source: Crystal: 32.768kHz		√
		Oscillator enable/disable		√
		Oscillator fail detect		√
2	Time	Time display	12-hour	√
			24-hour	√
		Century bit		-
3	Alarm interrupt			-
4	Programmable square wave output (Hz)			1, 4.096k, 8.192k, 32.768k
5	RAM			56×8
6	Battery backup			√

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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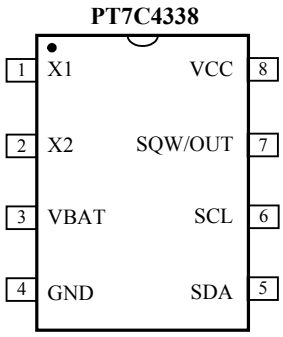
Pin Assignment



SOIC-8
MSOP-8

Pin Description

Pin no.	Pin	Type	Description
1	X1	I	**32.768kHz Crystal Connections.** The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5pF. Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is floated if an external oscillator is connected to pin X1. An external 32.768kHz oscillator can also drive the PT7C4338. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
2	X2	O	
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface.
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
7	SQW/OUT	O	**Square-Wave/Output Driver.** When enabled and the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). It is open drain and requires an external pull up resistor. Operates with either VCC or VBAT applied.
8	VCC	P	**Supply Voltage.** When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and VCC is below VPF, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.
3	VBAT	P	**+3V Battery Input.** Backup supply input for any standard 3V lithium cell or other energy source. Battery voltage must be held between the minimum and maximum limits for proper operation. If a backup supply is not required, VBAT must be grounded. **UL** recognized to ensure against reverse charging when used with a lithium battery.
4	GND	P	**Ground.** DC power is provided to the device on these pins. VCC is the primary power input. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and VCC is below VPF, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.

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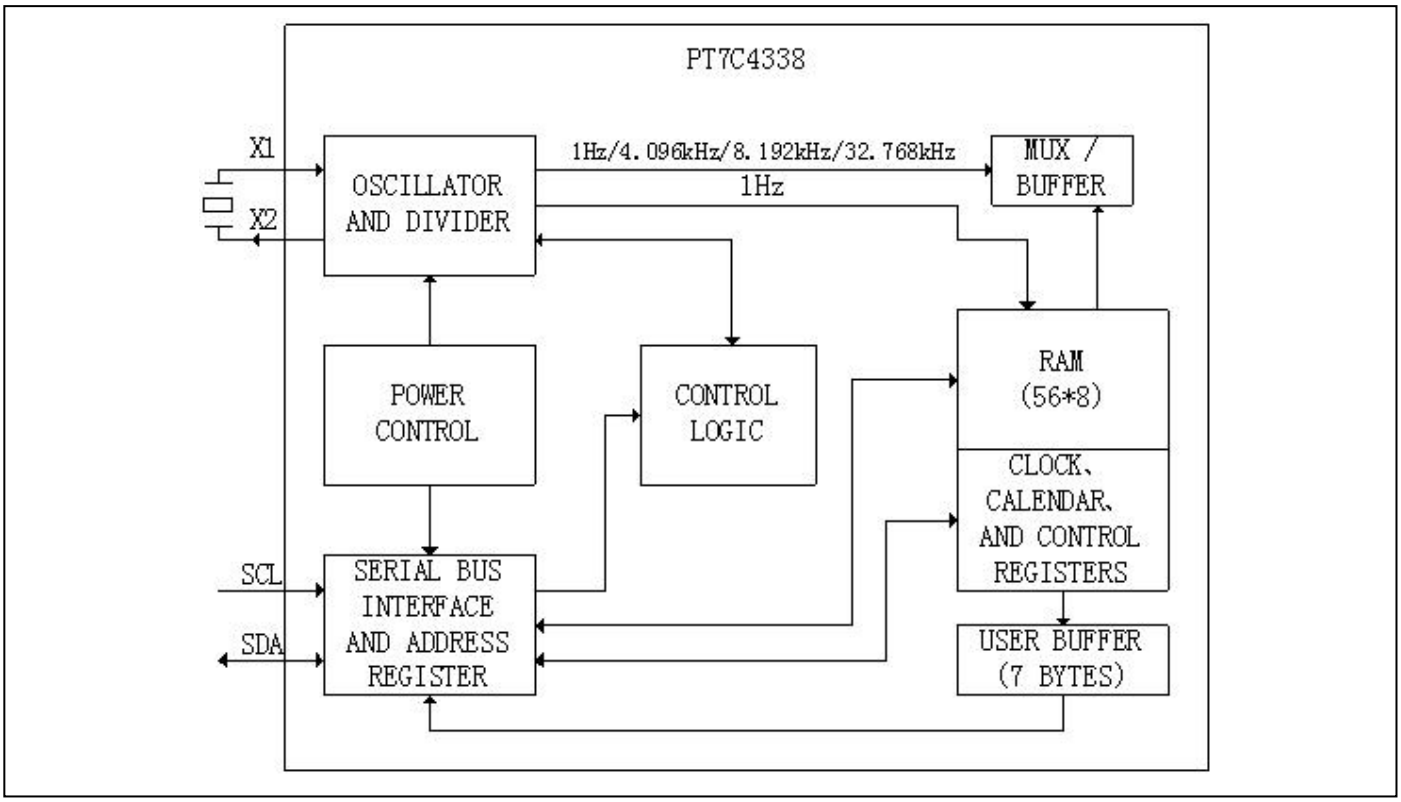
Function Block



Maximum Ratings

Storage Temperature	-55°C to +125°C
Junction Temperature	+125°C Max
Supply Voltage to Ground Potential (Vcc to GND)	-0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND)	-0.3V to +6.5V
DC Output Voltage (SDA, /INTA, /INTB pins)	-0.3V to +6.5V
DC Output Current (FOUT)	-0.3V to (V_{cc}+0.3V)
Power Dissipation	320mW (depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	PT7C433833A	2.7	3.3	5.5	V
V_{IH}	Logic 1	Note 2	0.7 * V_{CC}	-	V_{CC} + 0.3	
V_{IL}	Logic 0	Note 2	-0.3	-	+0.3 * V_{CC}	
V_{PF}	Power-Fail Voltage	PT7C433833A	1.5	1.75	2.0	
V_{BAT}	V_{BAT} Battery Voltage	Note 2	1.3	3.0	3.7	

Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.

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DC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{BAT}	V_{BAT} Battery Voltage	Note 2	1.3	-	3.7	V
I_{LI}	Input Leakage	Note 3	-1	-	1	µA
I_{LO}	I/O Leakage	Note 4	-1	-	1	µA
I_{OLSDA}	SDA Logic 0 Output	V_{CC} > =2V; V_{OL} = 0.4V	3.0	-	-	mA
		V_{CC} < 2V; V_{OL} = 0.2 V_{CC}	3.0	-	-	
I_{OLSQW}	SQW/OUT Logic 0 Output	V_{CC} > =2V; V_{OL} = 0.4V	1.0	-	-	mA
		1.3V < V_{CC} < 2V; V_{OL} = 0.2 V_{CC}	250	-	-	µA
I_{CCA}	Active Supply Current (Note 5)	PT7C433833A	-	40	120	µA
I_{CCS}	Standby Current (Note 6)	PT7C433833A	-	30	100	µA
I_{BATLKG}	V_{BAT} Leakage Current (V_{CC} Active)	-	-	10	100	nA

(V_{CC} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.0V, T_A = +25°C, unless otherwise noted.)

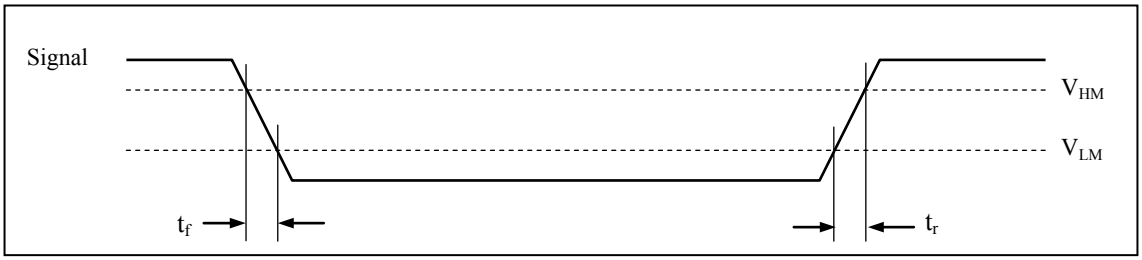
Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{BATOSC1}$	V_{BAT} Current (OSC ON); V_{BAT} =3.7V, SQW/OUT OFF (Note 7)	-	350	1000	nA
$I_{BATOSC2}$	V_{BAT} Current (OSC ON); V_{BAT} =3.7V, SQW/OUT ON (32kHz) (Note 7)	-	400	1200	nA
I_{BATDAT}	V_{BAT} Data-Retention Current (OSC OFF); V_{BAT} =3.7V (Note 7)	-	-	300	nA

Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.
Note 3: SCL only.
Note 4: SDA and SQW/OUT.
Note 5: ICCA------SCL clocking at max frequency = 400 kHz.
Note 6: Specified with the I2C bus inactive.
Note 7: Measured with a 32.768 kHz crystal attached to X1 and X2.

AC Electrical Characteristics

Sym	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.7 V_{CC}	V
V_{HL}	Rising and falling threshold voltage low	0.3 V_{CC}	V

Measurement level



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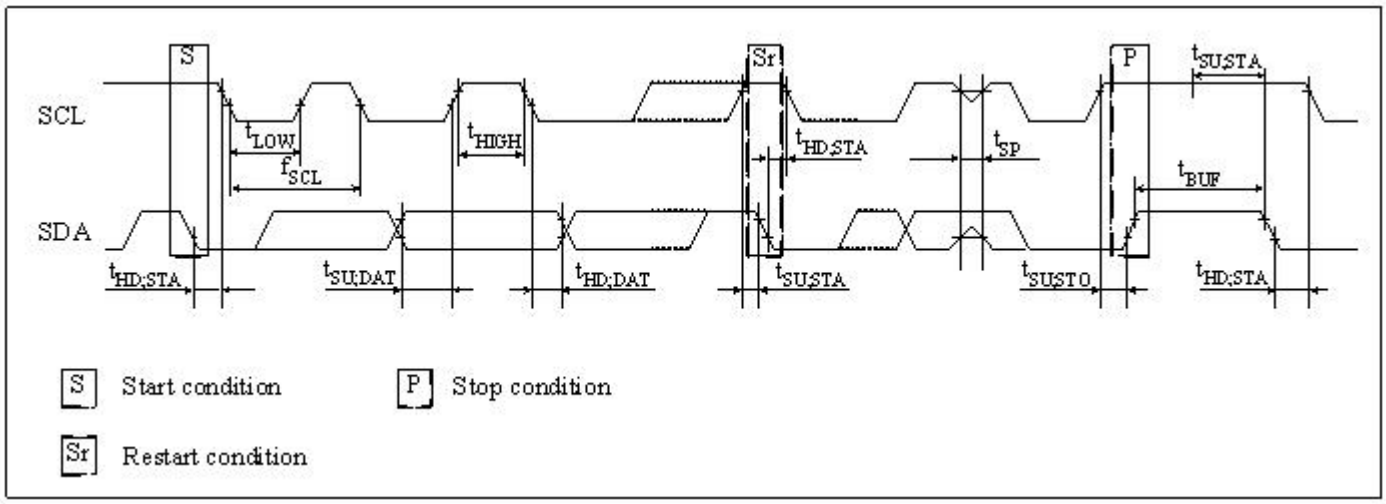
AC Electrical Characteristics

(T_A = -40℃ to +85℃) (Note 1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	-	-	-	400	kHz
t_{BUF}	Bus Free Time Between STOP and START condition	-	1.3	-	-	μs
$t_{HD:STA}$	Hold Time (Repeated) START Condition	Note 2	0.6	-	-	μs
t_{LOW}	LOW Period of SCL Clock	-	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	-	0.6	-	-	μs
$t_{SU:STA}$	Setup Time of Repeated START Condition	-	0.6	-	-	μs
$t_{HD:STA}$	Data Hold Time	Note3,4	0	-	0.9	μs
$t_{SU:STA}$	Data Setup Time	Note5	100	-	-	ns
t_r	Rise Time of Both SDA and SCL Signals (Note 6)	Fast mode	-	-	300	ns
		Standard mode	-	-	1000	
t_f	Fall Time of Both SDA and SCL Signals	Note6	-	-	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	-	0.6	-	-	μs
C_B	Capacitance Load for Each Bus Line	Note 6	-	-	400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)	Note 1	-	-	10	pF
t_{OSF}	Oscillator Stop Flag (OSF) Delay	Note 7	-	100	-	ms

Note 1: Limits of full temperature are guaranteed by design not production test.
Note 2: After this period, the first clock pulse is generated. A limit of min value at fast mode is 4.0us in UM10204 I2C-bus specification.
Note 3: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 4: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 5: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,MAX} + t_{SU:DAT}$ = 1000 +250 = 1250ns before the SCL line is released.
Note 6: C_B------total capacitance of one bus line in pF.
Note 7: The parameter t_{OSF} is the time period the oscillator must be stopped for the OSF flag to be set over the voltage range of $0.0V \leq V_{CC} \leq V_{CC\,MAX}$ and $1.3V \leq V_{BAT} \leq 3.7V$.

Timing Diagram



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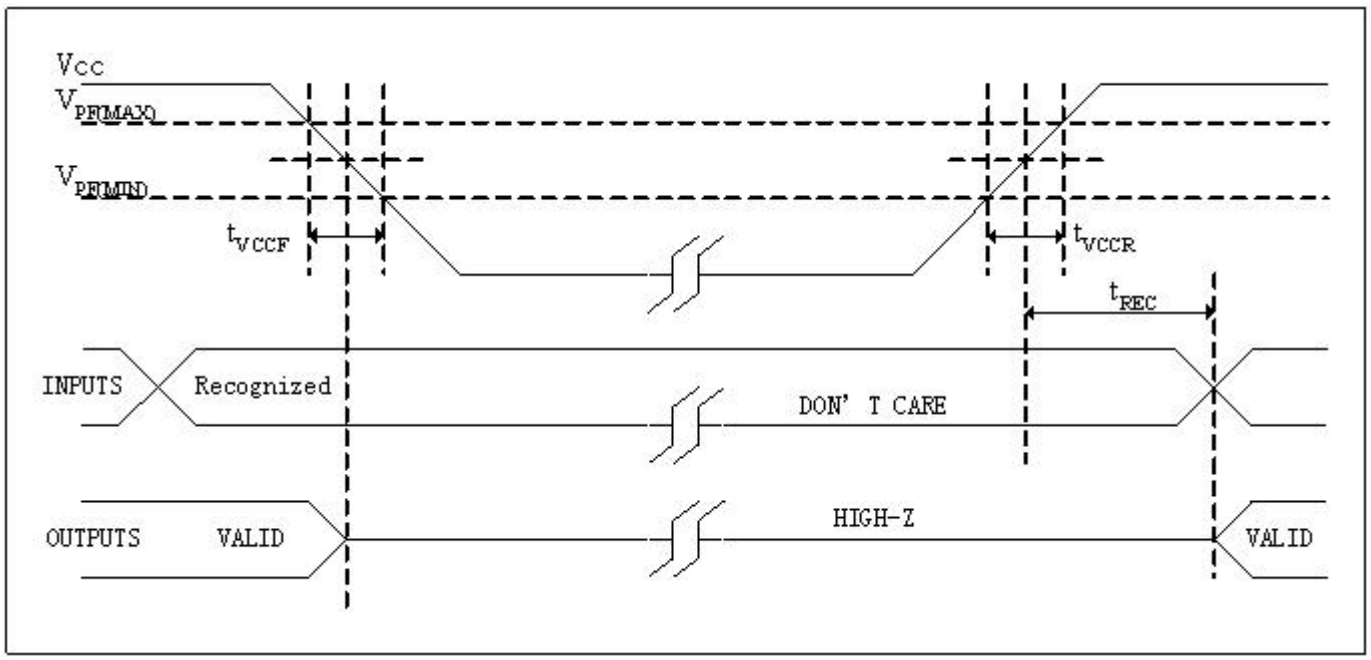
Power-Up/Power-Down Characteristics

(T_A = -40℃ to +85℃) (Note 1, Fig 3)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{REC}	Recovery at Power-Up (Note 2)	-	-	2	ms
t_{VCCF}	V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	300	-	-	µs
t_{VCCR}	V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	0	-	-	µs

Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

Fig 3. Power-Up/Power-Down Timing



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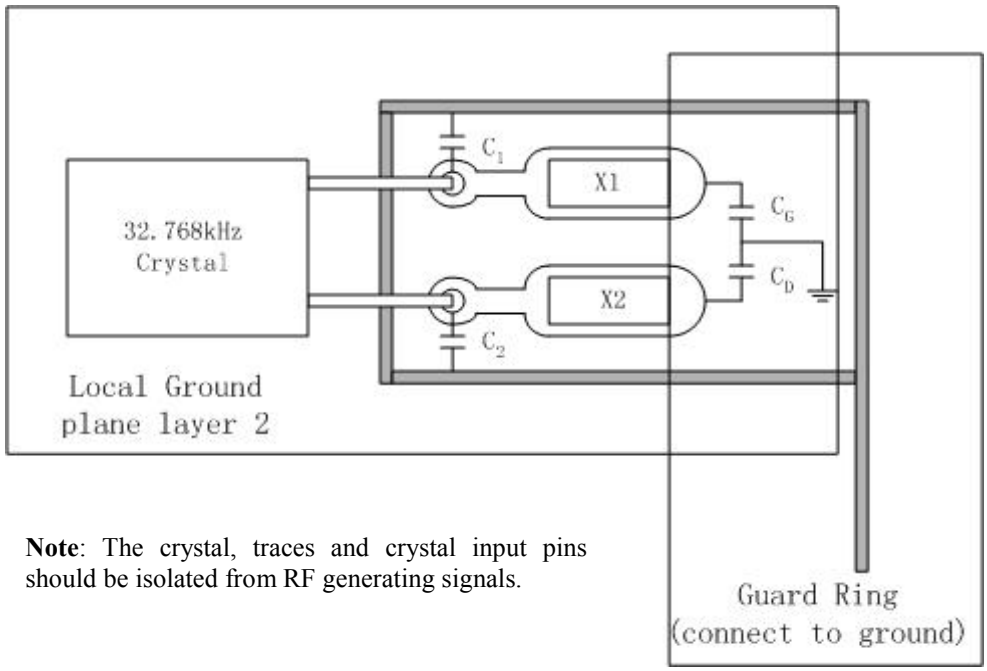
Recommended Layout for Crystal



Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.

Built-in Capacitors Specifications and Recommended External Capacitors

Parameter		Symbol	Typ	Unit
Build-in capacitors	X1 to GND	C_G	20	pF
	X2 to GND	C_D	20	pF
Recommended External capacitors	X1 to GND	C_1	4	pF
	X2 to GND	C_2	4	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2, for frequency=32.768 KHz, C_1 and C_2 should meet the equation as below:

$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] = C_L$

Cpar is all parasitical capacitor between X1 and X2.

C_L is crystal's load capacitance.

Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_L	-	12.5	-	pF

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Function Description

Overview of Functions

Clock Function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

Programmable Square Wave Output

A square wave output enable bit controls square wave output at pin 7. 4 frequencies are selectable: 1, 4.096k, 8.192k, 32.768k Hz.

Interface with CPU

Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).
Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.
The SCL's maximum clock frequency is 400 kHz, which supports the I^2C bus's high-speed mode.

Oscillator Enable/disable

Oscillator can be enabled or disabled by /EOSC bit.

Registers

Allocation of registers

Addr. (hex)*1	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	/EOSC*2	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	0	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
03	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
04	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
05	Months (01-12)	0	0	0	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Control*3	OUT*4	0	OSF	SQWE*5	0	0	RS1*6	RS0*6
08~3F	RAM*7	-	-	-	-	-	-	-	-

Caution points:

*1. PT7C4338 uses 6 bits for address. That is if write data to 41H, the data will be written to 01H address register.
*2. Oscillator Enable bit. When this bit is set to 1, oscillator is stopped but time count chain is still active.
*3. Control register was used to select SQW/OUT pin output square wave with one of 4 kinds of frequency or DC level.
*4. Control SQW/OUT pin output DC level when square wave is disabled.
*5. Square wave outputs enable at SQW/OUT pin.
*6. Square wave output frequency select.
*7. PT7C4338 has 56×8 static RAM for customer use. It is volatile RAM.
*8. All bits marked with "0" are read-only bits. Their value when read is always "0". All bits marked with "-" are customer using space.

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Control and Status Register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Control	OUT	0	OSF	SQWE	0	0	RS1	RS0
	(default)	1	0	1	1	0	0	1	1

- **OUT**

It controls the output level of the SQW/OUT pin when the square wave output is disabled.

OUT	Data	Description
Read / Write	0	When SQWE = 0, SQW/OUT pin output low.
	1	When SQWE = 0, SQW/OUT pin output high. Default

- **SQWE (Square Wave Enable)**

This bit, when set to logic 1, will enable the oscillator output. The frequency of the square wave output depends upon the value of the RS0 and RS1 bits. With the square wave output set to 1Hz, the clock registers update on the falling edge of the square wave.

- **RS (Rate Select)**

These bits control the frequency of the square wave output when the square wave output has been enabled.

RS1, RS0	Data	SQW output freq. (Hz)
Read / Write	00	1
	01	4.096k
	10	8.192k
	11	32.768k Default

- **OSF (Oscillator Stop Flag)**

Logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on VCC and VBAT is insufficient to support oscillation.
3) The /EOSC bit is set to 1, disabling the oscillator.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF bit to logic 1 leaves the value unchanged.

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Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds	/EOSC	S40	S20	S10	S8	S4	S2	S1
	(default)	0	0	0	0	0	0	0	0
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
	(default)	0	0	0	0	0	0	0	0
02	Hours	0	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	0	0	0	0	0	0	0	0

- **12, /24 bit**

This bit is used to select between 12-hour clock system and 24-hour clock system.

12, /24	Data	Description
Read / Write	0	24-hour system
	1	12-hour system

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

12, /24	Description	Hours register
0	24-hour time display	
1	12-hour time display	

24-hour clock	12-hour clock	24-hour clock	12-hour clock
00	52 (AM 12)	12	72 (PM 12)
01	41 (AM 01)	13	61 (PM 01)
02	42 (AM 02)	14	62 (PM 02)
03	43 (AM 03)	15	63 (PM 03)
04	44 (AM 04)	16	64 (PM 04)
05	45 (AM 05)	17	65 (PM 05)
06	46 (AM 06)	18	66 (PM 06)
07	47 (AM 07)	19	67 (PM 07)
08	48 (AM 08)	20	68 (PM 08)
09	49 (AM 09)	21	69 (PM 09)
10	50 (AM 10)	22	70 (PM 10)
11	51 (AM 11)	23	71 (PM 11)

* Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

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Days of the Week Counter

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Days of the week	0	0	0	0	0	W4	W2	W1
	(default)	0	0	0	0	0	0	0	1

Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
04	Dates	0	0	D20	D10	D8	D4	D2	D1
	(default)	0	0	0	0	0	0	0	1
05	Months	0	0	0	M10	M8	M4	M2	M1
	(default)	0	0	0	0	0	0	0	1
06	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	0	0	0	0	0	0	0	0

Note: Any registered imaginary time should be replaced by correct time, otherwise it will cause the clock counter malfunction.

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I²C Bus Interface

Overview of I²C-BUS

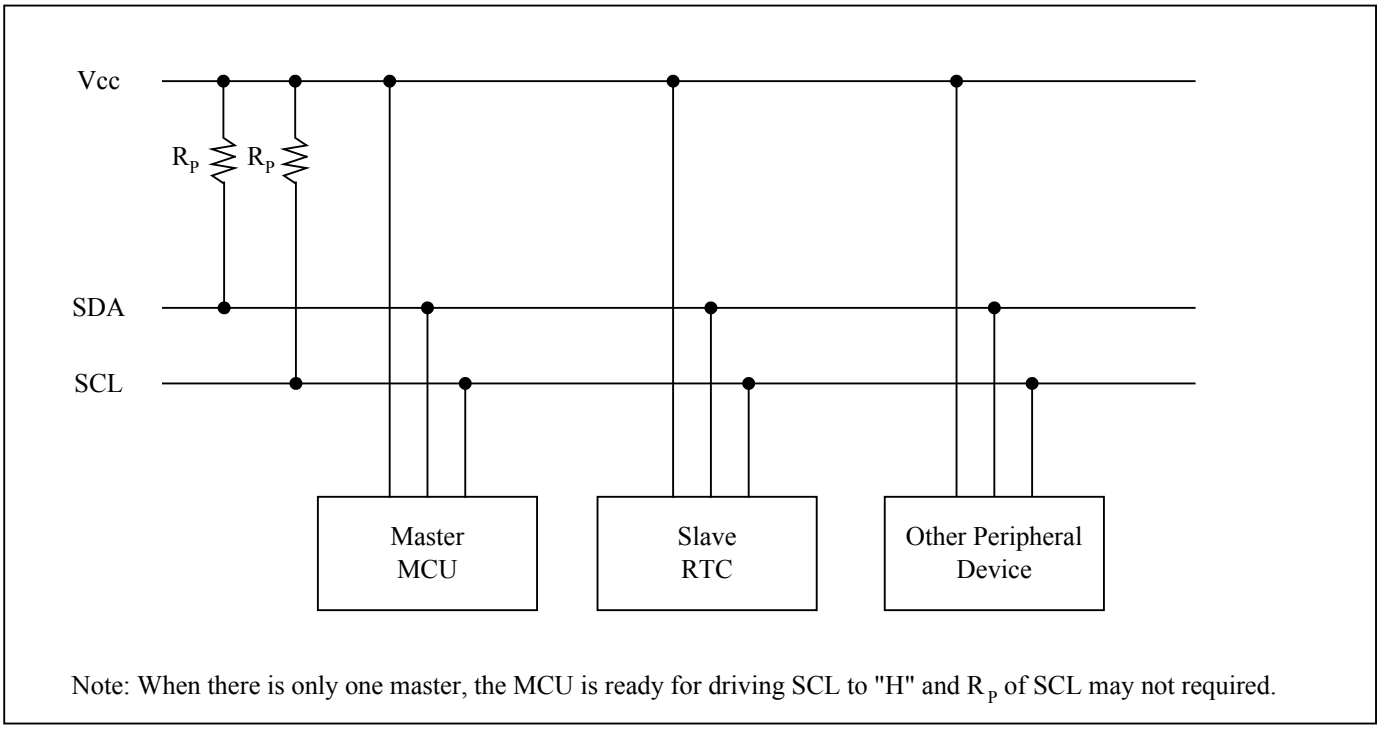
The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

System Configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

Fig 1. System configuration



Note: When there is only one master, the MCU is ready for driving SCL to "H" and R_p of SCL may not required.

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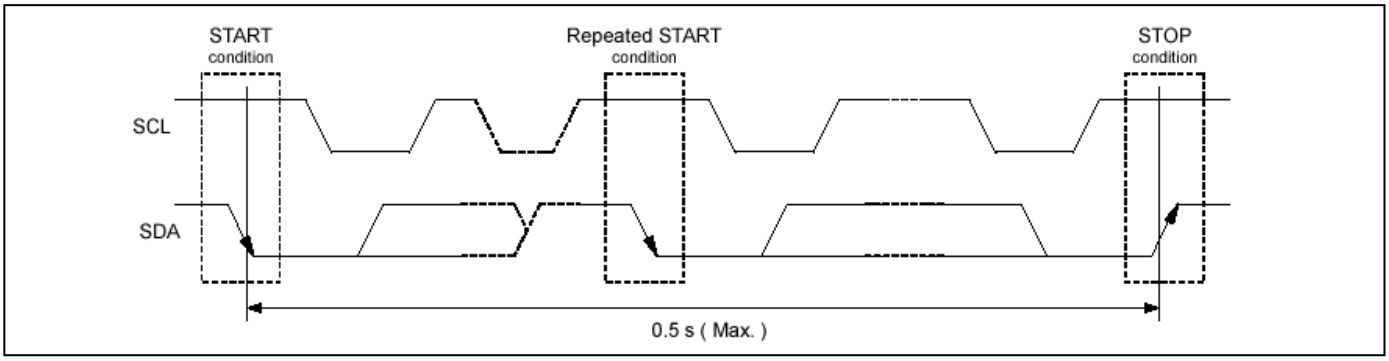
Starting and Stopping I²C Bus Communications

Fig 2. Starting and Stopping on I²C Bus



1) START Condition, Repeated START Condition, and STOP Condition

a) START condition
SDA level changes from high to low while SCL is at high level

b) STOP condition
SDA level changes from low to high while SCL is at high level

c) Repeated START condition (RESTART condition)

In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

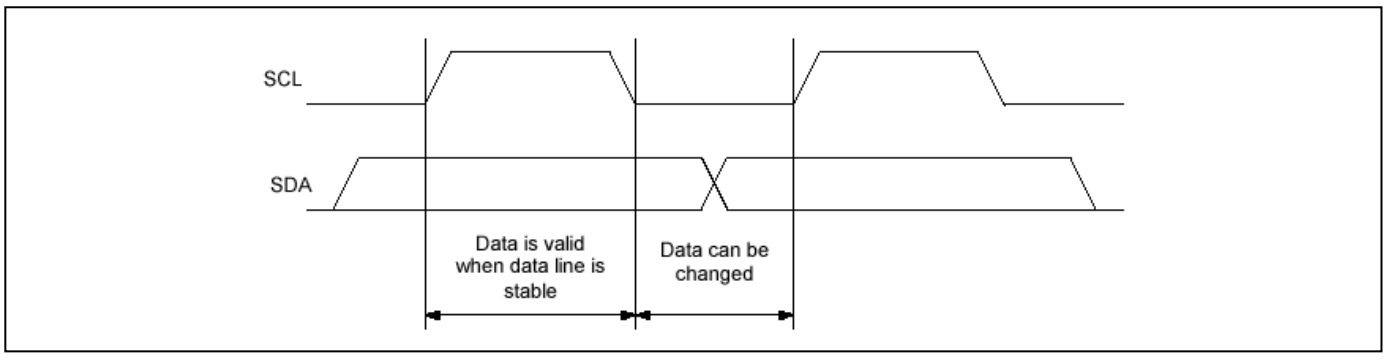
2) Data Transfers and Acknowledge Responses during I²C-BUS Communication

a) Data Transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.
The receiver (receiving side) captures data while the SCL line is at high level.



***Note** with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

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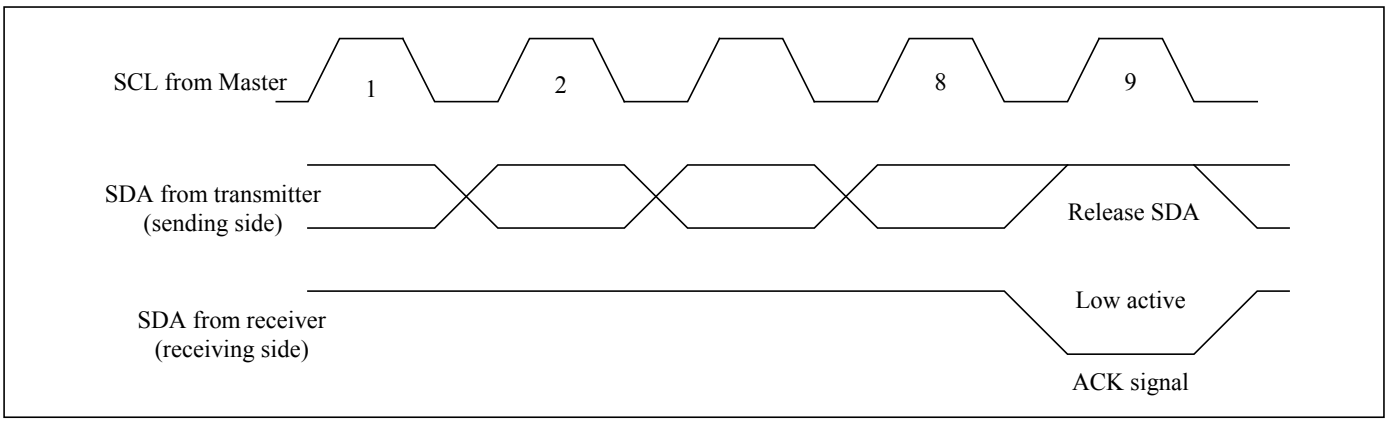
b) Data Acknowledge Response (ACK Signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

Slave Address

The I^2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.

All communications begin with transmitting the [START condition] + [slave address (+ $R/\overline{W}$ specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

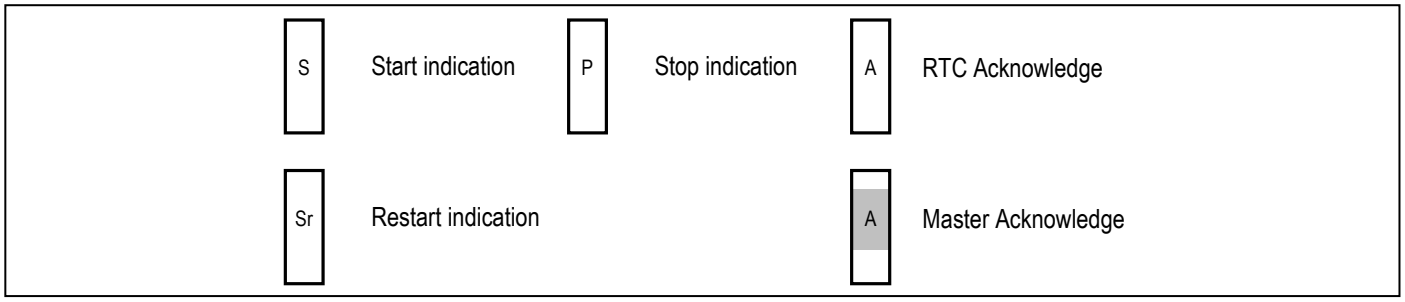
Slave addresses have a fixed length of 7 bits. See table for the details.

An $R/\overline{W}$ bit is added to each 7-bit slave address during 8-bit transfers.

Table

Operation	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	D1 h	1	1	0	1	0	0	0	1 (= Read)
Write	D0 h								0 (= Write)

I^2C Bus's Basic Transfer Format



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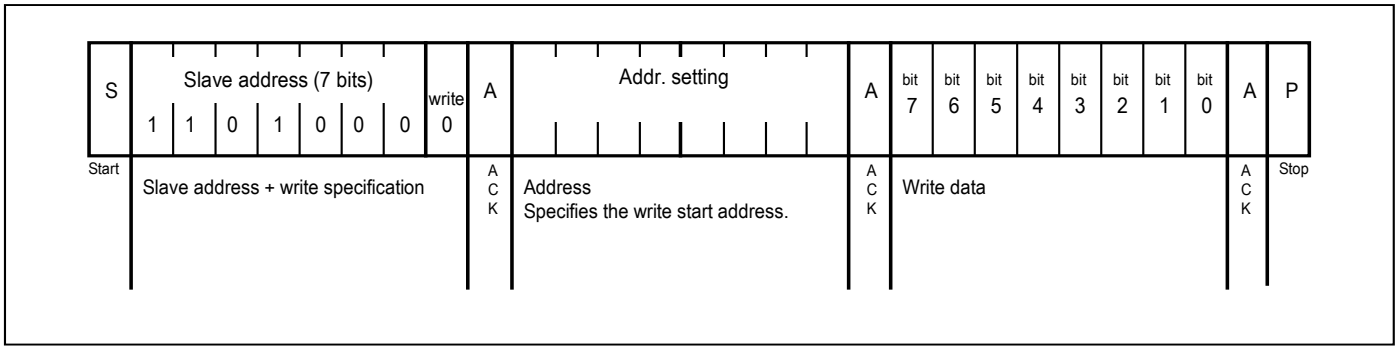
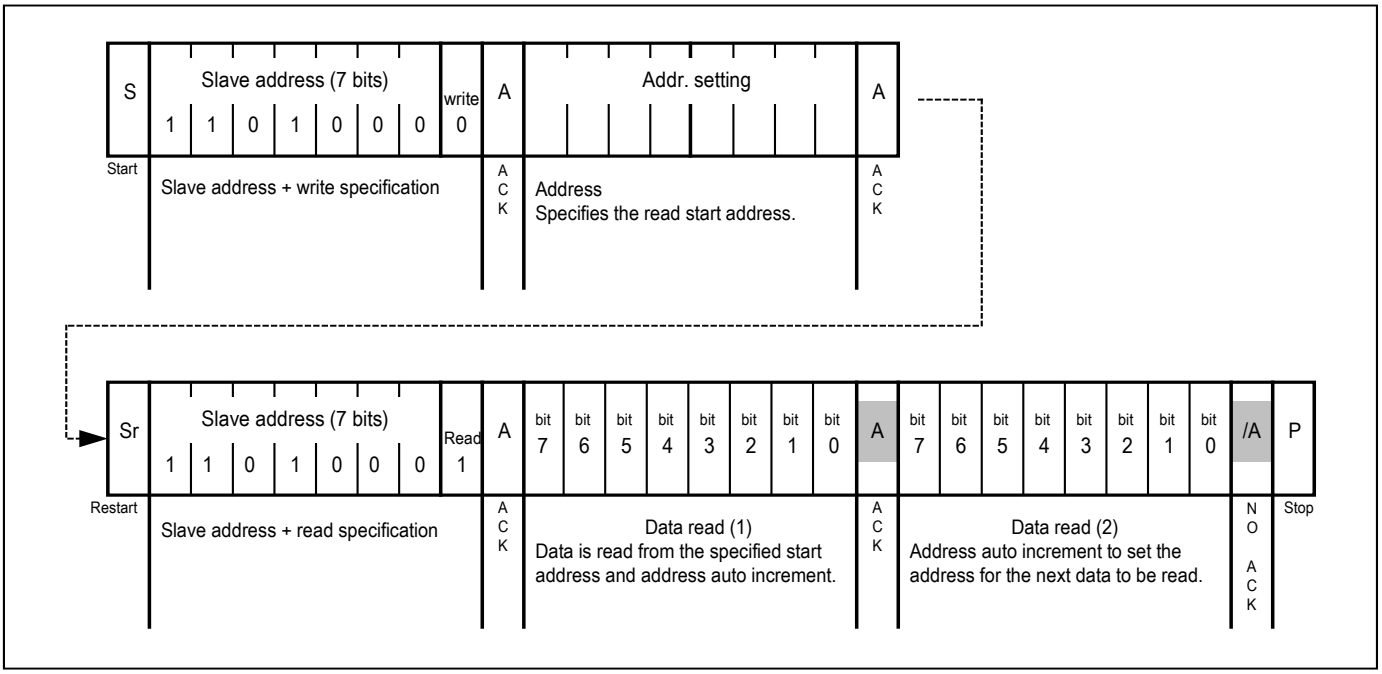
1) Write via I²C Bus

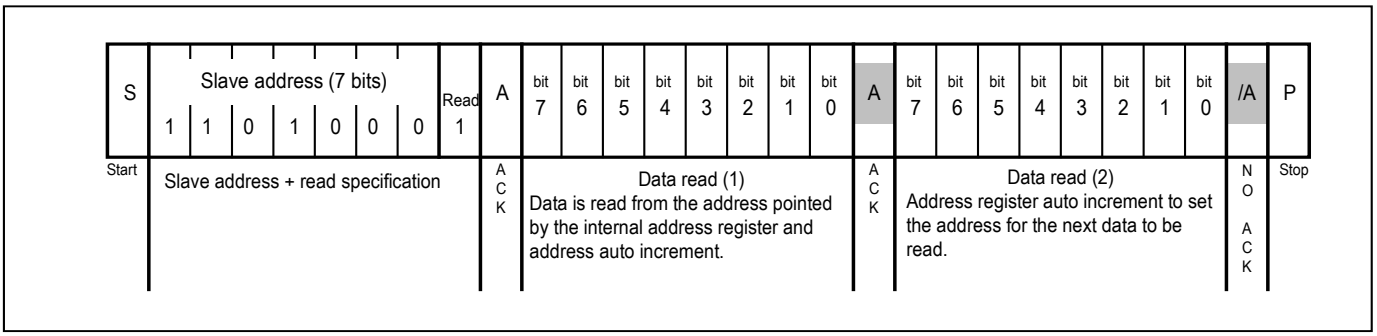


2) Read via I²C Bus

a) Standard Read



b) Simplified Read



Note:
1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.
2. 49H, 4AH are used as test mode address. Customer should not use the addresses.

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Part Marking

U Package

PT7C433833AUE



Z: Die Rev
YW: Date Code (Year & Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

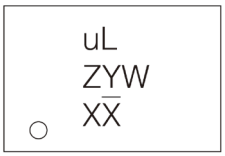
W Package



Z: Die Rev
YW: Date Code (Year & Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

ZE Package

uL = PT7C433833AZEE



Z: Die Rev
YW: Date Code (Year & Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

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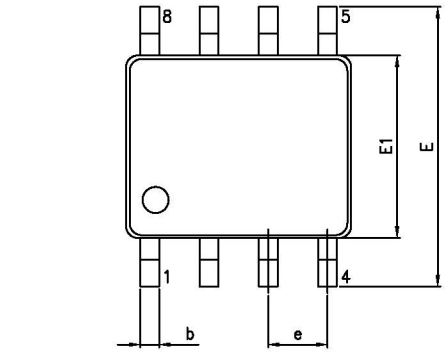
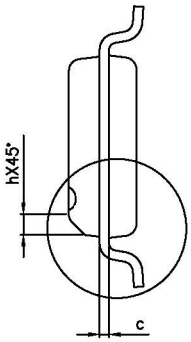
Packaging Mechanical

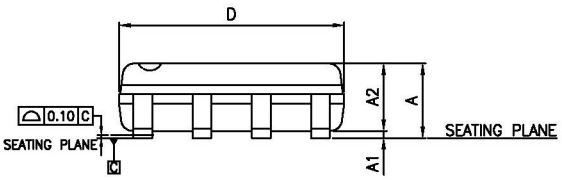
W (SOIC-8)

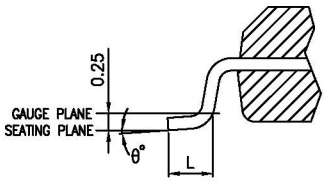




SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.10	—	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	—	1.27
h	0.25	—	0.50
θ°	0	—	8

UNIT : mm





NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012

PERICOM Enabling Serial Connectivity — DATE: 02/21/14

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 — REVISION: G

15-0103

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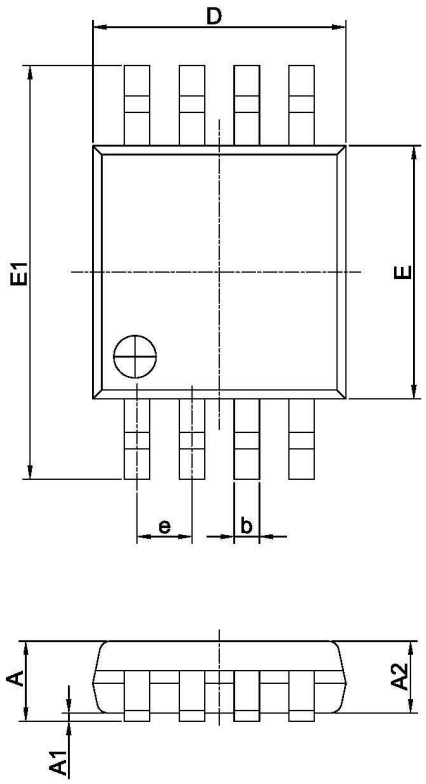
U (MSOP-8)



PKG. DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	–	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.65	5.15
e	0.65 BSC	
L	0.40	0.80
θ	0°	8°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. REFER JEDEC MO-187E/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

PERICOM Enabling Serial Connectivity

DATE: 10/20/14

DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP

PACKAGE CODE: U (U8)

DOCUMENT CONTROL #: PD-1261 REVISION: E

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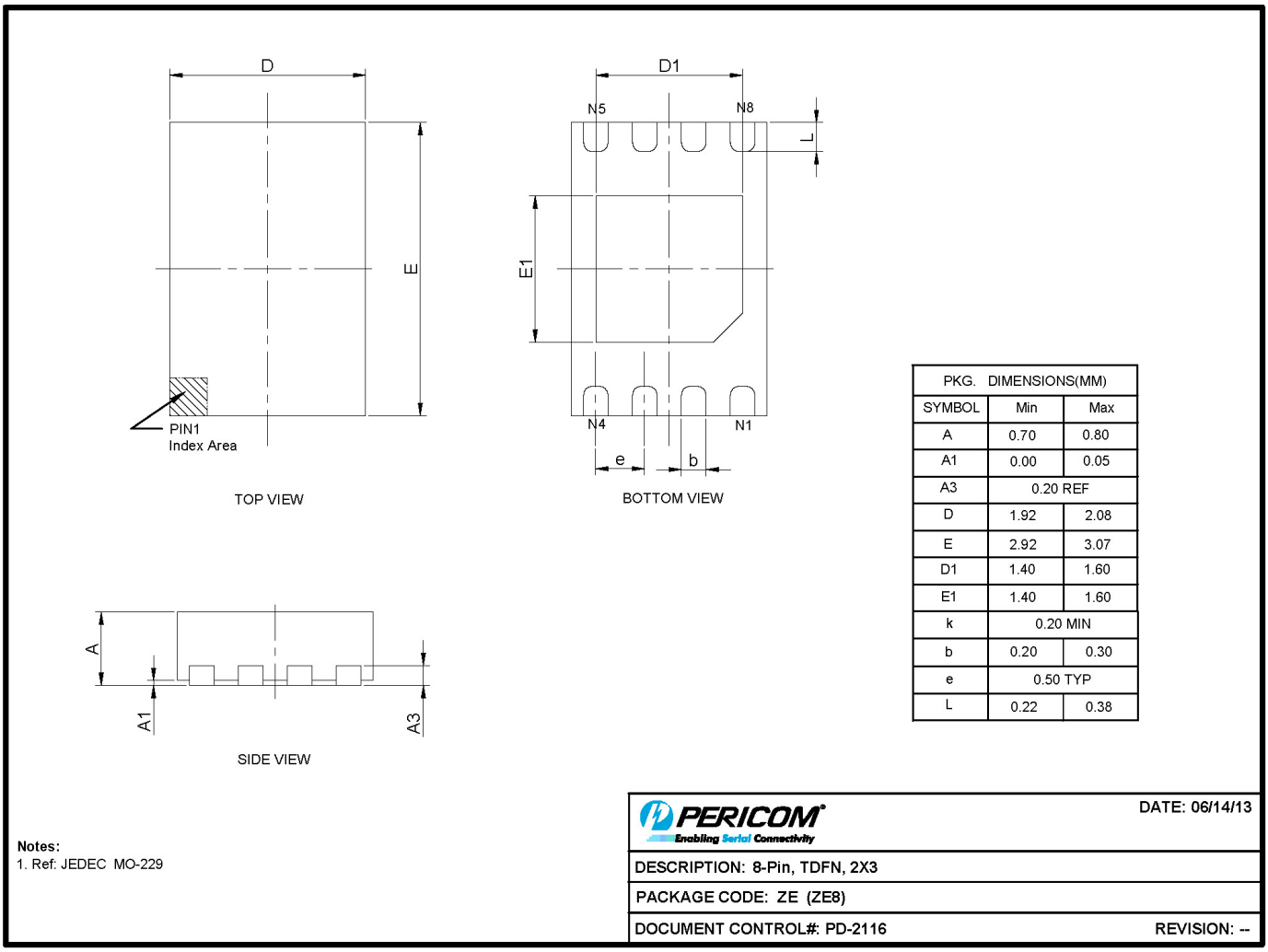
ZE (TDFN-8)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20 MIN	
b	0.20	0.30
e	0.50 TYP	
L	0.22	0.38

Notes:
1. Ref: JEDEC MO-229

PERICOM Enabling Serial Connectivity — DATE: 06/14/13

DESCRIPTION: 8-Pin, TDFN, 2X3

PACKAGE CODE: ZE (ZE8)

DOCUMENT CONTROL#: PD-2116 REVISION: --

13-0155

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Number	Package Code	Package
PT7C433833AWEX	W	8-Pin, 150mil-Wide (SOIC)
PT7C433833AUEX	U	8-Pin, Mini Small Outline Package (MSOP)
PT7C433833AZEEX	ZE	8-Pin, 2x3 (TDFN)

Notes:
- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
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- E = Pb-free and Green
- X suffix = Tape/Reel

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