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Network Camera Controller with JPEG Encoder

S1S65010
Evaluation Board
Technical Manual

Main Board(uITRON):S5U1S65K01H0300
Main Board(Linux) :S5U1S65K01H0400

SEIKO EPSON CORPORATION

Rev.3.0

NOTICE

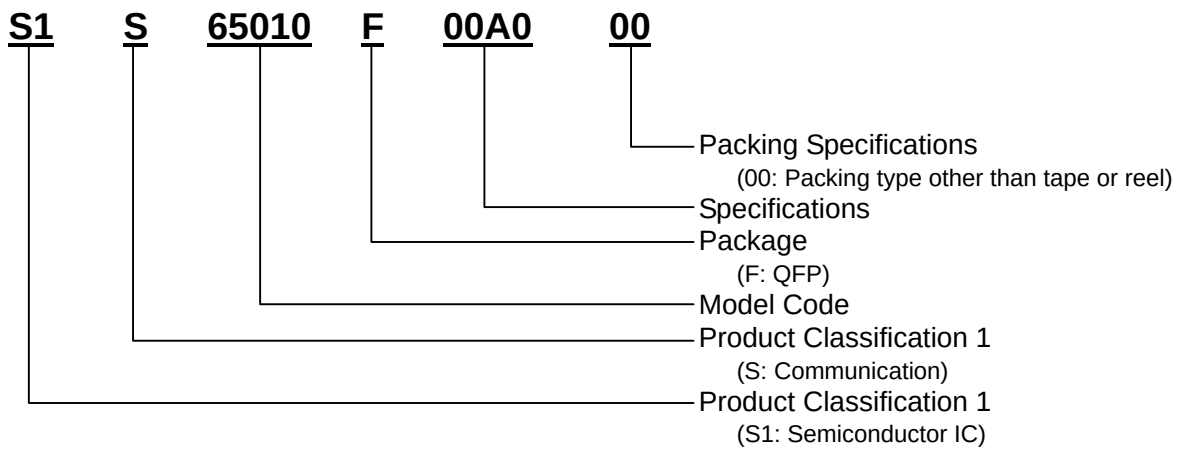
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Configuration of product number

●DEVICES



●Evaluation Board

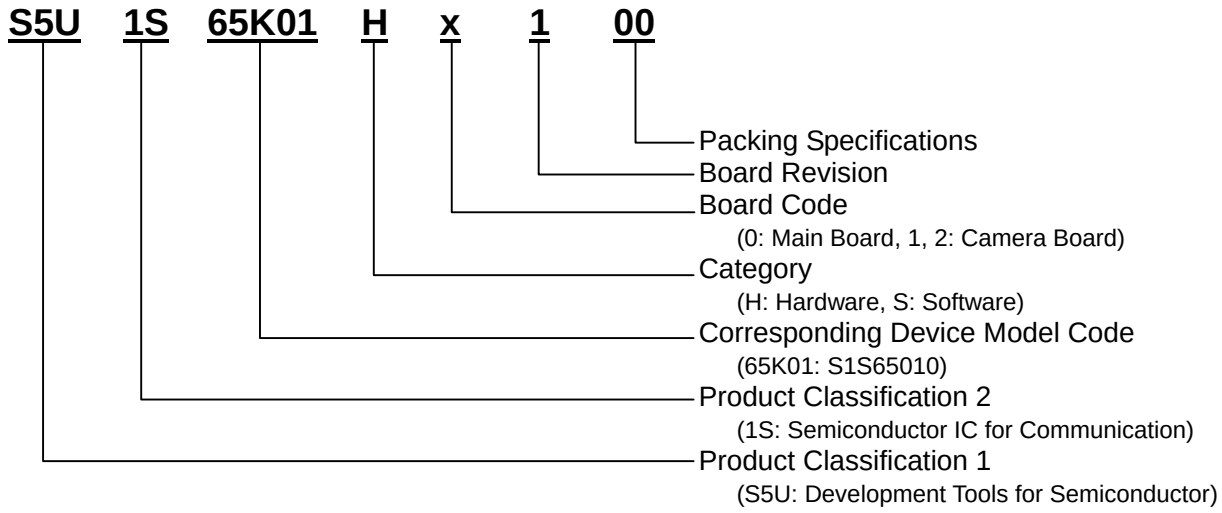


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1. OVERVIEW

This product, the S1S65010 Evaluation Board Kit, is for quickly building a network-accessible camera based on the Seiko Epson S1S65010 network camera chip. When shipping it, the sample software of the uITRON version is written in Flash ROM as for S5U1S65K01H0300. When shipping it, the sample software of the Linux version is written in Flash ROM as for S5U1S65K01H0400.

2. COMPONENTS

2.1 Main Board (Product Number S5U1S65K01H0300/0400)

Network camera IC:	S1S65010
Flash EEPROM:	4 MB (Toshiba TC58FVM5B2ATG65)
SRAM:	2 MB (Cypress CY62167DV30LL)
SDRAM:	16 MB (Micron MT48LC8M16A2TG-75)
Ethernet interface:	Support 10/100BaseT via MII RJ45 connector ↔ TG110-LC55NC ↔ ICS1893BF
JTAG debugging interface:	20-pin connector for in-circuit emulator or other debugger
Camera board interface:	16/40-pin connector for camera board
I^2C:	Part of the camera board interface connector is used for camera control. It is also connected to a serial EEPROM (BR24L56RFVM-W).
I^2S:	Part of the camera board interface connector is used for connecting a monaural codec IC.
GPIO:	Part of the camera board interface connector is used for evaluating GPIO operation.
Serial interface:	10-pin RS232-C connector
Power supply voltage:	5 V ± 10%

2.2 Block Diagram

The following figure gives block diagram for both the main and camera boards in this evaluation kit.

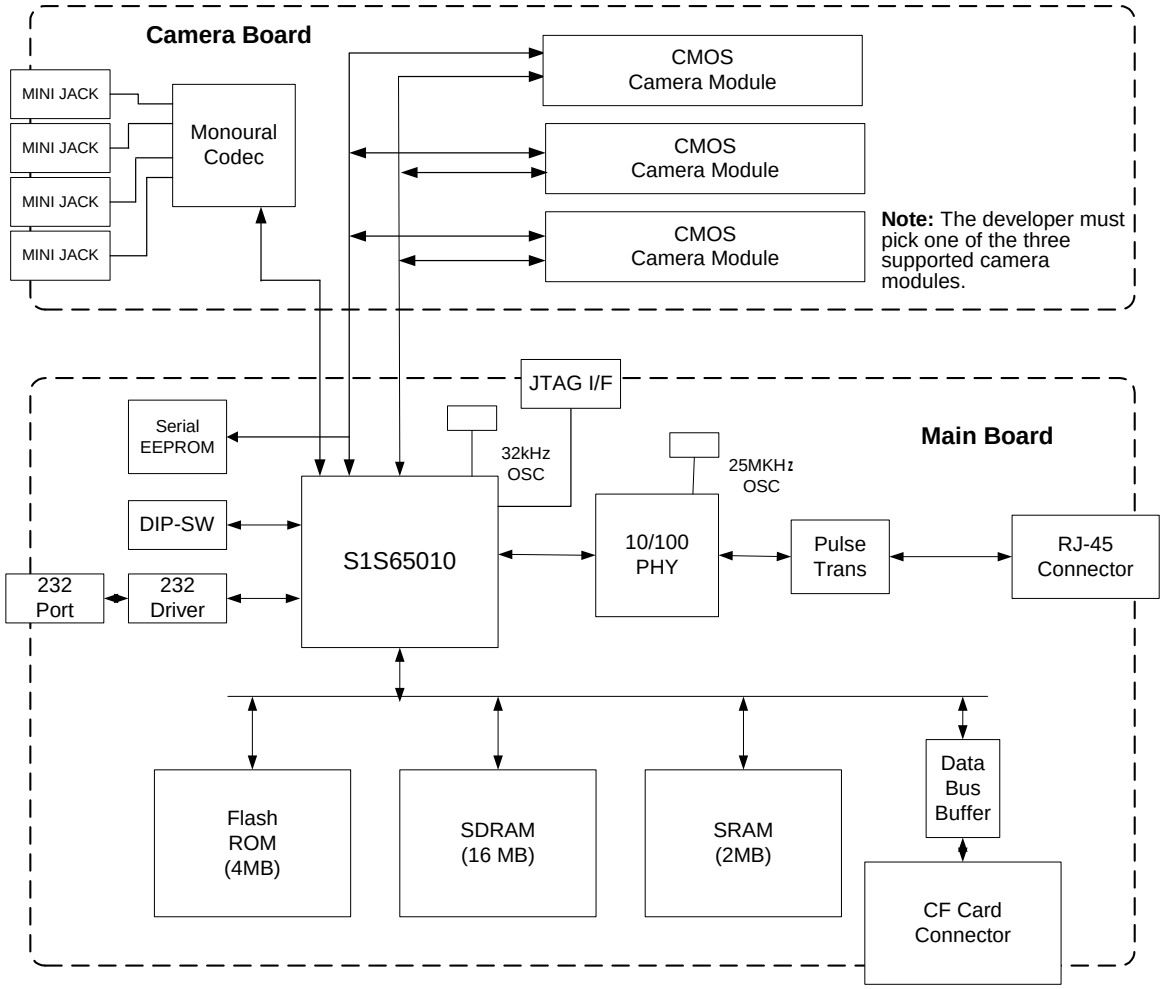


Fig.2.1 Block Diagram

3. MECHANICAL SPECIFICATIONS

The following figure3.1 show the layout and dimensions of the main board.

3.1 Main Board (Product Number S5U1S65K01H0300/0400) Layout and Dimensions

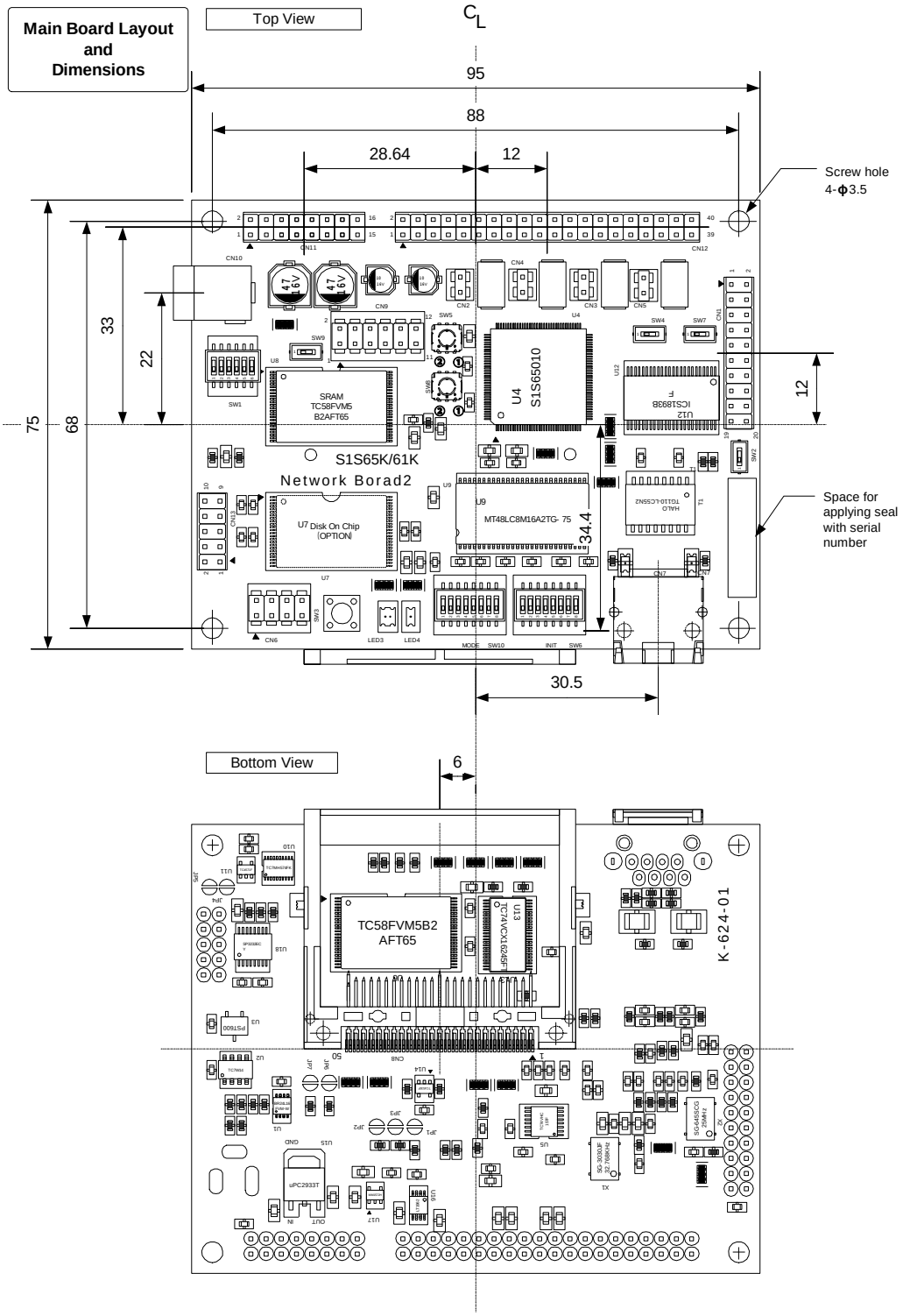


Fig.3.1 Main Board (Product Number S5U1S65K01H0300/0400) Layout and Dimensions

4. EXTERNAL PINS

4.1 Main Board Interface Connectors

The following Figure shows the locations of the external interface connectors on the main board. The Tables in the following six subsections list their pin assignments.

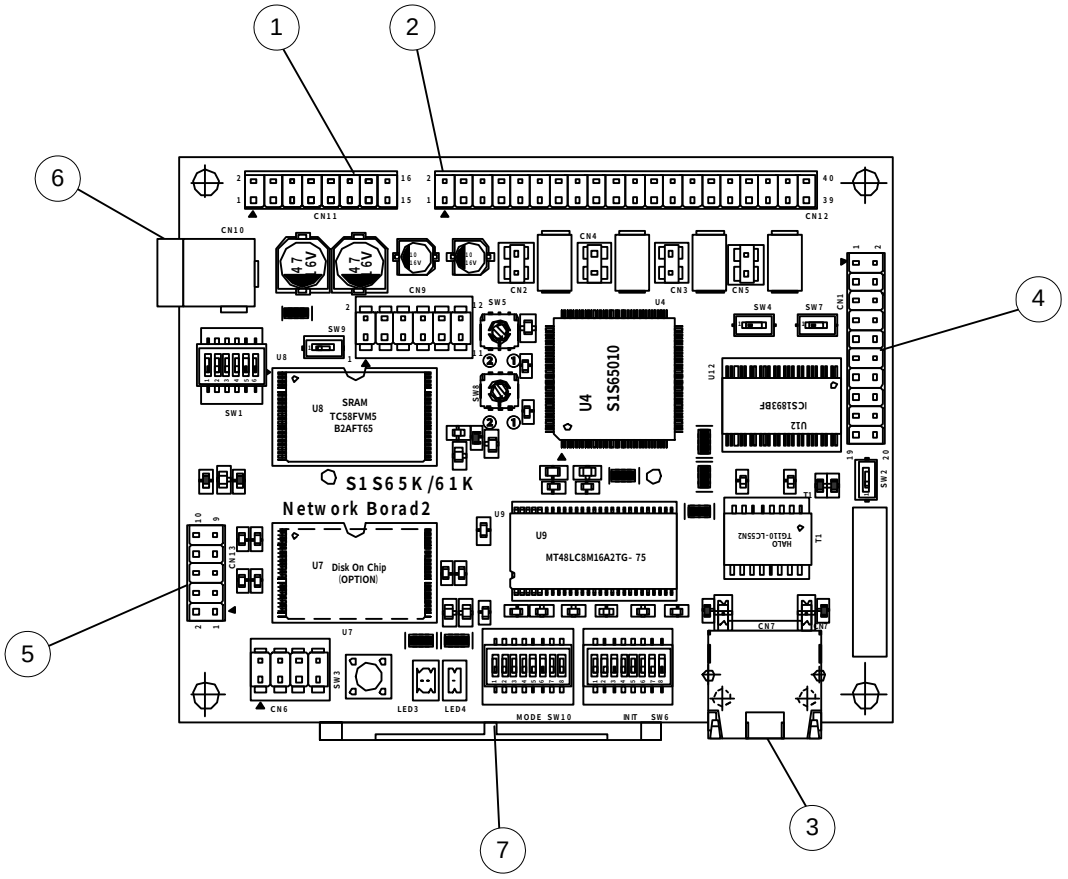


Fig.4.1 Main Board Layout

4.1.1 Camera Interface and Expansion Connectors

(1) GPIOD and GPIOE or CF control/monitor (CN11: XG8W-1631)

(1) in Fig.4.1

Pin Number	Function	Pin Number	Function
1	VDD (5 V)	2	VDD (5 V)
3	CFCE2# (GPIOD2)	4	CFCE1# (GPIOD3)
5	CFIORD# (GPIOE0)	6	CFIOWR# (GPIOE1)
7	CFIREQ (GPIOE4)	8	CFRST# (GPIOE3)
9	CFWAIT# (GPIOE2)	10	CFSTSCHG# (GPIOE5)
11	CFDEN# (GPIOE6)	12	CFDIR# (GPIOE7)
13	RESET#	14	GND
15	GND	16	GND

If the user application system does not use CF cards, the CF card interface lines are available for use as GPIOD[3:2] and GPIOE[7:0], as indicated with parentheses in the above Table.

(2) Camera interface and expansion connector (CN12: XG8W-4031)

(2) in Fig. 4.1

Pin Number	Function	Pin Number	Function
1	GND	2	GND
3	CAMDATA0	4	CAMDATA1
5	CAMDATA2	6	CAMDATA3
7	CAMDATA4	8	CAMDATA5
9	CAMDATA6	10	CAMDATA7
11	CMCLKOUT	12	CMCLKIN
13	CMVREF	14	CMHREF
15	CAMVDD	16	CAMVDD
17	I2C_SDA	18	I2C_SCL
19	3.3V	20	3.3V
21	GPIOA0	22	GPIOA1
23	GPIOA2 (TXD1/SPI_SS)	24	GPIOA3 (RXD1/SPI_SCLK)
25	GPIOA4 (SPI_MISO)	26	GPIOA5 (SPI_MOSI)
27	GPIOA6	28	GPIOA7
29	GPIOB0 (I2S0_WS)	30	GPIOB1 (I2S0_SCK)
31	GPIOB2 (I2S0_SD)	32	GPIOB3 (I2S1_SD)
33	GPIOB4 (Timer 1 out)	34	GPIOB5
35	GPIOB6	36	GPIOB7
37	GPIOD0	38	GPIOD1
39	GND	40	GND

4.1.2 Ethernet Interface (CN7: TM11R-5M2-88-LP)

(3) in Fig.4.1

Pin Number	Function	Pin Number	Function
1	TPTXDP	2	TPTXDN
3	TPRXDP	4	NC
5	NC	6	TPRXDN
7	NC	8	NC

4.1.3 JTAG In-Circuit Emulator Interface (CN1: XG8W-2031)

(4) in Fig. 4.1

Pin Number	Function	Pin Number	Function
1	3.3 V	2	3.3 V
3	nTRST	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	GND	12	GND
13	TDO	14	GND
15	nSRST	16	GND
17	NC	18	GND
19	NC	20	GND

4.1.4 Serial (RS232-C) Interface (CN13: XG8W-1031)

(5) in Fig. 4.1

Pin Number	Function	Pin Number	Function
1	NC	2	RXD
3	TXD	4	NC
5	GND	6	NC
7	RTS	8	CTS
9	NC	10	NC

This layout matches that used by such PC motherboard manufacturers as ASUS and GIGABYTE.

4.1.5 Power Supply Connector (CN10: MJ-179P)

(6) in Fig. 4.1

This is for connecting the AC power supply adapter included with the kit.

4.1.6 CF Card Interface (CN8: M21A-50PD-SF)

(7) in Fig. 4.1

Pin Number	Function	Pin Number	Function
1	GND	2	D3 (CF_D3)
3	D4 (CF_D4)	4	D5 (CF_D5)
5	D6 (CF_D6)	6	D7 (CF_D7)
7	CE1# (CFCE1#)	8	A10 (MA10)
9	OE# (CFOE#)	10	A9 (MA9)
11	A8 (MA8)	12	A7 (MA7)
13	VCC1 (3.3V)	14	A6 (MA6)
15	A5 (MA5)	16	A4 (MA4)
17	A3 (MA3)	18	A2 (MA2)
19	A1 (MA1)	20	A0 (MA0)
21	D0 (CF_D0)	22	D1 (CF_D1)
23	D2 (CF_D2)	24	WP (NC)
25	CD2# (NC)	26	CD1# (NC)
27	D11 (CF_D11)	28	D12 (CF_D12)
29	D13 (CF_D13)	30	D14 (CF_D14)
31	D15 (CF_D15)	32	CE2# (CFCE2#)
33	VS1# (NC)	34	IORD# (CFIORD#)
35	IOWR# (CFIOWR#)	36	WE# (MWE0#)
37	RDY/BSY (CFIREQ)	38	VCC1 (3.3V)
39	CSEL# (CSEL#)	40	VS2# (NC)
41	RESET (CFRST_CN)	42	WAIT# (CFWAIT#)
43	INPACK# (NC)	44	REG# (REG#)
45	BVD2 (BVD2/DASP)	46	BVD1 (CFSTSCHG#)
47	D8 (CF_D8)	48	D9 (CF_D9)
49	D10 (CD_D10)	50	GND

The following pins are nonfunctional on this evaluation board because the S1S65010 does not support them: VS1#, VS2#, WP, CD1#, CD2#, INPACK#, and BVD2.

5. FUNCTIONAL DESCRIPTION

Fig.5.1 and 5.2 show component locations on both sides of the main board. The following nine subsections describe their functions.

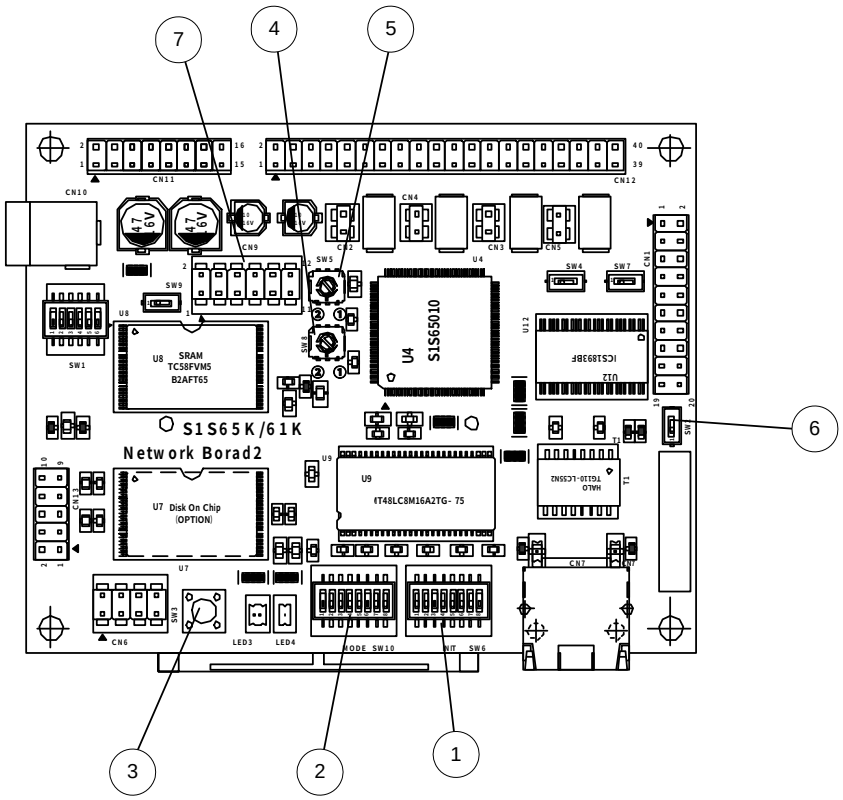


Fig.5.1 Main Board (Top View)

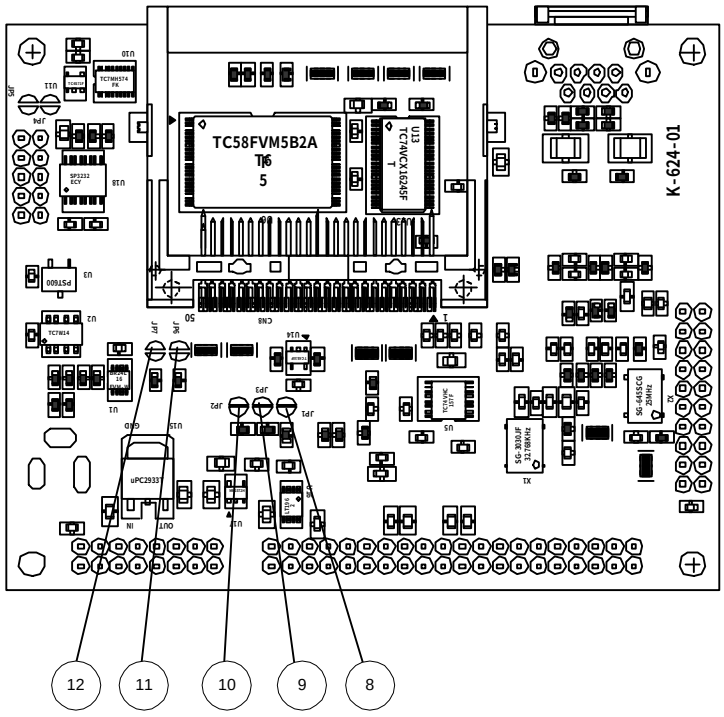


Fig.5.2 Main Board (Bottom View)

5. FUNCTIONAL DESCRIPTION

5.1 Mode Select DIP Switches (SW6)

(1) in Fig. 5.1

These switches (SW6) on the main board specify the system configuration inputs MODESEL[7:0] described in Section 4.1 of the S1S65010 Technical Manual. The following Table summarizes their function.

Table 5.1

Pin Number	Symbol	Abbreviation	Function		Note
			0 (OFF)	1 (ON)	
SW6 1-16	SW6 1	MD0 (MODESEL0)	Reserved (must be 0)		
SW6 2-15	SW6 2	MD1 (MODESEL1)	Reserved (must be 0)		
SW6 3-14	SW6 3	MD2 (MODESEL2)	Reserved (must be 0)		
SW6 4-13	SW6 4	MD3 (MODESEL3)	Reserved (must be 0)		
SW6 5-12	SW6 5	MD4 (MODESEL4)	User setting	User setting	
SW6 6-11	SW6 6	MD5 (MODESEL5)	User setting	User setting	
SW6 7-10	SW6 7	MD6 (MODESEL6)	Wired LAN connection	Wireless LAN connection	Only Linux
SW6 8-9	SW6 8	MD7 (MODESEL7)	User setting	User setting	

5.2 GPIOB DIP Switches (SW10)

(2) in Fig. 5.1

These switches (SW10) specify input to the corresponding GPIOB port pins: “1” for the OFF position and “0” for ON.

Table 5.2

Pin Number	Symbol	Abbreviation	Function		Note
			0 (OFF)	1 (ON)	
SW10 1-16	SW10 1	GPIOB0	Logical “1” input	Logical “0” input	
SW10 2-15	SW10 2	GPIOB1	Logical “1” input	Logical “0” input	
SW10 3-14	SW10 3	GPIOB2	Logical “1” input	Logical “0” input	
SW10 4-13	SW10 4	GPIOB3	Logical “1” input	Logical “0” input	
SW10 5-12	SW10 5	GPIOB4	Logical “1” input	Logical “0” input	
SW10 6-11	SW10 6	GPIOB5	Logical “1” input	Logical “0” input	
SW10 7-10	SW10 7	GPIOB6	Logical “1” input	Logical “0” input	
SW10 8-9	SW10 8	GPIOB7	Logical “1” input	Logical “0” input	

5.3 Hardware Reset Switch (SW3)

(3) in Fig. 5.1

This switch (SW3) is available for user application systems using hardware resets.

5.4 CF Card CFOE#/CFRST Select Switch (SW8)

(4) in Fig. 5.1

The (SW8) switch on this board configures the CFOE# and CFRST outputs to the CF card interface. The following Table describes the three configurations available.

If the user application system does not use CF cards, set this to the OFF position. Otherwise, set as C = (1), C = (1).

The default setting is OFF.

Display Position	C CFOE# (CF card input)	C CFRST_CN (CF card input)	Notes
(1)	MOE# (S1S65010 output)	CFRST (S1S65010 output)	
OFF	NC	NC	
(2)	GND	RESET# (HW-RESET)	

5.5 Memory Chip Select Switch (SW5)

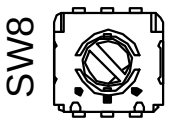
(5) in Fig. 5.1

This board includes Flash ROM and SRAM for use as external memory. The (SW5) switch on this board configures their chip select signals. The following Table describes the three configurations available.

The default setting is (1).

Display Position	C MCSB# (SRAM CS#)	C MCSA# (Flash ROM CS#)	Notes
(1)	MCS1# (S1S65010 output)	MCS0# (S1S65010 output)	
OFF	NC	NC	
(2)	MCS0# (S1S65010 output)	MCS1# (S1S65010 output)	

The following is a close-up view of the switches used in Sections 5.4 and 5.5 above. They each offer three settings: (1), (2), and OFF.



(2) (1)

5.6 Connection Switch for nSRST from JTAG In-Circuit Emulator (SW2)

(6) in Fig. 5.1

The (SW2) switch on this board controls the use of the nSRST signal from the JTAG in-circuit emulator as a system hardware reset signal.

The default setting is ON. Change this to OFF as necessary.

5.7 External Memory Control Signal Monitor Connector (CN9)

(7) in Fig. 5.1

The 12-pin connector (CN9) on this board is for monitoring control signals for external memory mounted on this evaluation board. The following Table lists the pin assignments.

Pin Number	Function	Pin Number	Function
1	MCS0#	2	MDQML
3	MCS1#	4	MDQMH
5	MCS2#	6	MCAS#
7	MOE#	8	MRAS#
9	MWE0#	10	MCLKEN
11	MWE1#	12	MCLK

5.8 External Memory Expansion SOLDER_JP (JP1-JP3)

(8) to (10) in Fig. 5.2

This evaluation board has JP2 and JP3 soldered together because it ships with 4 MB of Flash ROM in the external memory space. JP1 permits expansion to 8 MB. The default JP1 is no connection.

	Connection Source	Connection Target	Function
JP1	GPIOB6	MA22	GPIOB6 functions as MA22
JP2	GPIOD1	MA21	GPIOD1 functions as MA21
JP3	GPIOD0	MA20	GPIOD0 functions as MA20

Note: The firmware must configure the S1S65010 pins GPIOD0, GPIOD1, and GPIOB6 to match.

5.9 CF Card Interface SOLDER_JP (JP6, JP7)

(11) to (12) in Fig. 5.2

The JP6 and JP7 SOLDER_JP on this board control the connection of pull-up and pull-down resistances to this evaluation board's CF card interface BVD2/DASP signal.

	Connection Source	Connection Target	Function
JP6	BVD2/DASP	Pull_Up	Forces logic level "1" input for BVD2/DASP
JP7	BVD2/DASP	Pull_Down	Forces logic level "0" input for BVD2/DASP

6. SPECIFICATIONS

6.1 Power Supplies

The main board uses three regulators to generate internal 3.3 V, 2.7 V, 1.8 V power supplies from the 5 V ± 10% power supply connected to CN10. The following Table lists their applications.

Table 6.1 Main Board Power Supplies

	Location	Part No.	Application	Notes
3.3 V	U15	UPC2933T	S1S65010 I/O circuits and other chips on board	
2.7 V	U17	MM1572H	S1S65010 camera interface	The developer must match the parts used to camera module used.
1.8 V	U16	LT1962EMS8-1.8	S1S65010 core and analog PLL	

6.2 Operating Environment

For details on development and operating environments, see the “First Step Guide” or the “Development Environment Operating Manual.”

7. IMPORTANT USAGE NOTES

(1) This kit does not support hot-plugging of CF cards. The CF card must be in place when the power is first applied. The firmware assumes that it is always in place.

8. PARTS LISTS

8.1 Main Board Parts

The following Table lists the major parts on the main board—that is, all parts except resistors and capacitors.

Table 8.1 Main Board Parts

Name		Form (name)		Delivery destination	
TITLE	Main board	MODEL	S5U1S65K01H0300/0400	PYT.B	
PARTS NO	PARTS NAME		STANDARD		Q'TY
	PCB		K-624-01	MINICOM	1
U4	NETCAM CHIP		S1S65010 (144pinQFP)	EPSON	1
U6	FROM		TC58FVM5B2AFT65 (48pinTSOP)	Toshiba	1
U8	SRAM		CY62167DV30ll (48pinTSOP)	Cypress	1
U9	SDRAM		MT48LC8M16A2TG-75 (54pinTSOP)	MICRON	1
U12	10/100 PHYSICAL		ICS1893BF (48pinTSOP)	ICS	1
U1	SERIAL ROM		BR24L16RFVM-W (MSOP8)	Rohm	1
U3	Reset IC		PST600K (2.5V MMP3A)	Mitsumi	1
U13	Bus driver		TC74VCX16245FT (48pinTTSOP)	Toshiba	1
U15	Regulator		uPC2933T (3.3V)	NEC	1
U16			LT1962EMS8-1.8 (MS8)	Linear Technology	1
U17			MM1572H (2.7V 5pin SOT-25A)	Mitsumi	1
U18	RS232C driver		SP3232ECY (16pinTSSOP)	SIPEX	1
U2	Logic IC		TC7W14F	Toshiba	1
U5			TC74VCX157FT	Toshiba	1
U10			TC7MH574FK	Toshiba	1
U11			TC4S71F	Toshiba	1
U14			TC4S30F	Toshiba	1
X1	OSC		SG-3030JF (32.768KHz)	EPSON	1
X2	OSC		SG-645SCG (25MHz)	EPSON	1
T1	Pulse transformer		TG110-LC55N2	HALO	1
CN7	RJ45 connector		TM11R-5M2-88-LP	Hirose	1
CN10	Power supply connector		MJ-179P	Marushin Musen	1
CN2, CN3, CN4, CN5	Pin header		HW-2P-G	Mac Eight	4
CN6			HWW-4PW-G (No positioning pin)	Mac Eight	1
CN9			HWW-6PW-G (No positioning pin)	Mac Eight	1
CN13			XG8W-1031	OMRON	1
CN11			XG8W-1631	OMRON	1
CN1			XG8W-2031	OMRON	1
CN12			XG8W-4031	OMRON	1
CN11	CF card connector		MI21A-50PD-SF	Hirose	1
SW1	Tactile switch		B3FS-1000	OMRON	1
SW2, SW3, SW6	DIP switches		CHS-08B	COPAL	2
			CHS-06B	COPAL	1
			CHS-01A1	COPAL	4
			CS-4-22YA	COPAL	2

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