S1D13771 TV-Out Graphics Engine

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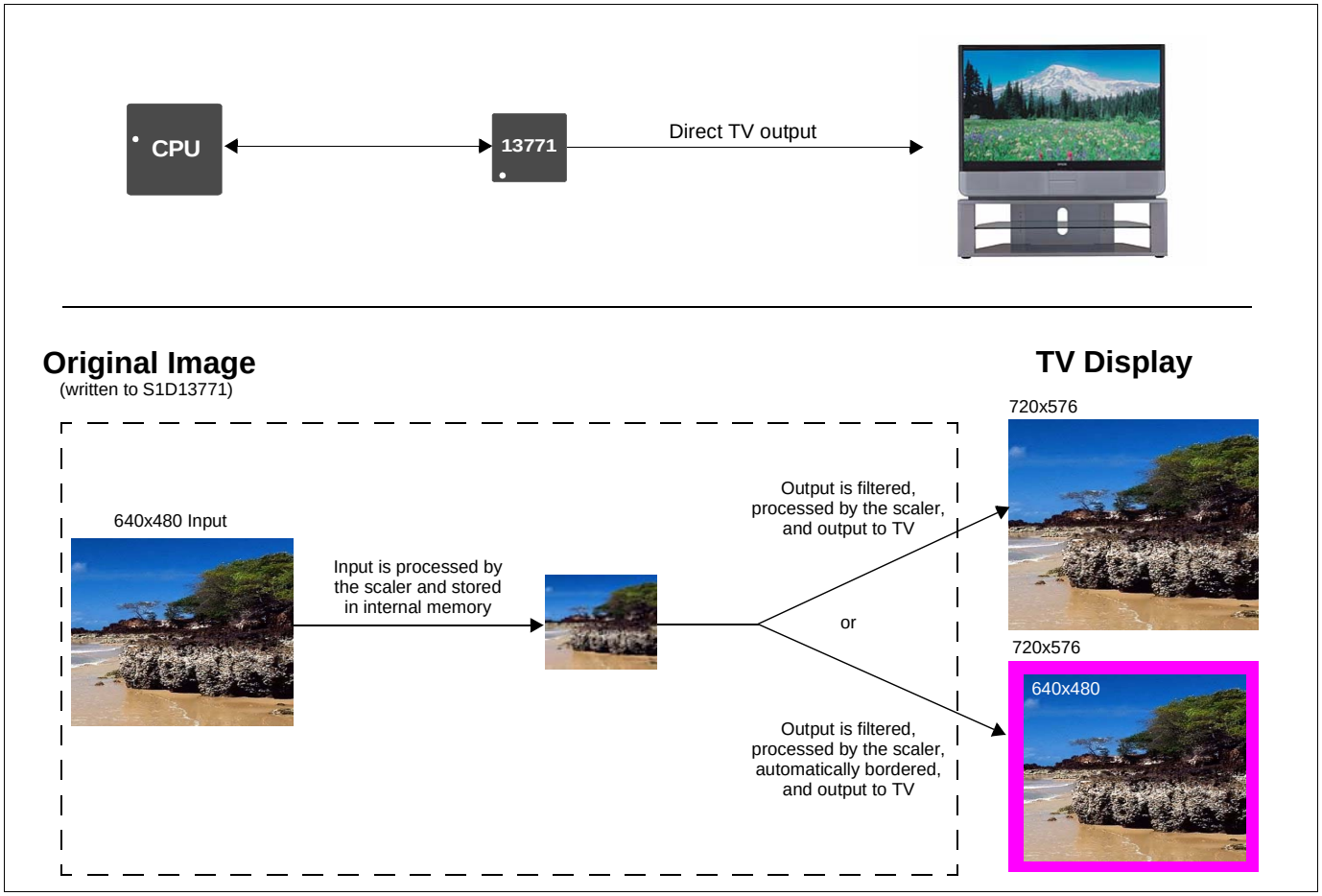
S1D13771 is an extremely low cost, low pin-count device providing direct support for TV output. A high quality internal scaler and complex TV filters allow for VGA resolution input to be stored using a minimum amount of memory, while still providing smoothly scaled output to the full resolution specified by either PAL or NTSC standards. S1D13771 is the ideal solution for cellular phone markets where TV output is a requirement.

The minimal feature set and high level of integration (embedded SRAM and high output DAC) provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring TV output, such as Mobile Communications devices.

FEATURES

- Embedded SRAM
- Low Operating Voltage
- Parallel Host Interface
- High Output DAC
- High Quality Scaler provides Bi-Cubic input/output scaling
- TV Connect/Disconnect Detection
- PAL and NTSC output
- Auto-Border / Auto-Center of TV Image with a programmable color
- 15-Tap Programmable Chrominance / Luminance Filters
- 3x3 Pixel Filter
- Software Initiated Power Save Mode

SYSTEM BLOCK DIAGRAM



DESCRIPTION

Integrated Frame Buffer

- Embedded SRAM

CPU Interface

- 8-bit Parallel Indirect Interface (Intel 80)
- Chip select is used to select device. When in-active, any input data/commands are ignored.

Input Formats

- RGB: 8:8:8, 6:6:6, 5:6:5
- YUV: 4:2:2
- All input data is processed by the scaler and stored in internal memory.

TV Output

- Composite PAL / NTSC output
- 15-Tap Programmable Chrominance / Luminance Filters
- Scaler uses Bi-Cubic scaling to scale-up or scale-down
- Auto-Border / Auto-Center
  - Programmable border color
- Square Pixel Correction
- Macrovision Protection Support (bond-out option)
- TV Connect/Disconnect Detection

Image Enhancement Engine

- 3x3 Pixel filter
  - User defined coefficients
  - Individual control for each YUV component
  - Display effects include: smooth, sharpen, blur, detail, edge enhance, emboss, contour, flicker filter, sepia, and dot crawl correction

Clock Input

- Single digital clock input used for: (18-27MHz typical)
  - Internal PLL reference clock (PLL used for system clock)
  - TV Timing (can optionally use PLL÷2)
  - DDS Timing (can optionally use PLL÷2)

Miscellaneous

- Power save mode
  - Software controllable via registers
- General purpose IO pins
  - Configurable interrupt associated with GPIO inputs
- $CORE_{VDD}$ 1.5 Volts and IO_{VDD} 1.8 to 3.3 Volts
- DAC power supply: 3.0 Volts
- Package: W-CSP 64-pin (4.46 x 4.46mm)

THEORY OF OPERATION

The S1D13771 contains an embedded SRAM frame buffer allowing up to VGA resolution to be stored using a high quality scaling algorithm. All stored images can be scaled-up or scaled-down for display on the TV using bi-cubic scaling. If the resulting image is not scaled-up to the maximum resolution defined by the TV standard, the image is automatically centered and bordered with a programmable border color.

A 3x3 pixel filter and programmable chrominance / luminance filters are provided to generate a high quality TV image.

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13771 Technical Documentation
- CPU Independent Software Utilities
- Evaluation Boards
- Royalty Free source level driver code

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