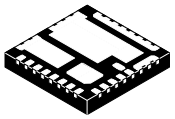
Smart Power Stage (SPS) Module

FDMF3035



PQFN31 5×5, 0.5P
CASE 483BR
SCALE 2.5:1

Description

The SPS family is **onsemi**'s next−generation, fully optimized, ultra−compact, integrated MOSFET plus driver power stage solution for high−current, high−frequency, synchronous buck, DC−DC applications. The FDMF3035 integrates a driver IC with a bootstrap Schottky diode and two power MOSFETs into a thermally enhanced, ultra−compact 5 mm x 5 mm package.

With an integrated approach, the SPS switching power stage is optimized for driver and MOSFET dynamic performance, minimized system inductance, and power MOSFET $R_{DS(ON)}$. The SPS family uses **onsemi**'s high−performance POWERTRENCH® MOSFET technology, which reduces switch ringing, eliminating the need for a snubber circuit in most buck converter applications.

A driver IC with reduced dead times and propagation delays further enhances the performance. The FDMF3035 supports diode emulation (using FCCM pin) for improved light−load efficiency. The FDMF3035 also provides a 3−state 5 V PWM input for compatibility with a wide range of PWM controllers.

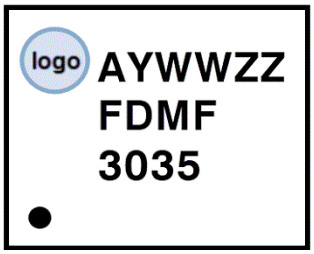
Features

- Supports PS4 Mode for IMVP−8
- Ultra−Compact 5 mm x 5 mm PQFN Copper−Clip Package with Flip Chip Low−Side MOSFET
- High Current Handling: 50 A
- 3−State 5 V PWM Input Gate Driver
- Low Shutdown Current I_{VCC} < 6 μA
- Diode Emulation for Enhanced Light Load Efficiency
- **onsemi** POWERTRENCH MOSFETs for Clean Voltage Waveforms and Reduced Ringing
- **onsemi** SyncFET™Technology (Integrated Schottky Diode) in Low−Side MOSFET
- Integrated Bootstrap Schottky Diode
- Optimized / Extremely Short Dead−Times
- Under−Voltage Lockout (UVLO) on VCC
- Optimized for Switching Frequencies up to 1.5 MHz
- Operating Junction Temperature Range: −40°C to +125°C
- **onsemi** Green Packaging and RoHS Compliance

Applications

- Notebook, Tablet PC and Ultrabook
- Servers and Workstations, V−Core and Non−V−Core DC−DC Converters
- Desktop and All−in−One Computers, V−Core and Non−V−Core DC−DC Converters
- High−Current DC−DC Point−of−Load Converters
- Small Form−Factor Voltage Regulator Modules

MARKING DIAGRAM



A = Assembly Site
Y = Year of Production, Last Number
WW = Work Week Number
ZZ = Assembly Lot Number, Last Two Numbers

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION

Part Number	Current Rating	Package	Top Mark
FDMF3035	50 A	31−Lead, Clip Bond PQFN SPS, 5.0 mm x 5.0 mm Package	FDMF3035

APPLICATION DIAGRAM

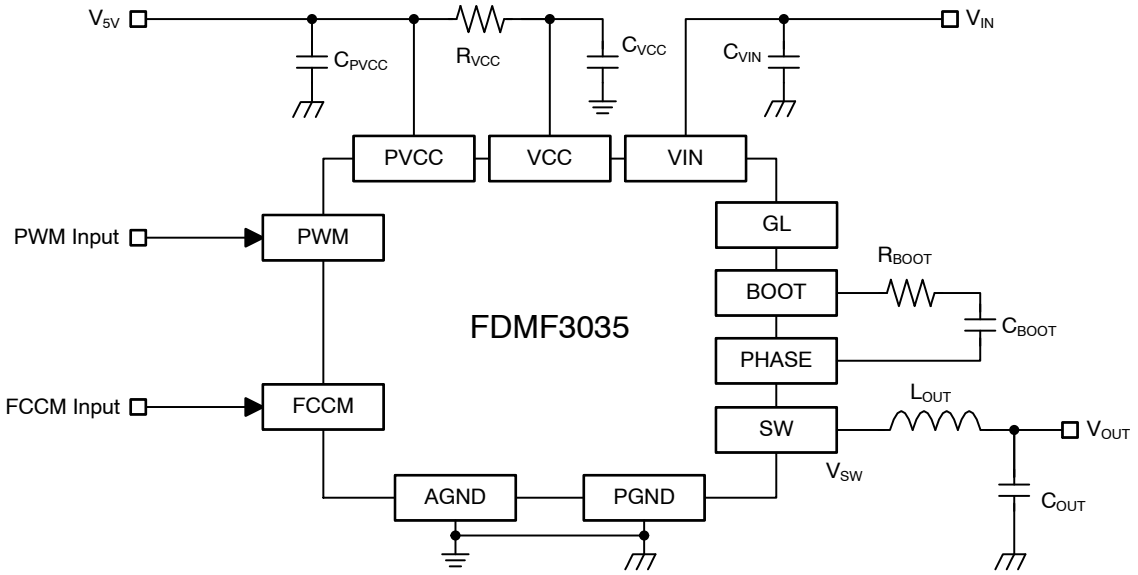


Figure 1. Typical Application Diagram

FUNCTIONAL BLOCK DIAGRAM

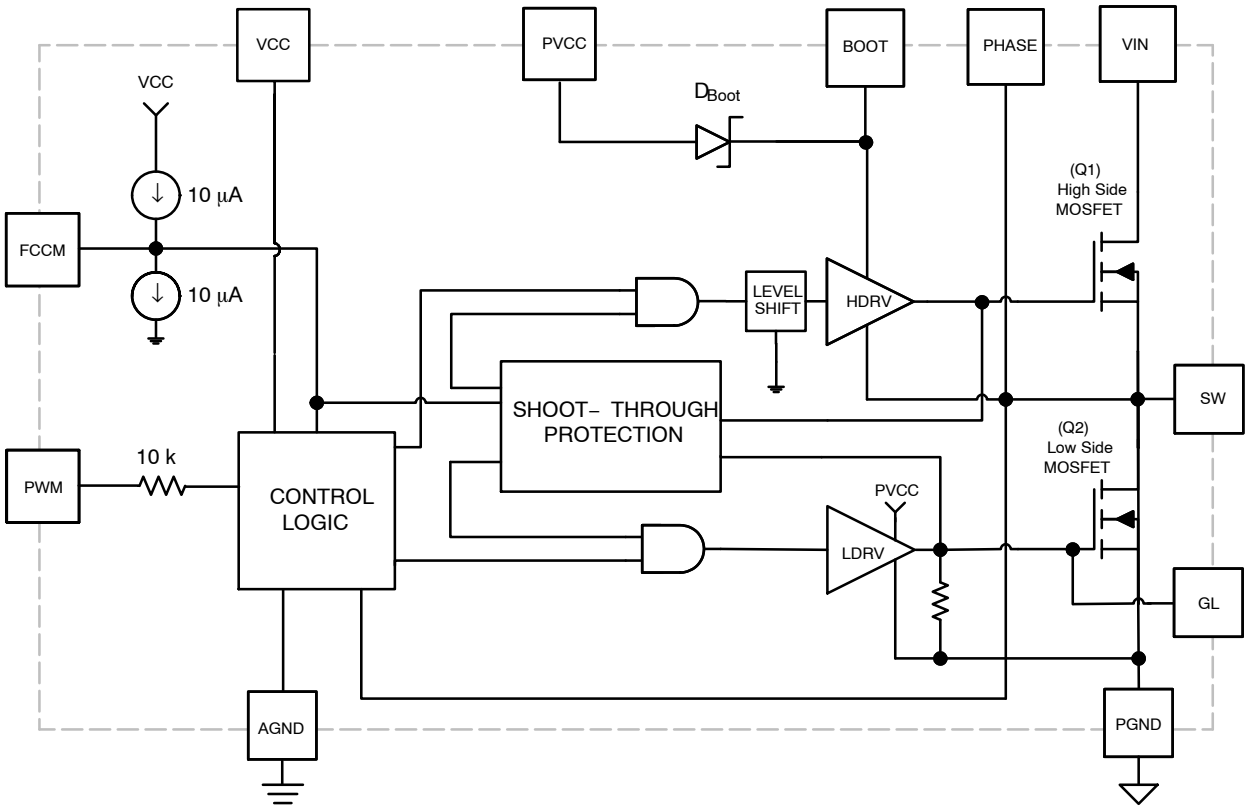


Figure 2. Functional Block Diagram

PIN CONFIGURATION

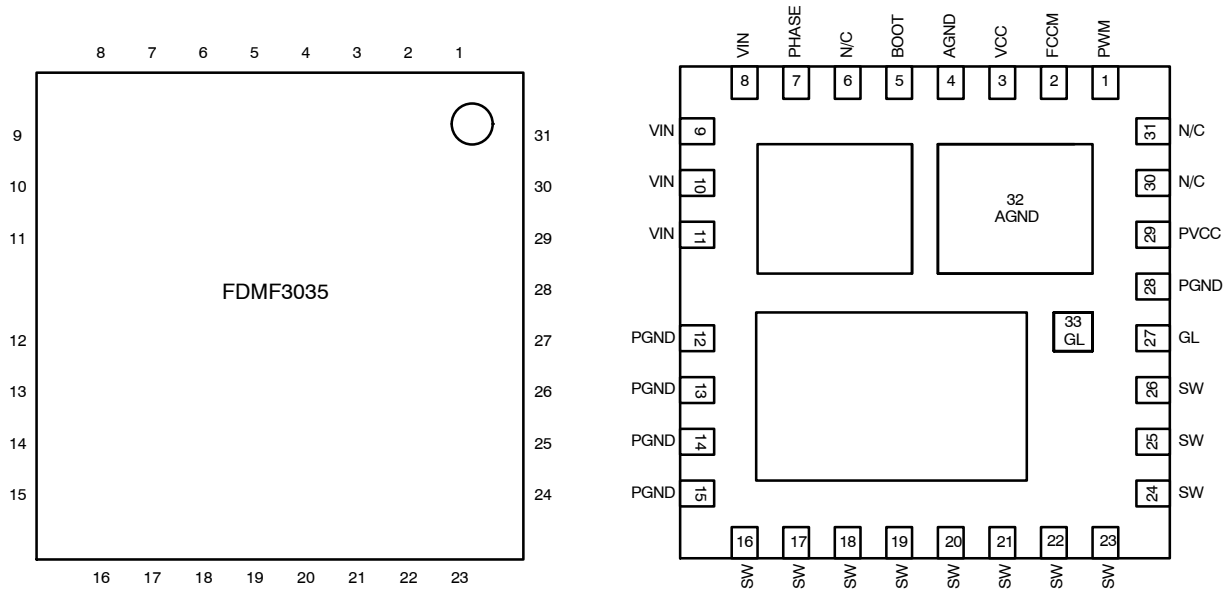


Figure 3. Pin Configuration – Top View and Transparent View

PIN DEFINITIONS

Pin #	Name	Description
1	PWM	PWM input to the gate driver IC
2	FCCM	The FCCM pin enables or disables Diode Emulation. When FCCM is LOW, diode emulation is allowed. When FCCM is HIGH, continuous conduction mode is forced. High impedance on the input of FCCM will shut down the driver IC (and module)
3	VCC	Power supply input for all analog control functions; this is the “quiet” V_{CC}
4, 32	AGND	Analog ground for analog portions of the IC and for substrate, pin 4 and pin 32 are internally fused (shorted)
5	BOOT	Supply for high−side MOSFET gate driver. A capacitor from BOOT to PHASE supplies the charge to turn on the N−channel high−side MOSFET. During the freewheeling interval (LS MOSFET on), the high side capacitor is recharged by an internal diode connected to PVCC
6, 30, 31	N/C	No connect
7	PHASE	Return connection for the boot capacitor
8~11	VIN	Power input for the power stage
12~15, 28	PGND	Power return for the power stage
16~26	SW	Switching node junction between high and low side MOSFETs; also the input into both the gate driver SW node comparator and the ZCD comparator
27, 33	GL	Low−side MOSFET gate monitor
29	PVCC	Power supply input for LS (Note 1) gate driver and boot diode

1. LS = Low Side.

ABSOLUTE MAXIMUM RATINGS (T_A = T_J = 25°C)

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage	Referenced to AGND	−0.3	7.0	V
PV_{CC}	Drive Voltage	Referenced to AGND	−0.3	7.0	V
V_{PWM}	PWM Signal Input	Referenced to AGND	−0.3	V_{CC} + 0.3	V
V_{FCCM}	Skip Mode Input	Referenced to AGND	−0.3	V_{CC} + 0.3	V
V_{GL}	Low Gate Manufacturing Test Pin	Referenced to PGND (DC)	GND − 0.3	V_{CC} + 0.3	V
		Referenced to AGND (AC < 20 ns, 10 μJ)	GND − 0.3	V_{CC} + 0.3	
V_{IN}	Power Input	Referenced to PGND	−0.3	30.0	V
V_{PHASE} V_{SW}	PHASE and SW	Referenced to PGND (DC)	−0.3	30.0	V
		Referenced to PGND (AC < 5ns)	−8.0	37.0	
V_{BOOT}	Bootstrap Supply	Referenced to AGND (DC)	−0.3	33.0	V
$V_{BOOT-PHASE}$	Boot to PHASE Voltage Boot to PHASE Voltage	DC	−0.3	7.0	V
		AC < 20 ns, 10 μJ	−0.3	9.0	V
$I_{O(AV)}$ (Note 2)	Output Current	f_{SW} = 300 kHz, V_{IN} = 12 V, V_{OUT} = 1 V		50	A
		f_{SW} = 1000 kHz, V_{IN} = 12 V, V_{OUT} = 1 V		45	
θ_{J-A}	Junction−to−Ambient Thermal Resistance			12.4	°C/W
θ_{J-PCB}	Junction−to−PCB Thermal Resistance (under **onsemi** SPS Thermal Board)			1.8	°C/W
T_A	Ambient Temperature Range		−40	+125	°C
T_J	Maximum Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range		−55	+150	°C
ESD	Electrostatic Discharge Protection	Human Body Model, JESD22−A114		1.5	kV
		Charged Device Model, JESD22−C101		2.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. $I_{O(AV)}$ is rated with testing **onsemi**'s SPS evaluation board at T_A = 25°C with natural convection cooling. This rating is limited by the peak SPS temperature, T_J = 150°C, and varies depending on operating conditions and PCB layout. This rating may be changed with different application settings.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Control Circuit Supply Voltage	4.5	5.0	5.5	V
PV_{CC}	Gate Drive Circuit Supply Voltage	4.5	5.0	5.5	V
V_{IN}	Output Stage Supply Voltage	4.5 (Note 3)	12.0	24.0 (Note 4)	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. 3.0 V V_{IN} is possible according to the application condition.
4. Operating at high V_{IN} can create excessive AC voltage overshoots on the SW−to−GND and BOOT−to−GND nodes during MOSFET switching transient. For reliable SPS operation, SW to GND and BOOT to GND must remain at or below the Absolute Maximum Ratings in the table above.

ELECTRICAL CHARACTERISTICS

(Typical value is under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V and T_A = T_J = + 25°C unless otherwise noted. Minimum / Maximum values are under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V + 10% and T_J = T_A = −40 ~ 125°C unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
BASIC OPERATION						
I_{CC_SD}	Quiescent Current with PWM and FCCM Pin Floating (PS4 Mode)	I_{CC} = I_{VCC} + I_{PVCC}, PWM = Floating, FCCM = Floating (Non−Switching)		6	11	μA
I_{CC_HIGH}	Quiescent Current with PWM Pin Floating and V_{FCCM} = 5 V	I_{CC} = I_{VCC} + I_{PVCC}, PWM = Floating, FCCM = 5 V		80		μA
I_{CC_LOW}	Quiescent Current with PWM Pin Floating and V_{FCCM} = 0 V	I_{CC} = I_{VCC} + I_{PVCC}, PWM = Floating, FCCM = 0V		120		μA
V_{UVLO_RISE}	UVLO Rising Threshold	V_{CC} Rising		3.4	3.9	V
V_{UVLO_FALL}	UVLO Falling Threshold	V_{CC} Falling	2.5	3.0		V
t_{D_POR}	POR Delay to Enable IC	V_{CC} UVLO Rising to Internal PWM Enable			15	μs
FCCM INPUT						
I_{FCCM_HIGH}	Pull−Up Current	V_{FCCM} = 5 V		50		μA
I_{FCCM_LOW}	Pull−Down Current	V_{FCCM} = 0 V		−50		μA
V_{IH_FCCM}	FCCM High Level Input Voltage	V_{CC} = PV_{CC} = 5 V	3.8			V
V_{TRI_FCCM}	FCCM 3−State Window	V_{CC} = PV_{CC} = 5 V	2.2		2.8	V
V_{IL_FCCM}	FCCM Low Level Input Voltage	V_{CC} = PV_{CC} = 5 V			1.0	V
t_{PS_EXIT}	PS4 Exit Latency	V_{CC} = PV_{CC} = 5 V			15	μs
PWM INPUT						
I_{PWM_HIGH}	Pull−Up Current	V_{FCCM} = 5 V		250		μA
I_{PWM_LOW}	Pull−Down Current	V_{FCCM} = 0 V		−250		μA
V_{IH_PWM}	PWM High Level Input Voltage	V_{CC} = PV_{CC} = 5 V	4.1			V
V_{TRI_PWM}	PWM 3−State Window	V_{CC} = PV_{CC} = 5 V	1.6		3.4	V
V_{IL_PWM}	PWM Low Level Input Voltage	V_{CC} = PV_{CC} = 5 V			0.7	V
$t_{D_HOLD-OFF}$	3−State Shut−off Time	V_{CC} = PV_{CC} = 5 V, T_J = 25°C	100	175	250	ns
PWM PROPAGATION DELAYS & DEAD TIMES (V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, F_{SW} = 1 MHz, I_{OUT} = 20 A, T_A = 25°C)						
t_{PD_PHGLL}	PWM HIGH Propagation Delay	PWM Going HIGH to GL Going LOW, V_{IH_PWM} to 90% GL		25		ns
t_{PD_PLGHL}	PWM LOW Propagation Delay	PWM Going LOW to GH (Note 5) Going LOW, V_{IL_PWM} to 90% GH		15		ns
t_{PD_PHGHH}	PWM HIGH Propagation Delay (FCCM Held LOW)	PWM Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH (FCCM = LOW, I_L = 0, Assumes DCM)		15		ns
t_{PD_TSGHH}	Exiting 3−State Propagation Delay	PWM (from 3−State) Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH		35		ns
t_{PD_TSGLH}	Exiting 3−State Propagation Delay	PWM (from 3−State) Going LOW to GL Going HIGH, V_{IL_PWM} to 10% GL		35		ns
t_{D_DEADON}	LS Off to HS On Adaptive Dead Time	SW ≤ −0.2 V with GH ≤ 10%, PWM Transition LOW to HIGH		25		ns
$t_{D_DEADOFF}$	HS Off to LS On Adaptive Dead Time	SW ≤ −0.2 V with GL ≤ 10%, PWM Transition HIGH to LOW		20		ns

ELECTRICAL CHARACTERISTICS

(Typical value is under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V and T_A = T_J = + 25°C unless otherwise noted. Minimum / Maximum values are under V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V + 10% and T_J = T_A = −40 ~ 125°C unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
HIGH−SIDE DRIVER (HDRV, V_{CC} = PV_{CC} = 5 V)						
R_{SOURCE_GH}	Output Impedance, Sourcing	Source Current = 100 mA		1.0	2.5	Ω
I_{SOURCE_GH}	Output Sourcing Peak Current	GH = 2.5 V		2		A
R_{SINK_GH}	Output Impedance, Sinking	Sink Current = 100 mA		1.0	2.5	Ω
I_{SINK_GH}	Output Sinking Peak Current	GH = 2.5 V		4		A
t_{R_GH}	GH Rise Time	GH = 10% to 90%, C_{LOAD} = 3.0 nF		8		ns
t_{F_GH}	GH Fall Time	GH = 90% to 10%, C_{LOAD} = 3.0 nF		8		ns
LOW−SIDE DRIVER (LDRV, V_{CC} = PV_{CC} = 5 V)						
R_{SOURCE_GL}	Output Impedance, Sourcing	Source Current = 100 mA		1.0	2.5	Ω
I_{SOURCE_GL}	Output Sourcing Peak Current	GL = 2.5 V		2		A
R_{SINK_GL}	Output Impedance, Sinking	Sink Current = 100 mA		0.5		Ω
I_{SINK_GL}	Output Sinking Peak Current	GL = 2.5 V		4		A
t_{R_GL}	GL Rise Time	GL = 10% to 90%, C_{LOAD} = 3.0 nF		8		ns
t_{F_GL}	GL Fall Time	GL = 90% to 10%, C_{LOAD} = 3.0 nF		4		ns
BOOT DIODE						
V_F	Forward−Voltage Drop	I_F = 10 mA		0.6		V
V_R	Breakdown Voltage	I_R = 1 mA	30			V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. GH = Gate High, internal gate pin of the high−side MOSFET.

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted)

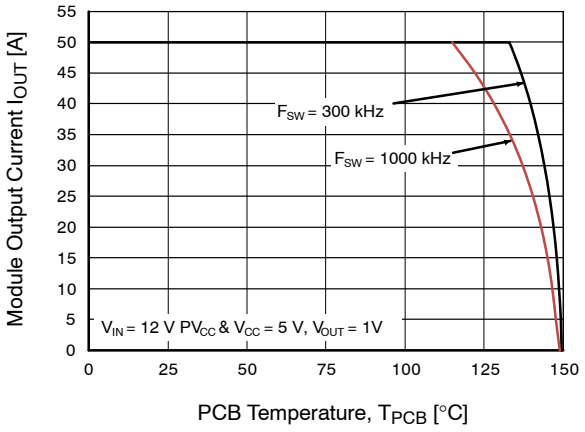


Figure 4. Safe Operating Area with 12 V_{IN}

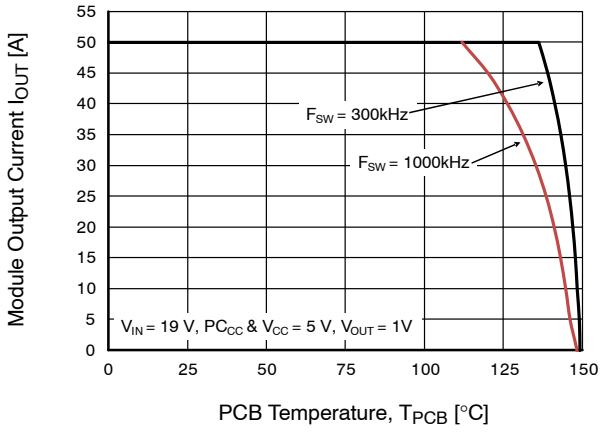


Figure 5. Safe Operating Area with 19 V_{IN}

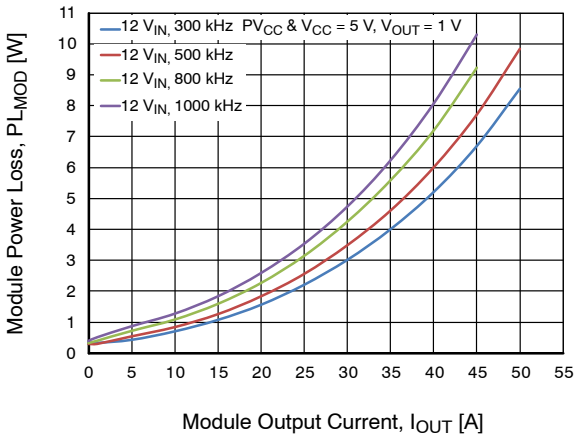


Figure 6. Power Loss vs. Output Current with 12 V_{IN}

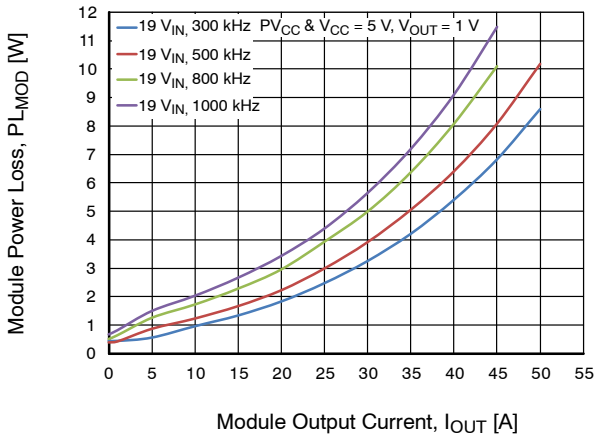


Figure 7. Power Loss vs. Output Current with 19 V_{IN}

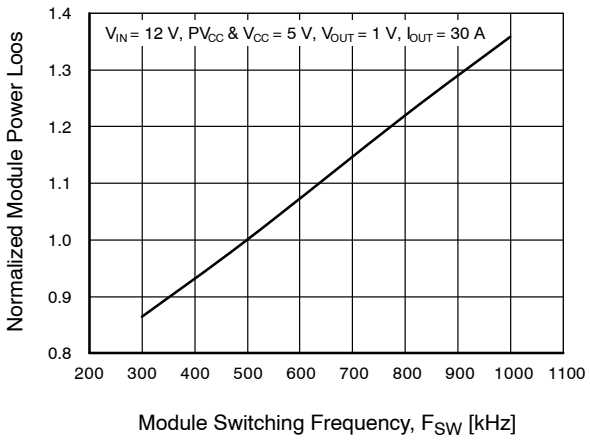


Figure 8. Power Loss vs. Switching Frequency

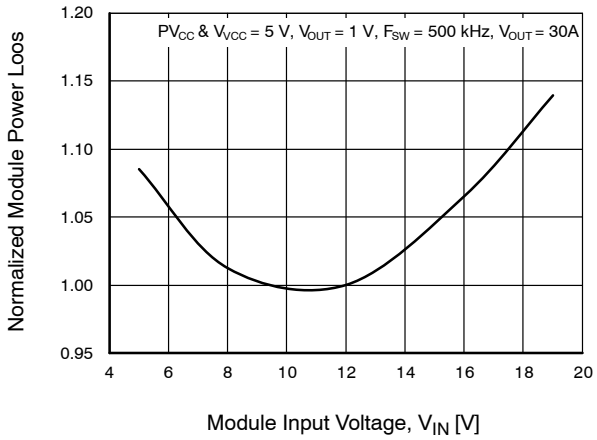


Figure 9. Power Loss vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted)

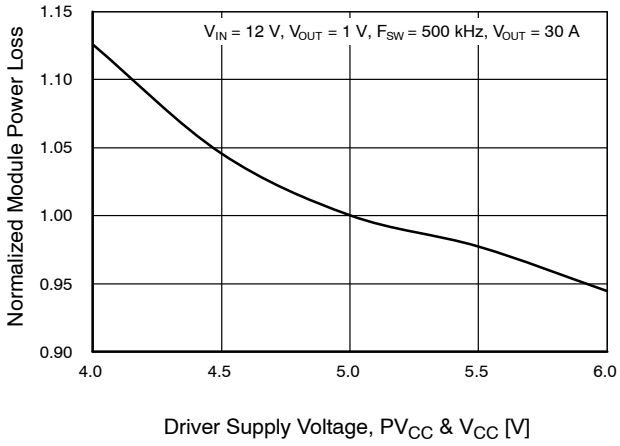


Figure 10. Power Loss vs. Driver Supply Voltage

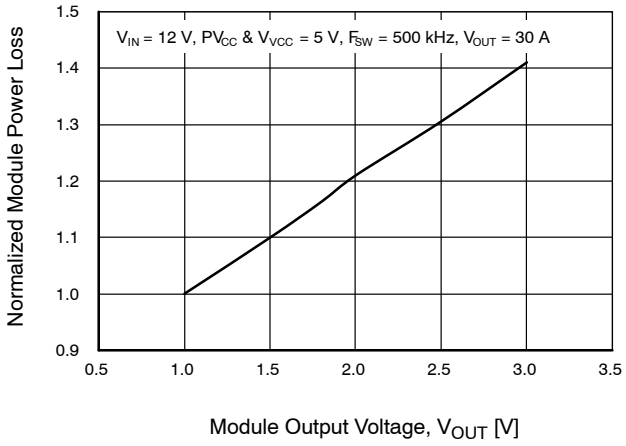


Figure 11. Power Loss vs. Output Voltage

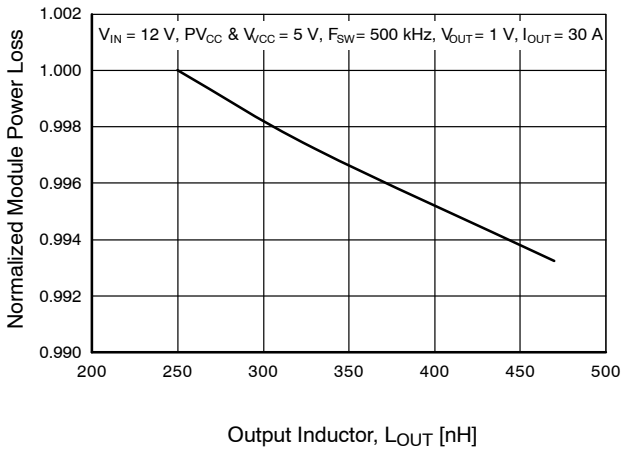


Figure 12. Power Loss vs. Output Inductor

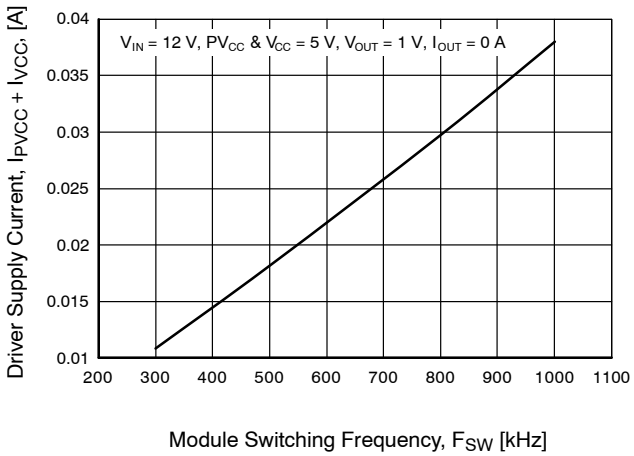


Figure 13. Driver Supply Current vs. Switching Frequency

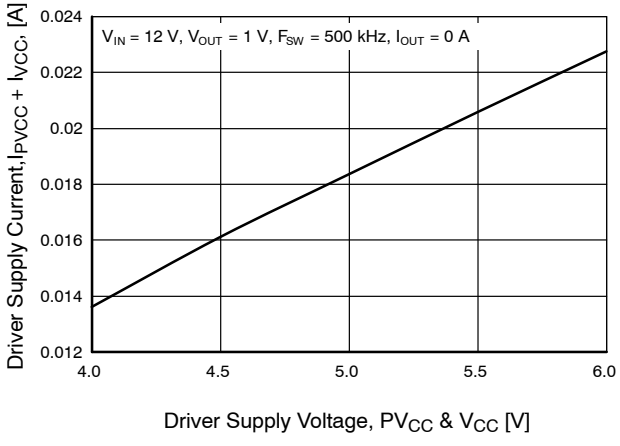


Figure 14. Driver Supply Current vs. Driver Supply Voltage

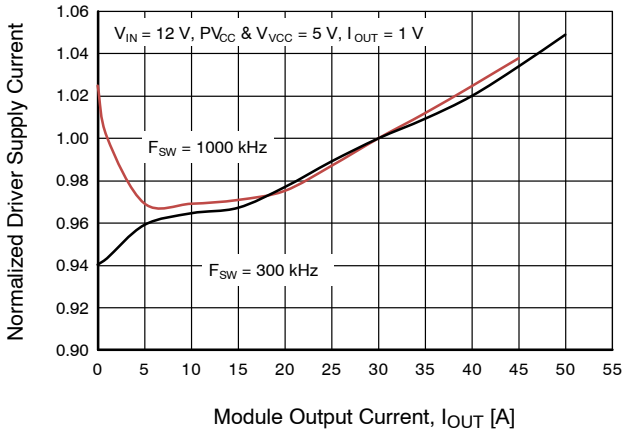


Figure 15. Driver Supply Current vs. Output Current

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted)

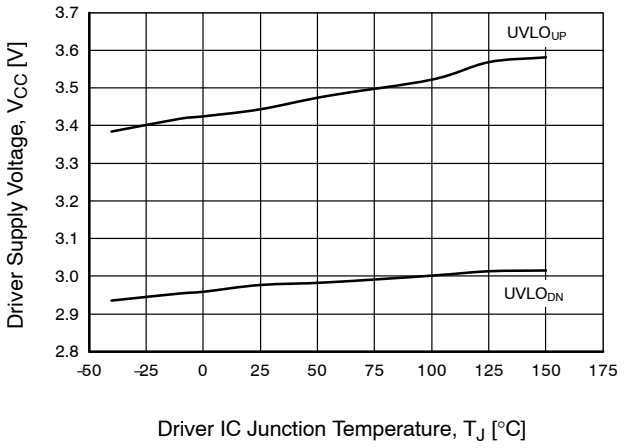


Figure 16. UVLO Threshold vs. Temperature

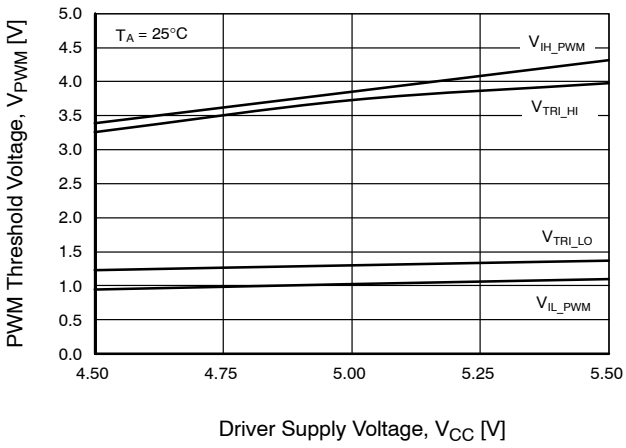


Figure 17. PWM Threshold vs. Driver Supply Voltage

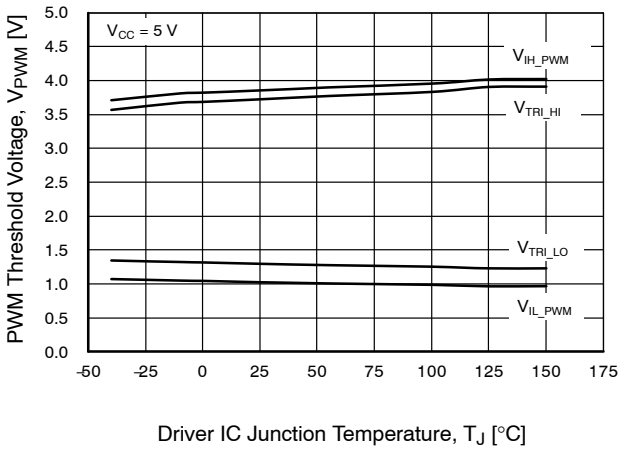


Figure 18. PWM Threshold vs. Temperature

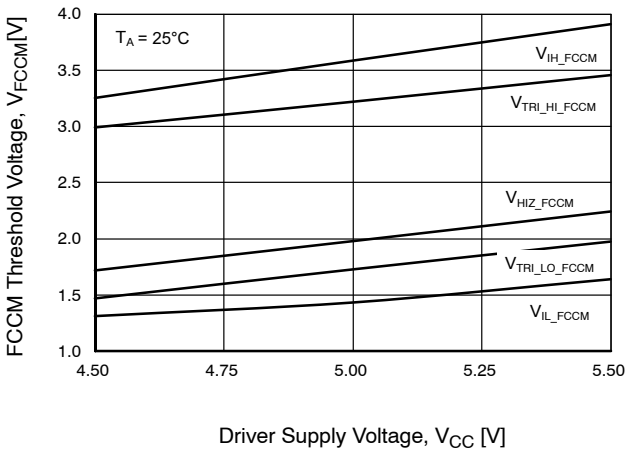


Figure 19. FCCM Threshold vs. Driver Supply Voltage

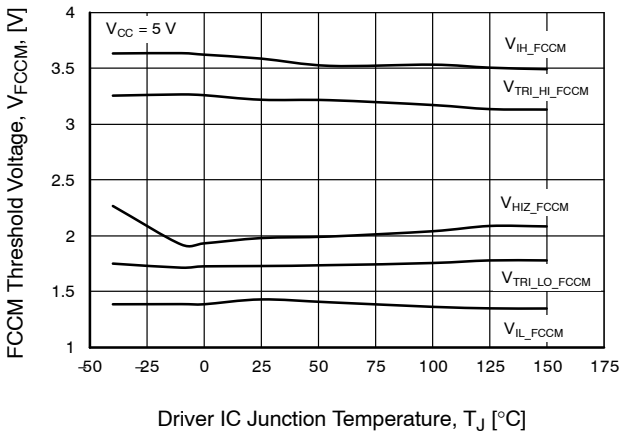


Figure 20. FCCM Threshold vs. Temperature

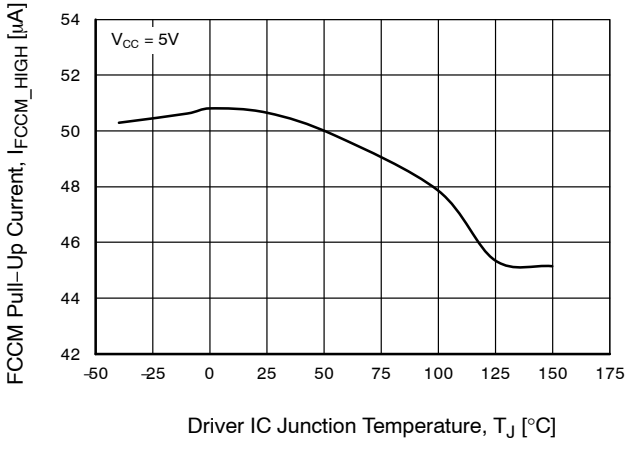


Figure 21. FCCM Pull−Up Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Test Conditions: V_{IN} = 12 V, V_{CC} = PV_{CC} = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH, T_A = 25°C and natural convection cooling, unless otherwise noted)

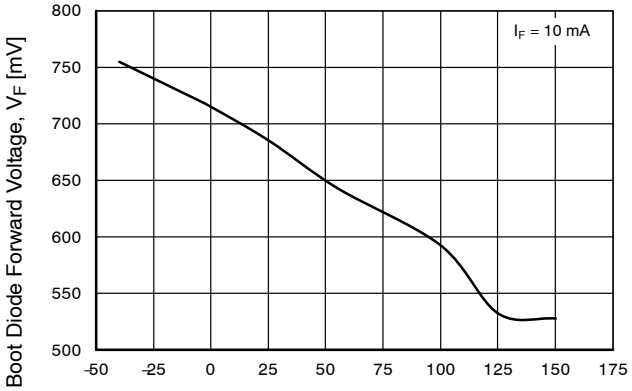


Figure 22. Boot Diode Forward Voltage vs. Temperature

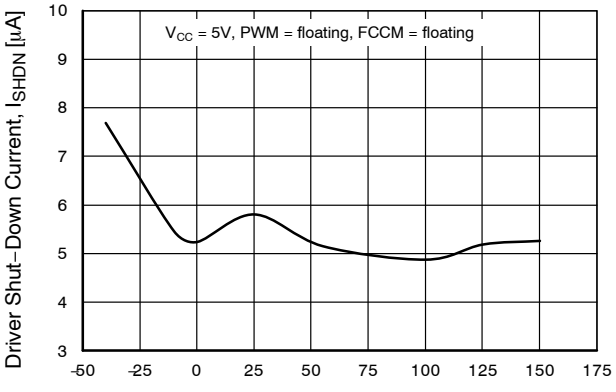


Figure 23. Driver Shutdown Current vs. Temperature

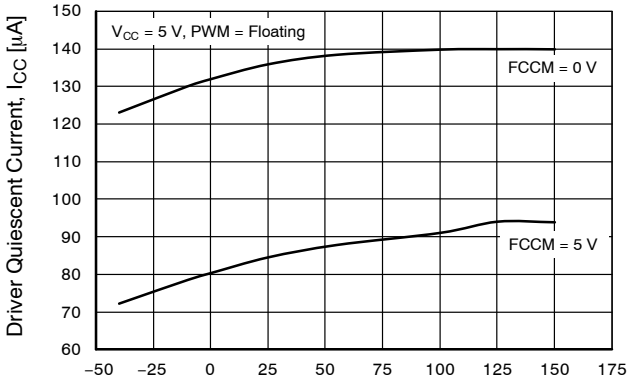
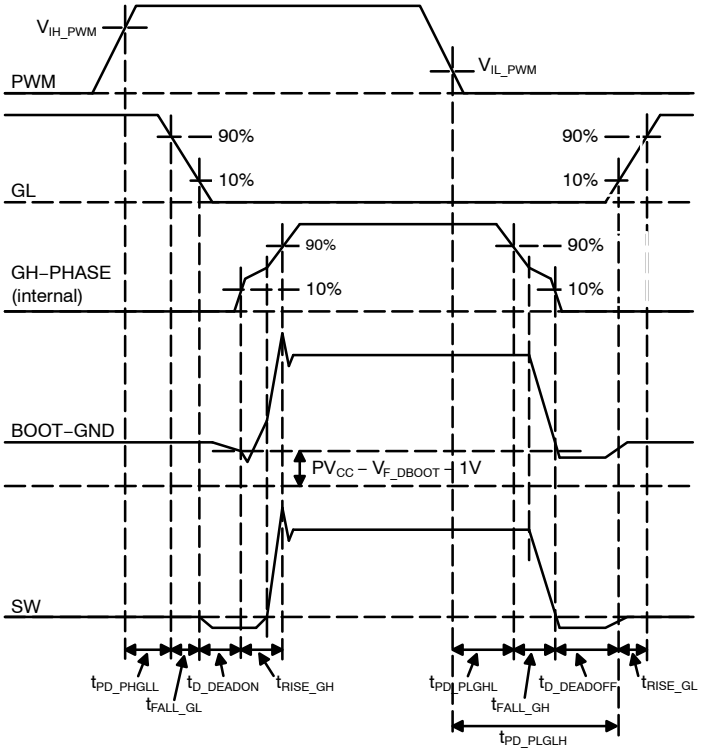


Figure 24. Driver Quiescent Current vs. Temperature



t_{PD_PHGLL} = PWM HI to GL LOW, V_{IH_PWM} to 90% GL

t_{FALL_GL} = 90% GL to 10% GL

t_{D_DEADON} = LS Off to HS On Dead Time, 10% GL to $V_{BOOT-GND}$ <= PV_{CC} − V_{F_DBOOT} − 1 V

t_{RISE_GH} = 10% GH to 90% GH, $V_{BOOT-GND}$ <= PV_{CC} − V_{F_DBOOT} − 1V to V_{SW_PEAK}

t_{PD_PLGHL} = PWM LOW to GH LOW, V_{IL_PWM} to 90% GH, t_{PD_PLGLH} − $t_{D_DEADOFF}$ − t_{FALL_GH}

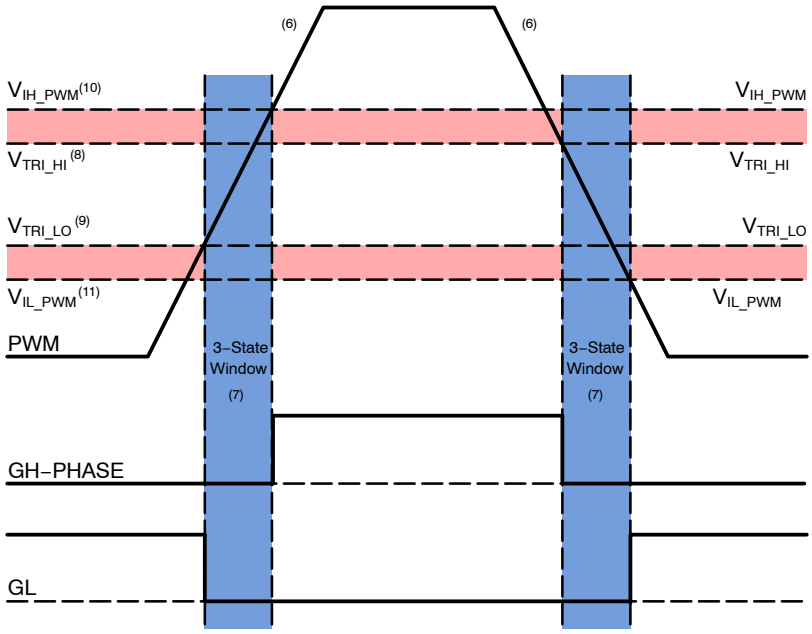
t_{FALL_GH} = 90% GH to 10% GH

$t_{D_DEADOFF}$ = HS Off to LS On Dead Time, V_{SW} <= 0 V to 10% GL

t_{PD_PLGLH} = PWM LOW to GL HI, V_{IL_PWM} to 10% GL

t_{RISE_GL} = 10% GL to 90% GL

Figure 25. PWM Timing Diagram



NOTES:
6. The timing diagram in Figure 26 assumes very slow ramp on PWM.
7. Slow ramp of PWM implies the PWM signal remains within the 3−state window for a time >>> $t_{D_HOLD-OFF}$.
8. V_{TRI_HI} = PWM trip level to enter 3−state on PWM falling edge.
9. V_{TRI_LO} = PWM trip level to enter 3−state on PWM rising edge.
10. V_{IH_PWM} = PWM trip level to exit 3−state on PWM rising edge and enter the PWM HIGH logic state.
11. V_{IL_PWM} = PWM trip level to exit 3−state on PWM falling edge and enter the PWM LOW logic state.

Figure 26. PWM Threshold Definition

FUNCTIONAL DESCRIPTION

The SPS FDMF3035 is a driver−plus−MOSFET module optimized for the synchronous buck converter topology. A PWM input signal is required to properly drive the high−side and the low−side MOSFETs. The part is capable of driving speed up to 1.5 MHz.

Power−On Reset (POR & UVLO)

The FDMF3035 incorporates a POR feature that ensures both LDRV and HDRV are forced inactive (LDRV = HDRV = 0) until UVLO > 3.4 V (typical rising threshold). UVLO is performed on VCC (not on PVCC or VIN).

After all gate drive blocks are fully powered on and have finished the startup sequence, the internal driver IC EN_PWM signal is released HIGH, enabling the driver outputs. Once the driver POR has finished, the driver follows the state of the PWM signal (it is assumed that at startup the controller is either in a high− impedance state or forcing the PWM signal to be within the driver 3−state window).

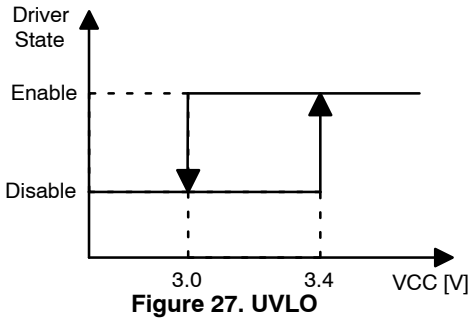


Figure 27. UVLO

3−State PWM Input

The FDMF3035 incorporates a 3−state 5 V PWM input gate drive design. The 3−state gate drive has both logic HIGH and LOW levels, along with a 3−state shutdown window. When the PWM input signal enters and remains within the 3−state window for a defined hold−off time ($t_{D_HOLD-OFF}$), both GL and GH are pulled LOW. This feature enables the gate drive to shutdown both the high−side and the low−side MOSFETs to support features such as phase shedding, a common feature on multi−phase voltage regulators.

Table 1. PWM LOGIC TABLE

PWM	FCCM	GH	GL
3−state	1	0	0
0	1	0	1
1	1	1	0

FCCM

The FCCM pin can be used to control Diode Emulation or used to shutdown the driver IC (with I_{CC} < 6 μA, I_{CC} = current consumed by VCC and PV_{CC}). When FCCM is LOW, diode emulation is allowed. When FCCM is HIGH, continuous conduction mode is forced. High impedance on the input of FCCM shuts down the driver IC (and module).

Table 2. FCCM LOGIC TABLE

PWM	FCCM	GH	GL	Driver Enable State
x	3−State	0	0	0 (I_{CC} < 6 μA)
3−State	0	0	0	1
3−State	1	0	0	1
0	0	0	1 when IL > 0 0 when IL < 0	1
1	0	1	0	1
0	1	0	1	1
1	1	1	0	1

(FCCM = 1 → Forced CCM)

Setting the FCCM pin to a HIGH state will allow for forced CCM operation. During forced CCM, the FDMF3035 will always follow the PWM signal and allow for negative inductor current.

(FCCM = 0 → Diode Emulation / DCM)

Setting the FCCM pin to a LOW state will enable diode emulation. Diode emulation allows for higher converter efficiency under light load situations. With diode emulation is activated, the FDMF3035 will detect the zero current crossing of the output inductor (at light loads) and will turn off low side MOSFET gate GL to prevent negative inductor current from flowing. Diode emulation ensures discontinuous conduction mode (DCM) operation. Diode emulation is asynchronous to the PWM signal. Therefore, the FDMF3035 will respond to the FCCM input immediately after it changes state.

(FCCM = HiZ → Shutdown)

Setting the FCCM pin to a HIGH impedance state (HiZ) will shutdown the driver IC with I_{CC} < 6 μA. The FDMF3035 requires a startup latency time of (<15 μsec) when exiting a HiZ FCCM state. Low I_{CC} driver shutdown is often needed to support power saving modes in multi−phase voltage regulator designs.

Power Sequence

The FDMF3035 requires four (4) input signals to perform normal switching operation: VIN, VCC / PVCC, PWM, and FCCM.

The VIN pins are tied to the system main DC power rail.

The PVCC and VCC pins are typically powered from the same 5 V source. These pins can be either tied directly together or tied together through an external RC filter. The filter resistor / capacitor is used to de−couple the switching noise from PVCC to VCC. Refer to Figure 1 for RC filter schematic.

The FCCM pin can be tied to the VCC rail with an external pull−up resistor and it will maintain HIGH once the VCC rail turns on. Or the FCCM pin can be directly tied to the PWM controller for other purposes.

SYNCHRONOUS BUCK OPERATING MODES

Continuous Current Mode with Positive Inductor Current (CCM1)

This condition is typical of a moderate−to−heavily loaded power stage. During this mode, the inductor current is always flowing towards the output capacitor. The high− side MOSFET is hard−switching during the turn−on and turn−off events. The low−side MOSFET acts a synchronous rectifier.

Continuous Current Mode with Negative Inductor Current (CCM2)

This operating mode can occur during two situations:

1. A converter load transient may force the power stage to pull energy from the output capacitors and deliver the energy back to the input capacitors (Boost Mode). This situation is common in synchronous buck applications that require output voltage load−line positioning.
   During this mode, the negative inductor current (current flowing into FDMF3035 SW node) may become large and persist for many cycles. This situation causes the low−side MOSFET to hard switch and the high−side MOSFET acts as a synchronous rectifier. It is highly recommended to check peak SW node voltage stress during any situation that can generate large negative inductor currents
2. A power stage that is operating in forced CCM mode with lighter converter loads. Here, the inductor peak−to−peak ripple current is greater than two times the load current and the inductor current is flowing both positive and negative in a switching cycle

Discontinuous Current Mode (DCM)

This condition is typical of a lightly loaded power stage. During DCM, the high−side MOSFET turns on into an un−energized out filter inductor (i.e. zero inductor current). The inductor current ramps up during the high− side MOSFET on−time and is then allowed to ramp back down to aero amps during the low−side on−time (i.e inductor current returns to zero every switching cycle.

High−Side Driver

The high−side driver (HDRV) is designed to drive a floating N−channel MOSFET (Q1). The bias voltage for the high−side driver is developed by a bootstrap supply circuit, consisting of the internal Schottky diode and external bootstrap capacitor (CBOOT). During startup, the SW node should be held at PGND, allowing CBOOT to charge to PVCC through the internal bootstrap diode. When the PWM input goes HIGH, HDRV begins to charge the gate of the high−side MOSFET (internal GH pin). During this transition, the charge is removed from the CBOOT and delivered to the gate of Q1. As Q1 turns on, SW rises to VIN, forcing the BOOT pin to VIN + VBOOT, which provides sufficient VGS enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling HDRV to SW. CBOOT is then recharged to PVCC when the SW falls to PGND. HDRV output is in phase with the PWM input. The high−side gate is held LOW when the driver is disabled or the PWM signal is held within the 3−state window for longer than the 3−state hold−off time, tD_HOLD−OFF.

Low−Side Driver

The low−side driver (LDRV) is designed to drive the gate−source of a ground−referenced, low−RDS(ON), N−channel MOSFET (Q2). The bias for LDRV is internally connected between the PVCC and AGND. When the driver is enabled, the driver output is 180° out of phase with the PWM input. When the driver is disabled (FCCM = 0 V), LDRV is held LOW.

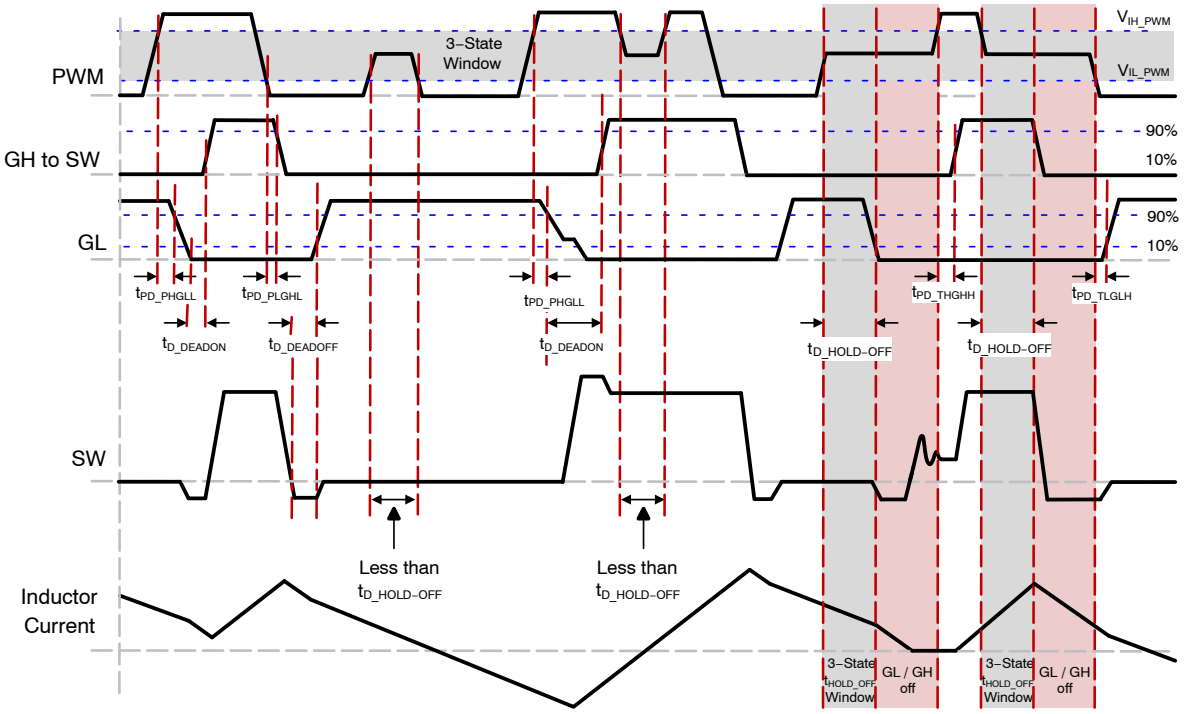


Figure 28. PWM 3−State Timing Diagram (FCCM Held HIGH)

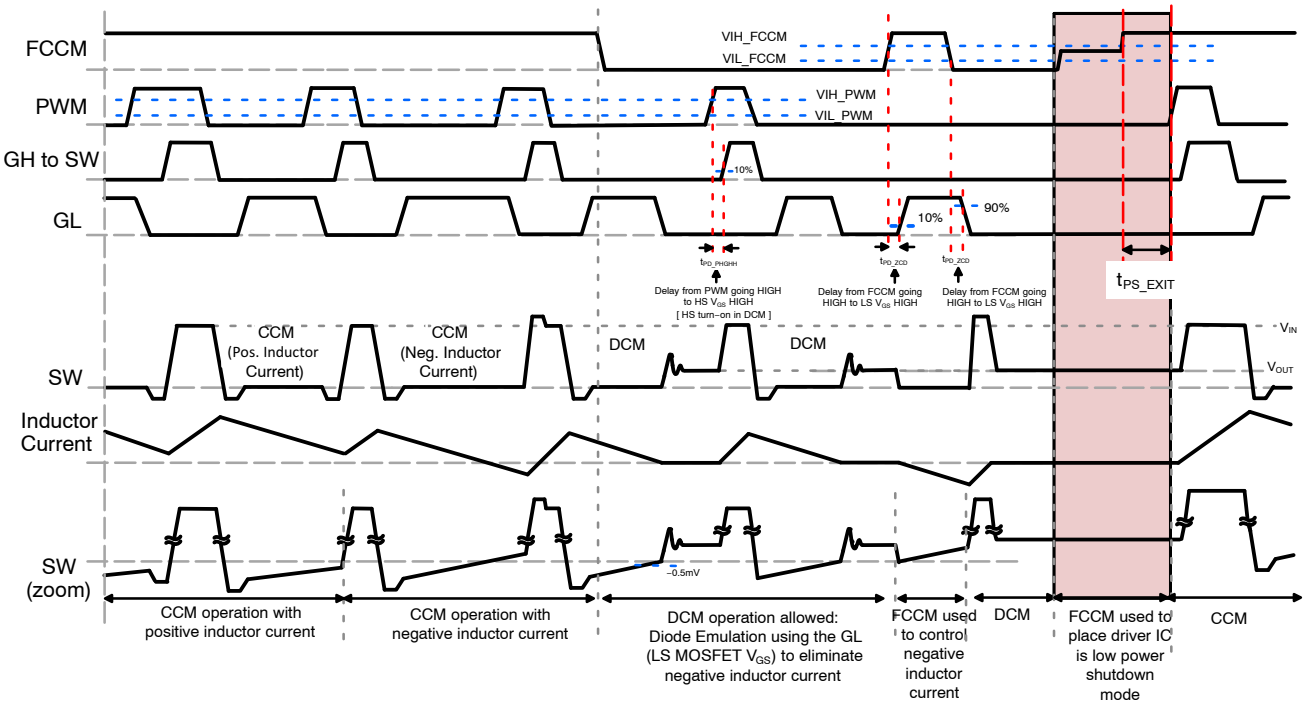


Figure 29. 3−State Timing Diagram

APPLICATION INFORMATION

Decoupling Capacitor for PVCC & VCC

For the supply inputs (PVCC and VCC pins), local decoupling capacitors are required to supply the peak driving current and to reduce noise during switching operation. Use at least 0.68 ~ 1 μF / 0402 ~ 0603 / X5R ~ X7R multi−layer ceramic capacitors for both power rails. Keep these capacitors close to the PVCC and VCC pins and PGND and AGND copper planes. If the de−coupling capacitors need to be located on the bottom side of board, place through−hole vias on each pad connecting top side and bottom side PVCC and VCC nodes with low impedance current paths, see Figure 31 and Figure 32.

The supply voltage range on PVCC and VCC is 4.5 V ~ 5.5 V, and typically 5 V for normal applications.

R−C Filter on VCC

The PVCC pin provides power to the gate drive of the high−side and low−side power MOSFETs. In most cases, PVCC can be connected directly to VCC, which is the pin that provides power to the analog and logic blocks of the driver. To avoid switching noise injection from PVCC into VCC, a filter resistor can be inserted between PVCC and VCC decoupling capacitors.

Recommended filter resistor value range is 0 ~ 4.7 Ω, typically 0 Ω for most applications.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}). A bootstrap capacitor of 0.1 ~ 0.22 μF / 0402 ~ 0603 / X5R ~ X7R is usually appropriate for most switching applications. A series bootstrap resistor may be needed for specific applications to lower high−side MOSFET switching speed. The boot resistor is required when the SPS is switching above 15 V V_{IN}; when it is effective at controlling VSW overshoot. R_{BOOT} value from zero to 4.7 Ω is typically recommended to reduce excessive voltage spike and ringing on the SW node. A higher R_{BOOT} value can cause lower efficiency due to high switching loss of high−side MOSFET.

Do not add a capacitor or resistor between the BOOT pin and GND.

PWM (Input)

The PWM pin recognizes three different logic levels from PWM controller: HIGH, LOW, and 3−state. When the PWM pin receives a HIGH command, the gate driver turns on the high−side MOSFET. When the PWM pin receives a LOW command, the gate driver turns on the low−side MOSFET. When the PWM pin receives a voltage signal inside of the 3−state window (V_{TRI_Window}) and exceeds the 3−state hold−off time, the gate driver turns off both high−side and low−side MOSFETs. To recognize the high−impedance 3−state signal from the controller, the PWM pin has an internal resistor divider from VCC to PWM to AGND. The resistor divider sets a voltage level on the PWM pin inside the 3−state window when the PWM signal from the controller is high−impedance.

FCCM (Input)

When the FCCM pin is set HIGH, the driver IC Zero Cross Detect (ZCD) comparator is disabled and the high−side and low−side MOSFETs switch in FCCM (Forced CCM) and follows the PWM signal. When the FCCM pin is set LOW, the low−side MOSFET turns off when the SPS driver detects negative inductor current during the low−side MOSFET turn−on period. This operating mode is commonly referred to as diode emulation. The diode emulation feature allows for higher converter efficiency during light−load condition and PFM / DCM operation.

Applications that require diode emulation and/or low shutdown current should actively drive the FCCM pin from a PWM controller. Do not add any noise filter capacitor on the FCCM pin.

POWER LOSS AND EFFICIENCY

Figure 30 shows an example diagram for power loss and efficiency measurement.

Power loss calculation and equation examples:

$P_{IN} = (V_{IN} \times I_{IN}) + (V_{CC} \times I_{CC})$ [W]

$P_{SW} = V_{SW} \times I_{OUT}$ [W]

$P_{OUT} = V_{OUT} \times I_{OUT}$ [W]

$P_{LOSS_MODULE} = P_{IN} - P_{SW}$ [W]

$P_{LOSS_TOTAL} = P_{IN} - P_{OUT}$ [W]

$EFFI_{MODULE} = (P_{SW} / P_{IN}) \times 100$ [%]

$EFFI_{TOTAL} = (P_{OUT} / P_{IN}) \times 100$ [%]

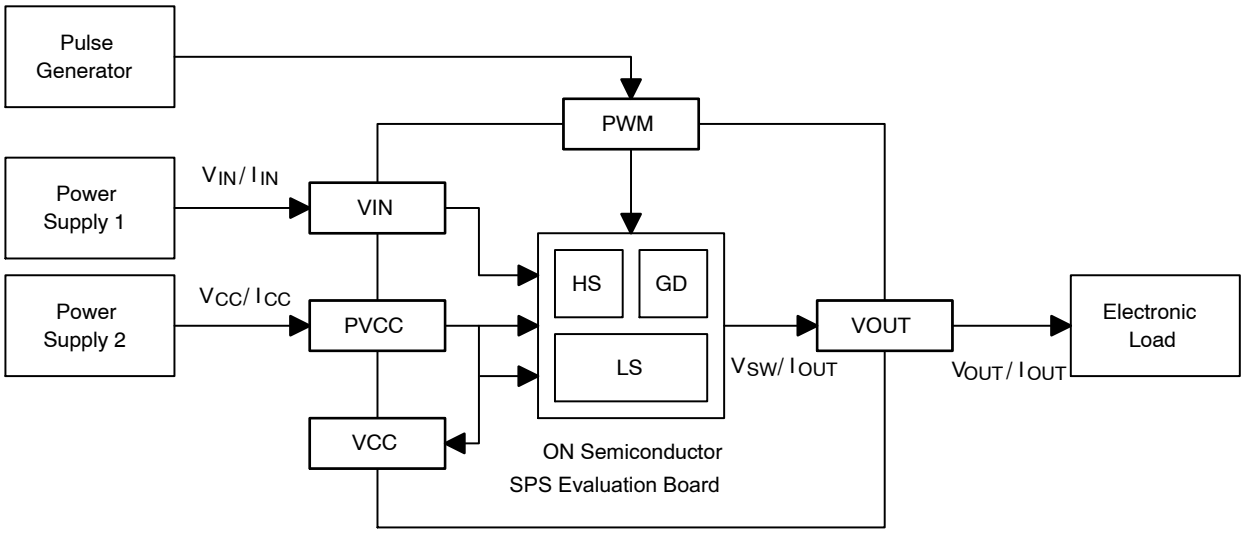


Figure 30. Power Loss and Efficiency Measurement Diagram

PCB LAYOUT GUIDELINE

Figure 31 and Figure 32 provide an example of single−phase layout for the FDMF3035 and critical components. All of the high−current paths; such as VIN, SW, VOUT, and GND coppers; should be short and wide for low parasitic inductance and resistance. This helps achieve a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Input ceramic bypass capacitors must be close to the VIN and PGND pins. This reduces the high−current power loop inductance and the input current ripple induced by the power MOSFET switching operation.

The SW copper trace serves two purposes. In addition to being the high−frequency current path from the SPS package to the output inductor, it serves as a heat sink for the low−side MOSFET. The trace should be short and wide enough to present a low−impedance path for the high−frequency, high−current flow between the SPS and the inductor. The short and wide trace minimizes electrical losses and SPS temperature rise. The SW node is a high−voltage and high−frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace acts as a heat sink for the low−side MOSFET, balance using the largest area possible to improve SPS cooling while maintaining acceptable noise emission.

An output inductor should be located close to the FDMF3035 to minimize the power loss due to the SW copper trace. Care should also be taken so the inductor dissipation does not heat the SPS.

PowerTrench MOSFETs are used in the output stage and are effective at minimizing ringing due to fast switching. In most cases, no RC snubber on SW node is required. If a snubber is used, it should be placed close to the SW and PGND pins. The resistor and capacitor of the snubber must be sized properly to not generate excessive heating due to high power dissipation.

Decoupling capacitors on PVCC, VCC, and BOOT capacitors should be placed as close as possible to the PVCC ~ PGND, VCC ~ AGND, and BOOT ~ PHASE pin pairs to ensure clean and stable power supply. Their routing traces should be wide and short to minimize parasitic PCB resistance and inductance.

The board layout should include a placeholder for small−value series boot resistor on BOOT ~ PHASE. The boot−loop size, including series R_{BOOT} and C_{BOOT}, should be as small as possible.

A boot resistor may be required when the SPS is operating above 15 V V_{IN} and it is effective to control the high−side MOSFET turn−on slew rate and SW voltage overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground bounce or high positive and negative V_{SW} ringing. Inserting a boot resistance lowers the SPS module efficiency. Efficiency versus switching noise must be considered. R_{BOOT} values from 0.5 Ω to 4.7 Ω are typically effective in reducing V_{SW} overshoot.

The VIN and PGND pins handle large current transients with frequency components greater than 100 MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is not recommended since this adds extra parasitic inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SW} ringing.

PGND pad and pins should be connected to the GND copper plane with multiple vias for stable grounding. Poor grounding can create a noisy and transient offset voltage level between PGND and AGND. This could lead to faulty operation of gate driver and MOSFETs.

Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add any additional capacitors between BOOT to PGND. This may lead to excess current flow through the BOOT diode, causing high power dissipation.

The FCCM pin integrates weak internal pull−up and pull−down current sources. The current sources are used to help hold the FCCM in the 3−state window. This pin should not have any noise filter capacitors if actively driven by a PWM controller. Do not float this pin.

Multiple vias should be placed on the VIN and VOUT copper areas to interconnect nodes that are located on multiple layers (top, inner, and bottom layers). The vias help to evenly distribute current flow and heat conduction.

Care should be taken when routing the copper pour area and via placement on the SW copper. A large SW node copper pour can result in excessive parasitic inductance and capacitance, which can increase switching noise. However, the copper pour area and via placement can affect the efficiency and thermal performance, where a large copper pour can help decrease thermal resistance and parasitic resistance. If possible, place the SW node copper on the top layer with no vias on the SW copper to minimize switch node parasitic noise. If multiple SW node layers are needed, vias should be relatively large and of reasonably low inductance.

Critical high−frequency components; such as R_{BOOT}, C_{BOOT}, RC snubber, and bypass capacitors; should be located as close to the respective SPS module pins as possible on the top layer of the PCB. If this is not feasible, they can be placed on the board bottom side and their pins connected from bottom to top through a network of low−inductance vias.

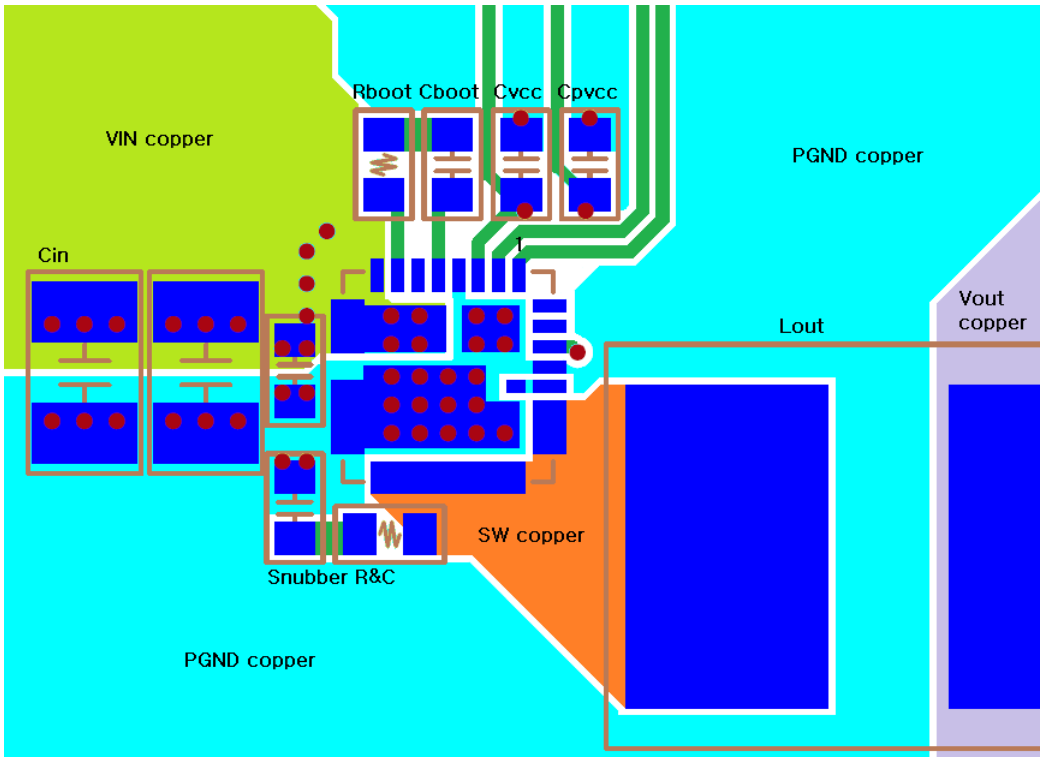


Figure 31. Single−Phase Board Layout Example − Top View

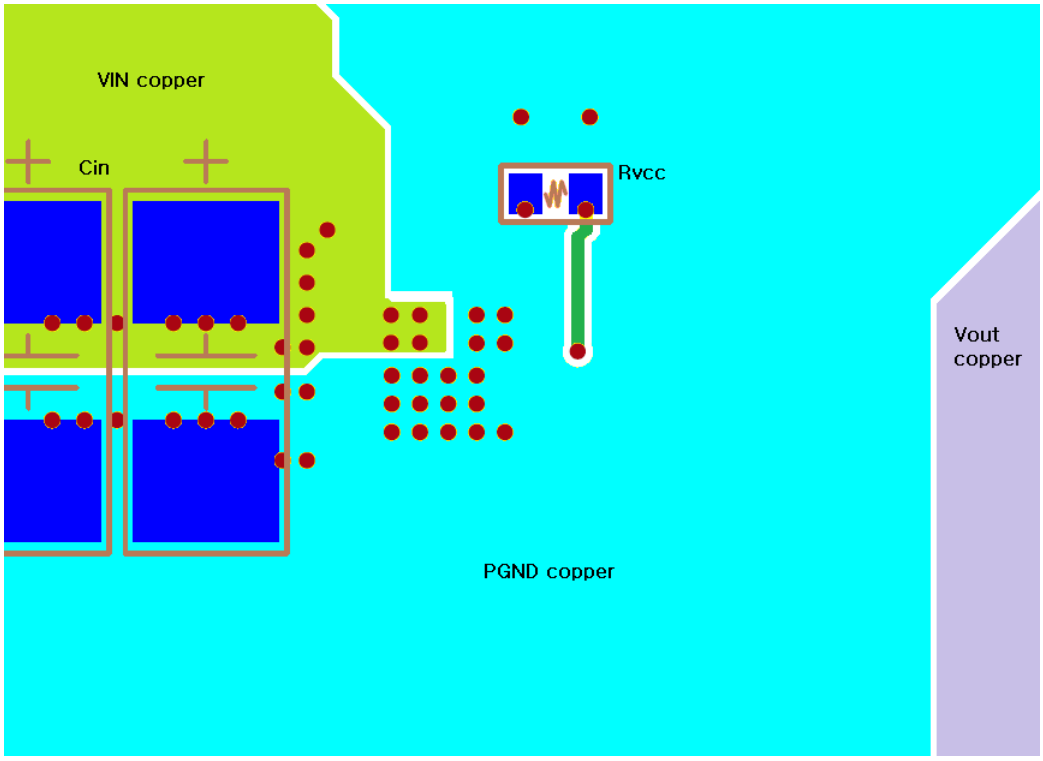


Figure 32. Single−Phase Board Layout Example − Bottom View (Mirrored)

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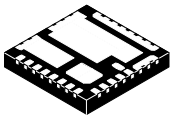

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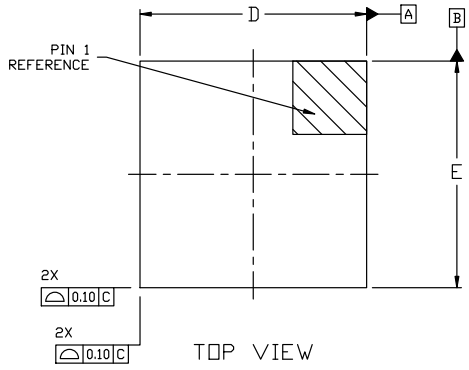
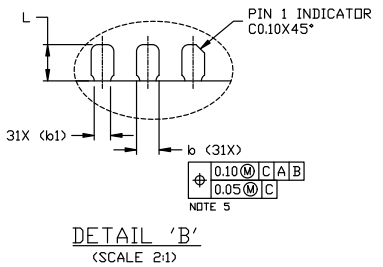
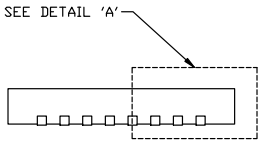
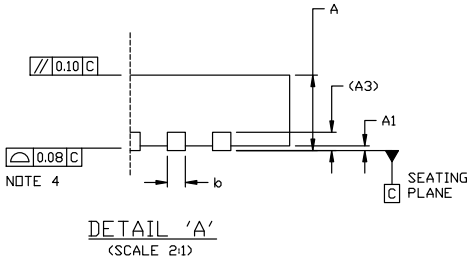


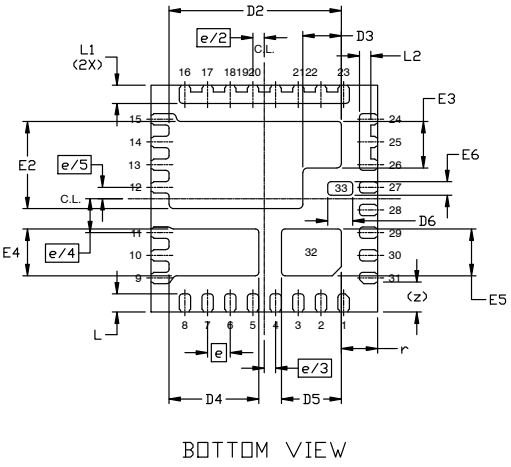
NOTES:

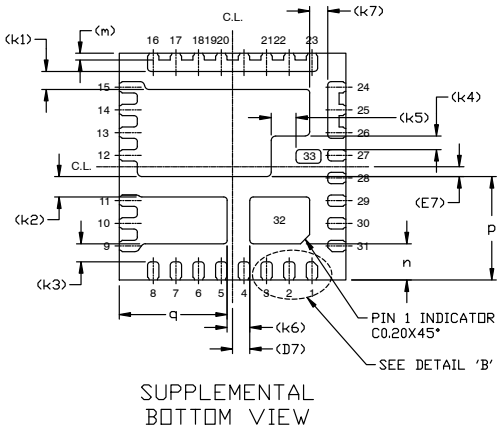
1. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, DATES MAY/2005.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS
4. DIMENSIONS DO NOT INCLUDE BURRS AND SMEAR OR MOLD FLASH.
   MOLD FLASH OR BURRS AND SMEAR DO NOT EXCEED 0.10MM.
5. DIMENSION b AND B1 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.











DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.15	0.20	0.25
b	0.20	0.25	0.30
b1	0.13	0.18	0.30
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
D3	0.75	0.85	0.95
D4	1.88	1.98	2.08
D5	1.22	1.32	1.42
D6	0.45	0.55	0.65
D7	0.38 REF		
E	4.90	5.00	5.10
E2	1.82	1.92	2.02
E3	0.93	1.03	1.13
E4	0.93	1.03	1.13
E5	0.93	1.03	1.13
E6	0.20	0.30	0.40
E7	0.22 REF		
e	0.50 BSC		
e/2	0.25 BSC		
e/3	0.25 BSC		
e/4	0.75 BSC		
e/5	0.25 BSC		
k1	0.40 REF		
k2	0.45 REF		
k3	0.40 REF		
k4	0.30 REF		
k5	0.55 REF		
k6	0.50 REF		
k7	0.40 REF		
L	0.30	0.40	0.50
L1	0.30	0.40	0.50
L2	0.15	0.25	0.35
m	0.15 REF		
n	0.80 REF		
p	2.28 REF		
q	2.38 REF		
r	0.80 REF		
z	0.625 REF		

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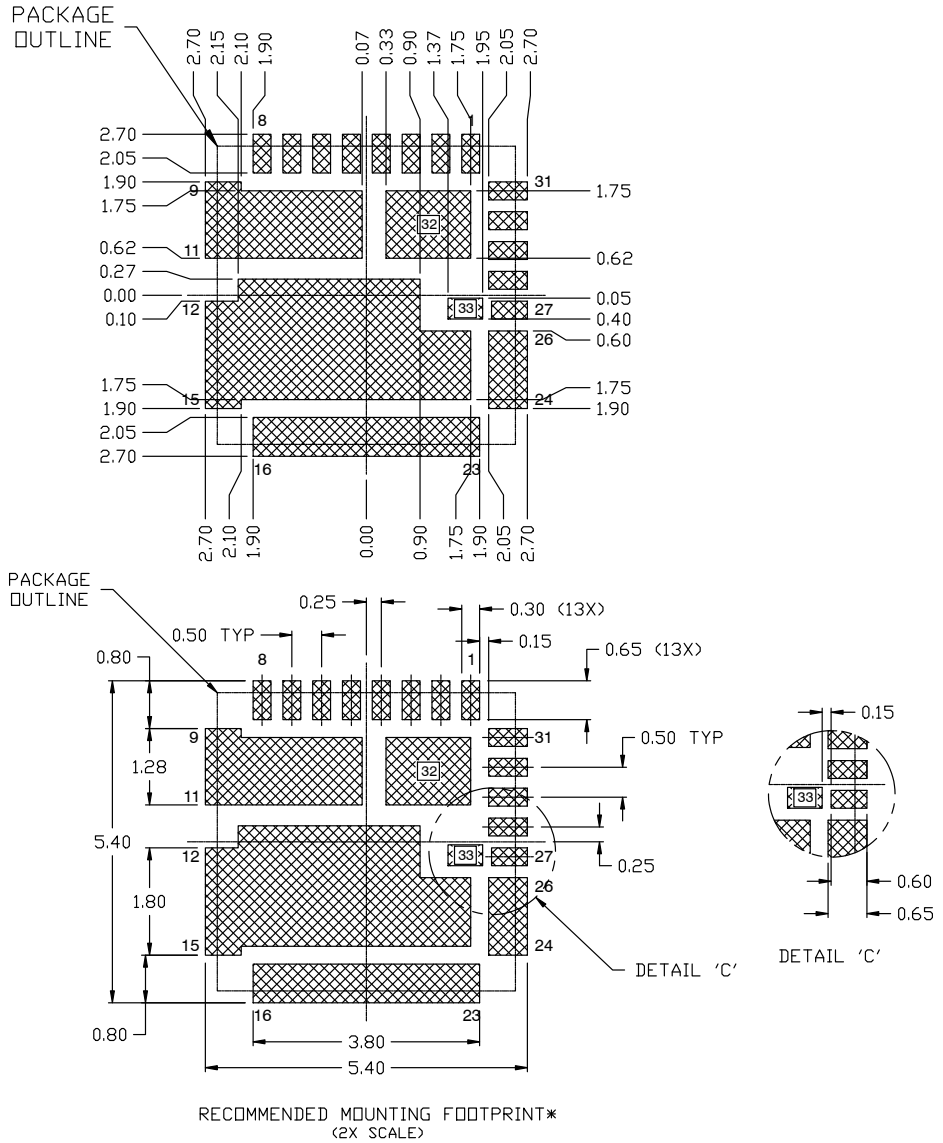
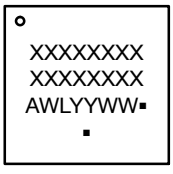


* For additional information on our Pb-Free strategy and soldering details, please download the ONSEMI Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**PQFN31 5X5, 0.5P**		**PAGE 2 OF 2**

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