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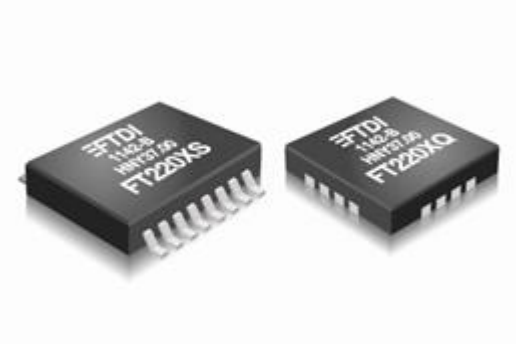
FT220X

(USB 4-BIT SPI/FT1248 IC)



The FT220X is a USB to FTDI's proprietary FT1248 interface and the following advanced features:

- FT1248 serial parallel interface in 1, 2 or 4 bit wide mode.
- Similar to an SPI slave in 1 bit mode
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- Fully integrated 2048 byte multi-time-programmable (MTP) memory, storing device descriptors and CBUS I/O configuration.
- Fully integrated clock generation with no external crystal required plus optional clock output selection enabling a glue-less interface to external MCU or FPGA.
- Data transfer rates to 500kByte/s.
- 512 byte receive buffer and 512 byte transmit buffer utilising buffer smoothing technology to allow for high data throughput.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Configurable CBUS I/O pin.
- USB Battery Charger Detection. Allows for USB peripheral devices to detect the presence of a higher power source to enable improved charging.
- Device supplied pre-programmed with unique USB serial number.
- USB Power Configurations; supports bus-powered, self-powered and bus-powered with power switching.
- Integrated +3.3V level converter for USB I/O.
- True 3.3V CMOS drive output and TTL input. (operates down to 1V8 with external pull-ups) Tolerant of 5V input.
- Configurable I/O pin output drive strength; 4 mA(min) and 16 mA(max)
- Integrated power-on-reset circuit.
- Fully integrated AVCC supply filtering - no external filtering required.
- + 5V Single Supply Operation.
- Internal 3V3/1V8 LDO regulators
- Low operating and USB suspend current; 8mA (active-typ) and 125uA (suspend-typ).
- Low USB bandwidth consumption.
- UHCI/OHCI/EHCI host controller compatible.
- USB 2.0 Full Speed compatible.
- Extended operating temperature range; -40 to 85ºC.
- Available in compact Pb-free 16 Pin SSOP and QFN packages (both RoHS compliant).

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1 Typical Applications

- USB to SPI interface in 1-bit mode
- Upgrading Legacy Peripherals to USB
- Utilising USB to add system modularity
- Incorporate USB interface to enable PC transfers for development system communication
- Interfacing MCU/PLD/FPGA based designs to add USB connectivity
- USB Industrial Control
- Detect USB dedicated charging ports, to allow for high current battery charging in portable devices.

1.1 Driver Support

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 10 32,64-bit
- Windows 8 32,64-bit
- Windows 7 32,64-bit
- Server 2008 R2 and later
- Windows CE 4.2 and later
- Mac OS-X
- Linux 3.2 and greater
- Android

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 10 32,64-bit
- Windows 8 32,64-bit
- Windows 7 32,64-bit
- Server 2008 R2 and later
- Windows CE 4.2 and later
- Mac OS-X
- Linux 2.6 and greater
- Android

The drivers listed above are all available to download for free from FTDI website (www.ftdichip.com). Various 3rd party drivers are also available for other operating systems - see FTDI website (www.ftdichip.com) for details.

For driver installation, please refer to http://www.ftdichip.com/Documents/InstallGuides.htm

1.2 Part Numbers

Part Number	Package
FT220XQ-x	16 Pin QFN
FT220XS-x	16 Pin SSOP

Note: Packing codes for x is:

- R: Taped and Reel, (SSOP is 3,000pcs per reel, QFN is 5,000pcs per reel).

- U: Tube packing, 100pcs per tube (SSOP only)

- T: Tray packing, 490pcs per tray (QFN only)

For example: FT220XQ-R is 5,000pcs taped and reel packing

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1.3 USB Compliant

The FT220X is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40001461 (Rev D).



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2 FT220X Block Diagram

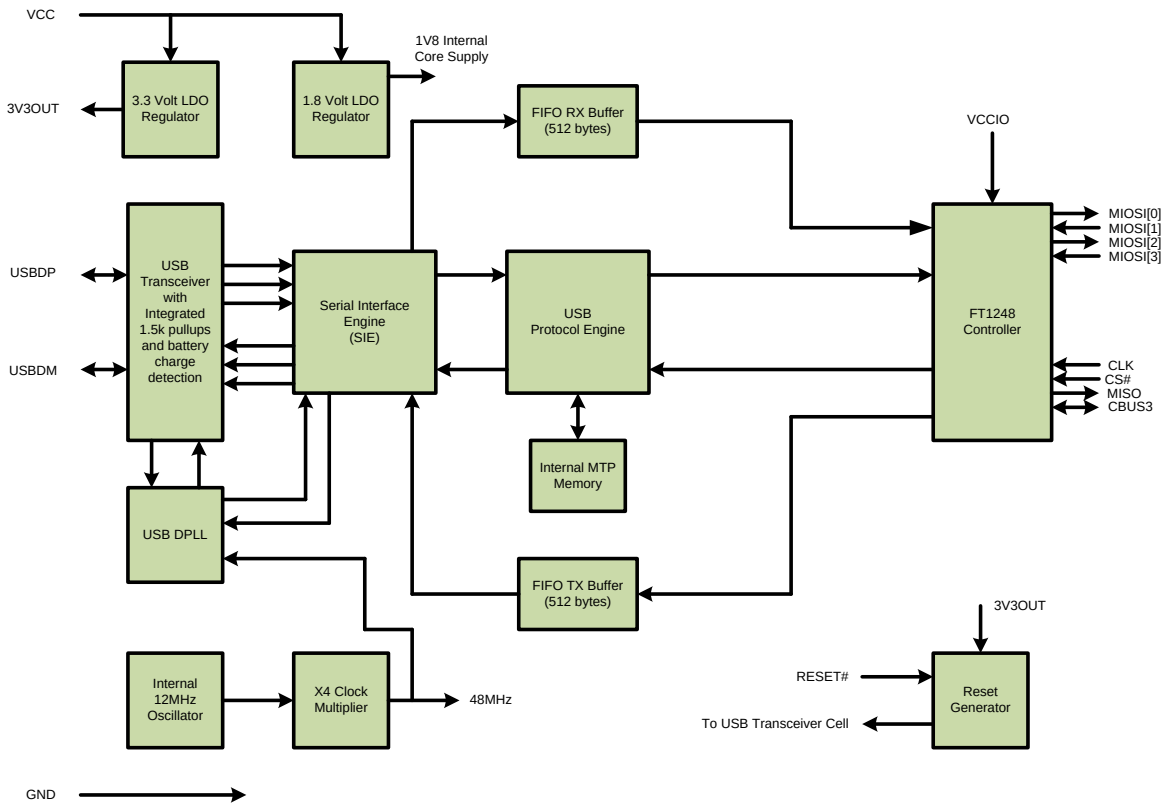

Figure 2.1 FT220X Block Diagram

For a description of each function please refer to Section 4.

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3 Device Pin Out and Signal Description

3.1 16-LD QFN Package

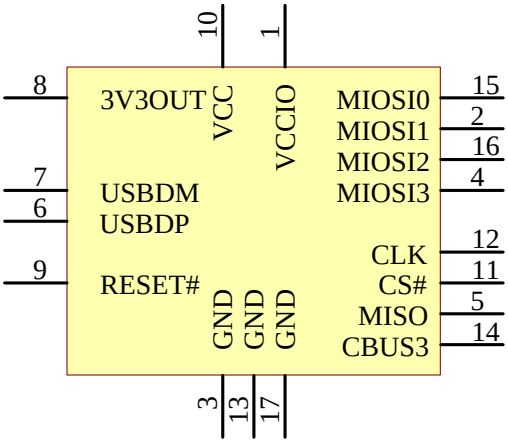

Figure 3.1 QFN Schematic Symbol

3.1.1 QFN Package Pinout Description

Note: # denotes an active low signal.

Pin No.	Name	Type	Description
10	** VCC	POWER Input	5 V (or 3V3) supply to IC
1	VCCIO	POWER Input	1V8 - 3V3 supply for the IO cells
8	** 3V3OUT	POWER Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3; pin 8 is an input pin. Connect to pin 10.
3, 13	GND	POWER Input	0V Ground input.

Table 3.1 Power and Ground

*Pin 17 is centre pad on base of chip package. Connect to GND.

** If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

Pin No.	Name	Type	Description
7	USBDM	INPUT	USB Data Signal Minus.
6	USBDP	INPUT	USB Data Signal Plus.
9	RESET#	INPUT	Reset input (active low).

Table 3.2 Common Function pins

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Pin No.	Name	Type	Description
15	MIOSI[0]	I/O	Bi-Directional data bit 0
2	MIOSI[1]	I/O	Bi-Directional data bit 1
16	MIOSI[2]	I/O	Bi-Directional data bit 2
4	MIOSI[3]	I/O	Bi-Directional data bit 3
12	CLK	Input	Clock input from FT1248 interface master
11	CS#	Input	Chip select input to enable the device interface. Active low logic.
5	MISO	Output	Master In Slave Out. Used to provide status information to the FT1248 interface master.
14	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.

Table 3.3 FT1248 Interface and CBUS Group (see note 1)

Notes:
1. When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx.) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the MTP memory.

3.2 16-LD SSOP Package

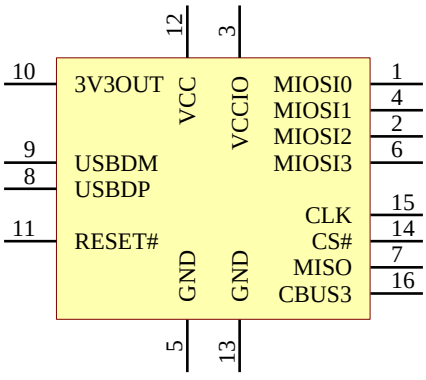

Figure 3.2 SSOP Schematic Symbol

3.2.1 SSOP Package Pinout Description

Note: # denotes an active low signal.

Pin No.	Name	Type	Description
12	** VCC	POWER Input	5 V (or 3V3) supply to IC

3	VCCIO	POWER Input	1V8 - 3V3 supply for the IO cells
10	** 3V3OUT	POWER Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3; pin 10 is an input pin. Connect to pin 12.
5, 13	GND	POWER Input	0V Ground input.

Table 3.4 Power and Ground

** If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

Pin No.	Name	Type	Description
9	USBDM	INPUT	USB Data Signal Minus.
8	USBDP	INPUT	USB Data Signal Plus.
11	RESET#	INPUT	Reset input (active low).

Table 3.5 Common Function pins

Pin No.	Name	Type	Description
1	MIOSI[0]	I/O	Bi-Directional data bit 0
4	MIOSI[1]	I/O	Bi-Directional data bit 1
2	MIOSI[2]	I/O	Bi-Directional data bit 2
6	MIOSI[3]	I/O	Bi-Directional data bit 3
15	CLK	Input	Clock input from FT1248 interface master
14	CS#	Input	Chip select input to enable the device interface. Active low logic.
7	MISO	Output	Master In Slave Out. Used to provide status information to the FT1248 interface master.
16	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.

Table 3.6 FT1248 Interface and CBUS Group (see note 1)

Notes:
1. When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx.) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the MTP memory.

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3.3 CBUS Signal Options

The following options can be configured on the CBUS I/O pin. CBUS signal options are common to both package versions of the FT220X. These options can be configured in the internal MTP memory using the software utility FT_PROG, which can be downloaded from the FTDI Utilities (www.ftdichip.com). The default configuration is described in Section 9.

CBUS Signal Option	Available On CBUS Pin	Description
TRI-STATE	CBUS3	IO Pad is tri-stated
DRIVE 1	CBUS3	Output a constant 1
DRIVE 0	CBUS3	Output a constant 0
PWREN#	CBUS3	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.
SLEEP#	CBUS3	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.
CLK24MHz	CBUS3	24 MHz Clock output.*
CLK12MHz	CBUS3	12 MHz Clock output.*
CLK6MHz	CBUS3	6 MHz Clock output.*
GPIO	CBUS3	CBUS bit bang mode option. Allows the CBUS pins to be used as general purpose I/O. Configured in the internal MTP memory. A separate application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes in more detail how to use CBUS bit bang mode.
BCD Charger	CBUS3	Battery Charger Detect, indicates when the device is connected to a dedicated battery charger port. Active high output.
BCD Charger#	CBUS3	Inverse of BCD Charger (open drain)
BitBang_WR#	CBUS3	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBang_RD#	CBUS3	Synchronous and asynchronous bit bang mode RD# strobe output.
VBUS Sense	CBUS3	Input to detect when VBUS is present.
Time Stamp	CBUS3	Toggle signal which changes state each time a USB SOF is received
Keep_Awake#	CBUS3	Prevents the device from entering suspend state when unplugged.

Table 3.7 CBUS Configuration Control

*When in USB suspend mode the outputs clocks are also suspended.

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4 Function Description

The FT220X is a USB to FTDI Proprietary FT1248 interface device which simplifies USB implementations and reduces external component count by fully integrating an MTP memory and an integrated clock circuit which requires no external crystal. It has been designed to operate efficiently with USB host controllers by using as little bandwidth as possible when compared to the total USB bandwidth available.

4.1 Key Features

Functional Integration. Fully integrated MTP memory, clock generation, AVCC filtering, Power-On-Reset and LDO regulator.

Configurable CBUS I/O Pin Options. The fully integrated MTP memory allows configuration of the Control Bus (CBUS) functionality and drive strength selection. There is 1 configurable CBUS I/O pin. The configurable options are defined in section 3.3.

The CBUS line can be configured with any one of these output options by setting bits in the internal MTP memory. The device is supplied with the most commonly used pin definitions pre-programmed - see Section 9 for details.

Asynchronous Bit Bang Mode with RD# and WR# Strobes. The FT220X supports FTDI's previous chip generation bit-bang mode. In bit-bang mode, the 4 MIOSI data lines can be switched from the regular interface mode to a 4-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate pre-scalar).

Synchronous Bit Bang Mode. The FT220X supports synchronous bit bang mode. This mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. This makes it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. An application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes this feature.

Source Power and Power Consumption. The FT220X is capable of operating at a voltage supply between +3.3V and +5.25V with a nominal operational mode current of 8mA and a nominal USB suspend mode current of 125µA. This allows greater margin for peripheral designs to meet the USB suspend mode current limit of 2.5mA. An integrated level converter within the FT1248 interface allows the FT220X to interface to logic running at +1.8V, 2.5V, +3.3V or +5V. (Note: External pull-ups are recommended for IO <3V3).

4.2 Functional Block Descriptions

The following paragraphs detail each function within the FT220X. Please refer to the block diagram shown in Figure 2.1

Internal MTP Memory. The internal MTP memory in the FT220X is used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other USB configuration descriptors. The internal MTP memory is also used to configure the CBUS pin functions. The FT220X is supplied with the internal MTP memory pre-programmed as described in Section 9. A user area of the internal MTP memory is available to system designers to allow storing additional data from the user application over USB. The internal MTP memory descriptors can be programmed in circuit, over USB without any additional voltage requirement. The descriptors can be programmed using the FTDI utility software called FT_PROG, which can be downloaded from FTDI Utilities on the FTDI website (www.ftdichip.com).

+1.8V LDO Regulator. The +1.8V LDO regulator generates the +1.8V reference voltage for driving the internal core of the IC.

+3.3V LDO Regulator. The +3.3V LDO regulator generates the +3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides +3.3V power to the 1.5kΩ internal pull up resistor on USBDP. The main function of the LDO is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, it can be used to supply external circuitry requiring a +3.3V nominal supply with a maximum current of 50mA.

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USB Transceiver. The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide +3.3V level slew rate control signalling, whilst a differential input receiver and two single ended input receivers provide USB data in, Single-Ended-0 (SE0) and USB reset detection conditions respectfully. This function also incorporates a 1.5kΩ pull up resistor on USBDP. The block also detects when connected to a USB power supply which will not enumerate the device but still supply power and may be used for battery charging.

USB DPLL. The USB DPLL cell locks on to the incoming NRZI USB data and generates recovered clock and data signals for the Serial Interface Engine (SIE) block.

Internal 12MHz Oscillator - The Internal 12MHz Oscillator cell generates a 12MHz reference clock. This provides an input to the x4 Clock Multiplier function. The 12MHz Oscillator is also used as the reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks.

Clock Multiplier / Divider. The Clock Multiplier / Divider takes the 12MHz input from the Internal Oscillator function and generates the 48MHz, 24MHz, 12MHz and 6MHz reference clock signals. The 48Mz clock reference is used by the USB DPLL and the Baud Rate Generator blocks.

Serial Interface Engine (SIE). The Serial Interface Engine (SIE) block performs the parallel to serial and serial to parallel conversion of the USB data. In accordance with the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation. It also checks the CRC on the USB data stream.

USB Protocol Engine. The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol requests generated by the USB host controller and the commands for controlling the functional parameters of the FT1245 in accordance with the USB 2.0 specification chapter 9.

FIFO RX Buffer (512 bytes). Data sent from the USB host controller to the FT1248 interface via the USB data OUT endpoint is stored in the FIFO RX (receive) buffer. Data is removed from the buffer to the FT1248 transmit register under control of the FT1248 FIFO controller. (Rx relative to the USB interface).

FIFO TX Buffer (512 bytes). Data from the FT1248 receive register is stored in the TX buffer. The USB host controller removes data from the FIFO TX Buffer by sending a USB request for data from the device data IN endpoint. (Tx relative to the USB interface).

FT1248 interface controller. Controls the FT1248 interface, dynamically switching the width of the bus as commanded by the external bus master.

RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT220X.

RESET# can be tied to 3V3OUT.

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5 FT1248 Interface Description

The FT1248 protocol has a dynamic bi-directional data bus interface that can be configured as 1, 2, 4, or 8-bits wide (only 4 bit wide on the FT220X) providing users with the flexibility to configure the interface with performance, pin count and PCB area in mind. For example, 1-bit mode it requires 8 clock cycles to get 8 data bits and in 8-bit mode all 8 bits are sent with one clock.

In the FT1248 there are 3 distinct phases:

While CS# is inactive, the FT1248 reflects the status of the write buffer and read buffers within the FT220X on the MIOSIO[0] and MISO wires respectively. The buffers are 512 Bytes each and the status will reflect if at least one byte of space is available for the external device to write to and whether at least one byte is available to be read by the external device.

Additionally, the FT1248 slave block supports multiple slave devices where a master can communicate with multiple SPI slave devices. When the slave is sharing buses with other SPI slave devices, the write and read buffer status cannot be reflected on the MIOSIO[0] and MISO wires during CS# inactivity as this would cause bus contention. Therefore, it is possible for the user to select whether they wish to have the buffer status switched on or off during inactivity.

(This setting may be applied in the internal MTP memory with FT_PROG at the same time as selecting FT1248 mode).

When CS# is active a command/bus size phase occurs first. Following the command phase is the data phase, for each data byte transferred the FT1248 slave drives an ACK/NAK status onto the MISO wire. The master can send multiple data bytes so long as CS# is active, if a unsuccessful data transfer occurs, i.e. a NAK happens on the MISO wire then the master should immediately abort the transfer by de-asserting CS#.

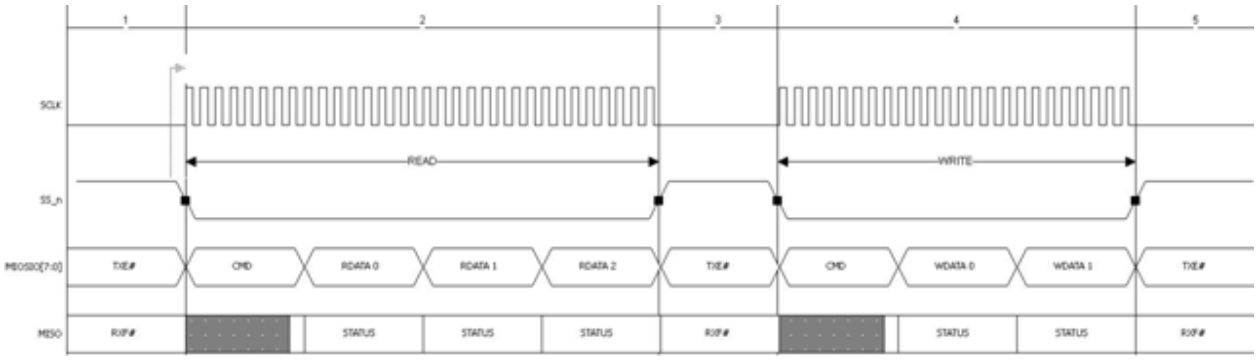

Figure 5.1: FT1248 Basic Waveform Protocol

5.1 Determining the Dynamic Bus Width

The bus width is dynamic. In order for the FT220X, in FT1248 mode, to determine the bus width within the command phase, the bus width is encoded along with the actual commands on the first active clock edge when CS# is active and has a data width of 4-bits.

If any of the MIOSIO[3:2] signals are driven low by the external host then the data transfer width equals 4-bits

If MIOSIO[1] signal is driven low by the external host then the data transfer width equals 2-bits

Else the bus width is defaulted to 1-bit

In order to successfully decode the bus width, all MIOSIO signals must have pull up resistors. By default, all MIOSIO signals shall be seen by the FT220X in FT1248 mode as logic '1'from the internal resistors. This means that when a FT1248 master does not wish to use certain MIOSIO signals, the slave (FT220X) is still capable of determining the requested bus width since any unused MIOSIO signals shall be pulled up by default.

The remaining bits used during the command phase are used to contain the command itself which means that it is possible to define up to 16 unique commands.

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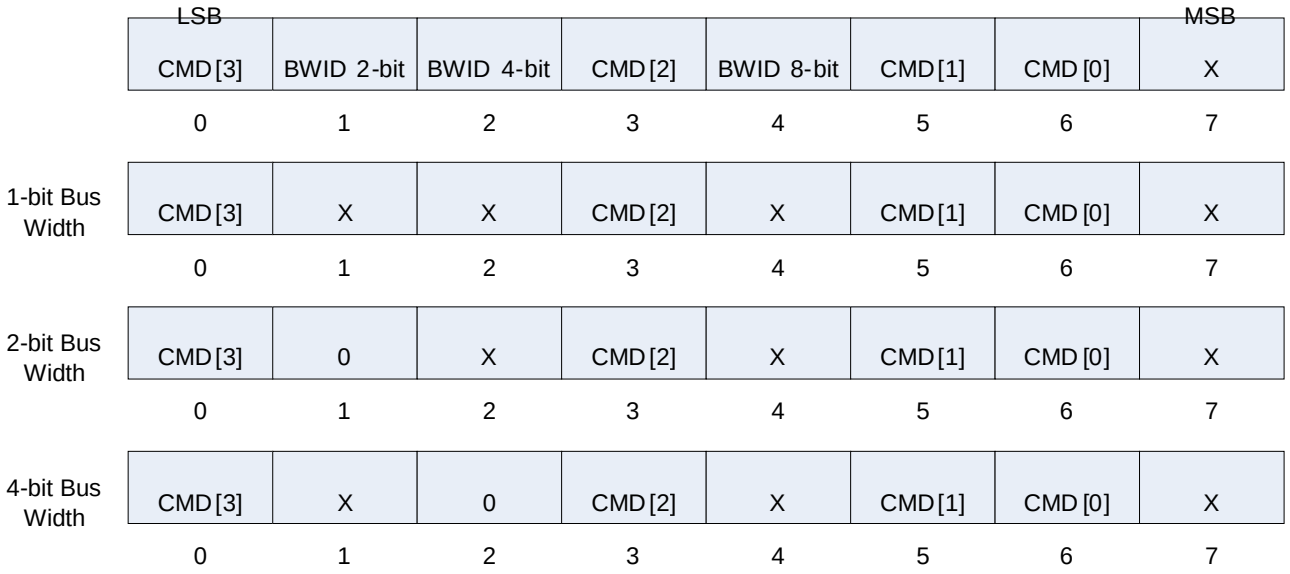

Figure 5.2: FT1248 Command Structure

5.2 Supported Commands on the FT1248 Interface

The FT1248 interface can accept and decode up to 16 unique commands. At this time only 9 unique commands are implemented as shown below.

Command	Identifier	Description
write	0x00	Write request command
read	0x01	Read request command
read modem status	0x02	Read modem status command, users may wish to emulate modem status control. A RMS command returns status bits RTS and DTR
write modem status	0x03	Write modem status command, users may wish to emulate modem status control. A WMS command allows users to set status bits: DCD, RI, DSR, CTS
write buffer flush	0x04	Write buffer flush request – This command is used to indicate to the FT1248 slave that its write buffers should be flushed rather than wait for any latency timers to expire. If this command is received the FT1248 block will flag the upstream controllers (USB FIFOs etc.) to flush their write buffers regardless of what content is present in the FT1248 write buffer
address eeprom	0x05	Address EEPROM command sets the address users wish to write or read from
write	0x06	Write EEPROM command sets the write data to be written into the EEPROM

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eeprom		
read eeprom	0x07	Read EEPROM command reads
read usb status	0x08	Read USB Status: 00 = suspended, 01 = default, 10 = addressed, 11 = configured
Reserved	0x09 – 0xF	Unused Commands

Table 5.1: FT1248 Commands

5.3 LSB or MSB Selection

The data can be sent/received Least Significant Bit First (LSB) or Most Significant Bit First (MSB). To determine which mode is used by the FT1248 interface of the FT220X the MTP memory must be set.

This may be selected with FT_PROG.

5.4 Clock Phase/Polarity

The FT1248 slave does not need to have any knowledge of clock rate as this is supplied by the FT1248 master. However the relationship between clock and data needs to be controllable, to allow the slave to operate in the same way as the master such that data is correctly driven and sampled on the correct clock phases. By configuring the polarity and phase of CLK with respect to the data it is possible to match the FT1248 master.

There are 4 possible modes which are determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) signals. The different combinations of these signals are commonly referred to as modes, see Table 5.2 below. For the FT1248 slave, only 2 of these 4 modes are supported. CPHA will always be set to 1 in the FT1248 slave because data is available or driven on to MIOSIO wires on the first clock edge after CS# is active and is therefore sampled on the trailing edge of the first clock pulse. When CPHA equals 0, it means data must be available or driven onto the MIOSIO wires on the first leading edge of the clock after CS# is active. However, during this period between CS# becoming active and the first leading clock edge is when the MIOSIO wires are being "turned around" as when CS# is inactive the FT1248 slave is driving the write buffer status. Supporting CPHA = 0 would result in bus contention and therefore, shall not be supported.

Mode	CPOL	CPHA	Supported
0	0	0	NO
1	0	1	YES
2	1	0	NO
3	1	1	YES

Table 5.2: CPOL & CPHA Mode Numbers

When CPOL is 1, the idle state of the clock is high. When CPOL is 0, the idle state of the clock is low. It should be noted that clock phase and polarity need to be identical for the master and attached slave device.

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5.4.1 CPHA = 1

When CPHA is set to '1', the first edge after CS# goes low will be used to shift (or drive) the first data bit onto MIOSIO. Every odd numbered edge after this will shift out the next data bit. Incoming data will be sampled on the second or trailing SCLK edge and every even edge thereafter.

Figure 5.3 shows this for both CPOL = 0 and CPOL = 1.

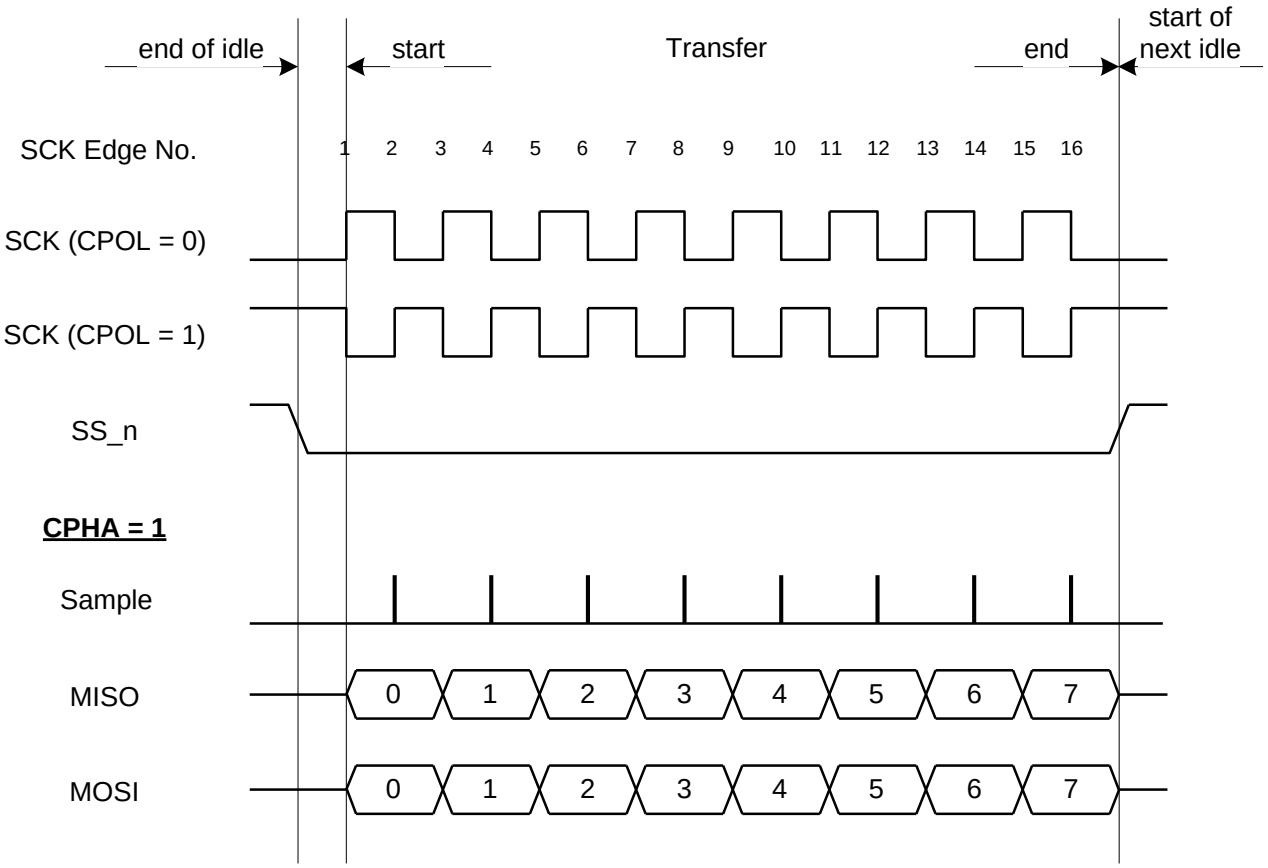

Figure 5.3: FT1248 Clock Format CPHA = 1

Note: The CPOL value may be selected in the MTP memory. This may be done with FT_PROG.

Note: Further information on this interface can be found in AN_167_FT1248 Parallel Serial Interface Basics from the FTDI website www.ftdichip.com.

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5.5 FT1248 Timing

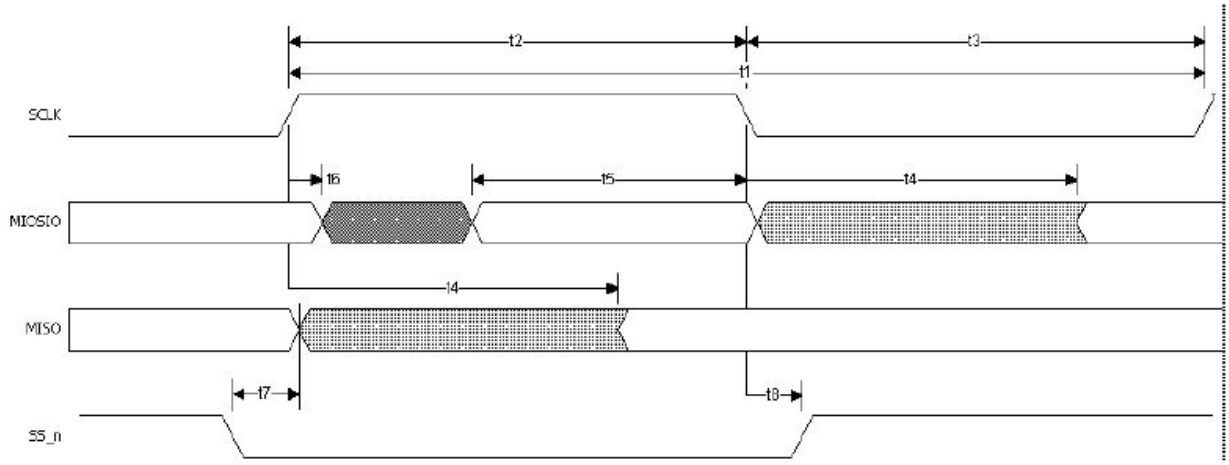

Figure 5.4: FT1248 Clock Format CPHA = 1

The timings will vary depending on VCCIO.

	Min (ns)	Typical (ns)	Max (ns)	Description
T1		83.33		SCLK Period
T2		41.67		SCLK HIGH
T3		41.67		SCLK LOW
T4		1	30	SCLK rising or falling driving edge to MIOSIO/MSIO
T5		25		MIOSIO setup time to rising or falling sample SCLK edge
T6		3		MIOSIO hold time from rising or falling sample SCLK edge
T7		5		SS_n setup time to rising or falling SCLK edge
T8		5		SS_n hold time from rising or falling sample SCLK edge

Table 5.3: 1V8 VCCIO timings

	Min (ns)	Typical (ns)	Max (ns)	Description
T1		83.33ns		SCLK Period
T2		41.67ns		SCLK HIGH
T3		41.67ns		SCLK LOW
T4		1	15	SCLK rising or falling driving edge to MIOSIO/MSIO
T5		22		MIOSIO setup time to rising or falling sample SCLK edge
T6		1		MIOSIO hold time from rising or falling sample SCLK edge
T7		5		SS_n setup time to rising or falling SCLK edge

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T8		5		SS_n hold time from rising or falling sample SCLK edge

Table 5.4: 2V5 VCCIO timings

	Min (ns)	Typical (ns)	Max (ns)	Description
T1		83.33ns		SCLK Period
T2		41.67ns		SCLK HIGH
T3		41.67ns		SCLK LOW
T4		1	10	SCLK rising or falling driving edge to MIOSIO/MSIO
T5		20		MIOSIO setup time to rising or falling sample SCLK edge
T6		0		MIOSIO hold time from rising or falling sample SCLK edge
T7		5		SS_n setup time to rising or falling SCLK edge
T8		5		SS_n hold time from rising or falling sample SCLK edge

Table 5.5: 3V3 VCCIO timings

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6 Devices Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT220X devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit	Conditions
Storage Temperature	-65°C to 150°C	Degrees C	
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours	
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C	
MTTF FT220XS	TBD	Hours	
MTTF FT220XQ	TBD	Hours	
VCC Supply Voltage	-0.3 to +5.5	V	
VCCIO IO Voltage	-0.3 to +4.0	V	
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V	
DC Input Voltage – High Impedance Bi-directional (powered from VCCIO)	-0.3 to +5.8	V	
DC Output Current – Outputs	22	mA	
ESD Charge Device Mode(CDM)	500	V	Class III
ESD Human Body Mode (HDM)	2000	V	Class 2

Table 6.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

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6.2 ESD and Latch-up Specifications

Description	Specification
Human Body Mode (HBM)	> ± 2kV
Machine mode (MM)	> ± 200V
Charged Device Mode (CDM)	> ± 500V
Latch-up	> ± 200mA

Table 6.2 ESD and Latch-Up Specifications

6.3 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC	VCC Operating Supply Voltage	2.97	5	5.5	V	Normal Operation
VCC2	VCCIO Operating Supply Voltage	1.62	---	3.63	V	
Icc1	Operating Supply Current	9.7	10.5	12.3	mA	Normal Operation
Icc2	Operating Supply Current		125		µA	USB Suspend
3V3	3.3v regulator output	2.97	3.3	3.63	V	VCC must be greater than 3V3 otherwise 3V3OUT is an input which must be driven with 3.3V

Table 6.3 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.97	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 16mA

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Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	2.0			V	LVTTL
Vt	Switching Threshold		1.49		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		1.15		V	
Vt+	Schmitt trigger positive going threshold voltage		1.64		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 6.4 I/O Pin Characteristics VCCIO = +3.3V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.25	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive

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						strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	0.8			V	LVTTL
Vt	Switching Threshold		1.1		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.8		V	
Vt+	Schmitt trigger positive going threshold voltage		1.2		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 6.5 I/O Pin Characteristics VCCIO = +2.5V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.62	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive

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						strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.77	V	LVTTL
Vih	Input High Switching Threshold	1.6			V	LVTTL
Vt	Switching Threshold		0.77		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.557		V	
Vt+	Schmitt trigger positive going threshold voltage		0.893		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 6.6 I/O Pin Characteristics VCCIO = +1.8V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	VCC-0.2			V	
Vol	Output Voltage Low			0.2	V	
Vil	Input low Switching Threshold		-	0.8	V	
Vih	Input High Switching Threshold	2.0	-		V	

Table 6.7 USB I/O Pin (USBDP, USBDM) Characteristics

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6.4 MTP Memory Reliability Characteristics

The internal 2048 Bytes MTP memory has the following reliability characteristics:

Parameter	Value	Unit
Data Retention	10	Years
Write Cycle	2,000	Cycles
Read Cycle	Unlimited	Cycles

Table 6.8 MTP Memory Characteristics

6.5 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics:

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Frequency of Operation (see Note 1)	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

Table 6.9 Internal Clock Characteristics

Note 1: Equivalent to +/-1667ppm

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7 USB Power Configurations

The following sections illustrate possible USB power configurations for the FT220X. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT220XS and FT220XQ package options.

All USB power configurations illustrated apply to both package options for the FT220X device. Please refer to Section 3 for the package option pin-out and signal descriptions.

7.1 USB Bus Powered Configuration

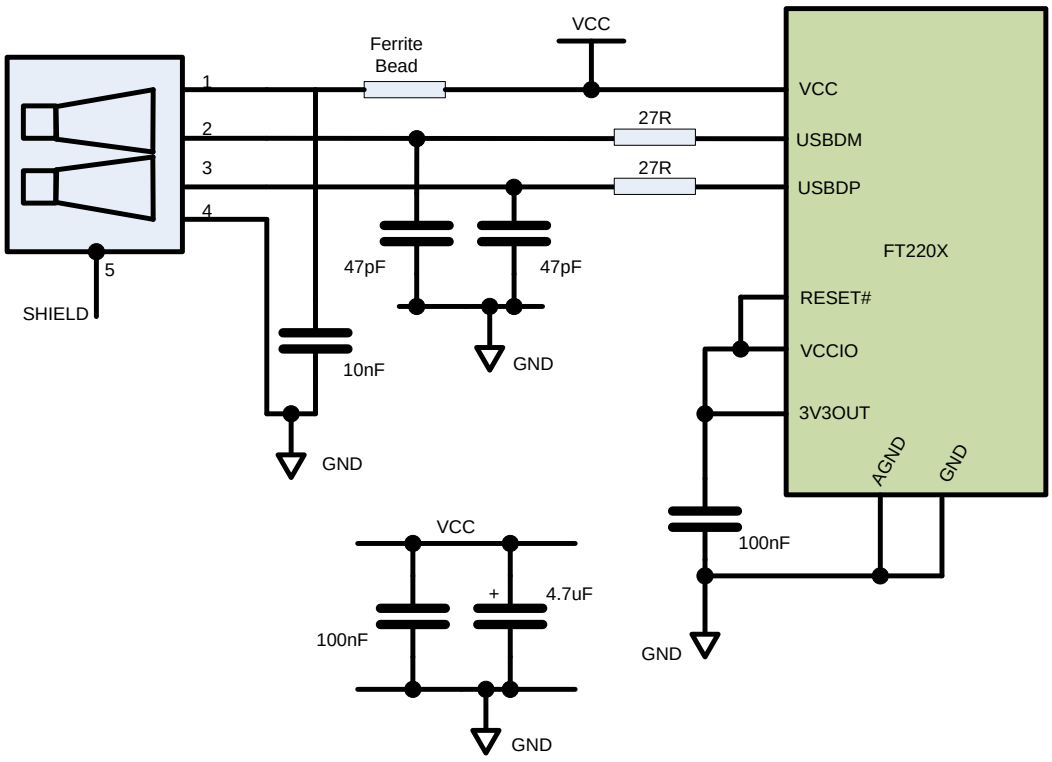

Figure 7.1 Bus Powered Configuration

Figure 7.1 Illustrates the FT220X in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus. Basic rules for USB bus power devices are as follows –

i) On plug-in to USB, the device should draw no more current than 100mA.
ii) In USB Suspend mode the device should draw no more than 2.5mA.
iii) A bus powered high power USB device (one that draws more than 100mA) should use one of the CBUS pins configured as PWREN# and use it to keep the current below 100mA on plug-in and 2.5mA on USB suspend.
iv) A device that consumes more than 100mA cannot be plugged into a USB bus powered hub.
v) No device can draw more than 500mA from the USB bus.

The power descriptors in the internal MTP memory of the FT220X should be programmed to match the current drawn by the device.

A ferrite bead is connected in series with the USB power supply to reduce EMI noise from the FT220X and associated circuitry being radiated down the USB cable to the USB host. The value of the Ferrite Bead depends on the total current drawn by the application. A suitable range of Ferrite Beads is available from Steward (www.steward.com), for example Steward Part # MI0805K400R-10.

Note: If using PWREN# (available using the CBUS) the pin should be pulled to VCCIO using a 10kΩ resistor.

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7.2 Self Powered Configuration

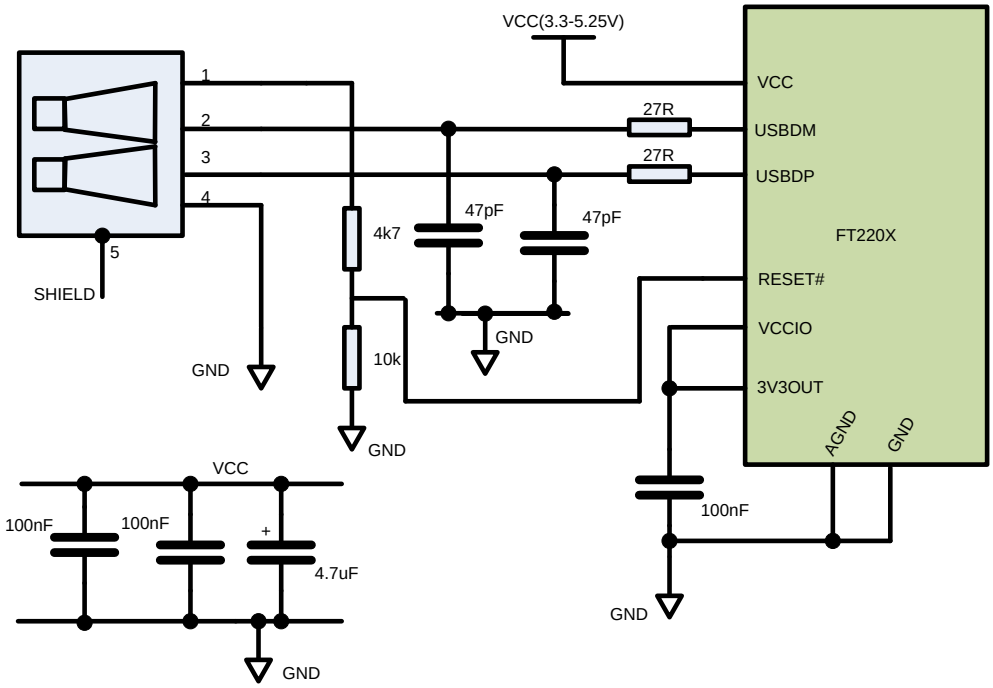

Figure 7.2 Self Powered Configuration

Figure 7.2 illustrates the FT220X in a typical USB self-powered configuration. A USB self-powered device gets its power from its own power supply, VCC, and does not draw current from the USB bus. The basic rules for USB self-powered devices are as follows –

i) A self-powered device should not force current down the USB bus when the USB host or hub controller is powered down.
ii) A self-powered device can use as much current as it needs during normal operation and USB suspend as it has its own power supply.
iii) A self-powered device can be used with any USB host, a bus powered USB hub or a self-powered USB hub.

The power descriptor in the internal MTP memory of the FT220X should be programmed to a value of zero (self-powered).

In order to comply with the first requirement above, the USB bus power (pin 1) is used to control the VBUS_Sense pin of the FT220X device. When the USB host or hub is powered up an internal 1.5kΩ resistor on USBDP is pulled up to +3.3V, thus identifying the device as a full speed device to the USB host or hub. When the USB host or hub is powered off, VBUS_Sense pin will be low and the FT220X is held in a suspend state. In this state the internal 1.5kΩ resistor is not pulled up to any power supply (hub or host is powered down), so no current flows down USBDP via the 1.5kΩ pull-up resistor. Failure to do this may cause some USB host or hub controllers to power up erratically.

Figure 7.2 illustrates a self-powered design which has a +3.3V to +5.25V supply.

Note:

1. When the FT220X is in reset, the FT1248 interface I/O pins are tri-stated. Input pins have internal 75kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

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7.3 USB Bus Powered with Power Switching Configuration

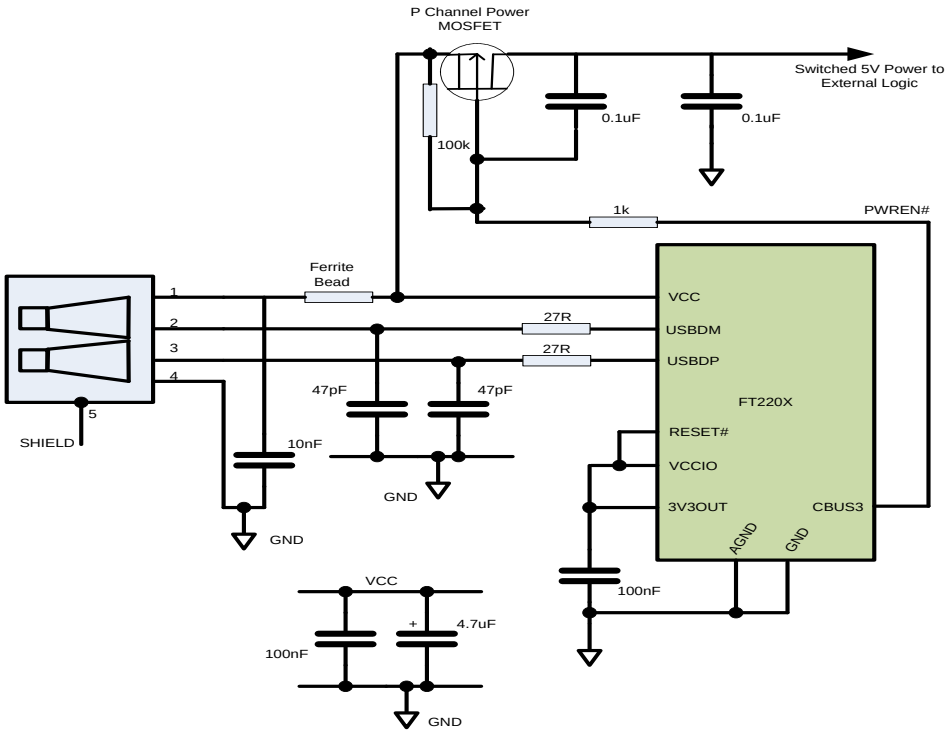

Figure 7.3 Bus Powered with Power Switching Configuration

A requirement of USB bus powered applications, is when in USB suspend mode, the application draws a total current of less than 2.5mA. This requirement includes external logic. Some external logic has the ability to power itself down into a low current state by monitoring the PWREN# signal. For external logic that cannot power itself down in this way, the FT220X provides a simple but effective method of turning off power during the USB suspend mode.

Figure 7.3 shows an example of using a discrete P-Channel MOSFET to control the power to external logic. A suitable device to do this is an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1kΩ series resistor and a 0.1µF capacitor is used to limit the current surge when the MOSFET turns on. Without the soft start circuit it is possible that the transient power surge, caused when the MOSFET switches on, will reset the FT220X or the USB host/hub controller. The soft start circuit example shown in Figure 7.3 powers up with a slew rate of approximaely12.5V/Ms. Thus supply voltage to external logic transitions from GND to +5V in approximately 400 microseconds.

As an alternative to the MOSFET, a dedicated power switch IC with inbuilt "soft-start" can be used. A suitable power switch IC for such an application is the Micrel (www.micrel.com) MIC2025-2BM or equivalent.

With power switching controlled designs the following should be noted:

i) The external logic to which the power is being switched should have its own reset circuitry to automatically reset the logic when power is re-applied when moving out of suspend mode.

ii) Set the Pull-down on Suspend option in the internal FT220X MTP memory.

iii) One of the CBUS Pins should be configured as PWREN# in the internal FT220X MTP memory, and used to switch the power supply to the external circuitry.

iv) For USB high-power bus powered applications (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the application must be set in the Max Power field in the internal FT220X MTP memory. A high-power bus powered application uses the descriptor in the internal FT220X MTP memory to inform the system of its power requirements.

v) PWREN# gets its VCC from VCCIO. For designs using 3V3 logic, ensure VCCIO is not powered down using the external logic. In this case use the +3V3OUT.

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7.4 USB Battery Charging Detection

A recent addition to the USB specification (http://www.usb.org/developers/devclass_docs/BCv1.2_011912.zip) is to allow for additional charging profiles to be used for charging batteries in portable devices. These charging profiles do not enumerate the USB port of the peripheral. The FT220X device will detect that a USB compliant dedicated charging port (DCP) is connected. Once detected while in suspend mode a battery charge detection signal is then provided to allow external logic to switch to charging mode as opposed to operation mode.

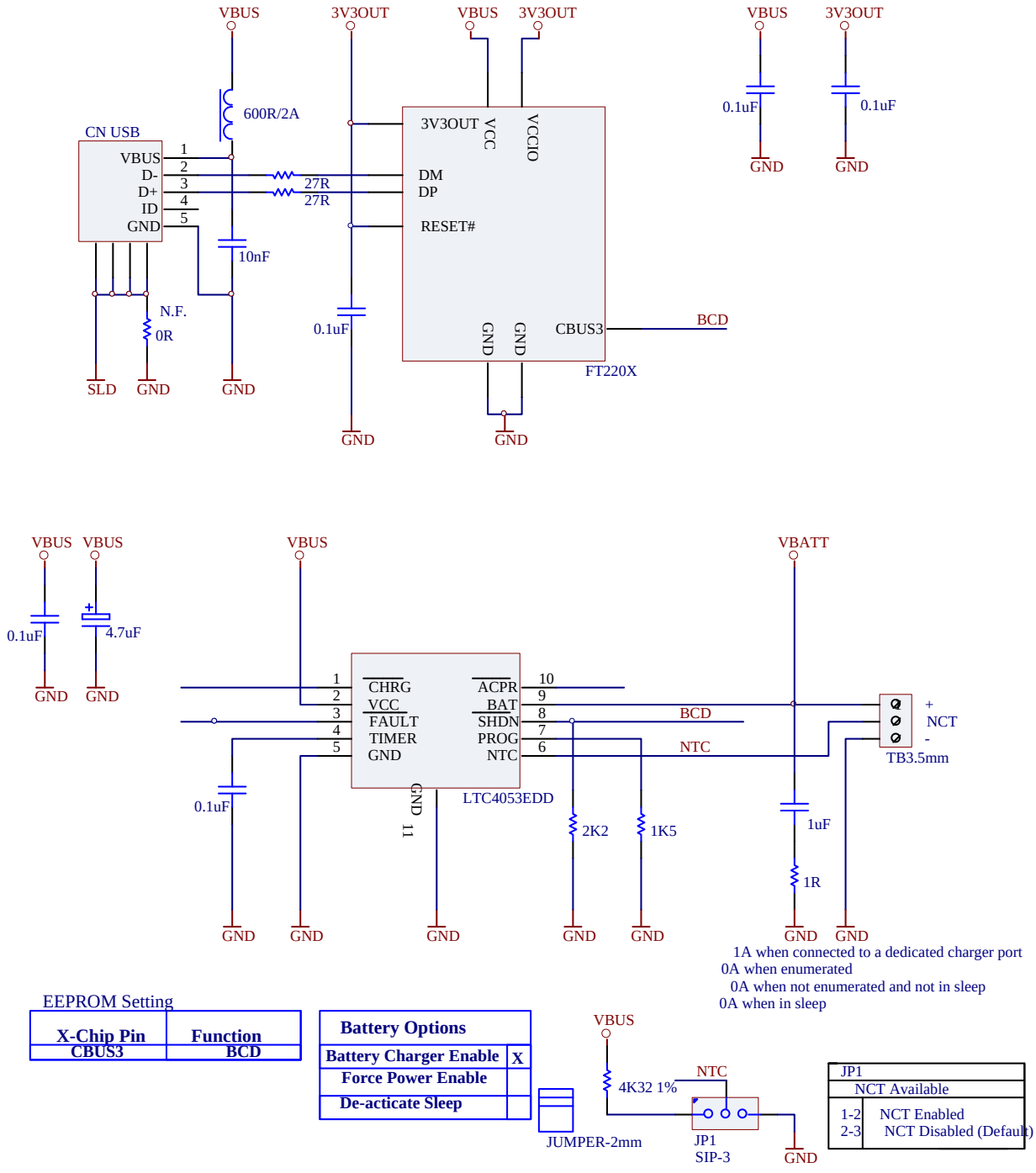

Figure 7.4 USB Battery Charging Detection

To use the FT220X with battery charging detection the CBUS pin must be reprogrammed to allow for the BCD Charger output to switch the external charger circuitry on. The CBUS pins are configured in the internal MTP memory with the free utility FT_PROG. If the charging circuitry requires an active low signal to enable it, the CBUS pin can be programmed to BCD Charger# as an alternative.

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When connected to a USB compliant dedicated charging port (DCP, as opposed to a standard USB host) the device USB signals will be shorted together and the device suspended. The BCD charger signal will bring the LTC4053 out of suspend and allow battery charging to start. The charge current in the example above is 1A as defined by the resistance on the PROG pin.

To calculate the equivalent resistance on the LTC4053 PROG pin select a charge current, then Res = $1500V/I_{chg}$

For more configuration options of the LTC4053 refer to:

AN_175_Battery Charging Over USB

Note: If the FT220X is connected to a standard host port such that the device is enumerated the battery charge detection signal is inactive as the device will not be in suspend.

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8 Application Examples

The following sections illustrate possible applications of the FT220X. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT220XS and FT220XQ package options.

8.1 USB to FT1248 Converter

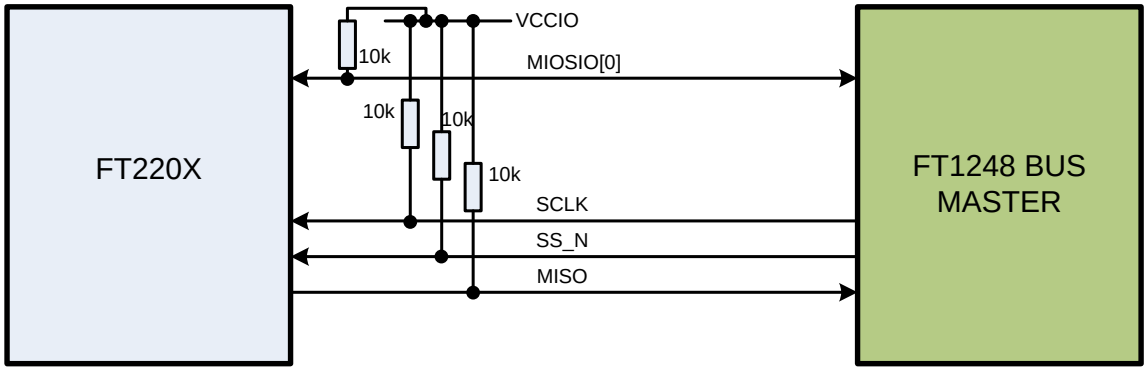

Figure 8.1 Application Example showing USB to FT1248 host

The FT1248 can be used with 1-bit. 2-bit, or 4-bit wide data. The Figure 8.1 is showing 1 bit mode. By using 4 data bits you need fewer clock cycles to get the data across.

The FT220X is the slave device and the external FPGA/MCU is the bus master. The FT220X will auto detect the bus width from the initial command byte sent by the controller. If not using all 4 data lines the pins may be left unterminated as an internal pull-up ensures the device detects logic 1.

Timing diagrams for 1-bit accesses can be seen in figures 8.2 and 8.3.

For further information on the mode see AN_167 FT1248 Basics from the FTDI website.

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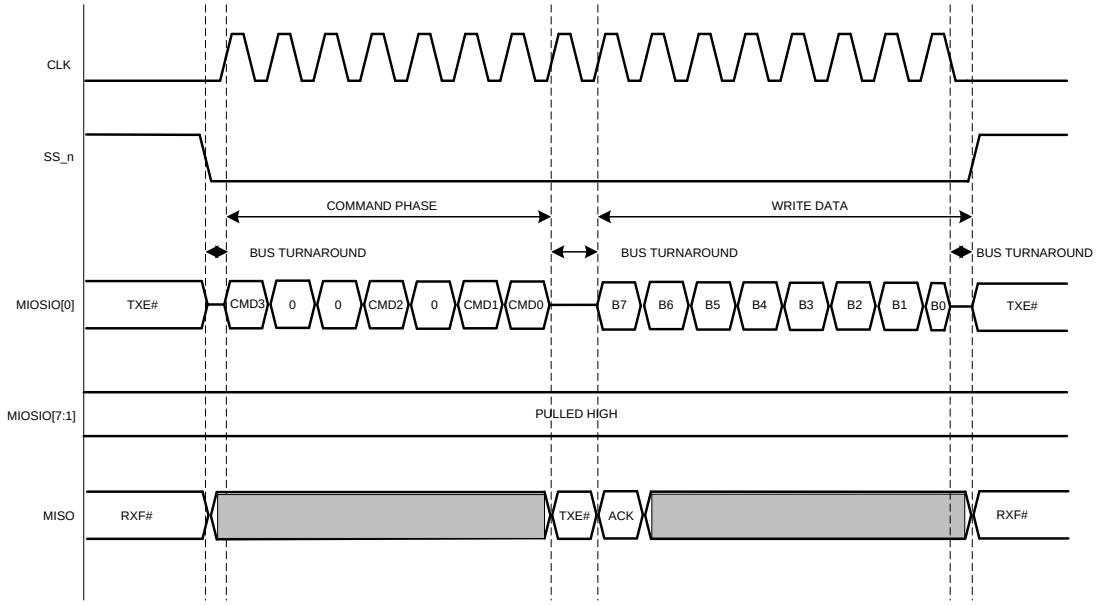

Figure 8.2 FT1248 1- bit write timing diagram

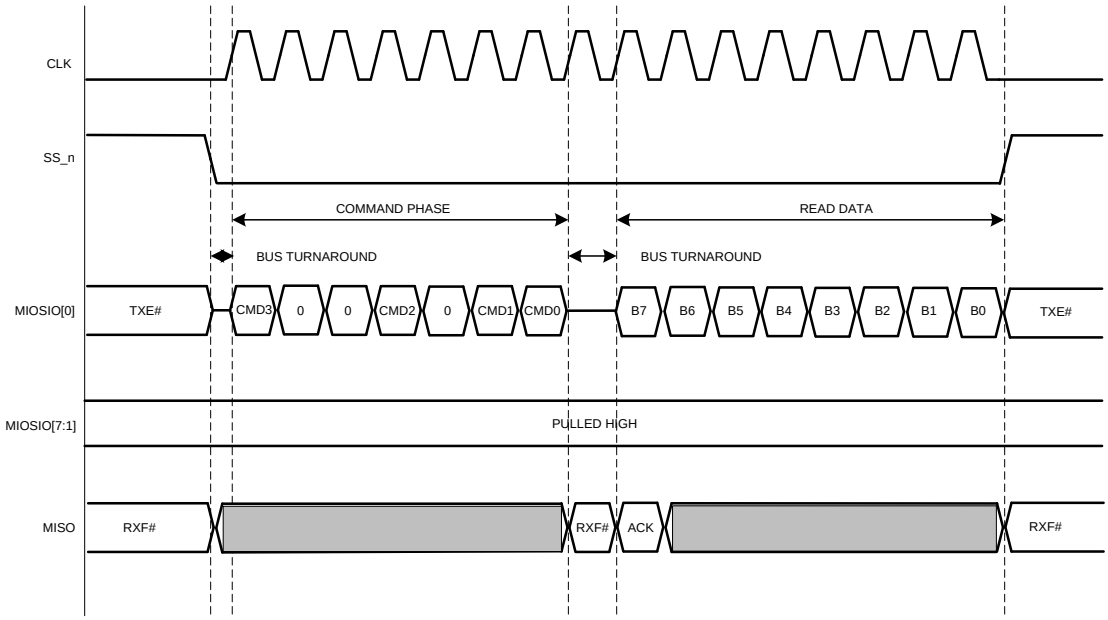

Figure 8.3 FT1248 1- bit read timing diagram

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9 Internal MTP Memory Configuration

The FT220X includes an internal MTP memory which holds the USB configuration descriptors, other configuration data for the chip and also user data areas. Following a power-on reset or a USB reset the FT220X will scan its internal MTP memory and read the USB configuration descriptors stored there.

In many cases, the default values programmed into the MTP memory will be suitable and no re-programming will be necessary. The defaults can be found in Section 9.1.

The MTP memory in the FT220X can be programmed over USB if the values need to be changed for a particular application. Further details of this are provided from section 9.2 onwards.

Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. See TN_100 – USB Vendor ID/Product ID Guidelines for more details.

9.1 Default Values

The default factory programmed values of the internal MTP memory are shown in Table 9.1.

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product UD (PID)	6015h	FTDI default PID (hex)
Serial Number Enabled?	Yes	
Serial Number	See Note	A unique serial number is generated and programmed into the MTP memory during device final test.
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	FT220X 4-BIT FT1248	
Max Bus Power Current	90mA	
Power Source	Bus Powered	
Device Type	FT220X	
USB Version	0200	Returns USB 2.0 device description to the host. Note: The device is a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
Remote Wake Up	Disabled	
DBUS Drive Current Strength	4mA	Options are 4mA, 8mA, 12mA, 16mA
DBUS slew rate	Slow	Options are slow or fast

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Parameter	Value	Notes
DBUS Schmitt Trigger Enable	Normal	Options are normal or Schmitt
CBUS Drive Current Strength	4mA	Options are 4mA, 8mA, 12mA, 16mA
CBUS slew rate	Slow	Options are slow or fast
CBUS Schmitt Trigger Enable	Normal	Options are normal or Schmitt
Load VCP Driver	Disabled	Enabling this will load the VCP driver interface for the device.
CBUS3	Keep_Awake#	Prevents the device from entering suspend state when unplugged.

Table 9.1 Default Internal MTP Memory Configuration

9.2 Method of Programming the MTP Memory

9.2.1 Programming the MTP memory over USB

The MTP memory on all FT-X devices can be programmed over USB. This method is the same as for the EEPROM on other FTDI devices such as the FT232R. No additional hardware, connections or programming voltages are required. The device is simply connected to the host computer in the same way that it would be for normal applications, and the FT_Prog utility is used to set the required options and program the device.

The FT_Prog utility is provided free-of-charge from the FTDI website, and can be found at the link below. The user guide is also available at this link.

http://www.ftdichip.com/Support/Utilities.htm#FT_Prog

Additionally, D2XX commands can be used to program the MTP memory from within user applications. For more information on the commands available, please see the D2XX Programmers Guide below.

9.3 Memory Map

The FT-X family MTP memory has various areas which come under three main categories:

- User Memory Area
- Configuration Memory Area (writable)
- Configuration Memory Area (non-writable)

Memory Area Description	Word Address
User Memory Area 2 Accessible via USB, I^2C and FT1248	0x3FF - 0x80

Configuration Memory Area Accessible via USB, I²C and FT1248	0x7E - 0x50
Configuration Memory Area Cannot be written	0x4E - 0x40
User Memory Area 1 Accessible via USB, I²C and FT1248	0x3E - 0x12
Configuration Memory Area Accessible via USB, I²C and FT1248	0x10 - 0x00

Figure 9.1: Simplified Memory Map for the FT-X

User Memory Area

The User Memory Areas are highlighted in Green on the memory map. They can be read and written via both USB and FT1248 on the FT220X. All locations within this range are freely programmable; no areas have special functions and there is no checksum for the user area.

Note: The application should take into account the specification for the number of write cycles in Section 6.4 if it will be writing to the MTP memory multiple times.

Configuration Memory Area (writable)

This area stores the configuration data for the device, including the data which is returned to the host in the configuration descriptors (e.g. the VID, PID and string descriptions) and also values which set the hardware configuration (the signal assigned to each CBUS pin for example).

These values can have a significant effect on the behaviour of the device. Steps must be taken to ensure that these locations are not written to un-intentionally by an application which is intended to access only the user area.

This area is included in a checksum which covers configuration areas of the memory, and so changing any value can also cause this checksum to fail.

Configuration Memory Area (non-writable)

This is a reserved area and the application should not write to this area of memory. Any attempt to write these locations will fail.

9.4 Hardware Requirements

The hardware is the same as for a typical USB-FT1248 application and no additional hardware or programming voltages are required. For the USB connections, either a bus-powered configuration (see Section 7.1and 7.3) or a self-powered configuration (see Section 7.2) could be used.

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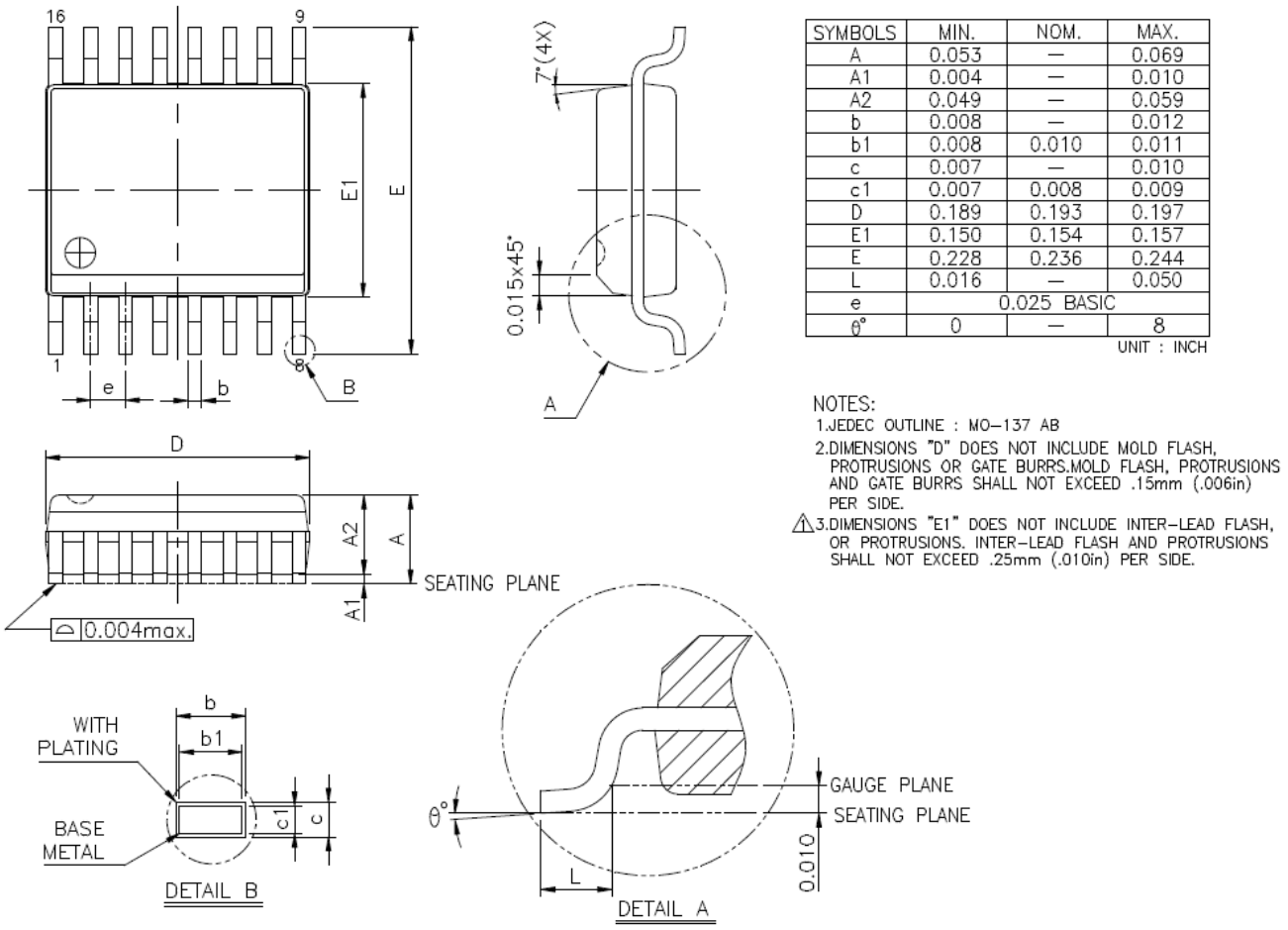
10 Package Parameters

The FT220X is available in two different packages. The FT220XS is the SSOP-16 option and the FT220XQ is the QFN-16 package option. The solder reflow profile for both packages is described in Section 10.5.

10.1 SSOP-16 Package Mechanical Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	0.053	—	0.069
A1	0.004	—	0.010
A2	0.049	—	0.059
b	0.008	—	0.012
b1	0.008	0.010	0.011
c	0.007	—	0.010
c1	0.007	0.008	0.009
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
E	0.228	0.236	0.244
L	0.016	—	0.050
e	0.025 BASIC		
θ°	0	—	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MO-137 AB
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
⚠3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

Figure 10.1 SSOP-16 Package Dimensions

The FT220XS is supplied in a RoHS compliant 16 pin SSOP package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 4.90mm x 3.91mm body (4.90mm x 5.99mm including pins). The pins are on a 0.635 mm pitch. The above mechanical drawing shows the SSOP-16 package.

All dimensions are in inches.

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10.2 SSOP-16 Package Markings

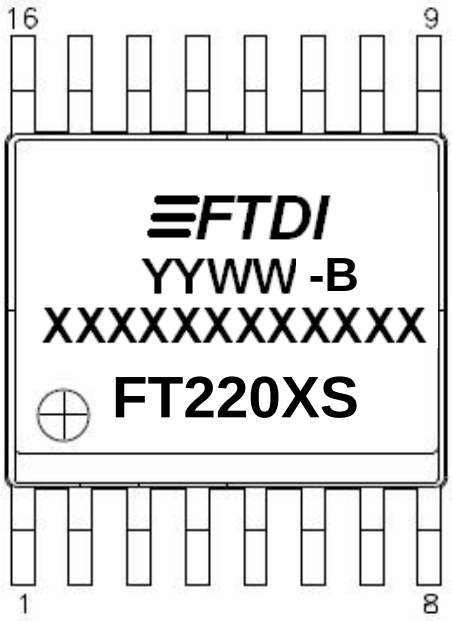

Figure 10.2 SSOP-16 Package Markings

The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number. This is followed by the revision number.

The code **XXXXXXXXXXXX** is the manufacturing LOT code.

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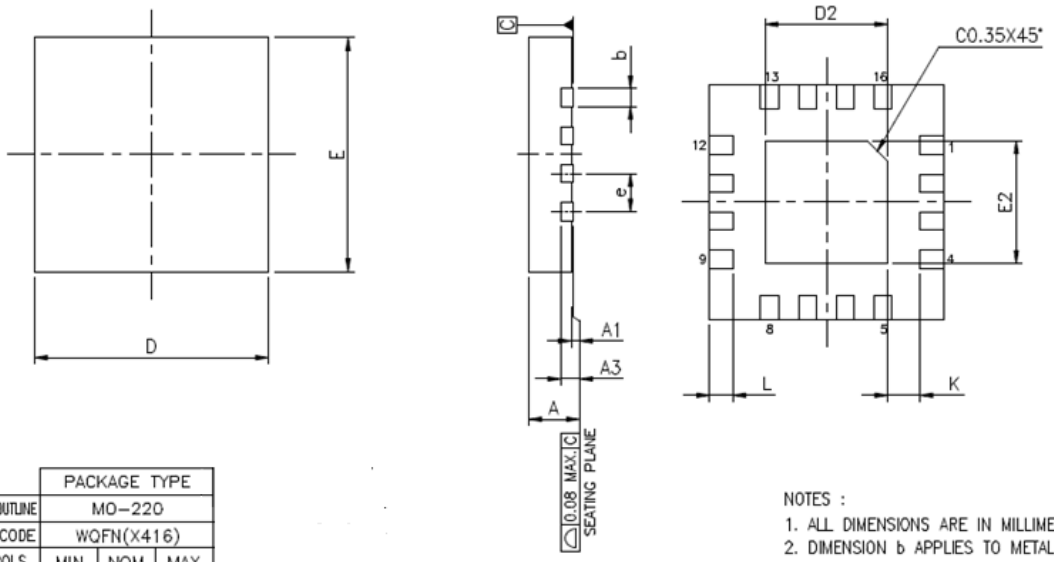
10.3 QFN-16 Package Mechanical Dimensions



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X416)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.25	0.30	0.35
D	4.00 BSC		
E	4.00 BSC		
e	0.65 BSC		
K	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	E2			D2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
98X98 MIL	2.00	2.10	2.15	2.00	2.10	2.15	0.35	0.40	0.45	V	X	W(V)GGC

Figure 10.3 QFN-16 Package Dimensions

The FT220XQ is supplied in a RoHS compliant leadless QFN-16 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 4.00mm x 4.00mm. The solder pads are on a 0.65mm pitch. The above mechanical drawing shows the QFN-16 package. All dimensions are in millimetres.

The centre pad on the base of the FT220XQ is internally connected to GND and the PCB should not have signal tracking on the top layer under this area. Connect to GND.

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10.4 QFN-16 Package Markings

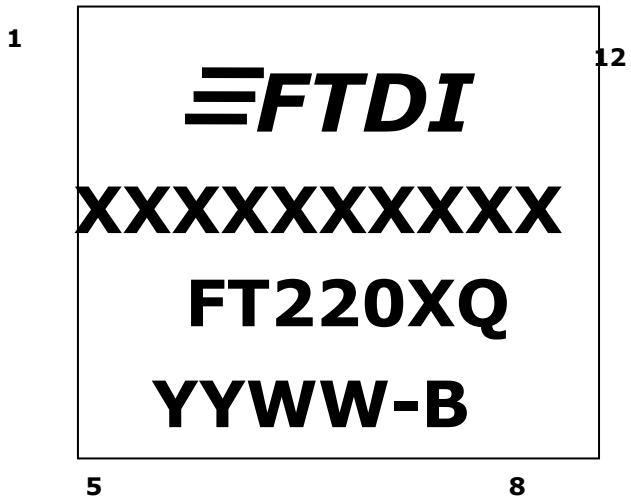

Figure 10.4 QFN-16 Package Markings

The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number. This is followed by the revision number.

The code **XXXXXXX** is the manufacturing LOT code

10.5 Solder Reflow Profile

The FT220X is supplied in Pb free 16 LD SSOP and QFN-16 packages. The recommended solder reflow profile for both package options is shown in Figure 10.5.

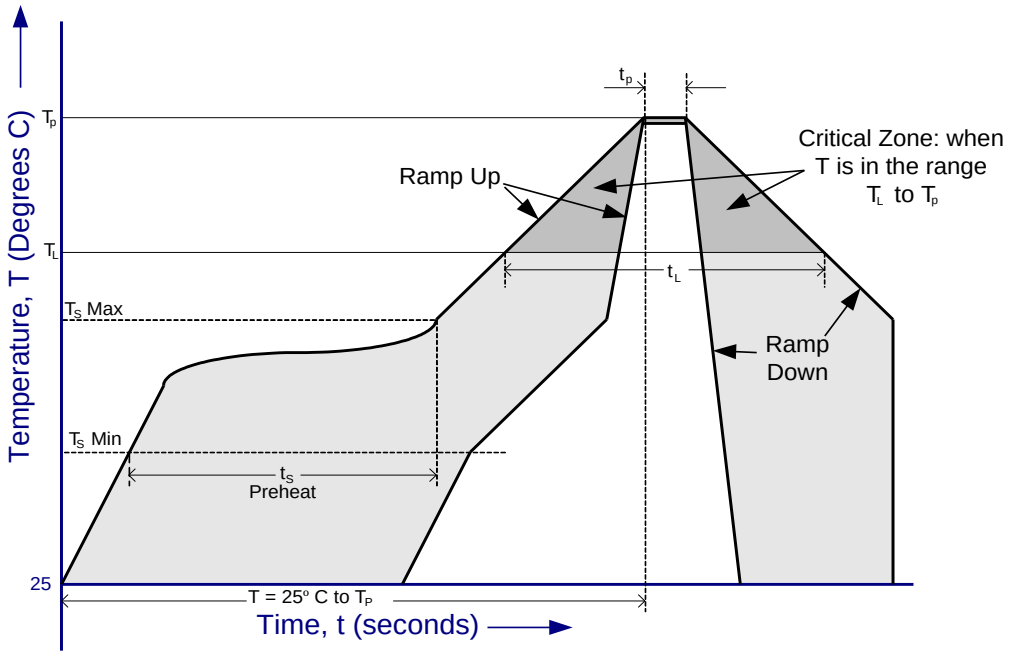

Figure 10.5 FT220X Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 10.1. Values are shown for both a completely Pb free solder process (i.e. the FT220X is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT220X is used with non-Pb free solder).

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Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 10.1 Reflow Profile Parameter Values

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Appendix A – References

Document References

AN232R-01 FT232RBitBangModes

AN_107 Advanced Driver Options

AN_121 FTDI Device EEPROM User Area Usage

AN_167 FT1248 Parallel Serial Interface Basics

http://www.ftdichip.com/Documents/InstallGuides.htm

TN_100 USB VID-PID Guidelines

AN_175 Battery Charging Over USB with FTEX Devices

http://www.usb.org/developers/devclass_docs/BCv1.2_011912.zip

Acronyms and Abbreviations

Terms	Description
DCP	Dedicated Charging Port
FIFO	First In First Out
LSB	Least Significant Bit First
MSB	Most Significant Bit First
MTP	Multi-time Programmable memory
QFN	Quad Flat Non-leaded package
SIE	Serial Interface Engine
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver / Transmitter

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Appendix C - Revision History

Document Title: USB 4-BIT SPI/FT1248 IC FT220X
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Clearance No.: FTDI# 262
Product Page: http://www.ftdichip.com/FT-X.htm
Document Feedback: Send Feedback

Revision	Changes	Date
Version 1.0	Initial Release	2012-02-08
Version 1.1	Added USB compliance in section 1.3; Clarified MTP Reliability in table 6.8; Edited EEPROM Table 9.1 changed Load VCP; Driver to Disabled and edited Product Description	2012-04-17
Version 1.2	Removed references to LED signals on the CBUS pins as these are not available on the FT220X; Removed section 8.2 showing connection of the Tx/Rx LEDs; Updated TID; Updated US address; Added clarification on front page about 5V tolerant	2013-02-14
Version 1.3	Removed references to MTP programming over FT1248 and Clarified package dimensions.	2014-02-10
Version 1.4	Remove the incorrect typical application items and update the driver support list	2018-05-07

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