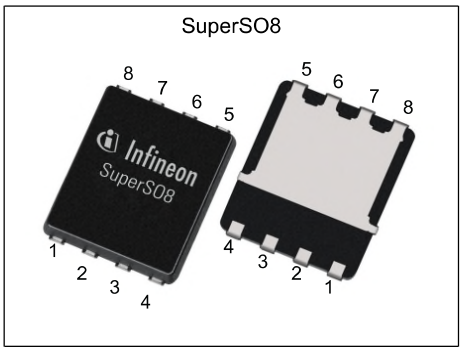
MOSFET

OptiMOS™ 3 Power-Transistor, 80 V



Features

- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC[1] for target applications
- Halogen-free according to IEC61249-2-21

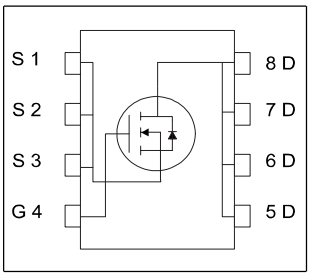


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	4.7	mΩ
I_D	125	A

Type / Ordering Code	Package	Marking	Related Links
BSC047N08NS3 G	PG-TDSON-8	047N08NS	-

[1] J-STD20 and JESD22

Table of Contents

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	125 79 18	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	500	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	310	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	125 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	18	K/W	-
Device on PCB, minimal footprint	R_{thJA}	-	-	62	K/W	-
Device on PCB, 6 cm^2 cooling area[2]	R_{thJA}	-	-	50	K/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For higher case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2	2.8	3.5	V	V_{DS}=V_{GS}, I_D=90 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	3.9 5.6	4.7 8.9	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=6 V, I_D=25 A
Gate resistance	R_G	-	2.2	-	Ω	-
Transconductance	g_{fs}	60	120	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	3600	4800	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	960	1300	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	36	-	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	18	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=25 A, R_G=1.6 Ω
Rise time	t_r	-	17	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=25 A, R_G=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	44	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=25 A, R_G=1.6 Ω
Fall time	t_f	-	11	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=25 A, R_G=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	16	-	nC	V_{DD}=40 V, I_D=25 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	10	-	nC	V_{DD}=40 V, I_D=25 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	10	-	nC	V_{DD}=40 V, I_D=25 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	17	-	nC	V_{DD}=40 V, I_D=25 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	52	69	nC	V_{DD}=40 V, I_D=25 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	V_{DD}=40 V, I_D=25 A, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	70	93	nC	V_{DD}=40 V, V_{GS}=0 V

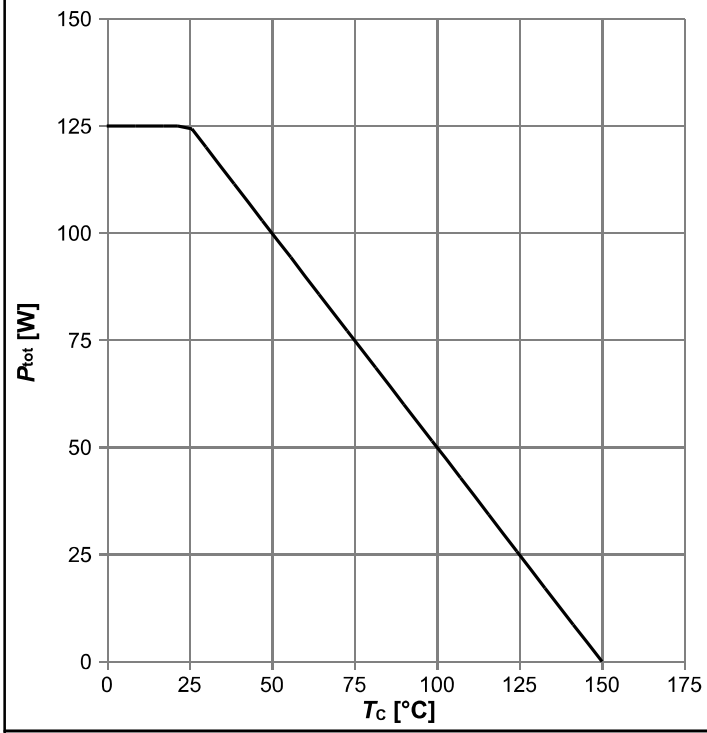
[1] Defined by design. Not subject to production test
[2] See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	107	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	500	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	1.0	1.2	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	61	-	ns	V_R=40 V, I_F=25A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	109	-	nC	V_R=40 V, I_F=25A, di_F/dt=100 A/µs

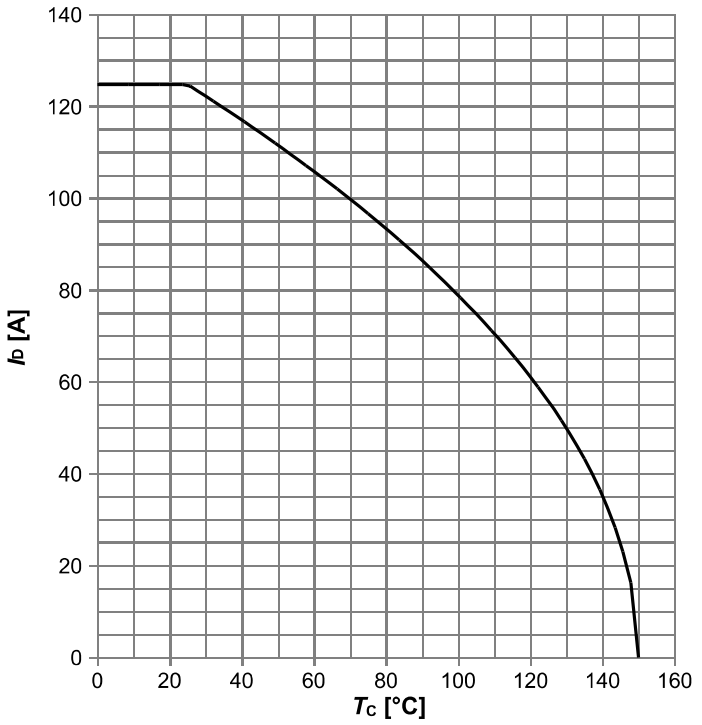
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



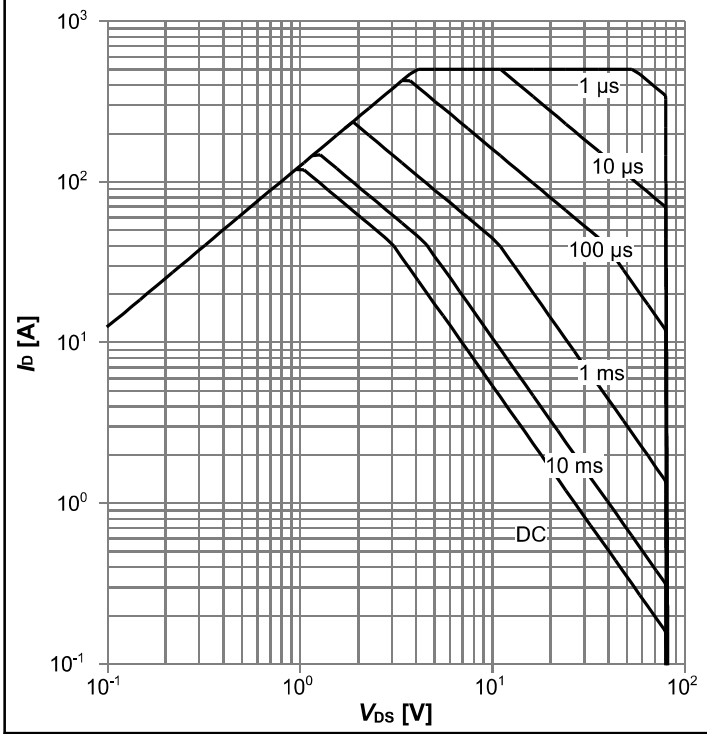
$P_{tot}=f(T_C)$

Diagram 2: Drain current



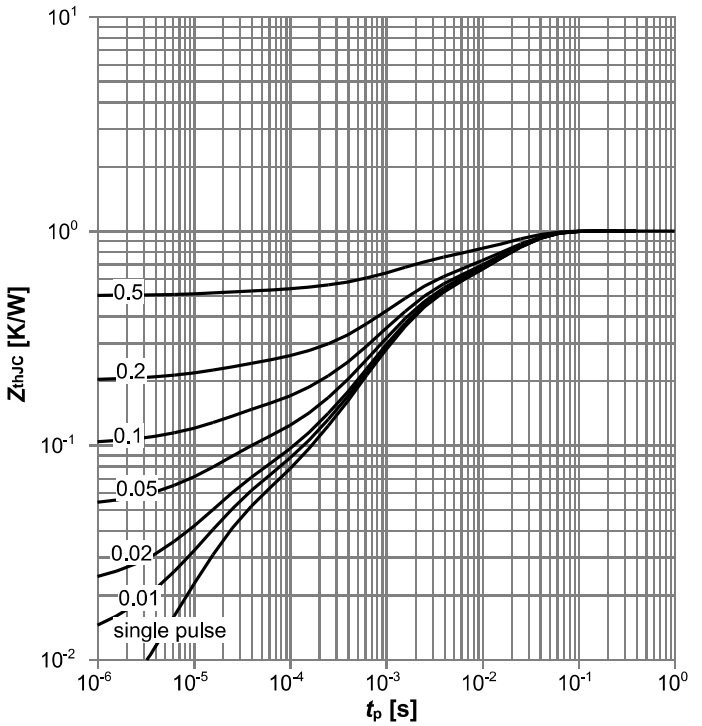
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



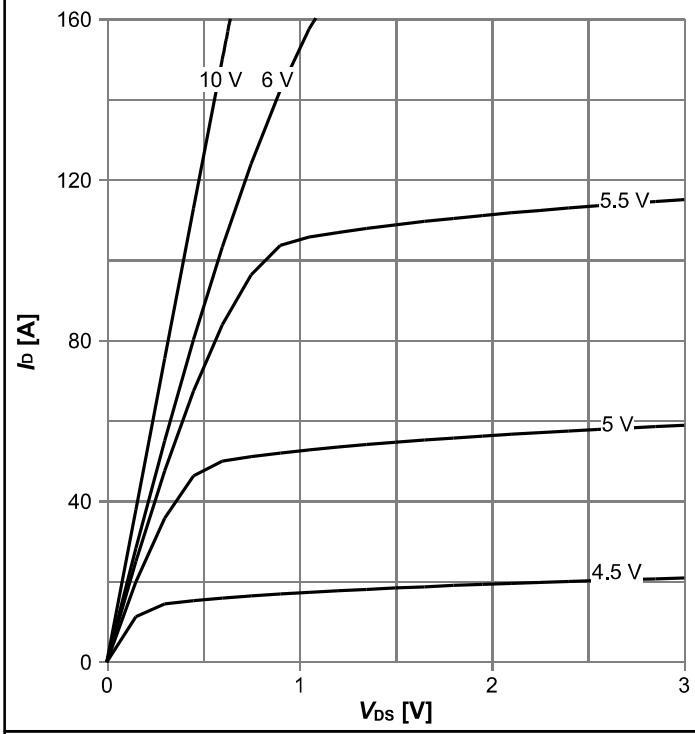
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



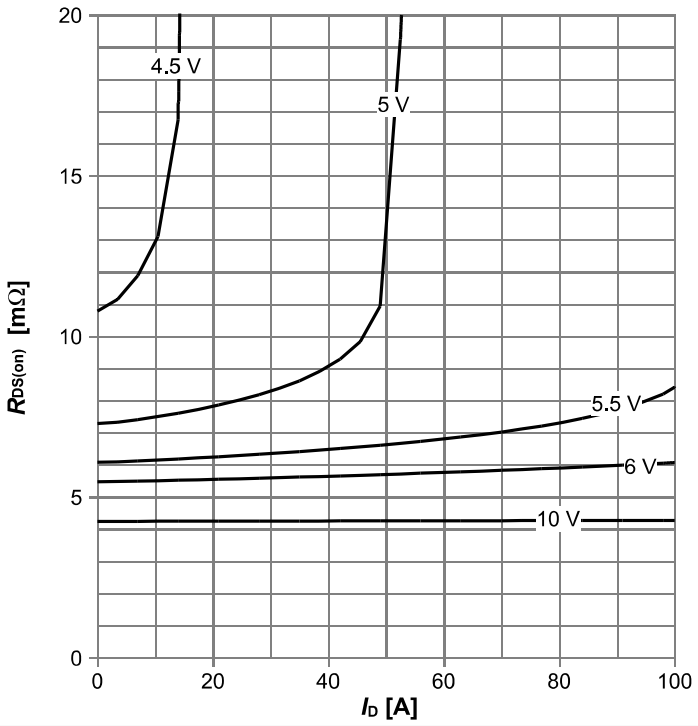
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



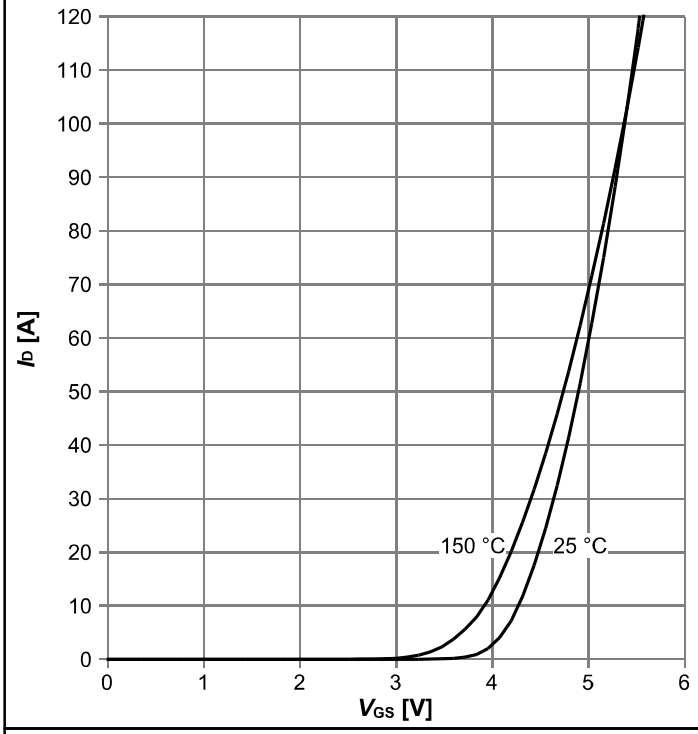
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



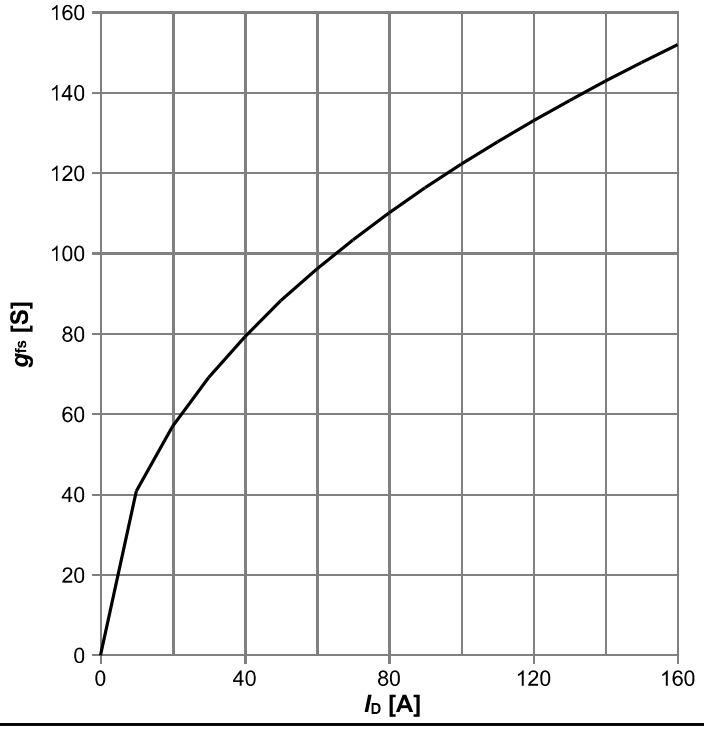
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



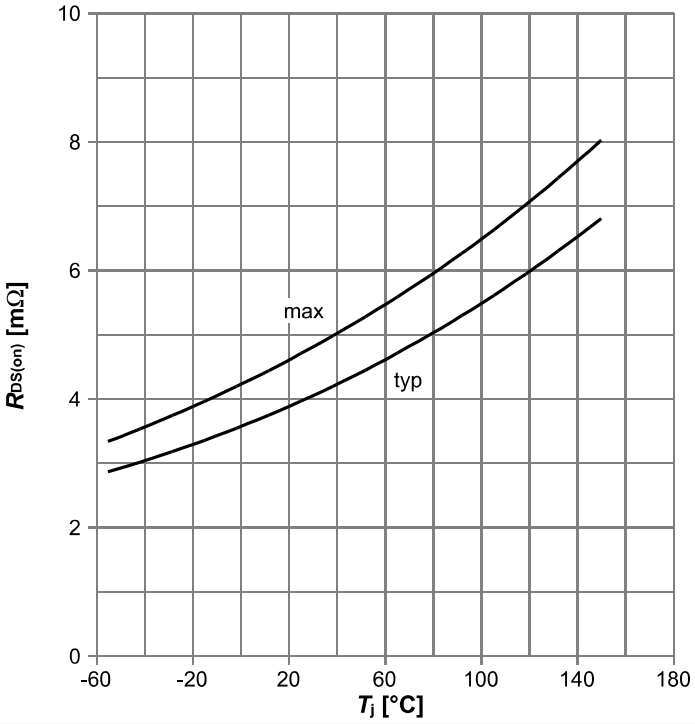
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



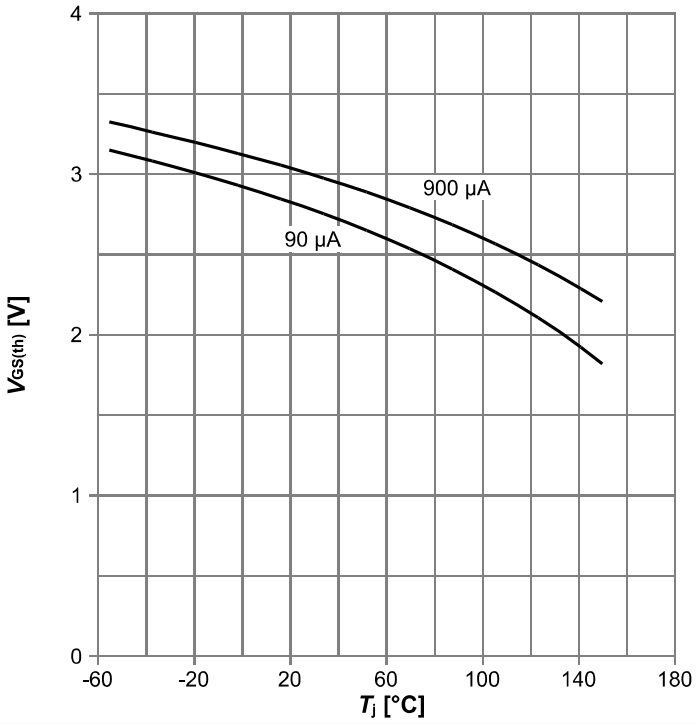
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on-state resistance



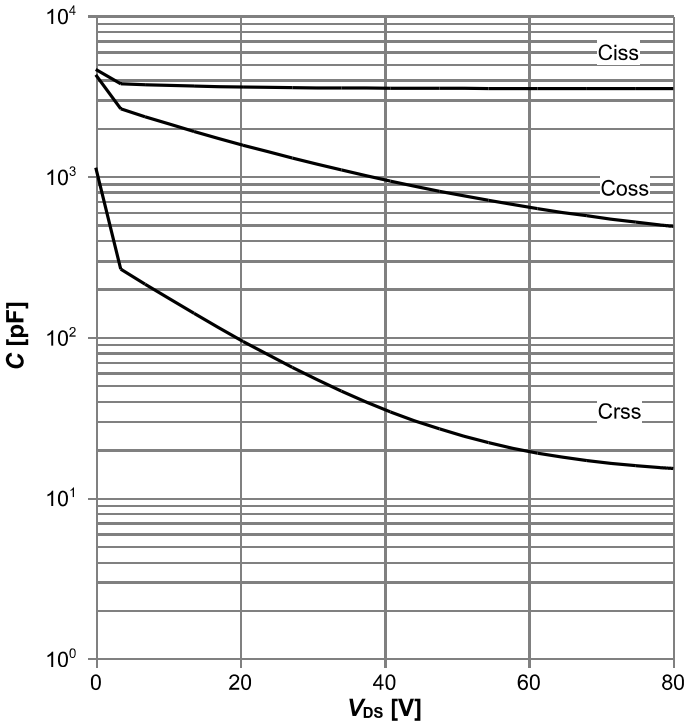
$R_{DS(on)}=f(T_j)$; $I_D=50$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



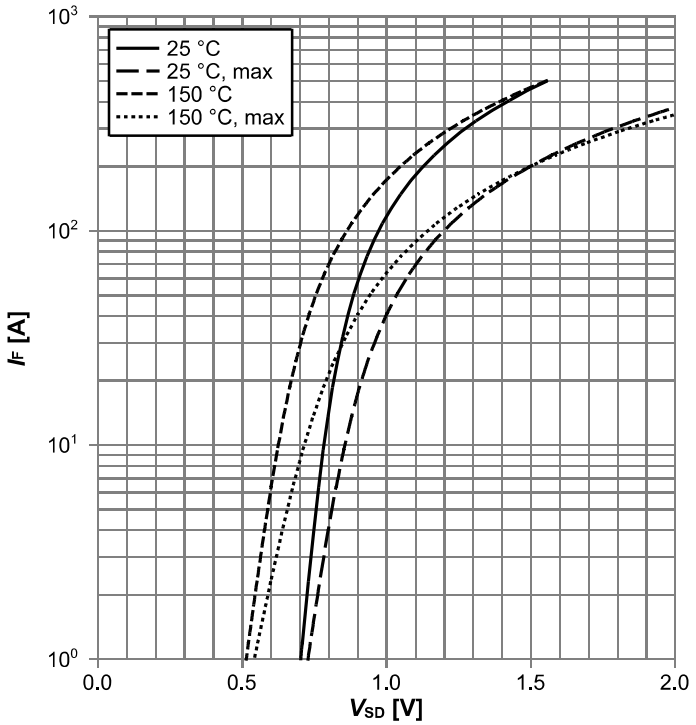
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



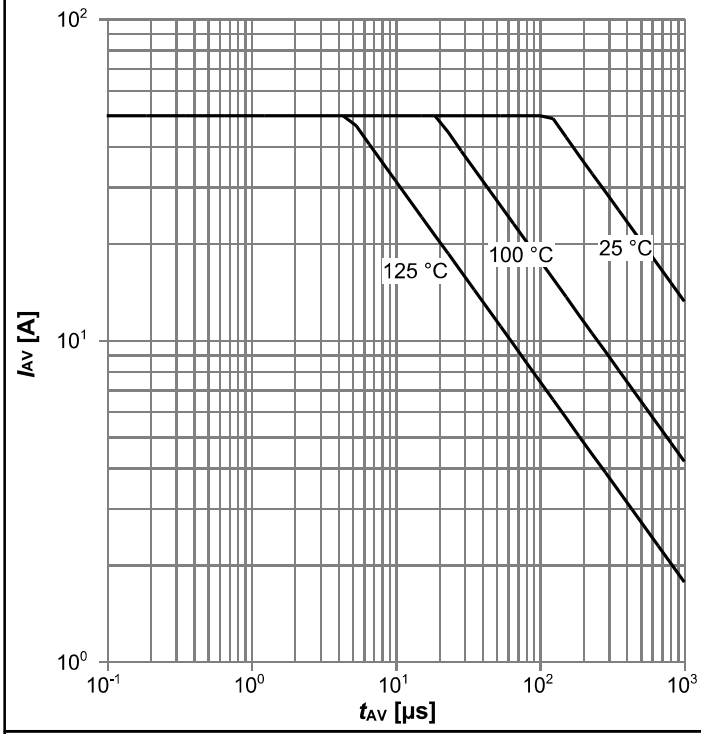
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



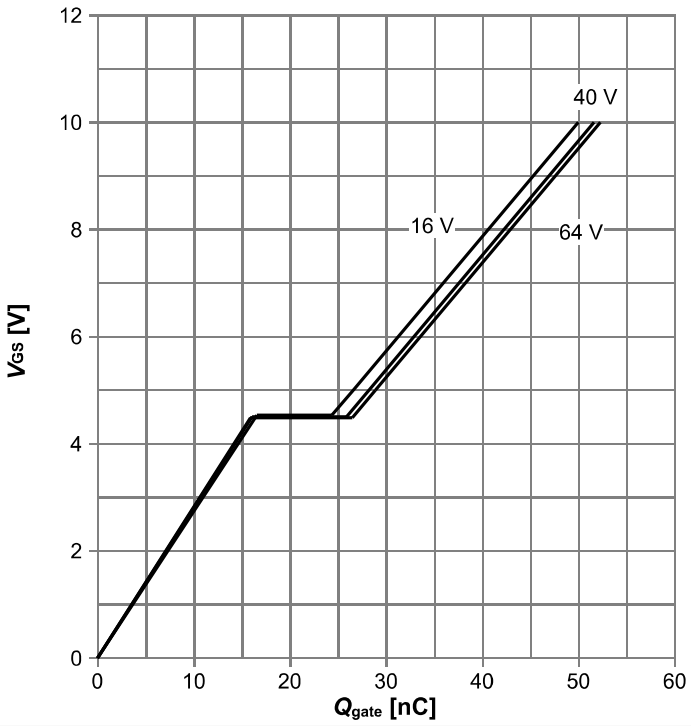
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



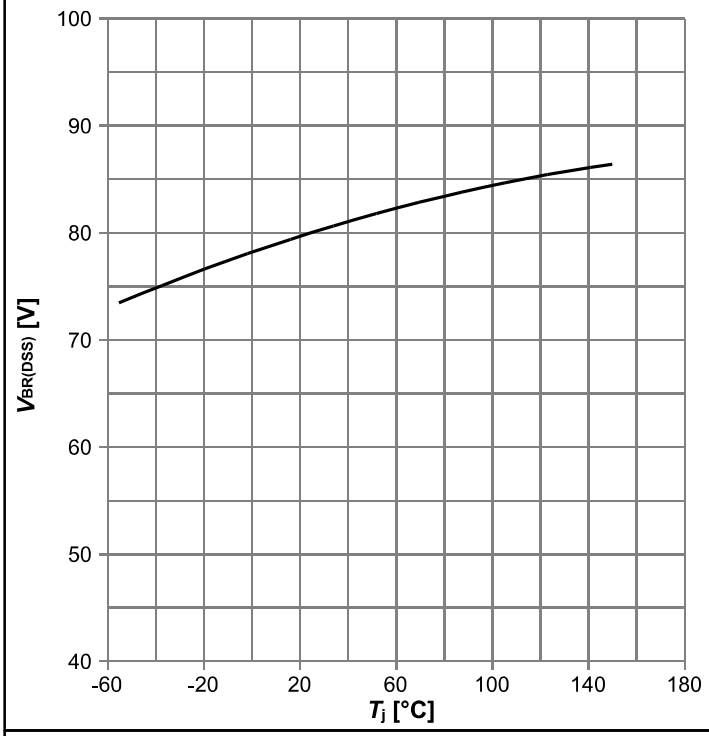
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



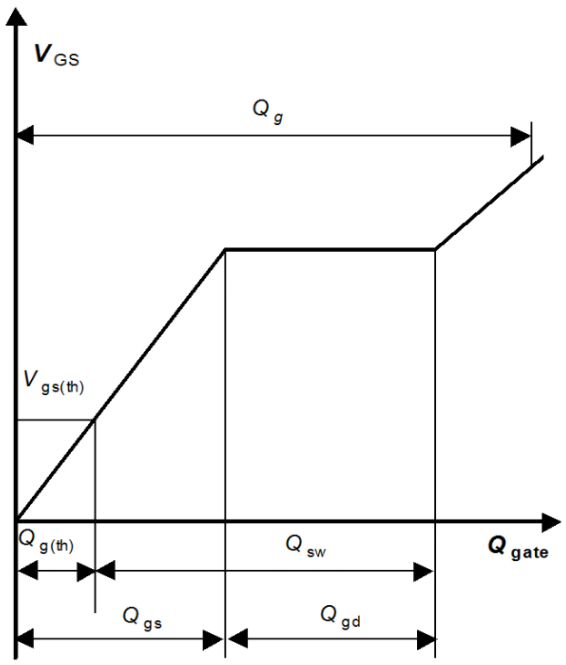
V_{GS}=f(Q_{gate}); I_D=25 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

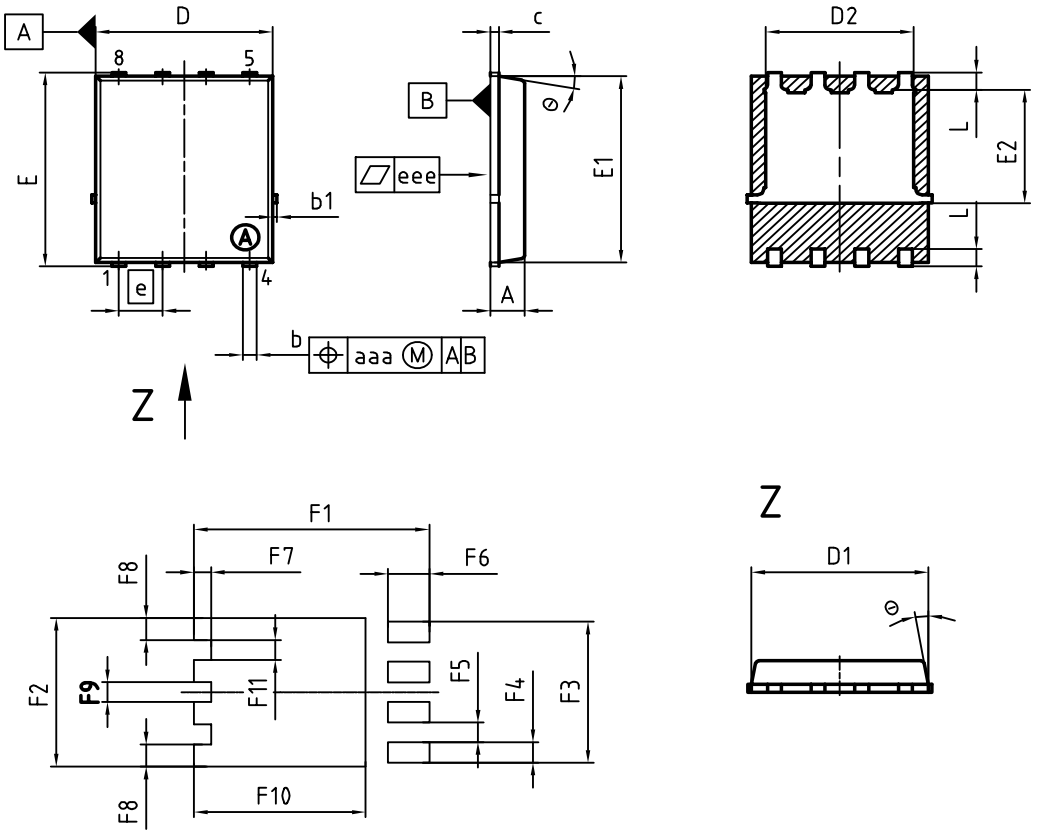


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.008
c	0.15	0.35	0.006	0.014
D=D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	3.40	3.80	0.134	0.150
e	1.27		0.050	
N	8		8	
L	0.45	0.65	0.018	0.026
Θ	8.5°	11.5°	8.5°	11.5°
aaa	0.25		0.010	
eee	0.05		0.002	
F1	6.75	6.95	0.266	0.274
F2	4.60	4.80	0.181	0.189
F3	4.36	4.56	0.172	0.180
F4	0.55	0.75	0.022	0.030
F5	0.52	0.72	0.020	0.028
F6	1.10	1.30	0.043	0.051
F7	0.40	0.60	0.016	0.024
F8	0.60	0.80	0.024	0.031
F9	0.53	0.73	0.021	0.029
F10	4.90	5.10	0.193	0.201
F11	0.53	0.73	0.021	0.029

DOCUMENT NO.
Z8B00003332

SCALE
0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
08-03-2007

REVISION
03

Figure 1 Outline PG-TDSON-8, dimensions in mm/inches

Revision History

BSC047N08NS3 G

Revision: 2020-11-12, Rev. 2.8

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.8	2020-11-12	Update current rating and footnotes

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