International
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REFERENCE DESIGN

IRPLCFL5E

International Rectifier • 233 Kansas Street, El Segundo, CA 90245 • USA

CFL Ballast for 26W/Spiral Lamp, 220VAC Input

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1. Overview

The IRPLCFL5E reference design is an electronic ballast for driving 26W compact fluorescent lamps from 220VAC. The circuit provides all of the necessary functions for preheat, ignition and on-state operation of the lamp and also includes the EMI filter and the rectification stage. The circuit is built around the IR2520D Ballast Control IC. The IR2520D provides adjustable preheat time, adjustable run frequency to set the lamp power, high starting frequency for soft start and to avoid lamp flash, fault protection for open filament condition and failure to strike, low AC line protection and auto-restart after line brownout conditions. The IR2520D is a low-cost solution specific for CFL applications. The IR2520D has only 8 pins and allows the component count for the complete ballast to be reduced down to 19 components.

2. Features

Programmable run frequency
Programmable preheat time
Open filaments and no-lamp protection
Failure to Strike and deactivated-lamp protection
Low AC line protection

3. Electrical Characteristics

Input Power: 24W @ 220VAC
Input Current: 168mArms @ 220VAC
Starting Frequency: 100KHz
Run Frequency: 40KHz
Ballast turn-on voltage: 120VAC
Ballast turn-off voltage: 70VAC

Input (VAC)	Pin (W)	Iinrms (mA)	Vbusav (V)	Freq. (KHz)	PF	THD (%)
200	21	160	280	40.3	0.63	115
210	22	160	290	40.3	0.625	117
220	24	168	300	40.3	0.62	118
230	24.2	168	310	40.3	0.62	118
240	24.5	168	320	40.3	0.61	118

4. IR2520D Ballast Control IC

The IR2520D is intended for driving CFL and TL lamps in CFL or small size ballasts applications. The IR2520D integrates all of the necessary functions for preheat, ignition and on-state operation of the lamp, plus, lamp fault protection and low AC-line protection, together with a complete high- and low-side 600V half-bridge driver, the IR2520D has only 8 pins and fits into a standard SO8 or DIP8 package. The IR2520D has been designed to overcome the disadvantage of discrete self-oscillating solutions while maintaining low cost.

In the CFL market, the self-oscillating bipolar transistor solution remains very popular. This approach is very simple in nature but has many disadvantages including: DIAC or additional circuit required for starting, additional free-wheeling diodes required, operating frequencies determined by bipolar transistor storage time and toroid saturation (not easy to design, very dependent on tolerances in production and difficult to set the frequencies precisely), unreliable “always hot” PTC thermistor used for preheat that often fails in the field, no protection against lamp non-strike or open filaments conditions, no smooth frequency ramping during ignition, capacitive mode operations, high crest factor in the lamp current. These drawbacks can result in high susceptibility to components and load tolerances, short lamp life and/or catastrophic failure of ballast output stage components.

The heart of the IR2520D is a voltage controlled oscillator (VCO) with externally programmable minimum frequency and 0-5VDC analog voltage input. The IC includes adaptive zero-voltage switching

(ZVS) and non-ZVS protection, as well as an integrated bootstrap diode. The IC protects against non-ZVS by automatically setting the frequency to ensure ZVS. The IC will eventually shut-down if the non-ZVS condition cannot be achieved.

One of the biggest advantages of the IR2520D is that it incorporates an internal current crest factor driven shutdown function and it eliminates the need for a high-precision current sensing resistor that is typically used to detect over current. The IC uses the VS pin and the RDSon of the low-side half-bridge MOSFET for over-current protection and to detect non-ZVS conditions. An internal 600V FET connects the VS pin to the VS sensing circuitry and allows for the VS pin to be accurately measured during the time when pin LO is high, while withstanding the high DC bus voltage during the other portion of the switching cycle when the high-side FET is turned on and VS is at the DC bus potential. Please refer to the IR2520D data sheet for further information on the IR2520D including electrical parameters, state diagram and complete functional description. As a result of the IR2520D features, the IRPLCFL5E circuit using the IR2520D is a complete CFL solution that offers better reliability and longer lamp life than self oscillating solutions while reducing component count and ballast size.

5. Circuit Description

The schematic for IRPLCFL5E is shown in figure 5.1. The BOM with the components values is shown in table 5.2.

The ballast incorporates a fuse, EMI filter, input rectifier, bus capacitor, half-bridge, control and output stage. The output stage is the classical resonant circuit consisting of an inductor, LRES, and a capacitor, CRES. The circuit is built around the IR2520D Ballast Control IC. The IR2520D provides adjustable preheat time, adjustable run frequency to set the lamp power, high starting frequency (about 2.5 times fmin) to avoid lamp flash, capacitive mode protection for open filament condition and current crest factor protection for failure to strike or no lamp conditions.

The AC line input voltage is rectified to provide a bus voltage of approximately 300 volts. The start up resistors, Rsupply1 and Rsupply2, are sized such that they can supply the micro-power current during under-voltage lockout (UVLO). When VCC exceeds the UVLO+ threshold, the IR2520D begins to oscillate and the charge pump circuit (CSNUB, DCP1 and DCP2) supplies the current to VCC that causes the internal 15.6V zener clamp to regulate.

The IR2520D Ballast Control IC controls the frequency of the half-bridge as well as the ballast states and protection modes such as lamp preheat, lamp ignition, running mode, low AC line protection and lamp/ballast fault protection.

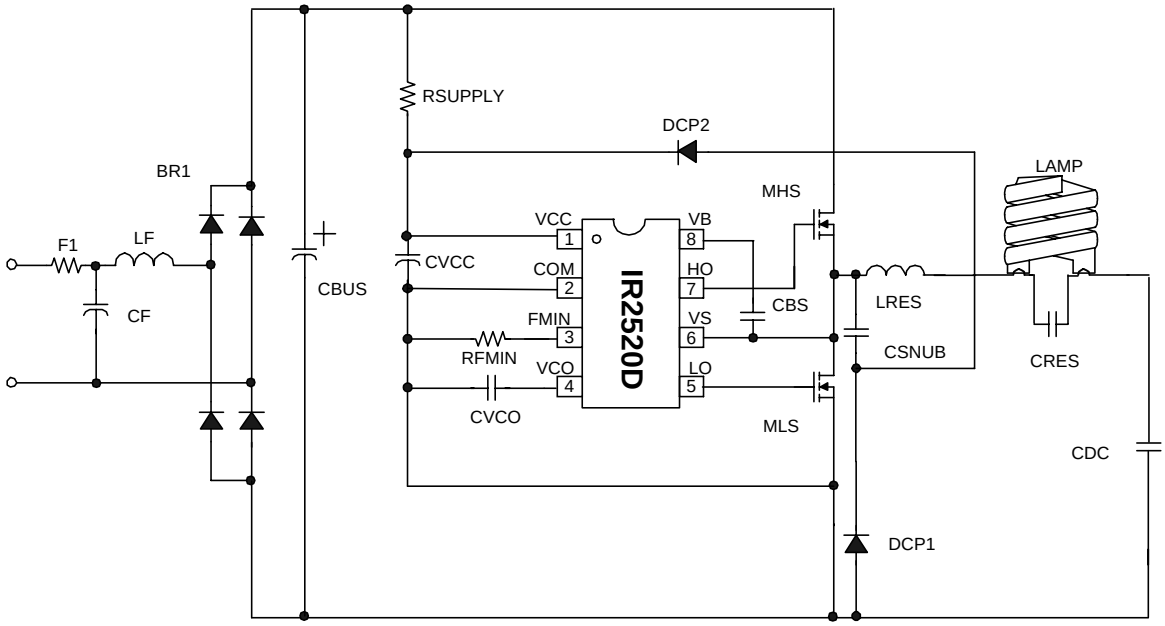

Fig. 5.1) IRPLCFL5E Circuit Diagram

Item #	Qty	Manufacturer	Part Number	Description	Reference
1	1	International Rectifier	DF10S	Bridge Rectifier, 1A 1000V	BR1
2	1	Dale	CW-1/2	Resistor, 0.5Ohm, 1/2W	F1
3	1	Panasonic	ECQ-U2A104ML	Capacitor, 0.1uF 275 VAC	CF
		Digikey	P10730-ND		
4	1	Epcos	B82145-A1105-J	EMI Inductor, 1mH 370mA	LF
		Digikey	M5830-ND	RF Chockes 1mH 200mA	
5	1	Wima	MKS2 Series	Capacitor, 47nF 400V	CDC
6	1	Panasonic	EEU-EB2V100	Capacitor, 10uF 350VDC 105C	CBUS
7	1	Panasonic	ECJ-3VB1H104K	Capacitor, 0.1uF 50V 1206	CBS
8	1	Panasonic	ECJ-3VF1E474Z	Capacitor, 0.47uF 25V 1206	CVCO
9	1	Panasonic	ECY-3YB1E105K	Capacitor, 1uF 25V 1206	CVCC
10	1	AVX Johanson	1812AA681J 102S43W681KV	Capacitor, 680pF 1KV SMT 1812	CSNUB

Item #	Qty	Manufacturer	Part Number	Description	Reference
11	1	Wima	MKP4 Series	Capacitor, 4.7nF 1KV Polypropylene	CRES
12	1	International Rectifier	IR2520D	IC, Ballast Driver	IC BALLAST
13	1	VOGT	5750924800	Inductor, 2.25mH, 5%, 1Apk	LRES
14	2	International Rectifier	IRFU320	Transistor, MOSFET	MHS, MLS
15	2	Panasonic		Resistor, 1M, 1206, 100V	RSUPPLY1, RSUPPLY2
16	1	Panasonic	ERJ-8ENF6812V	Resistor, 68.1K, 1%, 1206	RFMIN
17	2	Diodes	LL4148DICT-ND	Diode, 1N4148 SMT DL35	DCP1, DCP2
Total	20				

TABLE 5.2) IRPLCFL5E Bill Of Materials. Lamp type: Spiral CFL 26W, Line Input Voltage:190-240 VAC. Note: Different lamp types may require BOM changes.

6. Functional Description

Figure 6.1 shows the voltage across the lamp and the current in the resonant inductor LRES during Startup, Preheat, Ignition and Run Mode.

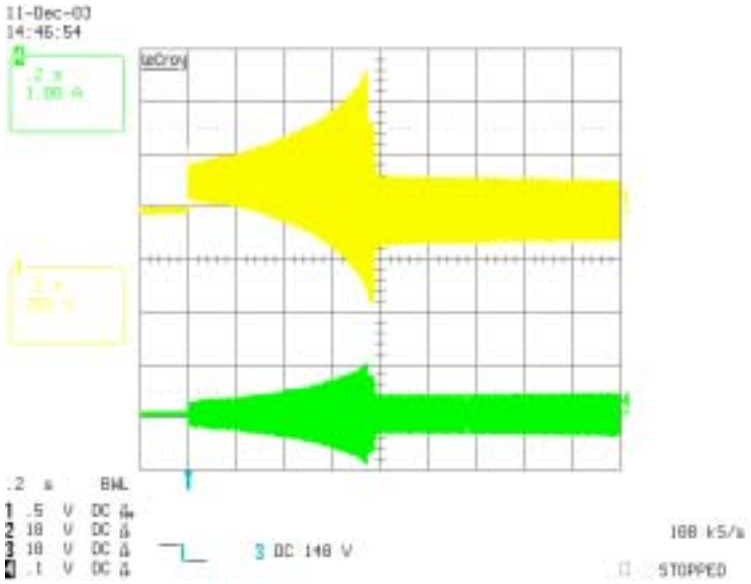

Fig. 6.1: Voltage across the lamp (yellow waveform) and current in the resonant inductor (green waveform) during Startup, Preheat, Ignition and Run Mode

When power is turned on, the IR2520D goes into Under Voltage Lockout (UVLO) mode.
The UVLO mode is designed to maintain a very low (<200uA) supply current and to guarantee that the IC is fully functional before the high- and low-side output drivers are activated. During UVLO, the high- and low-side driver outputs (LO and HO) are both low and pin VCO is pulled down to COM for resetting the starting frequency to the maximum.

Once VCC reaches the startup threshold (UVLO+), the IR2520D turns on and the half-bridge FETs start to oscillate. The IC goes into Frequency Sweep Mode. At startup, VCO is 0V and the frequency is very high (about 2.5 times fmin). This minimizes voltage spikes and lamp flash at startup. The frequency ramps down towards the resonant frequency of the high-Q ballast output stage, causing the lamp voltage and lamp current to increase. During this time, the filaments of the lamp are pre-heated to the emission temperature to guarantee a long lamp life. The frequency keeps decreasing until the lamp ignites. If the lamp ignites successfully, the IR2520D enters RUN Mode. If the minimum frequency has been chosen below or very close to the resonant frequency, the IC will work near resonance and will adjust the frequency continuously to maintain ZVS at the half-bridge and to minimize the losses in the FETs. If the minimum frequency has been chosen higher than the resonant frequency the IR2520D will work at the minimum frequency. Figure 6.2 shows the current across the resonant inductor and the voltage across the lamp filaments at startup.

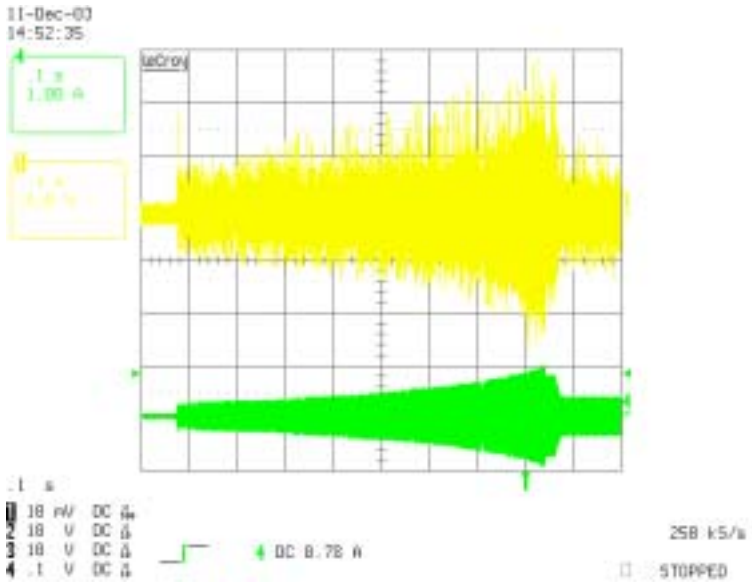

Figure 6.2: Voltage across the lamp filaments (yellow) and current in the resonant inductor (green) at startup

Figure 6.3 shows the VS (HB) Voltage, the lamp voltage and the lamp current during Run Mode.

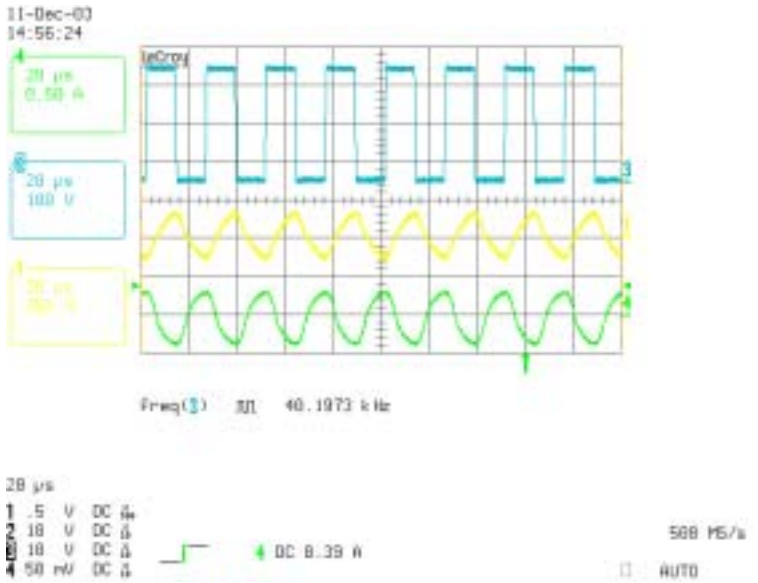

Figure 6.3: VS (HB) Voltage (blue), Lamp Voltage (yellow) and the Lamp Current (green) during Run Mode.

7. Fault Conditions

In case of fault conditions such as open filaments, failure to strike, deactivated lamp or no lamp, the IR2520D will go into Fault Mode. In this mode the oscillator is latched off. To reset the IC back to preheat mode, VCC must be recycled below and above the UVLO thresholds. This is done by resetting the mains. In case of low AC line, the IR2520D will automatically increase the frequency to maintain ZVS. In this way, the ballast will work at a lower power during a low AC line condition and will operate at the proper power again when the line increases again.

7.1. Failure To Strike/ Deactivated Lamp Protection

This protection relies on the crest factor protection together with the non-ZVS circuit of the IR2520D, both enabled when the voltage at the VCO pin reaches 4.6V.

In order to detect failure to strike conditions, the IR2520D performs an internal crest factor measurement for detecting excessive dangerous currents or inductor saturation that can occur during a lamp non-strike fault condition or a deactivated lamp condition. The IR2520D measures the VS pin during the entire on-time of the low-side MOSFET. Should the peak current exceed the average current by a factor of 5 during the on-time of LO, the IC will enter Fault Mode and both gate driver outputs will be latched 'low'.

Performing the crest factor measurement provides a relative current measurement that cancels temperature and/or tolerance variations of the RDSon of the low-side half-bridge MOSFET and does not need to be programmed differently for different lamp types. During normal operation, the current will increase until the lamp ignites. After lamp ignition the current will decrease down to the nominal current. Should a lamp non-strike condition occur where the filaments are intact but the lamp does not ignite, the lamp voltage and output stage current will increase during the ignition ramp until excessive currents occur or the resonant inductor saturates. The non-ZVS circuit or the crest factor circuit will detect this condition and the IC will enter Fault Mode and both gate driver outputs will be latched 'low'. This will prevent damaging of the half-bridge MOSFETs.

Fig. 7.1 shows the inductor current and the lamp voltage in case of failure to strike condition together with the VCO pin voltage. At initial turn-on of the ballast, the frequency will ramp down from fmax, through resonance, to fmin. If the lamp does not ignite, the inductor will saturate and high-voltages will occur across the lamp as the frequency sweeps through resonance. The voltages and currents in the output stage will decrease as the frequency continues to decrease to the capacitive side of resonance. The voltages and currents will be low but hard-switching will occur (non-ZVS). When the frequency reaches fmin (VCO > 4.6V), the non-ZVS and crest-factor protection will be activated and the frequency will increase again to try and maintain ZVS. The frequency will sweep back through resonance (from the capacitive side) and the crest-factor protection will shutdown the IC on the first event when the inductor saturates to a level where the crest factor exceeds 5 (see Fig. 7.1).

Fig. 7.2 shows pin LO, pin VS and the current in the resonant inductor during shutdown, with a shorter time scale. The final shortened pulse of LO just before shutdown (Fig. 7.2) occurs due to the internal 1us blank time of the crest-factor detection during each turn-on rising edge of LO (to provide immunity to noise and transients).

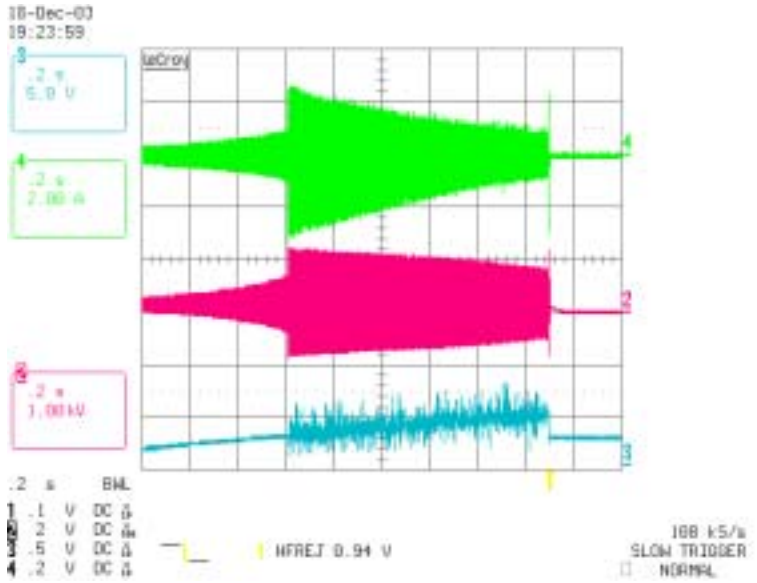

Fig. 7.1: 4 is the current in the resonant inductor, 2 is the lamp voltage, 3 is the voltage in pin VCO

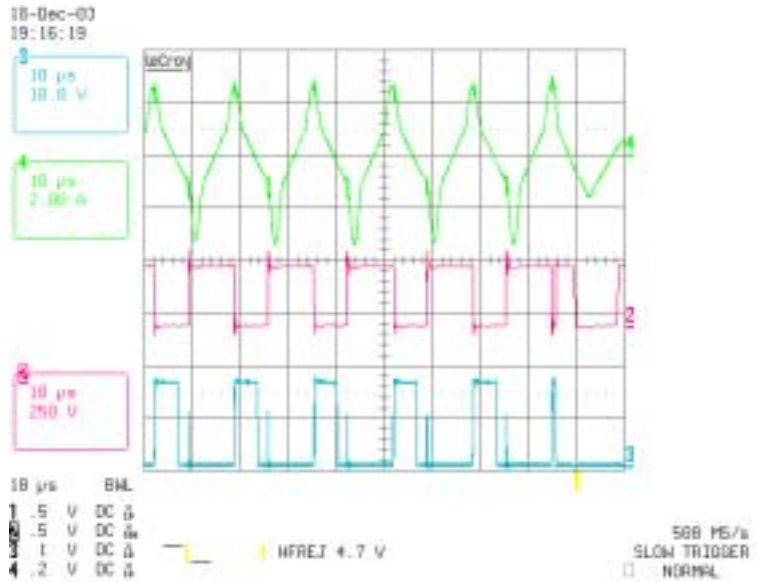

Fig. 7.2: 4 is the current in the resonant inductor, 2 is pin VS (HB Voltage), 3 is pin LO

7.2. Open Filaments Protection

The open filament protection relies on the non-ZVS circuit of the IR2520D, enabled when pin VCO reaches 4.6V. Should an open filament lamp fault occur, hard-switching will occur at the half-bridge and the non-ZVS circuit inside the IR2520 will detect this condition, increase the frequency each cycle and shut down when VCO decreases below 0.85V; both gate driver outputs will be latched 'low'. This will prevent hard-switching and damaging of the half-bridge MOSFETs.

Fig. 7.3 shows the VCO pin and VS pin at the shutdown with open filament. As you can see, at startup the VCO pin charges from 0V up to 4.6V, at 4.6V the non-ZVS circuit is enabled, CVCO discharges and the frequency increases. When the voltage at the VCO pin decreases below 0.85V we have latched shutdown. Fig. 7.4 shows the voltage at the VCO pin (HB Voltage) at the shutdown with a shorter time scale. The FMIN pin can be used as trigger as this pin transitions from 5V to COM when the IC enters fault mode or UVLO-.

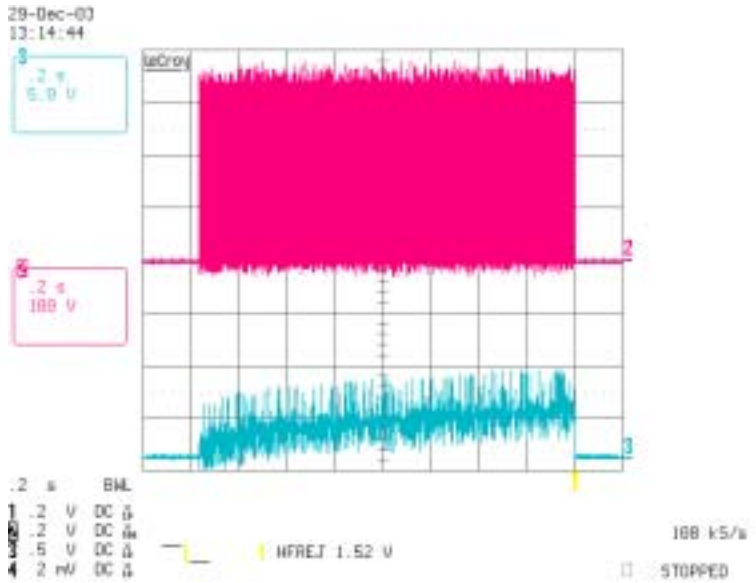

Fig. 7.3: 3 is the voltage in pin VCO and 2 is pin VS

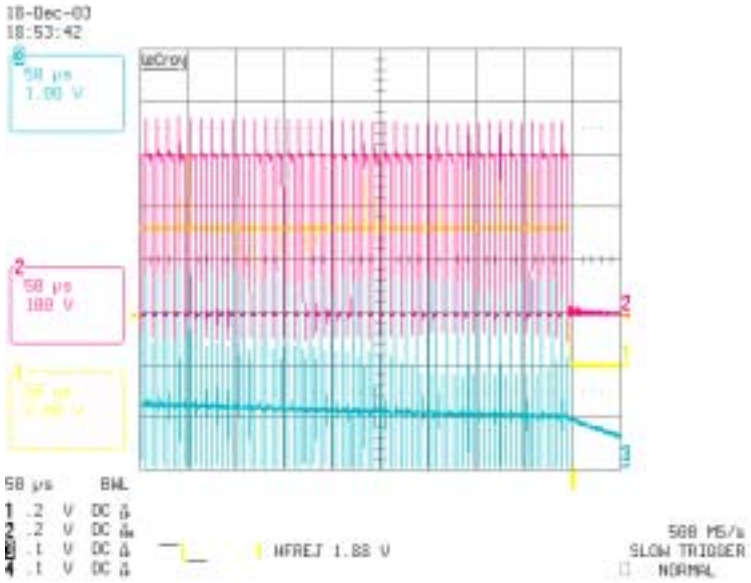

Fig. 7.4: 1 is the voltage in pin FMIN, 3 is the voltage in pin VCO, 2 is pin VS

7.3. Low AC line Protection

As you can see from figure 7.5, varying the AC line from 220V to 130VAC the ZVS circuit of the IR2520D increases automatically the frequency to maintain ZVS.
When the mains voltage decreases, the resonant frequency increases, becoming close to the run frequency. This will cause non-ZVS. The IR2520D will detect non-ZVS and increase the frequency continuously as long as non-ZVS is detected. This will protect the half-bridge MOSFETs against hard-switching.

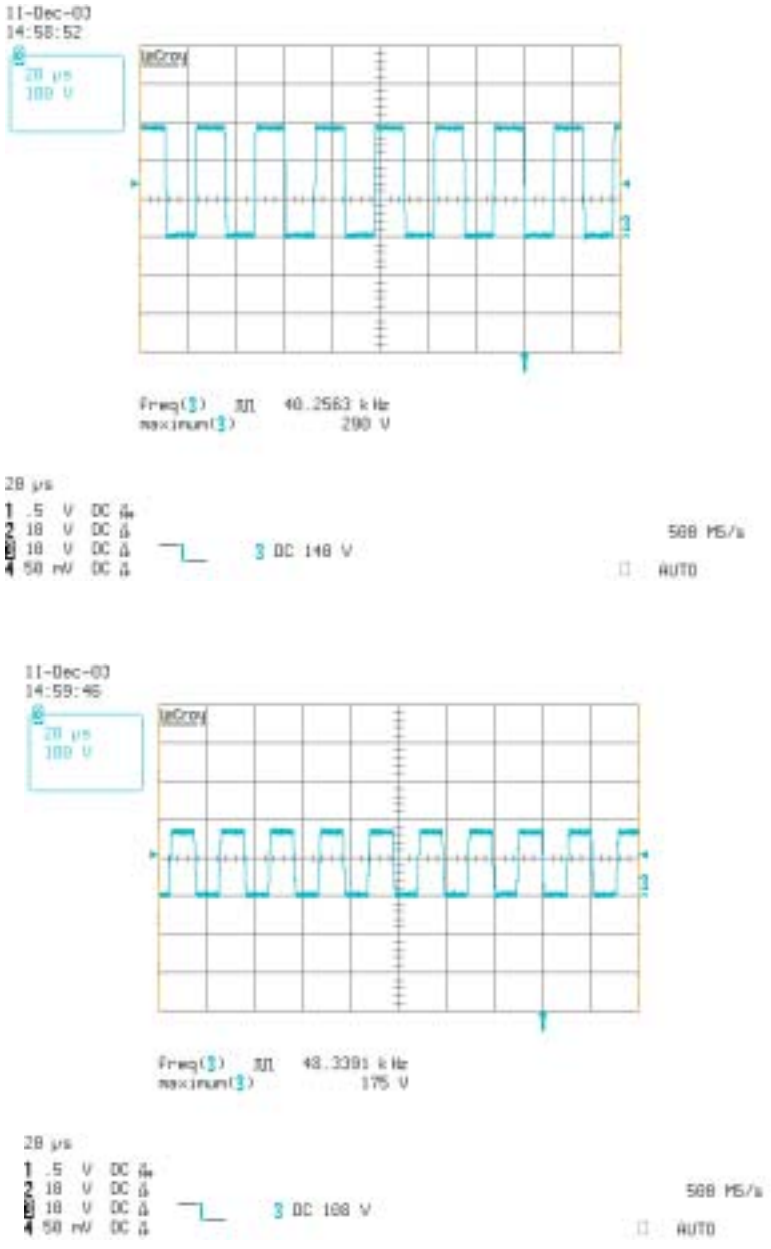

Figure 7.5: VS PIN for AC line 220V (on the top) and AC line 130V (on the bottom)

8. IRPLCFL5E Layout

The Layout of the Reference Kit IRPLCFL5E is shown in Fig. 8.1.
The critical components are CVCC, CVCO, RFMIN and CBOOT. They must be placed as close as possible to the pins of the IR2520D. The ground of CCVO, RFMIN and CVCC need to be connected to pin COM of the IR2520D and this ground path must be connected to the power ground at a single point.

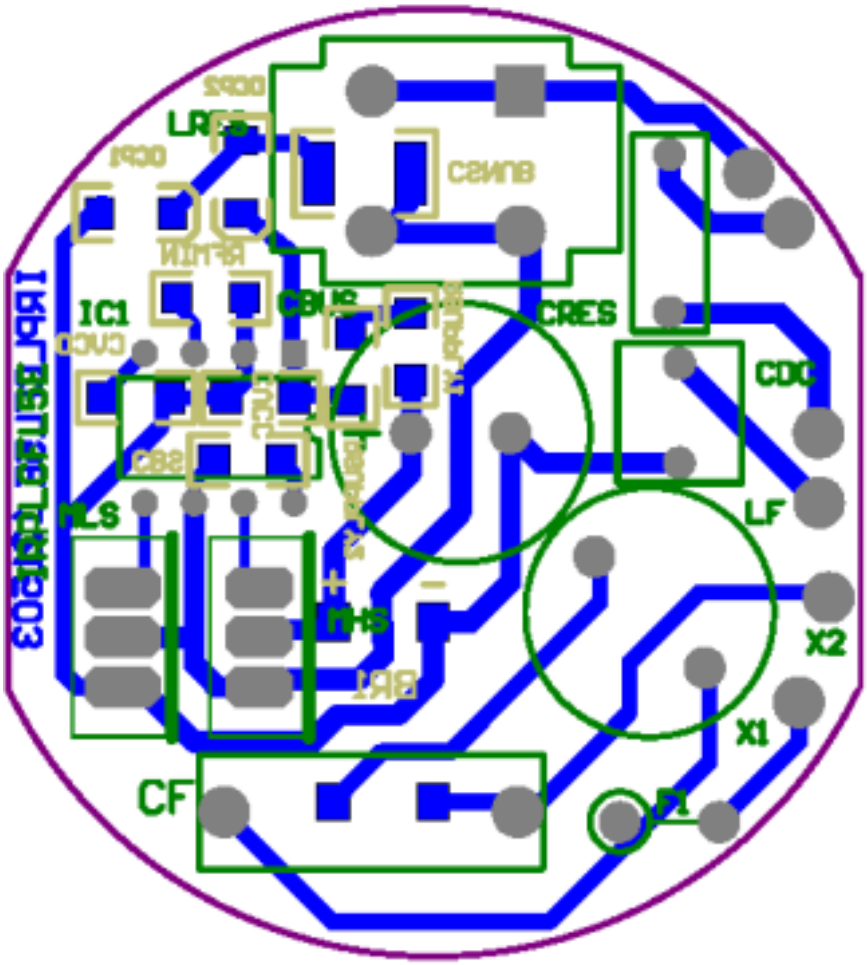

Figure 8.1: IRPLCFL5E Layout

9. Design Procedure to adapt the design to different lamps types

Designing with the IR2520D is very simple because it only has 2 control pins: VCO (0-5VDC oscillator voltage input) and FMIN (minimum frequency setting). To modify the design for a higher lamp power, you will need to modify RFMIN, CVCO, LRES and CRES. Make sure that the FETs and inductors are rated for the current you need with the new lamp and that VCC is stable. To modify the design to a lower lamp power, you will need to decrease RFMIN and, in some cases, to also modify CVCO, LRES and CRES. In most cases you can use FETs and inductors with lower current ratings.

The FMIN pin is connected to ground through a resistor (RFMIN). The value of this resistor programs the minimum frequency (fmin) of the IC and the starting frequency of the IC (about 2.5xfmin). The IR2520D will work in run mode at the minimum frequency unless non-ZVS is detected. Generally, to work with constant frequency, the minimum frequency needs to be chosen above the resonant frequency of the low-Q R-C-L circuit. In this case, one can increase the value of RFMIN to decrease the frequency and increase the lamp power, or, decrease the value of RFMIN to increase the run frequency and decrease the lamp power.

The VCO pin is connected to ground through a capacitor (CVCO). The value of this capacitor programs the time the frequency needs to ramp down from 2.5 times fmin (fmax) to fmin. One can increase the capacitor value to increase the preheat time, or, decrease the capacitor value to decrease the preheat time.

The suggested design procedure is as follows:

1) Use the Ballast Design Assistant (BDA) software to calculate LRES and CRES.
Select the input configuration without PFC, select the IR2156 IC and select single lamp current mode configuration. Select the new lamp in the database or add the lamp parameters by hand selecting the “Advanced” option.
Calculate the operating point and chose the right values of L and C that satisfy:

1.1) Run frequency (best working range) 40-50KHz
1.2) C as small as possible to minimize losses (suggested value 4.7nF)
1.3) L values you have available

2) While measuring LO, apply 15V between the VCC pin and the COM pin and adjust the value of RFMIN to obtain the right minimum frequency (it is suggested set fmin = run frequency obtained with the BDA software). Increase RFMIN to decrease the minimum frequency or decrease RFMIN to increase the minimum frequency.

3) Apply the AC input and check preheat, ignition and run states of the lamp.

3.1) If the lamp ignites during preheat, the preheat current is too small or the starting voltage across the lamp is too big, increase the value of CRES to decrease the voltage across

the lamp during preheat and startup while increasing the preheat current. LRES may need to be decreased to maintain the same power and the same frequency.

3.2) If the IC works at a frequency greater than fmin, increase CRES or LRES to decrease the resonant frequency avoiding hard-switching, or, decrease the value of the snubber capacitor CSNUB (a CSNUB minimum value of 680pF is suggested to make sure VCC stays above the UVLO-).

3.3) If VCC drops, increase the value of CSNUB or CVCC

4) Adjust the value of RFMIN to have the right power on the lamp (increase RFMIN to increase power or decrease RFMIN to decrease power) and the value of CVCO to set the correct preheat time (increase CVCO to increase the preheat time and decrease CVCO to decrease the preheat time).

5) Test the ballast over the entire input range and make sure that the frequency does not change dramatically in your working range. Select the value of RSUPPLY to have startup at the correct AC line voltage. Increase the value of RSUPPLY to start the IC at higher AC voltages and decrease the value of RSUPPLY to start the IC at lower AC voltages.

6) Test your lamp life (number of starts). A good design should guarantee at least 5,000 starts. To increase the number of starts, increase CRES or the preheat time (CVCO).