Z86C83/C84/E83

CMOS Z8® MCU

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86C83	4	237	21	3.0V to 5.5V
Z86E83	4 (OTP)	237	21	3.5V to 5.5V
Z86C84	4	237	17	3.0V to 5.5V

Note: * General-Purpose

- 28-Pin DIP, SOIC, and PLCC Packages
- Clock Speed: 16 MHz
- Three Expanded Register Groups
- 8-Channel, 8-Bit A/D Converter with Track and Hold, and Unique R-Ladder A_{GND} Offset Control
- Z86C84 has two 8-Bit D/A Converters with Programmable Gain Stages, 3 µs Settling Time
- Six Vectored, Prioritized Interrupts from Six Different Sources
- Two Analog Comparator Inputs with Programmable Interrupt Polarity
- Two Programmable 8-Bit Timers, each with a 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer
- Permanent Watch-Dog Timer (WDT) Option
- Software-Programmable Pull-Up Resistors (Port 2 Only)
- On-Chip Oscillator for Crystal, Resonator or LC
- ROM Protect

GENERAL DESCRIPTION

The Z86C83/C84/E83 are full-featured members of the Z8® MCU family offering a unique register-to-register architecture that avoids accumulator bottlenecks for higher code efficiency than RISC processors.

The Z86C83/C84/E83 are designed to be used in a wide variety of embedded control applications, such as appliances, process controls, keyboards, security systems, battery chargers, and automotive modules.

For applications requiring powerful I/O capabilities, the Z86C83/C84/E83 devices can have up to 21/17 (83/84 respectively) pins dedicated to input and output. These lines are grouped into three ports, and are configured by software to provide digital/analog I/O timing and status signals.

An on-chip, half-flash 8-bit ±1/2 Least Significant Bit (LSB) A/D converter can multiplex up to eight analog inputs. Unused analog inputs revert to standard digital I/O use. Unique, programmable A_{GND} offset control of the A/D resistor ladder compresses the converter's dynamic range for maximum effective 9-bit A/D resolution.

The Z86C84 has two 8-bit ±1/2 LSB D/A converters. High and low reference voltages provide precise control of the output voltage range. Programmable gain for each D/A converter provides a maximum effective 10-bit resolution for many tasks.

On-chip 8-bit counter/timers with many user-selectable modes simplify real-time tasks, such as counting, timing, and generation of PWM signals.

The designer can prioritize six different maskable, vectored, internal or external interrupts for efficient interrupt handling and multitasking functions.

GENERAL DESCRIPTION (Continued)

By means of an expanded register file, the designer has access to additional control registers for configuring peripheral functions including the A/D and D/A converters, counter/timers, and I/O port functions (Figure 1).

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{CC}
Ground	GND	V_{SS}

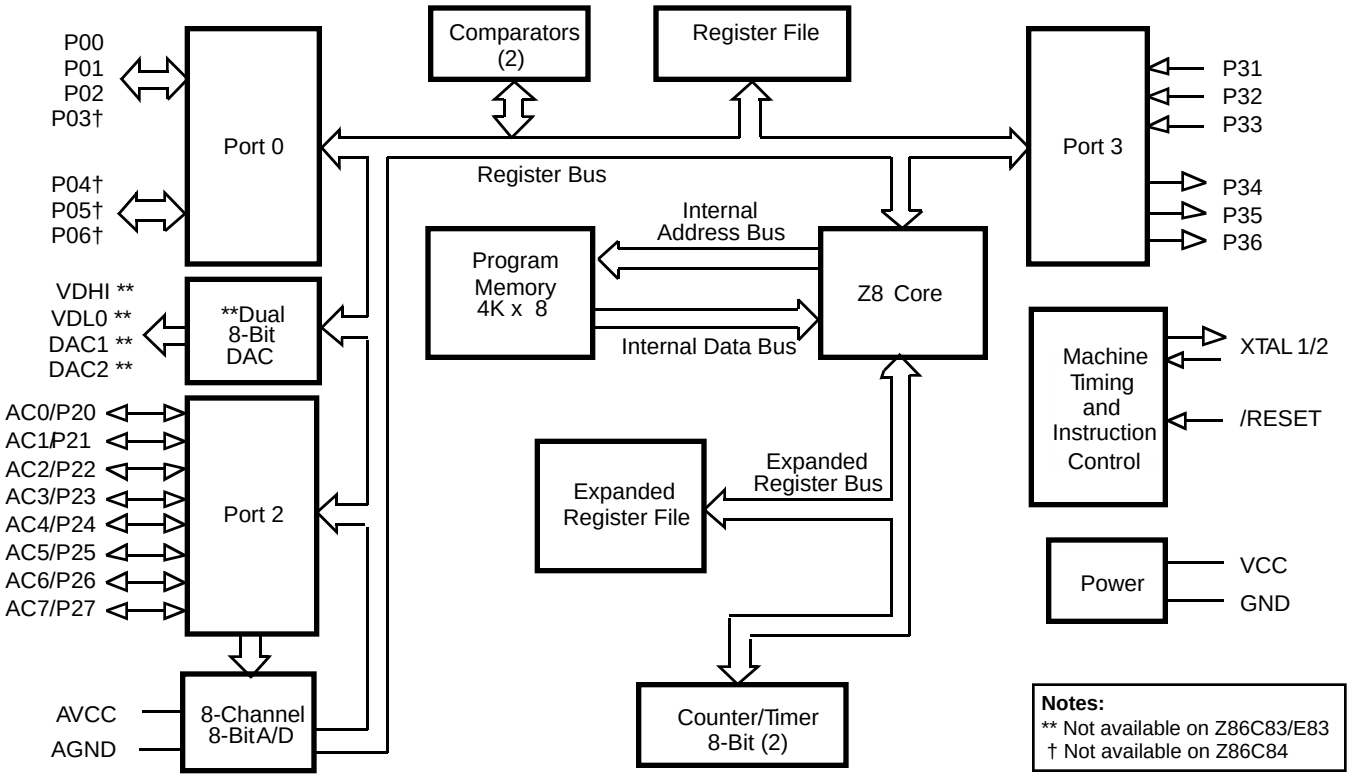


Figure 1. Z86C83/C84/E83 Functional Block Diagram

PIN DESCRIPTION

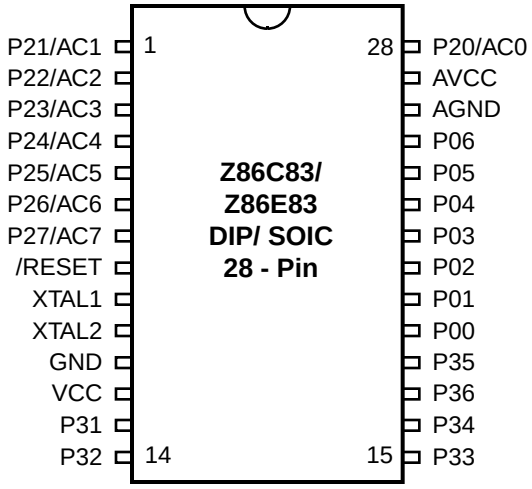


Figure 2. Z86C83 and Standard Mode Z86E83 28-Pin DIP and SOIC Pin Configuration*

Table 1. Z86C83 and Standard Mode Z86E83 28-Pin DIP, SOIC, PLCC Pin Identification*

No	Symbol	Function	Direction
1-7	P21-P27 or AC1-AC7	Port 2, Bit 1-7 Analog In 1-7	Input/Output
8	/RESET	Reset	Input
9	XTAL1	Oscillator Clock	Input
10	XTAL2	Oscillator Clock	Output
11	GND	Ground	
12	V_{CC}	Power	
13-15	P31-P33	Port 3, Bits 1-3	Input
16	P34	Port 3, Bit 4	Output
17	P36	Port 3, Bit 6	Output
18	P35	Port 3, Bit 5	Output
19-25	P00-P06	Port 0, Bits 0-6	Input/Output
26	A_{GND}	Analog Ground	
27	AV_{CC}	Analog Power	
28	P20 or AC0	Port 2, Bit 0 Analog In 0	Input/Output

Note: * DIP and SOIC Pin Description and Configuration are identical.

PIN DESCRIPTION (Continued)

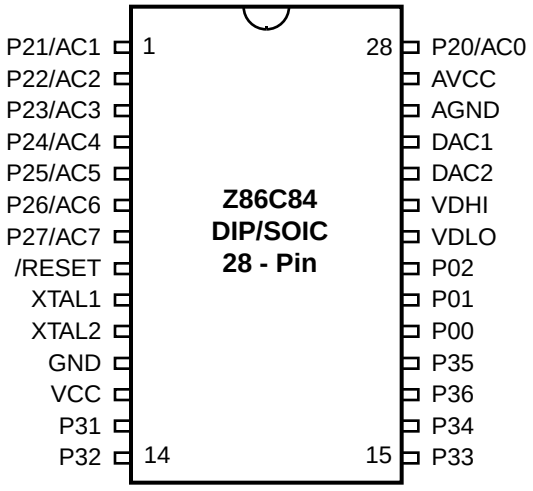


Figure 3. Z86C84 28-Pin DIP and SOIC Pin Configuration

Table 2. Z86C84 28-Pin DIP, SOIC, PLCC Pin Identification*

No	Symbol	Function	Direction
1-7	P21-P27 or AC1-AC7	Port 2, Bit 1-7 Analog In 1-7	Input/Output
8	/RESET	Reset	Input
9	XTAL1	Oscillator Clock	Input
10	XTAL2	Oscillator Clock	Output
11	GND	Ground	
12	V_{CC}	Power	
13-15	P31-P33	Port 3, Bits 1-3	Input
16	P34	Port 3, Bit 4	Output
17	P36	Port 3, Bit 6	Output
18	P35	Port 3, Bit 5	Output
19-21	P00-P02	Port 0, Bits 0-3	Input/Output
22	VDLO	D/A Ref. Volt.,Low	Input
23	VDHI	D/A Ref. Volt.,High	Input
24-25	DAC2-1	D/A Converter	Output
26	A_{GND}	Analog Ground	
27	AV_{CC}	Analog Power	
28	P20 or AC0	Port 2, Bit 0 Analog In 0	Input/Output

Note: * DIP, PLCC and SOIC Pin Description and Configuration are identical

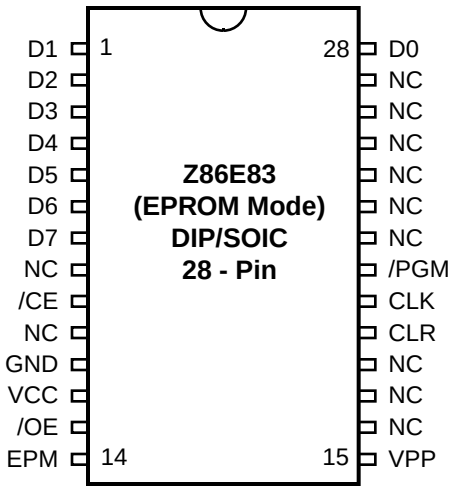


Figure 4. Z86E83 EPROM Programing Mode 28-Pin DIP and SOIC Pin Configuration

Table 3. Z86E83 EPROM Programming Mode 28-Pin DIP, PLCC and SOIC Pin Identification

No	Symbol	Function	Direction
1-7	D1-D7	Data 1,2,3,4,5,6,7	Input/Output
8	NC	No Connection	
9	/CE	Chip Enable	Input
10	NC	No Connection	
11	GND	Ground	
12	V_{CC}	Power	
13	/OE	Output Enable	Input
14	EPM	EPROM Program Mode	Input
15	V_{PP}	Program Voltage	Input
16-18	NC	No Connection	
19	CLR	Clear CLock	Input
20	CLK	Address	Input
21	/PGM	Program Mode	Input
22-27	NC	No Connection	
28	D0	Data 0	Input/Output

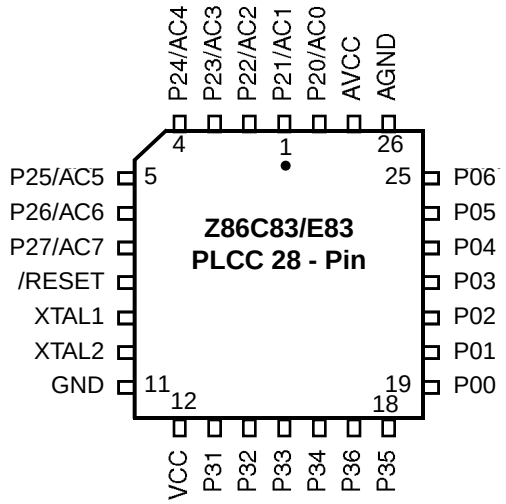


Figure 5. Z86C83 and Standard Mode Z86E83 28-Pin PLCC Pin Configuration

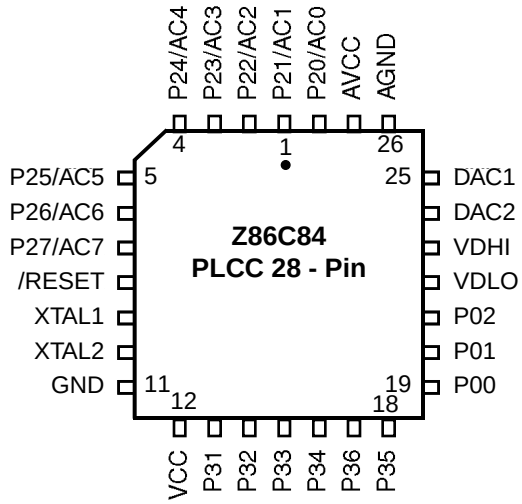


Figure 6. Z86C84 28-Pin PLCC Pin Configuration

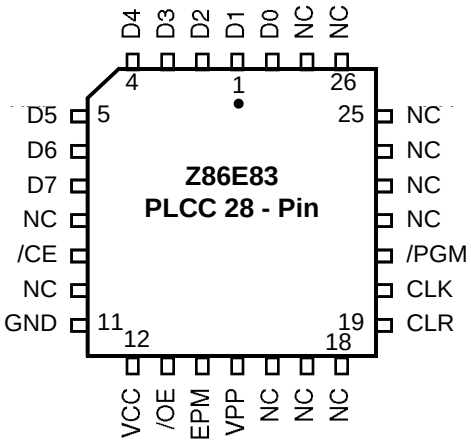


Figure 7. Z86E83 EPROM Programming Mode 28-Pin PLCC Pin Configuration

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{CC} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{CC}+1	V	2
Voltage on P32, P33 and /Reset Pin with Respect to V_{SS}	-0.6	V_{CC}+1	V	2,5
Total Power Dissipation		770	mW	
Maximum Current out of V_{SS}		140	mA	
Maximum Current into V_{CC}		125	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		25	mA	
Maximum Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{CC}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.
5. For Z86E83 only

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package.
Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 8).

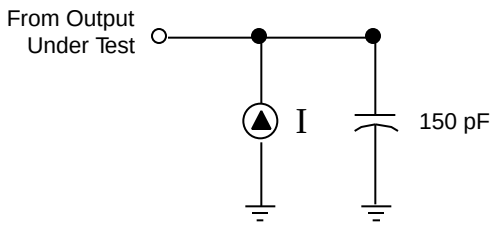


Figure 8. Test Load Diagram

V_{DD} SPECIFICATION

V_{DD} = 3.5V to 5.5V (Z86E83 only at 0° C to 70° C)

V_{DD} = 3.0V to 5.5V (Z86C83/C84)

V_{DD} = 4.5V to 5.5V (Z86E83 only at -40° C to 105° C)

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	15 pF
I/O capacitance	0	15 pF

DC ELECTRICAL CHARACTERISTICS

For Z86C83/C84 Only

Sym	Parameter	V_{CC} Note 3	T_A = 0° C to +70°C Min	T_A = 0° C to +70°C Max	T_A = –40°C to +105°C Min	T_A = –40°C to +105°C Max	Typical [13] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC} -0.4		V_{CC} -0.4		3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC} -0.4		V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	8
		5.5V		1.2		1.2	0.3	V	I_{OL} = +10 mA	8
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.5	V		
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V		-130		-130	-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	1,4
		5.5V		25		25	20	mA	@ 16 MHz	1,4
		5.0V		7		7	3	mA	@ 3.58 MHz	1,4,15
		5.5V		10		10	5	mA	@ 8 MHz	1,4,15

Sym	Parameter	V_{cc} Note 3	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [13] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		15	1	µA	V_{IN} = 0V,V_{CC} Vcc WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11,14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11,14
V_{ICR}	Input Common Mode	3.0	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
	Voltage Range	5.5	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.0V		8		10	5	µA	0V < V_{IN} < V_{CC}	9
		5.5V		15		20	11	µA	0V < V_{IN} < V_{CC}	9
I_{ALH}	Auto Latch High Current	3.0V		-5		-7	-3	µA	0V < V_{IN} < V_{CC}	9
		5.5V		-8		-10	-6	µA	0V < V_{IN} < V_{CC}	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max Int. CLK Freq.	7

Notes:

1. Combined digital V_{CC} and Analog AV_{CC} supply currents.
2. GND = 0V.
3. V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 22 pF.
6. Same as note [4] except inputs at V_{cc}.
7. The V_{LV} increases as the temperature decreases.
8. Standard Mode (not Low EMI).
9. Auto Latch (mask option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Typicals are at V_{CC} = 5.0V and 3.3V.
14. Internal RC selected
15. For Z86C83 only

AC ELECTRICAL CHARACTERISTICS

For Z86C83/C84 Only. Low EMI Mode Only.

				T_A = 0°C to +70°C		T_A = -40° to +105°C			
				4 MHz		4 MHz			
No	**Symbol**	**Parameter**	**V_{CC} [6]**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC, TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.0V	125		125		ns	1,7,8
			5.5V	125		125		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC		ns	1,7,8
			5.5V	3TpC		3TpC		ns	1,7,8
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1,7,8
			5.5V	4TpC		4TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC		ns	1,3,7,8
			5.5V	3TpC		3TpC		ns	1,3,7,8
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC		ns	1,2,7,8
			5.5V	3TpC		3TpC		ns	1,2,7,8
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P33-P31)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode delay is on.
5. Reg. WDTMR
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode
9. For LC oscillator and for oscillator driven by clock driver

For Z86E83 Only

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	Max	T_A = -40° C to +105° C Min	Max	Typical [13] @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Ouput High Voltage	3.5V	V_{CC}-0.4				3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.5V		0.6			0.2	V	I_{OH} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OH} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.5V		1.2			0.3	V	I_{OH} = +6.0 mA	8
		5.5V		1.2		1.2	0.3	V	I_{OH} = +10.0 mA	8
V_{RH}	Reset Input High Voltage	3.5V	0.8V_{CC}	V_{CC}			1.5	V		
		5.5V	0.8V_{CC}	V_{CC}	0.8V_{CC}	V_{CC}	2.1	V		
		3.5V	GND-0.3	0.2V_{CC}			1.1	V		
		5.5V	GND-0.3	0.2V_{CC}	GND-0.3	0.2V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25			10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V		-130			-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.5V		20			7	mA	@16 MHz	1,4
		5.5V		25		25	20	mA	@16 MHz	1,4
I_{CC1}	Standby Current (HALT Mode)	3.5V		4.5			2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		3.5V		3.4			1.5	mA	Clock divide by 16 @ 16 MHz	1,4
		5.5V		7.0		7.0	2.9	mA	Clock divide by 16 @ 16 MHz	1,4

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	T_A = 0° C to +70° C Max	T_A = -40° C to +105° C Min	T_A = -40° C to +105° C Max	Typical [13] @25°C	Units	Conditions	Notes
I_{CC2}	Standby Current (STOP Mode)	3.5V		8			1	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.5V		500			310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
V_{ICR}	Input Common Mode	3.5V	0	V_{CC}-1.0V	0			V		10
		5.5V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.5V		8			5	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		15		20	11	µA	$0V<V_{IN}<V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.5V		-5			-3	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		-8		-10	-6	µA	$0V<V_{IN}<V_{CC}$	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max. Int. CLK Frequency	7

Notes:

1. Combined digital V_{CC} and analog AV_{CC} supply currents
2. GND = 0V
3. V_{CC} voltage specification of 3.5V guarantees 3.5V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V
4. All outputs unloaded, I/O pins floating, inputs at rail
5. CL1 = CL2 = 100 pF
6. Same as note [4] except inputs at V_{CC}
7. The V_{LV} increases as the temperature decreases
8. Standard Mode (not Low EMI)
9. Auto Latch (mask option) selected
10. For analog comparator, inputs when analog comparators are enabled
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating
12. Excludes clock pins
13. Typicals are at V_{CC} = 3.5V and 5.0V
14. Internal RC selected

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

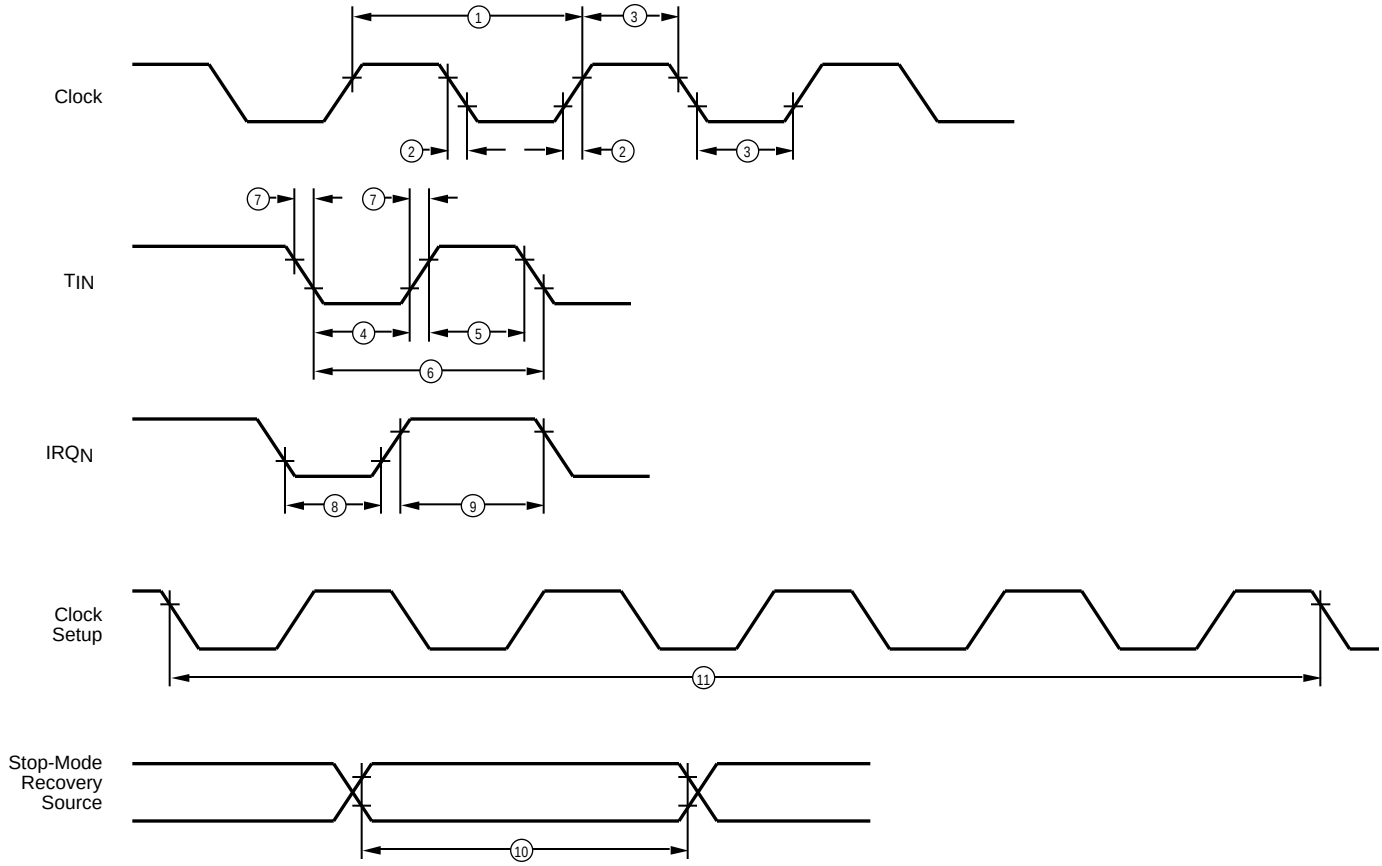


Figure 9. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2) For Z86E83 Only

No	Symbol	Parameter	V_{CC} Note 6	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.5V	83	DC	62.5	DC	ns	1
			5.5V	83	DC	62.5	DC	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		15	ns	1
			5.5V		15		15	ns	1
3	TwC	Input Clock Width	3.5V	41		31		ms	1
			5.5V	41		31		ns	1
4	TwTinL	Timer Input Low Width	3.5V	100		100		ms	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin,	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1
	TfTin		5.5V		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3
			5.5V	5TpC		5TpC			1,3
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.5V	12		12		ns	
			5.5V	12		12		ns	
11	Tost	Oscillator Start-up Time	3.5V		5TpC		5TpC		4
			5.5V		5TpC		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time					**WDTMR**	**Reg**	**D1,D0**
			5.5V	6.25		6.25		ms	0,0,[7]
			5.5V	12.5		12.5		ms	0,1,[7]
			5.5V	25		25		ms	1,0,[7]
			5.5V	100		100		ms	1,1,[7]
13	T_{POR}	Power On Reset Delay	3.5V	7	24	7	25	ms	7
			5.5V	3	13	3	14	ms	7

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.5V guarantees 3.5V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
7. Using internal on-board RC oscillator.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Low EMI Mode Only) For Z86E83 Only

No	Symbol	Parameter	V_{CC} [Note 6]	T_A = 0°C to +70°C 4 MHz Min	4 MHz Max	T_A = -40°C to +105°C 4 MHz Min	4 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC			ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25			ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	125				ns	1,7,8
			5.5V	125		125		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.5V	100				ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.5V	3TpC					1,7,8
			5.5V	3TpC		3TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	4TpC					1,7,8
			5.5V	4TpC		4TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100			ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.5V	100				ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	3TpC					1,3,7,8
			5.5V	3TpC		3TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	3TpC					1,2,7,8
			5.5V	3TpC		2TpC			1,2,7,8
10	Twsm	Stop-Mode Recovery Width Spec	3.5V	12				ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Start-up Time	3.5V		5TpC				4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode delay is on.
5. Reg. WDTMR
6. The V_{CC} voltage specification of 3.5V guarantees 3.5V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For LC oscillator and for oscillator driven by clock driver

CAPACITANCE (Continued)

Additional Timing Table (SKLK/TCLK = XTAL/2) For Z86C83/C84 Only

				T_A = 0°C to +70°C				T_A = -40°C to +150°C					
			VCC	12 MHz		16MHz		12 MHz		16 MHz			
No	Sym	Parameter	[6]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1
2	TrC, TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	1
			5.5V		15		15		15		15	ns	1
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	1
			5.5V	41		31		41		31		ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,3
			5.5V	5TpC		5TpC		5TpC		5TpC			1,3
9	TwIH	Int. Request High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,2
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		5TpC		5TpC		
			5.5V		5TpC		5TpC		5TpC		5TpC		
12	Twdt	Watch-Dog Timer Delay Time										WDTMR Reg	D1,D0
			5.5V	6.25		6.25		6.25		6.25		ms	0,0 [6]
			5.5V	12.5		12.5		12.5		12.5		ms	0,1 [6]
			5.5V	25		25		25		25		ms	1,0 [6]
			5.5V	100		100		100		100		ms	1,1 [6]
13	T_{POR}	Power On Reset Delay	3.0V	7	24	7	25	7	24	7	25	ms	6
			5.5V	3	13	3	14	3	13	3	14	ms	6

Notes:

1. Timing References used 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 0
5. The V_{CC} voltage specification of 3.0V guarantees 3.3V± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
6. Using internal on-board RC oscillator

For Z86C84 Only

Table 4. D/A Converter Electrical Characteristics
V_{CC} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		0.25	0.5	LSB
Supply Range	3.0	3.3	3.6	Volts
Power dissipation, no load		10		mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 3 volts	1.5	1.8	2.1	Volts
VDLO range at 3 volts	0.2	0.5	0.8	Volts
VDHI–VDLO, at 3 volts	1.3	1.6	1.9	Volts
Capacitive output load, CL			20	pF
Resistive output load, RL	50K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 3.0V – 3.6V
Temp: 0–70°C

For Z86C84 Only

Table 5. D/A Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0†	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		1	2	% FSR
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 5 volts	2.6		3.5	Volts
VDLO range at 5V volts	0.8		1.7	Volts
VDHI–VDLO, at 5V volts	0.9		2.7	Volts
Capacitive output load, CL			30	pF
Resistive output load, RL	20K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 4.5V - 5.5V
Temp: 0-70°C
† The C86C84 Emulator has maximum setting time of 20 µsec. (10 µsec. typical).

CAPACITANCE (Continued)

For Z86C83/C84

Table 6. A/D Converter Electrical Characteristics
V_{cc} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	2.7	3.0	3.3	Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.0V – 3.6V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86C83/C84

Table 7. A/D Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86E83

Table 8. A/D Converter Electrical Characteristics
V_{CC} = 3.5V

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	3.5			Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86E83

Table 9. A/D Converter Electrical Characteristics
V_{CC} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time	4.3		35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

PIN FUNCTIONS

EPROM Programming Mode (E83 Only)

D7-D0. *Data Bus.* The data can be read from or written to the EPROM through the data bus.

Clock. *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock signal.

Clear. *Clear.* (active High). This pin resets the internal address counter at the High Level.

$V_{CC.}$ *Power Supply.* This pin must supply 5V during the EPROM Read Mode and 6V during other modes.

/CE. *Chip Enable* (active Low). This pin is active during EPROM Read, Program, and Program Verify Modes.

/OE. *Output Enable* (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM. *EPROM Program Mode.* This pin controls the different EPROM Program Mode by applying different voltages.

$V_{PP.}$ *Program Voltage.* This pin supplies the program voltage.

/PGM. *Program Mode* (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise surges above V_{cc}*** occur on the /RESET pin.

Processor operation of Z8 OTP devices may be affected by excessive noise surges on the VPP, /EPM, /OE pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to /RESET, VPP, /EPM, /OE
- Adding a capacitor to the affected pin

Z86C83, Z86C84, and Standard Mode Z86E83

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC network to the on-chip oscillator output.

Port 0 P00-P06 (P03-P06 is not available on the Z86C84). Port 0 is a 7-bit, bidirectional, CMOS-compatible I/O port. These seven I/O lines can be nibble programmable as P00-P03 input/output and P04-P06 input/output, separately (Figure 10). All input buffers are Schmitt-triggered and output drivers are push-pull.

Port 0 Auto Latch. (P03-P06 has the Auto Latches permanently enabled). The Auto Latch provides valid CMOS Levels when P03-P06 are selected as inputs and not externally driven. It is impossible to determine if a non-driven input is 1 or 0, however; the Auto Latch will sense the input condition and drive a valid CMOS level, thereby eliminating a floating mode that could cause excessive current.

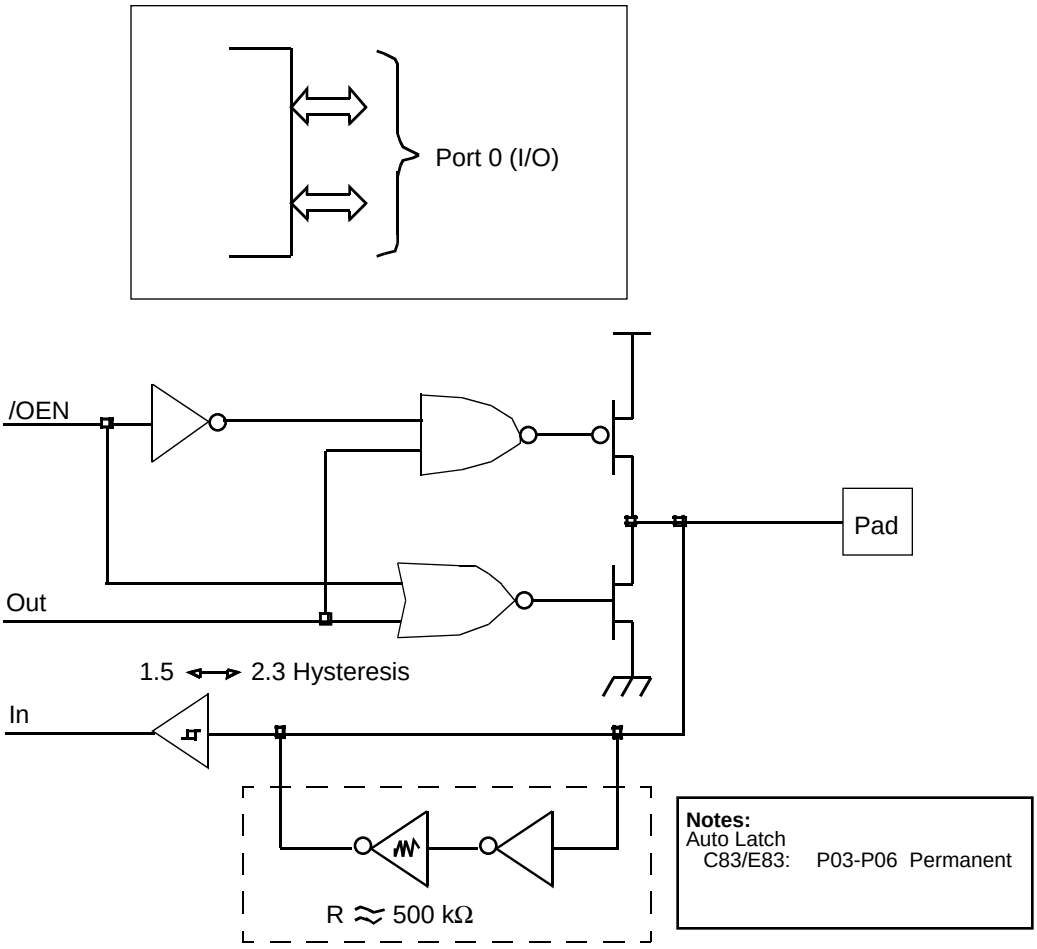


Figure 10. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20) Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port and an 8-channel muxed input to the 8-bit ADC. When configured as a digital input, by programming the Port2 Mode register, the Port 2 register can be evaluated to read digital data applied to Port 2, or the ADC result register can be read to evaluate the analog signals applied to Port 2 after configuring the ADC Control Registers. The direction of each of the eight Port 2 I/O lines can be configured individually (Figure 11).

In addition, all four versions of the device provide the capability of connecting 10K (±20%) pull-up resistors to each of the Port 2 I/O lines individually. The pull-ups are connected when activated through software control of P2RES register (Figure 67) when the corresponding Port 2 pin is configured to be an input. The pull-up resistor of a Port 2 I/O line is automatically disabled when the corresponding I/O is an output, regardless of the state of the corresponding P2RES bit value.

Note: The Z86C83/C84 Emulator does not emulate the P2RES Register. Selection of the pull-ups are done via jumper settings on the emulator.

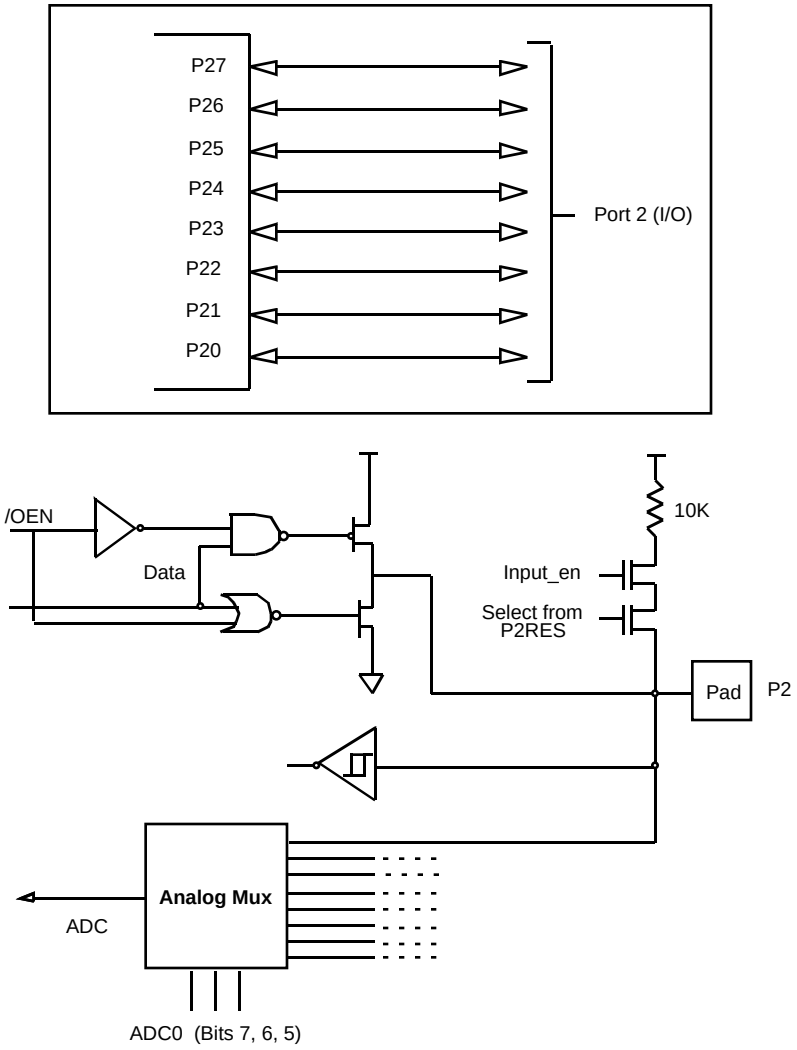


Figure 11. Port 2 Configuration

Port 3 (P36-P31) Port 3 is a 6-bit, CMOS-compatible port, with three fixed inputs (P33-P31) and three fixed outputs (P34-P36), configured under software control for Input/Output, Counter/Timers, interrupt, and port handshake. P31, P32, and P33 are standard CMOS inputs (no Auto Latches). Pins P34, P35, and P36 are push-pull output lines (Figure 11). Low EMI output buffers can be globally programmed by the software.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For Interrupt functions, Port 3, pin 3 is falling-edge interrupt input. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and bit 7). P33 is the comparator reference voltage input when in Analog Mode. Access to Counter/Timers 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are available on P31/P36 and P32/P35 (Table 10).

Port 3 also provides the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); three external interrupt request signals (IRQ2-IRQ0); timer input and output signals (T_{IN} and T_{OUT}).

Table 10. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P2 HS
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT		AN1-OUT			
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Auto Latch. The Auto-Latch instruction puts valid CMOS levels on CMOS inputs that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Note: Pins 03, 04, 05, 06 have permanently enabled Auto Latches.

Comparator Inputs. Port 3, P31 and P32, each have a comparator front end. The comparator reference voltage, P33, is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. In Analog Mode, the internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR register. In this mode, any of the Stop-Mode Recovery sources are used to toggle the P33 bit or generate IRQ1. In Digital Mode, P33 can be used as a Port 3 register input or IRQ1 source. P34 outputs the comparator outputs by software programming the PCON Register bit D0 to 1.

Note: When enabling/or disabling the analog mode, the following is recommended:

1. allow two NOP delays before reading the comparator output

2. disable interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.

PIN FUNCTIONS (Continued)

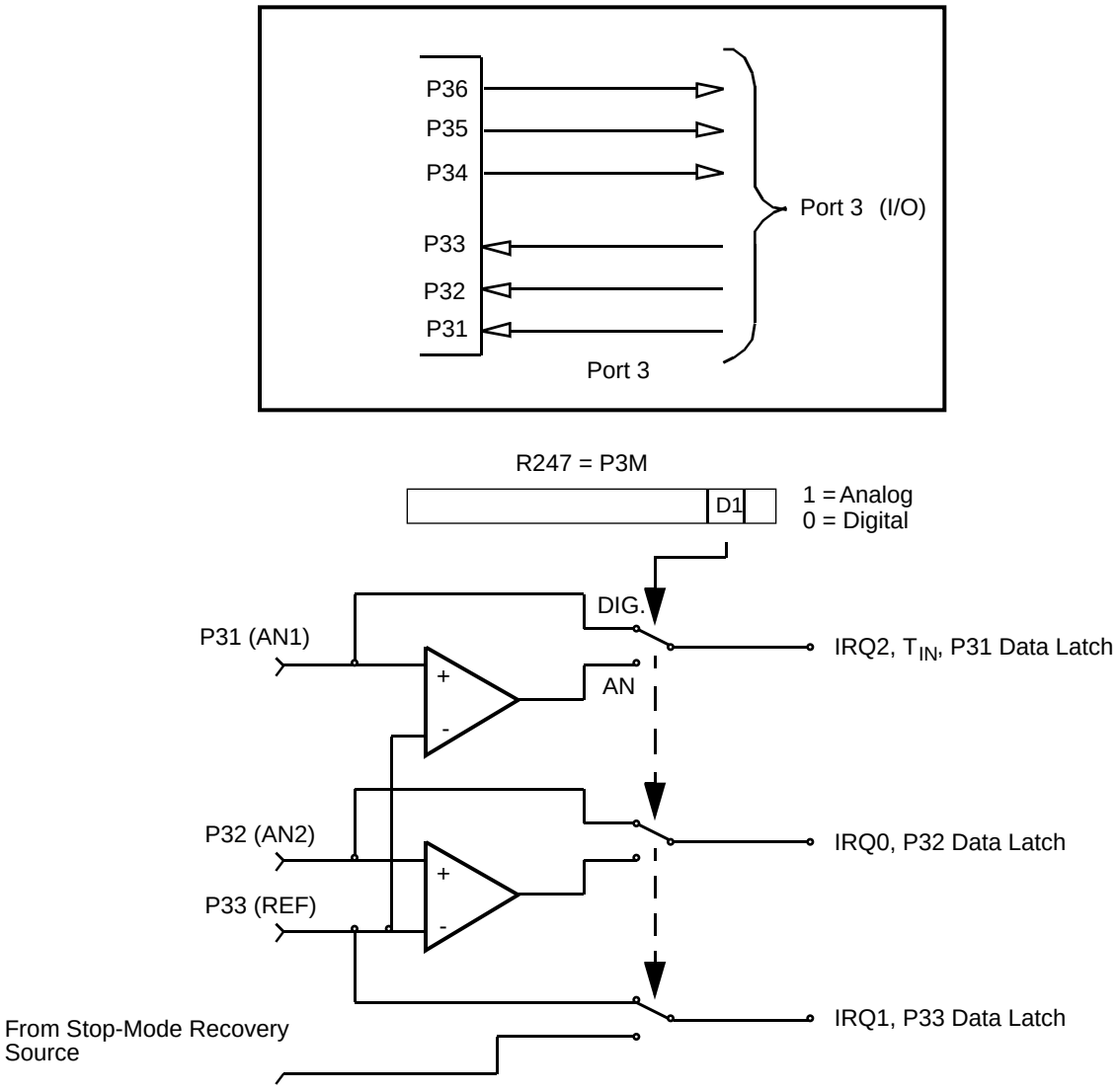


Figure 12. Port 3 Input Configuration

Port Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3. The PCON Register is located in the Expanded Register File at Bank F, location 00 (Figure 13).

Bit 0 multiplexes comparator AN1 Output at P34. A "1" in this location brings the comparator output to P34 (Figure 14), and a "0" puts P34 into its standard I/O configuration.

Note: Only comparator output AN1 is multiplexed to a Port 3 output. Comparator AN2 output is not connected to any pins. Note that the PCON Register is reset upon the occurrence of a WDT RESET (not in STOP Mode), and Power-On Reset (POR).

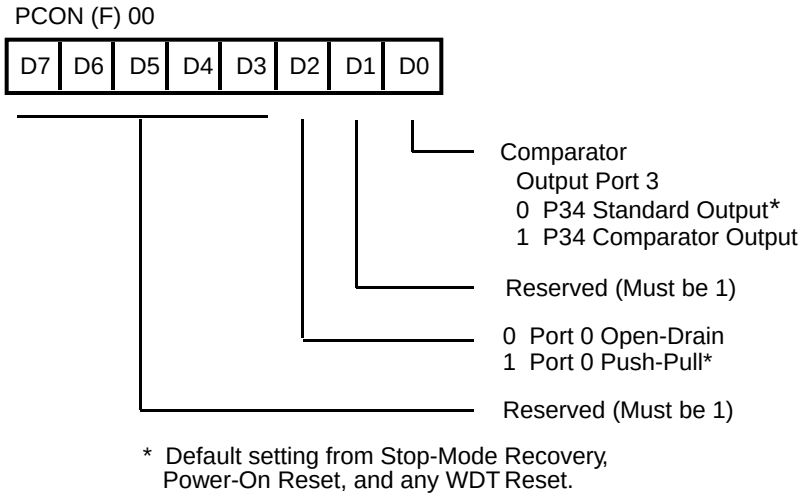


Figure 13. Port Configuration Register (PCON) (Write-Only)

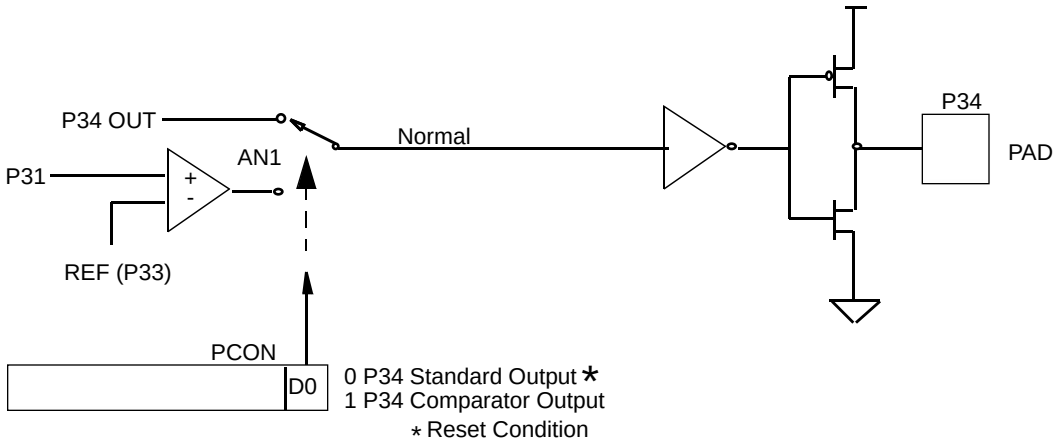


Figure 14. Port 3 P34 Output Configuration

FUNCTIONAL DESCRIPTION

RESET. (Input, Active Low). This pin initializes the MCU. Reset is accomplished either through Power-On Reset (POR), Watch-Dog Timer (WDT) Reset, or external reset. During POR, and WDT Reset, the internally generated reset is driving the reset pin Low for the POR time. **Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions.** Pull-up is provided internally.

After the POR time, /RESET is a Schmitt-triggered input. After the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. Program execution begins at location 000C (hex), 5-10 TpC cycles after the RST is released. For POR, the reset output time is T_{POR}.

Program Memory. C83/C84/E83/E84 can address up to 4 KB of internal Program Memory (Figure 15). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 13 to 4095 consist of on-chip, mask-programmed ROM.

ROM Protect. The 4 KB of Program Memory is mask programmable. A ROM protect feature will prevent dumping of the ROM contents from an external program outside the ROM.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 16). These register banks are known as the Expanded Register File (ERF). Bits 3-0 of the Register Pointer (RP) select the active ERF bank. Bits 7-4 of register RP select the working register group (Figure 16). Four system configuration registers reside in the ERF address space in Bank F and eight registers reside in Bank C. The rest of the ERF addressing space is not physically implemented, and is open for future expansion.

Note: When using Zilog's Cross Assembler version 2.1 or earlier, use the LD RP, #0X instruction rather than the SRP #0X instruction to access the ERF.

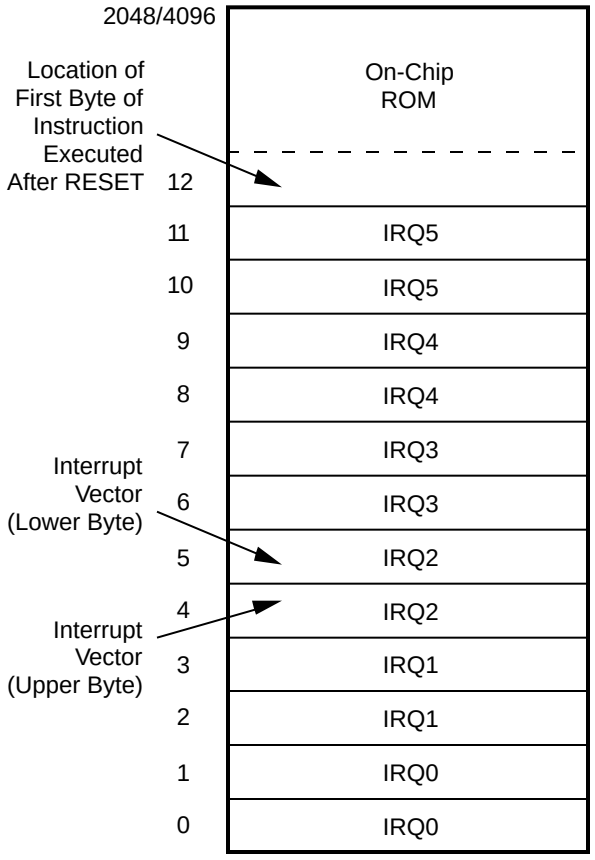


Figure 15. Program Memory Map

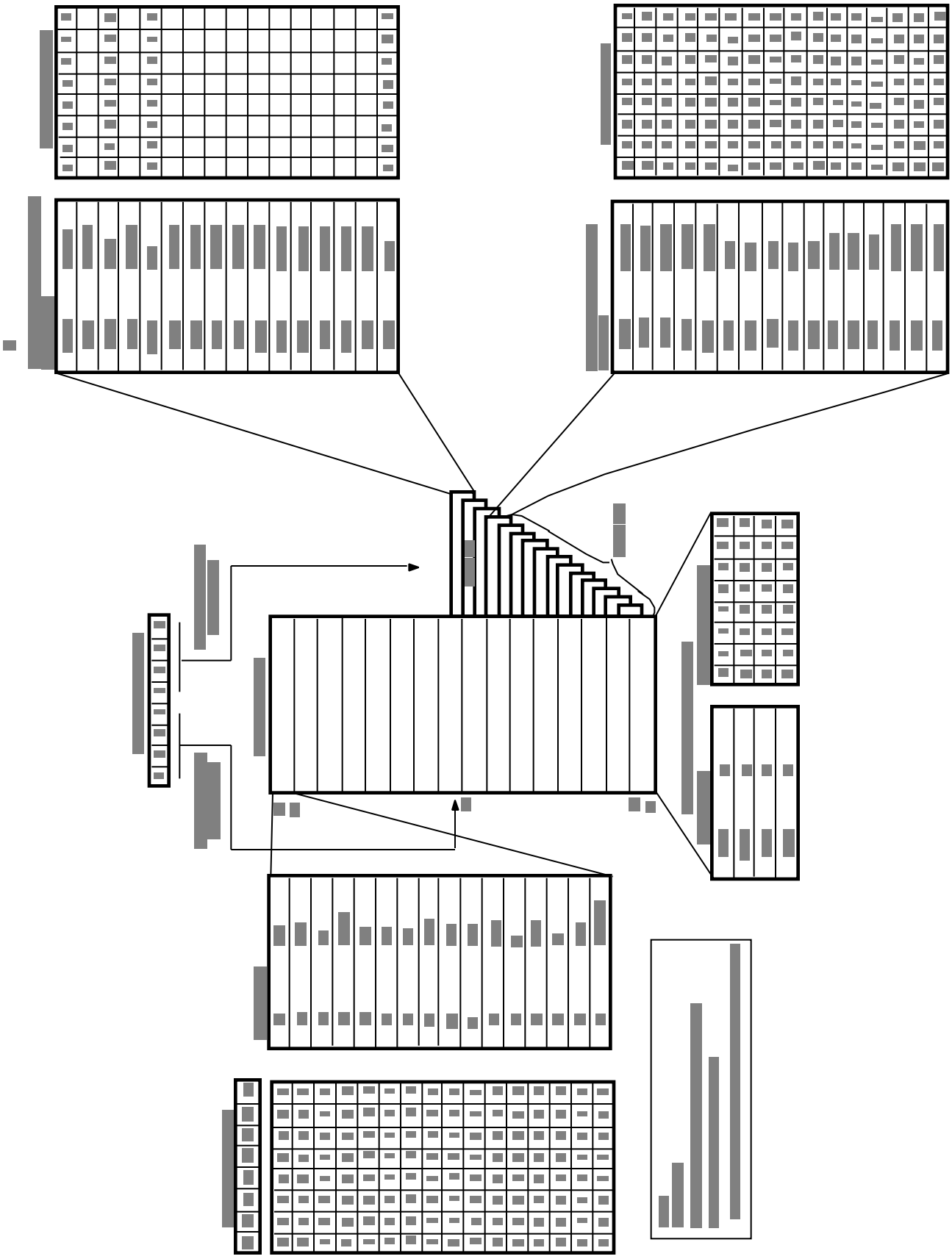


Figure 16. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

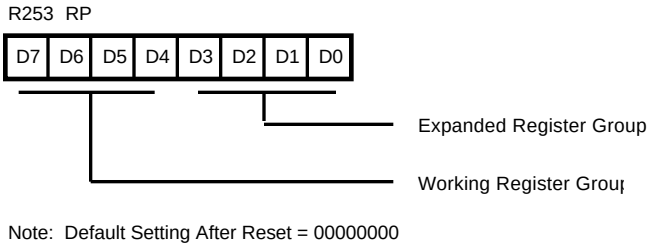


Figure 17. Register Pointer Register

Register File. The Register File consists of three I/O port registers, 237 general-purpose registers, 15 control and status registers, and four system configuration registers in the Expanded Register Group (Figure 16). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 18). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 17) addresses the starting location of the active working-register group.

Note: Register Bank E0-EF is only accessed either as working registers or through indirect addressing modes.

CAUTION: D4 of Control Register P01M (R251) must be 0.

R254. The C83/C84/E83 has one extra general-purpose register located at FEH (R254).

Stack. The C83/C84/E83 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 236 general-purpose registers. Register R254 cannot be used for stack.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V. This includes Register R254.

Note: Register Bank E0-EF is only accessed either as working register or through indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from writing. The user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the Interrupt Mask (IMR) register, bit D6. A 1 in D6 enables RAM Protect.

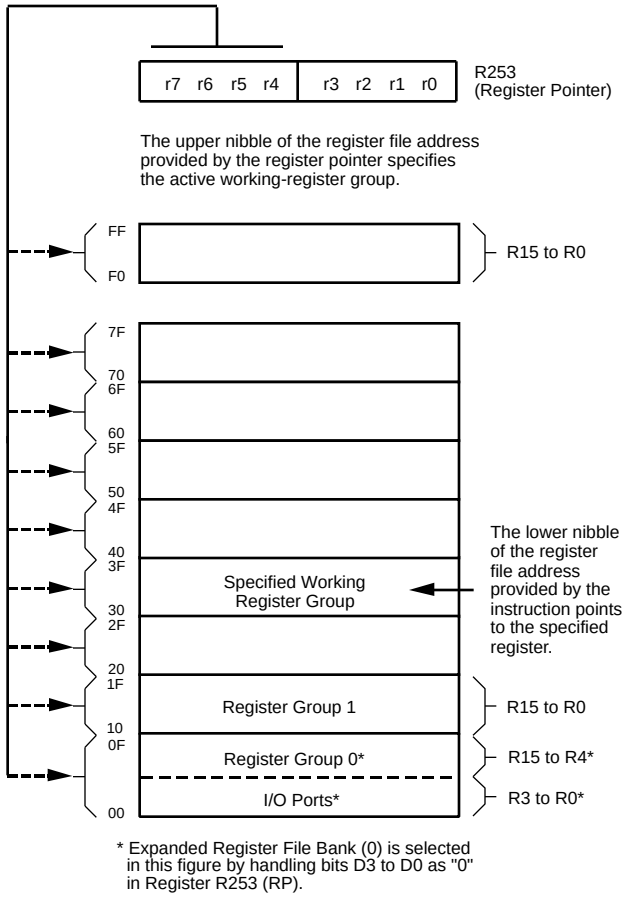


Figure 18. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 19).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, **but not the prescalers**, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 Bit D1 to 0.

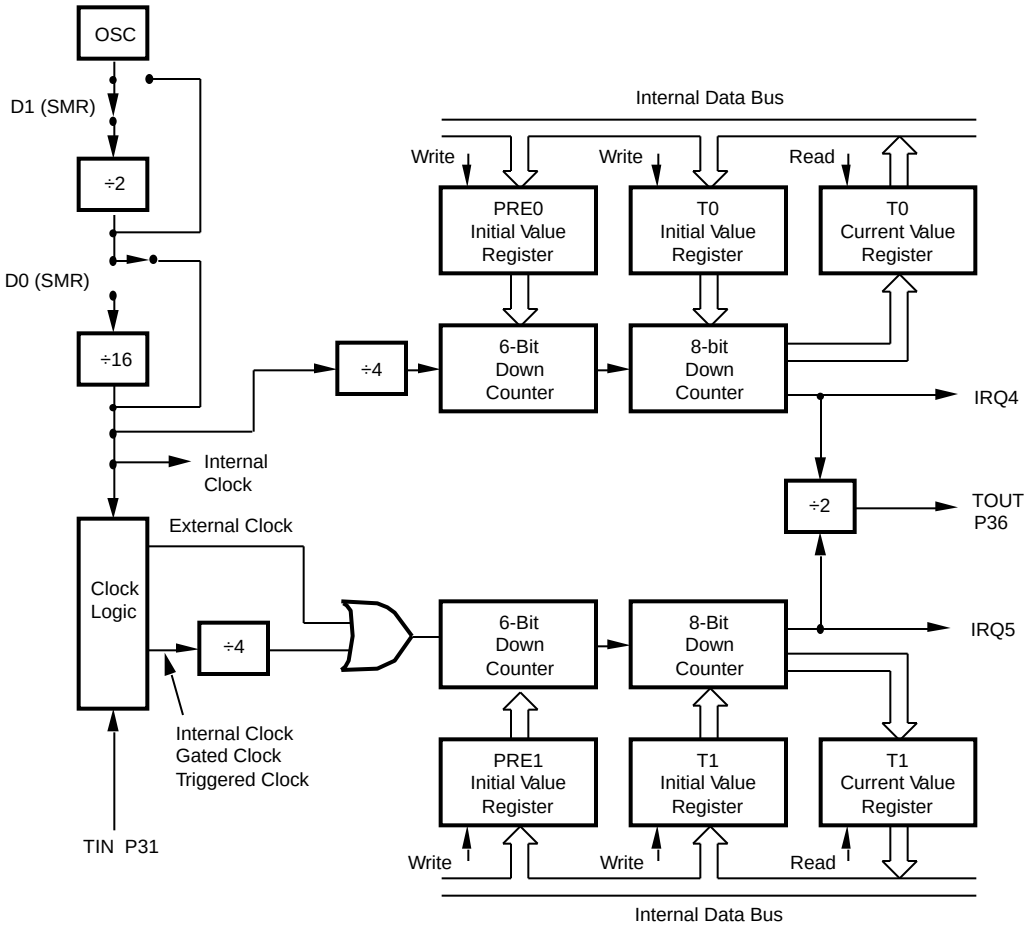


Figure 19. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 20) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 11). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

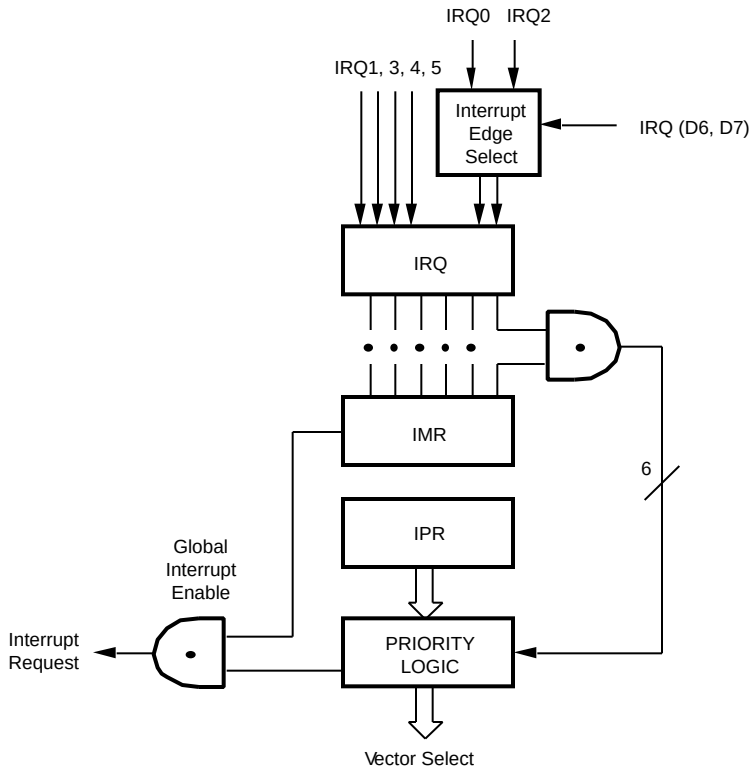


Figure 20. Interrupt Block Diagram

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	By User Software
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 12.

Table 12. IRQ Register

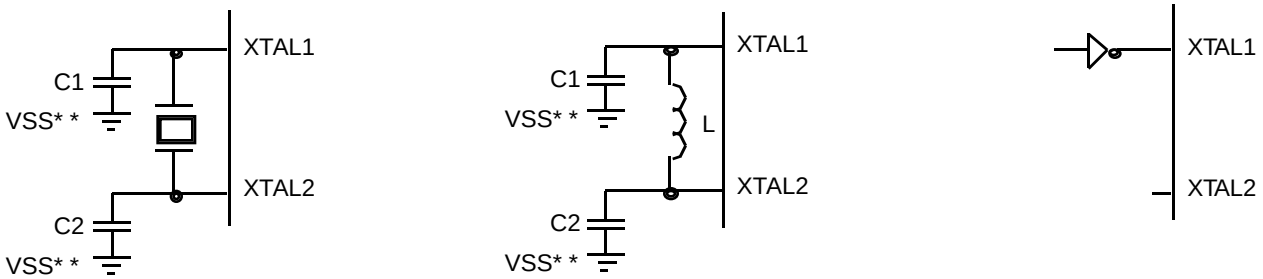
IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 16 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms when clocking from 1 MHz to 16 MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce Ground noise injection into the oscillator (Figure 21).

Note: For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).



Ceramic Resonator or Crystal
C1, C2 = 22 pF TYP *
f = 8 MHz

LC

External Clock

* Preliminary value including pin parasitics
* * Device ground pin

Figure 21. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Analog-to-Digital Converter

The Analog-to-Digital (ADC) is an 8-bit half flash converter that uses two reference resistor ladders for its upper 4 bits (MSBs) and lower 4 bits (LSBs) conversion. Two reference voltage pins, AV_{CC} and A_{GND}, are provided for external reference voltage supplies. During the sampling period from one of the eight channel inputs, the converter is also being auto-zeroed before starting the conversion. The conversion time is dependent on the internal clock frequency. The minimum conversion time is 35 x SCLK (see Figure 22).

The ADC is controlled by the Z8 and its three registers (two Control and one Result) are mapped into the Extended Register File. A conversion can be initiated by writing to the ADC Control Register 0 after the ADC Control Register 1 is configured.

The start command is implemented in such a way as to begin a conversion at any time, if a conversion is in progress and a new start command is received, then the conversion in progress will be aborted and a new conversion will be initiated. This allows the programmed values to be changed without affecting a conversion-in-progress. The new values will take effect only after a new start command is received.

The ADC can be disabled (for low power) or enabled by a Control Register bit.

Though the ADC will function for a smaller input voltage and voltage reference, the noise and offsets remain constant over the specified electrical range. The errors of the converter will increase and the conversion time may also take slightly longer due to smaller input signals.

ADC Calibration Offset

Specially matched resistors are program-enabled to allow 35 percent or 50 percent offset from A_{GND}. They may selectively enable these resistors to offset the A_{GND} by 50 percent (2.5V to 5V) or 35 percent (1.75V to 5V) thereby allowing the 8-bit ADC across a narrower voltage range. This will allow significant resolution improvement within the reduced voltage range.

Note: The AV_{CC} must be the same value as V_{CC} and A_{GND} must be the same value as GND.

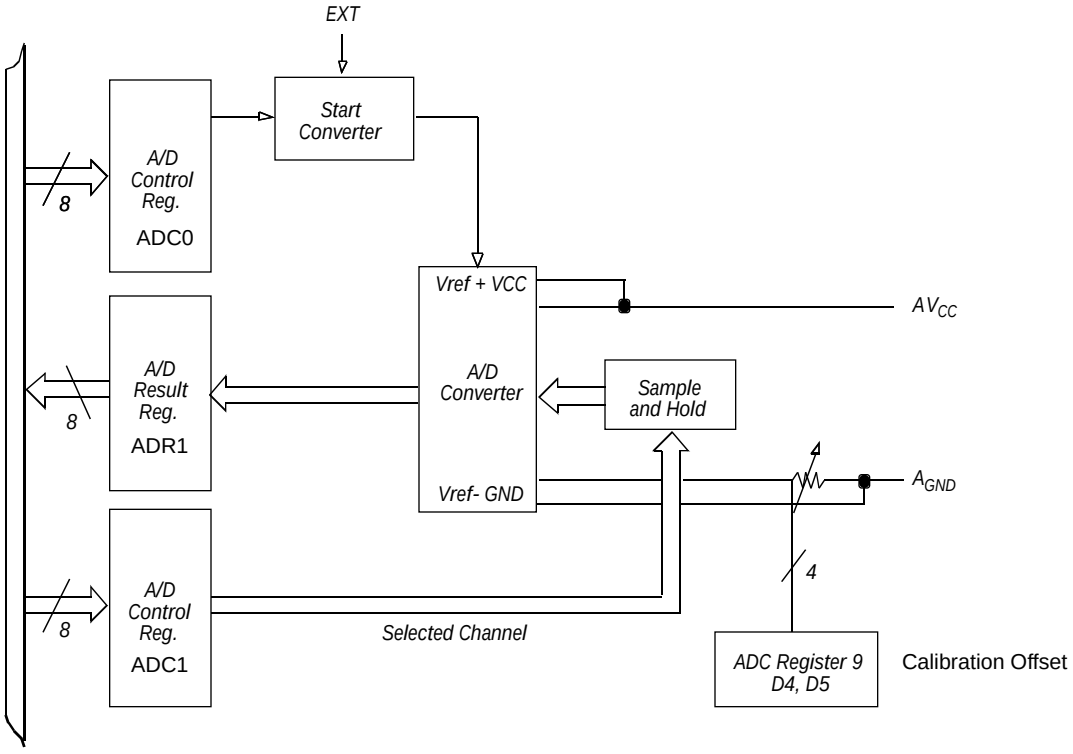


Figure 22. ADC Architecture

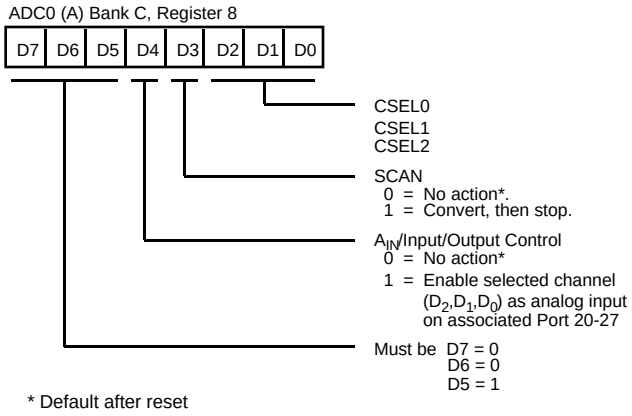


Figure 23. ADC Control Register 0 (Read/Write)

SCAN	
0	No action*
1	Convert channel then stop

Channel Select (bits 2, 1, 0)
* Default after reset

CSEL2	CSEL1	CSEL0	Channel
0	0	0	0 (P20)*
0	0	1	1 (P21)
0	1	0	2 (P22)
0	1	1	3 (P23)
1	0	0	4 (P24)
1	0	1	5 (P25)
1	1	0	6 (P26)
1	1	1	7 (P27)

Note: ADCO D4 must equal 1 to allow Port bit as ADC input.

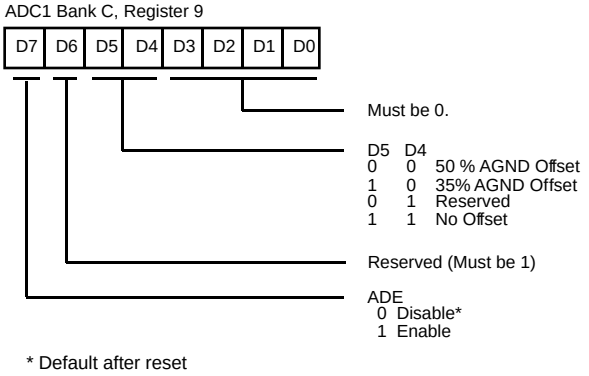


Figure 24. ADC Control Register 1 (Read/Write)

ADE (bit 7). A zero powers down and disables power and any A/D conversions or accessing any ADC registers except writing to ADE bit. A one Enables all ADC accesses. ADC result register is shown in Figure 25.

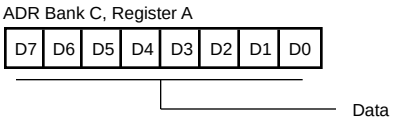


Figure 25. Result Register (Read-Only)

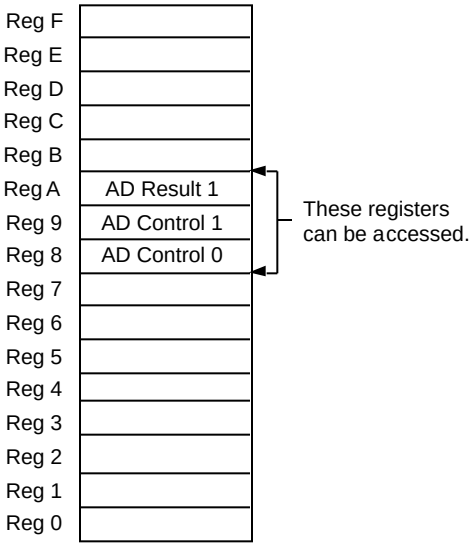


Figure 26. Bank C

FUNCTIONAL DESCRIPTION (Continued)

Figure 27 shows the input circuit of the ADC. When conversion starts the analog input voltage is connected to the MSB and LSB flash converter inputs as shown in the Input Impedance CKT diagram. Effectively, shunting 31 parallel internal resistance of the analog switches and simultaneously charging 31 parallel 0.5 pF capacitors, which is equivalent to seeing a 400 Ohms input impedance in parallel with a 16 pF capacitor. Other input stray capacitance adds about 10 pF to the input load. For input source resistances up to 2 Kohms can be used under normal operating condition without any degradation of the input settling time. For larger input source resistance, increasing conversion cycle time or adding a capacitor to the input may be required to compensate the input settling time problem.

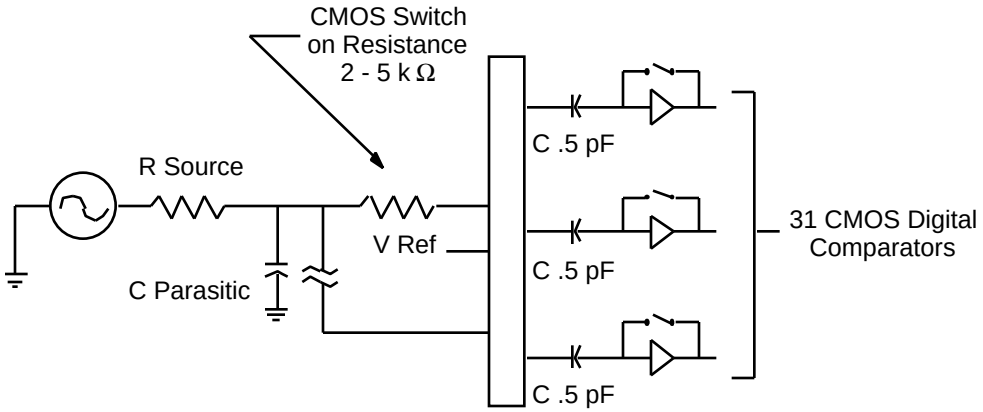


Figure 27. Input Impedance of ADC

Typical Z8 A/D Conversion Sequence

3. Set the register pointer to Extended Bank (C), that is, SRP #%0C instruction.

4. Next, set ADE flag by loading ADC1 Control Register Bank (C) Register 9, bit 7. Also, load bits 0-4 of this same register to select a AV_{CC} or A_{GND} offset value. A precision voltage divider connected to the A/D resistive ladder can offset conversion dynamic range to specified limits within the AV_{CC} and A_{GND} limits. By loading Bank (C) Register 9, bits 0-4, with the appropriate value it is possible to select from these groups:

   a. No Offset. The Converter Dynamic range is from 0V to 5.0V for AV_{CC} = 5.0V.

   b. 35 Percent A_{GND} Offset. The Converter Dynamic range is 1.75V - 5.0V for AV_{CC} = 5.0V.

   c. 50 Percent A_{GND} Offset. The Converter Dynamic range is 2.5V - 5.0V for AV_{CC} = 5.0V.

5. Select one of the eight A/D inputs for conversion by loading Bank (C) Register 8 with the desired attributes: Bits 0 - 2 select an A/D input, bits 3 and 4 select A/D conversion (or digital port I/O).

6. Set Bank (C) Register 8, bit 3 to enable A/D conversion. (This flag can be set concurrently with step 3.) This flag is automatically reset when the A/D conversion is completed, so a bit test can be performed to determine A/D readiness if necessary.

7. Read the A/D result in Bank (C) Register A. Please note that the A/D result is not valid (indeterminate) unless ADE flag (Register 9, bit 7) was previously set, otherwise A/D converter output is tri-stated.

Digital-to-Analog Converters

The Z86C84 has two Digital-to-Analog Converters (DACs). Each DAC is an 8-bit resistor string, with a programmable 0.25X, 0.5X, or 1X gain output buffer. The DAC output voltage settles after the internal data is latched into the DAC Data register. The top and bottom ends of the resistor ladder are register-selected to be connected to either the analog supply rails, AV_{CC} and A_{GND}, or two externally-provided reference voltages, VDHI and VDLO. External references are recommended to explicitly set the DAC output limits. Since the gain stage cannot drive to the supply rails, VDHI and VDLO must be within ranges shown in the specifications. If either reference approaches the analog supply rails, the output will be unable to span the reference voltage range. The externally provided reference voltages should not exceed the supply voltages. The DAC outputs are latch-up protected and can drive output loads (Figure 28).

Note: The AV_{CC} must be the same value as V_{CC} and A_{GND} must be the same value as GND

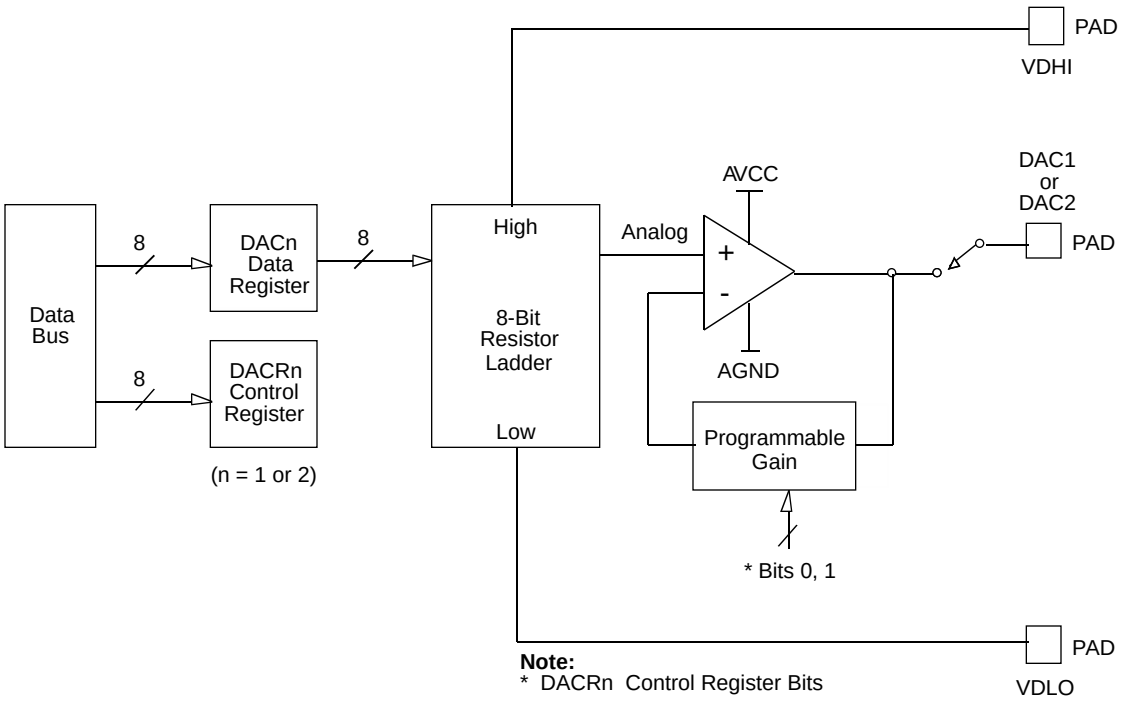


Figure 28. DAC Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

The D/A conversion for DAC1 is driven by writing 8-bit data to the DAC1 data register (Bank C, Register 06H). The D/A conversion for DAC2 is controlled by the DAC2 data register (Bank C, Register 07H). Each DAC data register is initialized to midrange 80H on power-up.

There are two DAC control registers: DACR1 (Bank C, Register 04H) for DAC1, and DACR2 (Bank C, Register 05H) for DAC2. Control register bits 0 and 1 set the DAC gain. When DAC data is 80H, the DAC output is constant for any gain setting (Figure 29 and Figure 31).

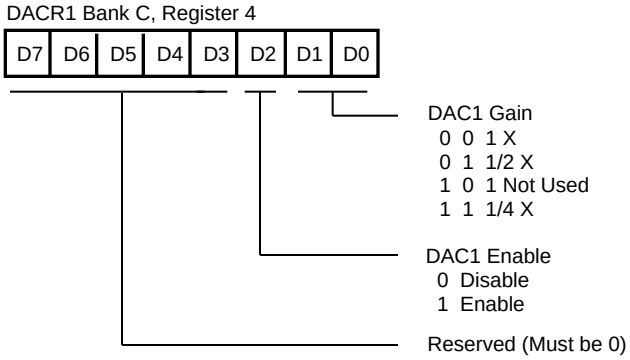


Figure 29. D/A 1 Control Register

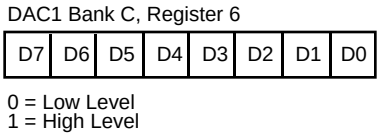


Figure 30. D/A 1 Data Register

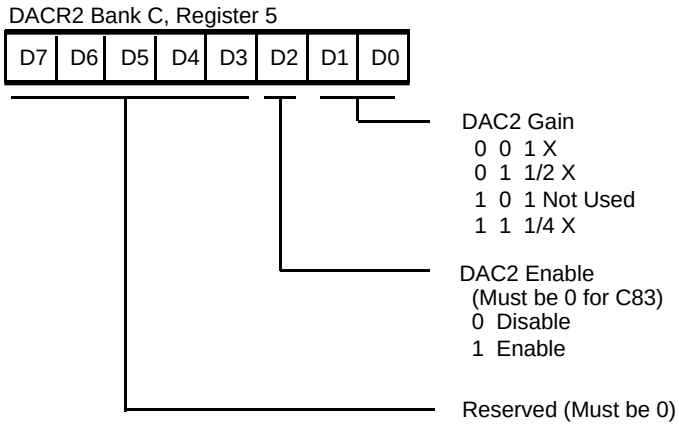


Figure 31. D/A 2 Control Register

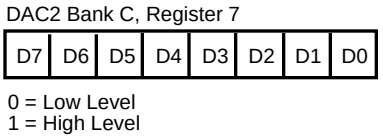


Figure 32. D/A 2 Data Register

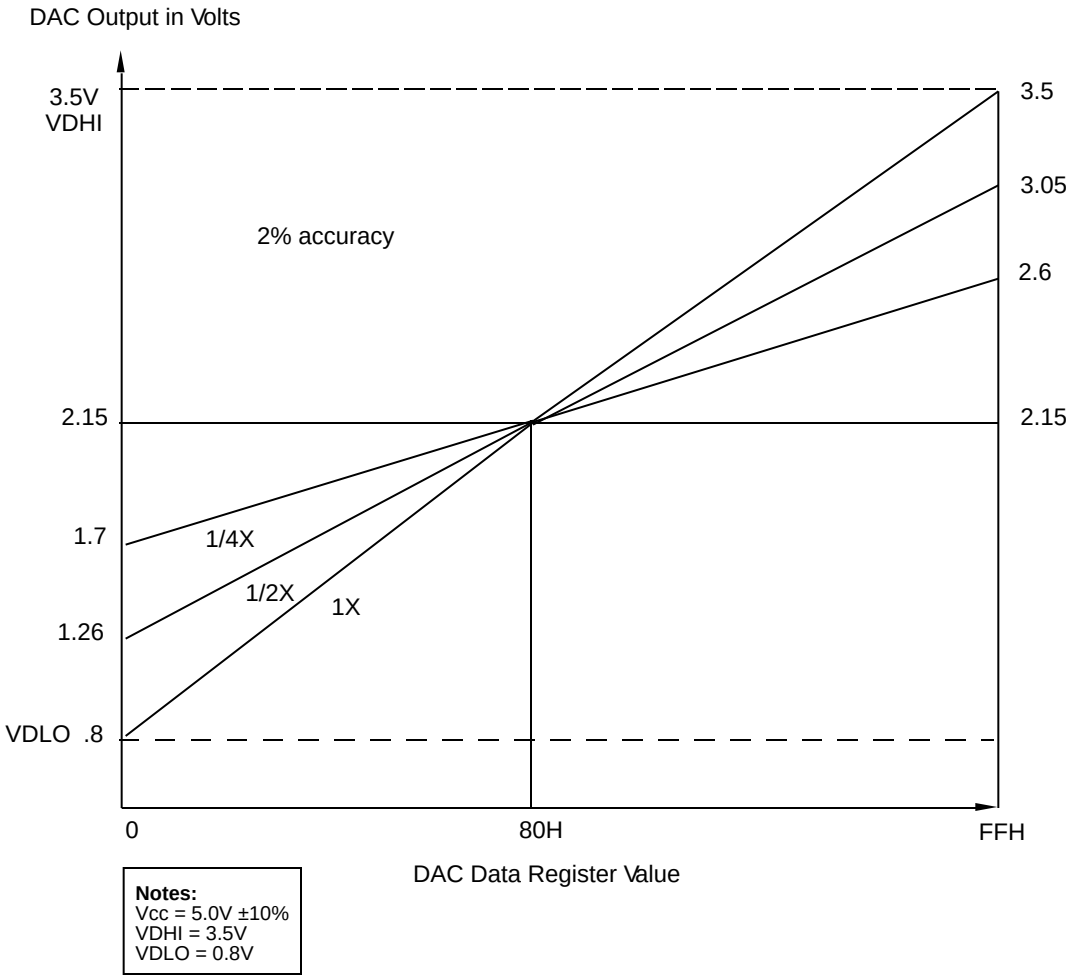


Figure 33. Gain Control on DAC

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator or by the XTAL oscillator is used for the POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK Status
- Stop-Mode Recovery (If D5 of SMR Register = 1)
- WDT Time-Out (Including from STOP Mode)

The POR time is T_{POR} minimum. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock and LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated (a POR or a WDT time-out). An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In case of a POR or a WDT time-out, program execution will restart at address 000CH.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. The STOP Mode is terminated by a reset of either WDT time-out, POR, or Stop-Mode Recovery. This causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, that is**,**

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                        or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Stop-Mode Recovery (SMR) Register. This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 34 and Figure 35). All bits are Write-Only, except bit 7, which is Read-Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR Register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR Register is located in Bank F of the Expanded Register Group at address 0BH. When the Stop-Mode Recovery sources are selected in this register, then SMR2 Register bits D0,D1 must be set to 0.

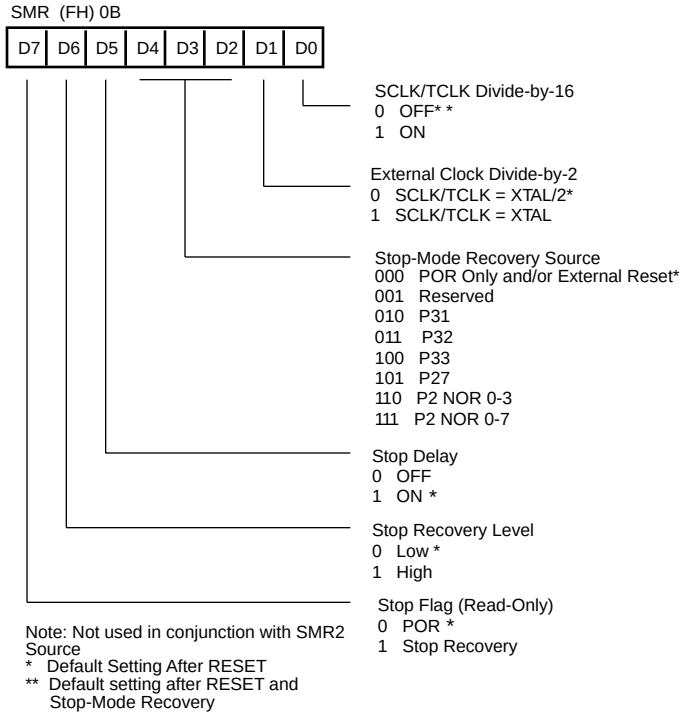


Figure 34. Stop-Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

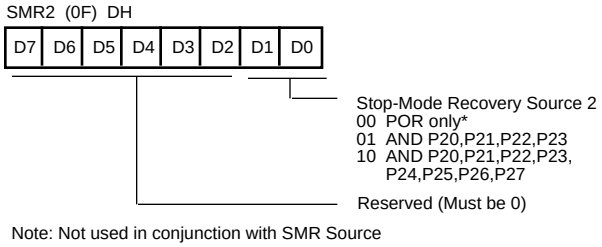


Figure 35. Stop-Mode Recovery Register 2 ([0F] DH: Write-Only)

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The control selectively reduces device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery, WDT Time-out, and POR.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock HALT Mode frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero. Maximum external clock frequency is 8 MHz when SMR Bit D1 = 1 where SCLK/TCLK = XTAL.

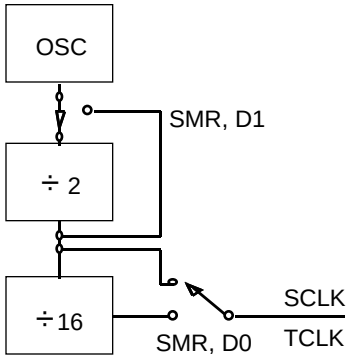


Figure 36. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake-up source of the STOP recovery (Figure 37 and Table 13). When the Stop-Mode Recovery Sources are selected in this register then SMR2 register bits D0,D1 must be set to zero. P33-P31 and Port 2 cannot wake up from STOP Mode if the input lines are configured as analog inputs to the Analog comparator or Analog-to-Digital Converter.

Note: If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.

Table 13. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition (not in Analog Mode)
0	1	1	P32 transition (not in Analog Mode)
1	0	0	P33 transition (not in Analog Mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). This bit, if High, enables the T_{POR} /RESET delay after Stop-Mode Recovery. The default configuration of this bit is "1". A POR or WDT reset will override the selection and cause the reset delay to occur.

Stop-Mode Recovery Edge Select (D6). A "1" in this bit position indicates that a high level on the output to the exclusive Or-Gate input from the selected recovery source wakes the Z86C83/C84/E83 from STOP Mode. A "0" indicates low-level recovery. The default is 0 on POR. This bit is used for either SMR or SMR2.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT reset. A "1" in this bit (warm) indicates that the device awakens by a Stop-Mode Recovery source.

Note: A WDT reset out of STOP Mode will also set this bit to a "1".

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

Table 14. Stop-Mode Recovery Source

SMR:10		Operation
D1	D0	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

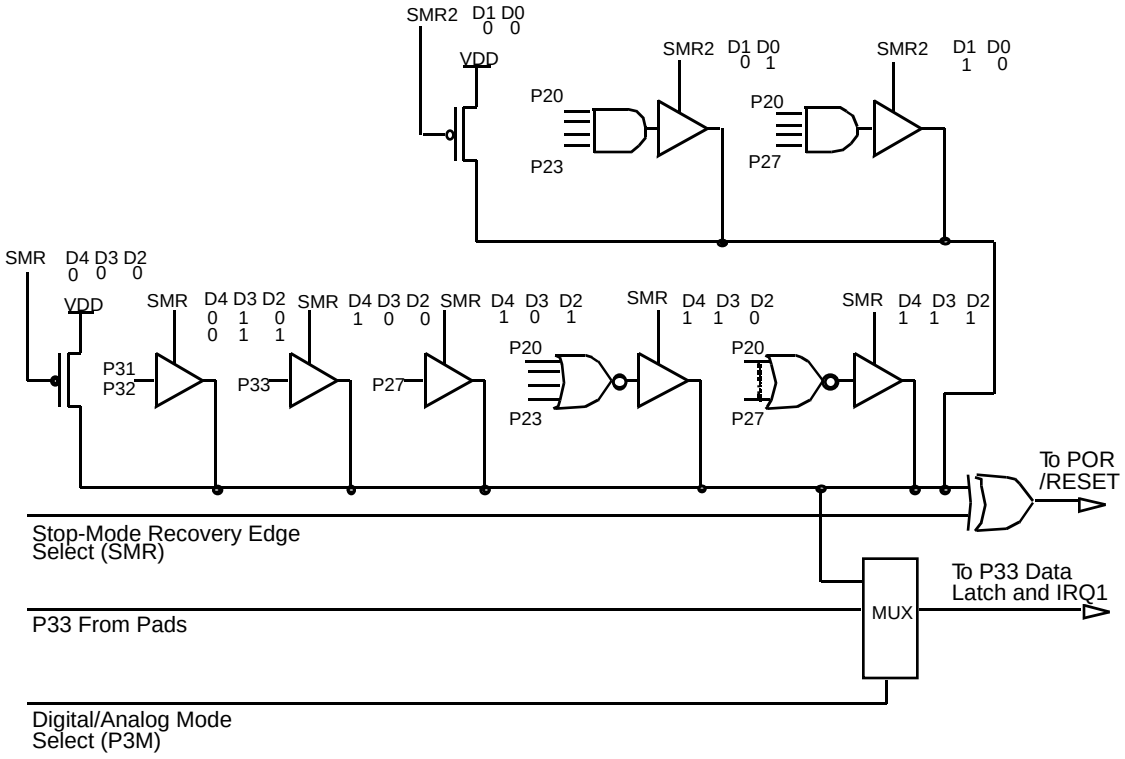


Figure 37. Stop-Mode Recovery Source

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 38).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

Note: WDT time-out while in Stop-Mode will not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 and 3 Data Registers, but will cause the reset delay to occur.

The Power-On Reset (POR) clock source is selected with bit 4 of the WDTMR. Bits 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to "1," the WDT is only driven by the external clock during STOP Mode. This feature makes it possible to wake up from STOP Mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 39). This register is accessible only during the first 60 processor cycles (60 SCLKs) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register group at address location 0FH.

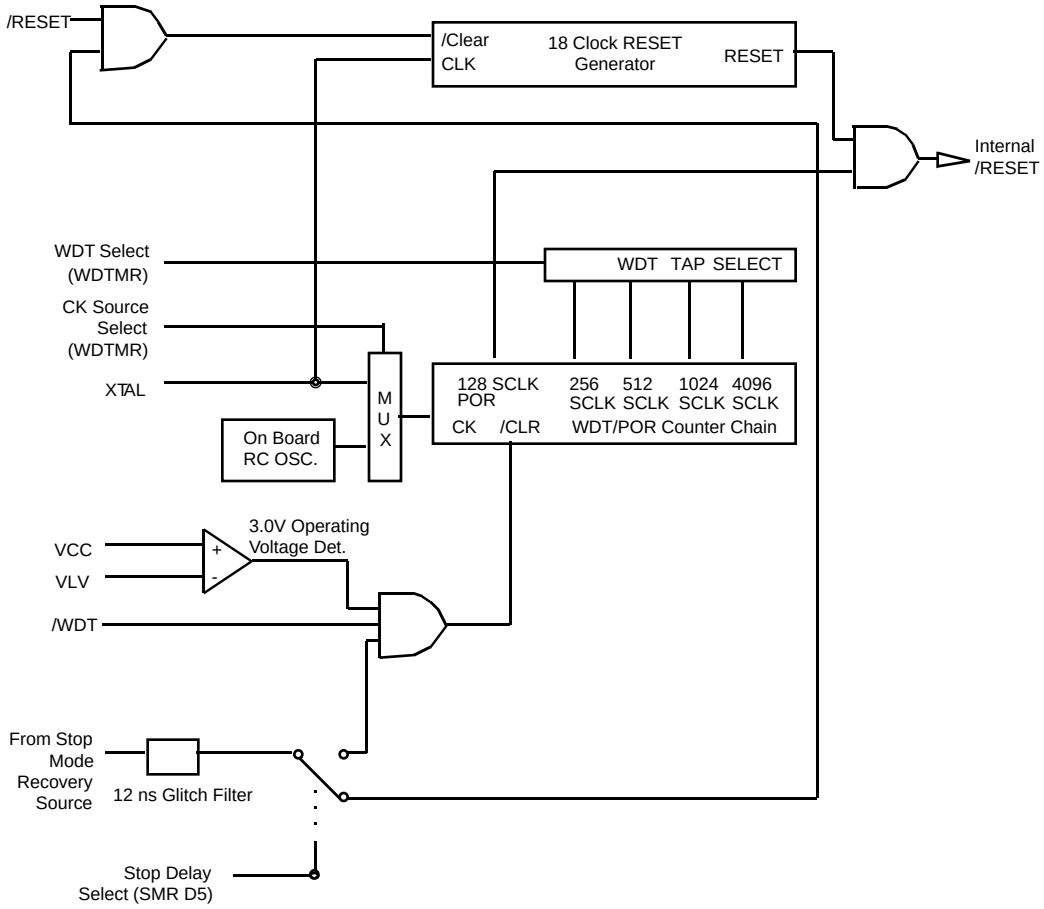


Figure 38. Resets and WDT

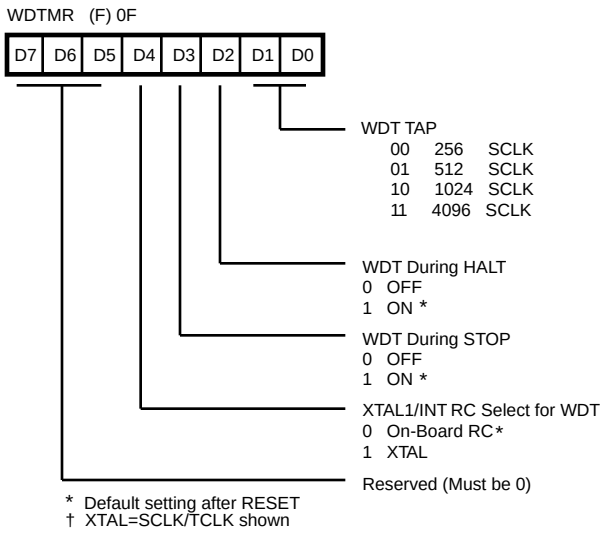


Figure 39. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D1, D0). Selects the WDT time-out period. It is configured as shown in Table 15.

Table 15. WDT Time Select (Min. @ 5.0V)

D1	D0	Time-Out of Internal RC OSC	Time-Out of SCLK Clock
0	0	6.25 ms min	256 SCLK
0	1	12.5 ms min	512 SCLK
1	0	25 ms min	1024 SCLK
1	1	100 ms min	4096 SCLK

Note: The minimum time shown is for V_{CC} @ 5.0V.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates active during HALT. The default is "1".

Note: If WDT is permanently selected (always ON mode), the WDT will continue to run even if set not to run in STOP or HALT Mode.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC has to be selected as the clock source to the POR counter. A "1" indicates active during STOP. The default is "1". If bits D3 and D4 are both set to "1", the WDT only, is driven by the external clock during STOP Mode.

Notes:

1. If WDT is permanently selected (always ON mode) using internal on-board RC oscillator, the WDT will continue to run even if set not to run in STOP or HALT Mode.

2. WDT instructions affect the Z (Zero), S (Sign), and V (Overflow) flags.

On-Board, Power-On-Reset RC or External XTAL1 Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a "1", the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. If the XTAL1 pin is selected as the oscillator source for the WDT, during STOP Mode, the oscillator will be stopped and the WDT will not run. This is true even if the WDT is selected to run during STOP Mode.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{CC} is below the specified voltage (typically 2.6V).

ROM Protect. ROM Protect is mask or OTP bit-programmable. It is selected by the customer at the time the ROM code is submitted.

ROM Mask Selectable Options

There are two ROM mask options that must be selected at the time the ROM mask is ordered (ROM code submitted) for the Z86C83/C84 and three Z86E83 OTP bit options.

Table 16. Selectable Options

Option	Selection
Permanent WDT	Yes/No
ROM Protect	Yes/No
EPROM/TEST Mode Disable*	Yes/No

Note:
*For Z86E83 only
EPROM/TEST Mode Disable - On the Z86E83, the user can permanently disable entry into EPROM Mode and TEST Mode by programming this bit.

EXPANDED REGISTER FILE CONTROL REGISTERS (0C)

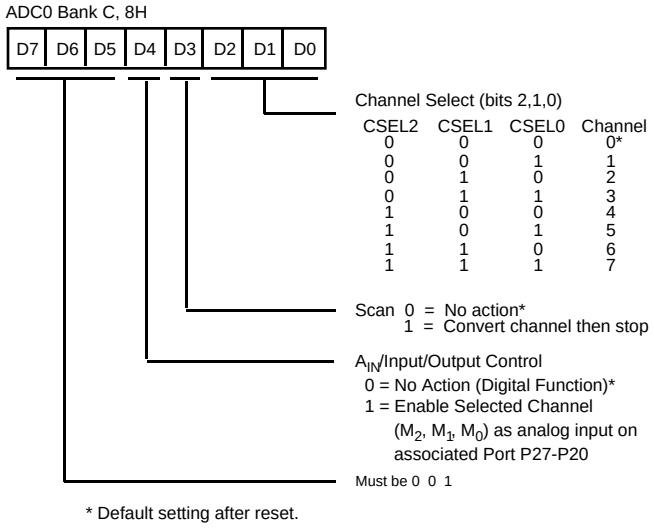


Figure 40. ADC Control Register 0 (Read/Write)

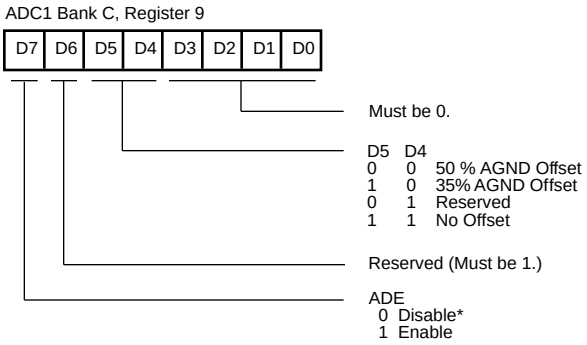


Figure 41. ADC Control Register 1 (Read/Write)

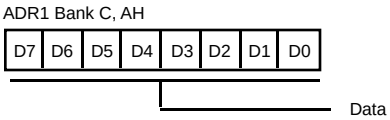


Figure 42. AD Result Register (Read Only)

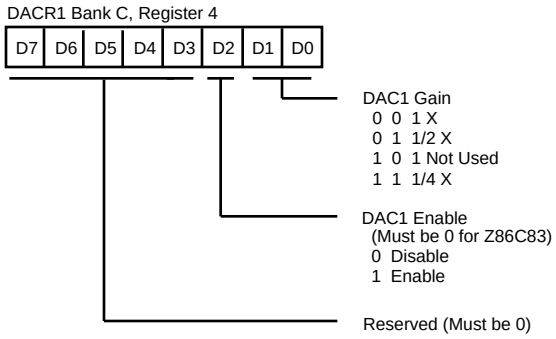


Figure 43. D/A 1 Control Register

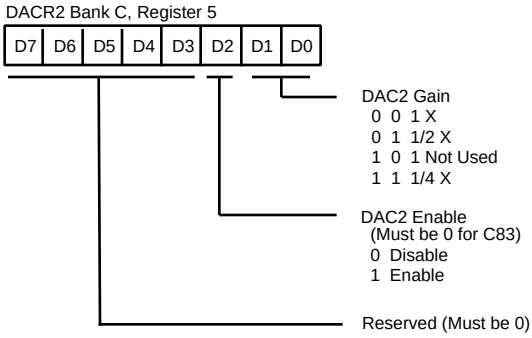


Figure 44. D/A 2 Control Register

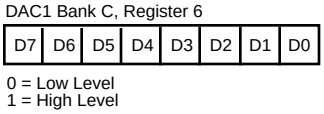


Figure 45. D/A 1 Data Register

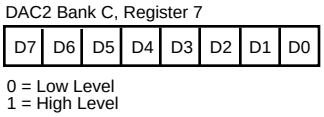
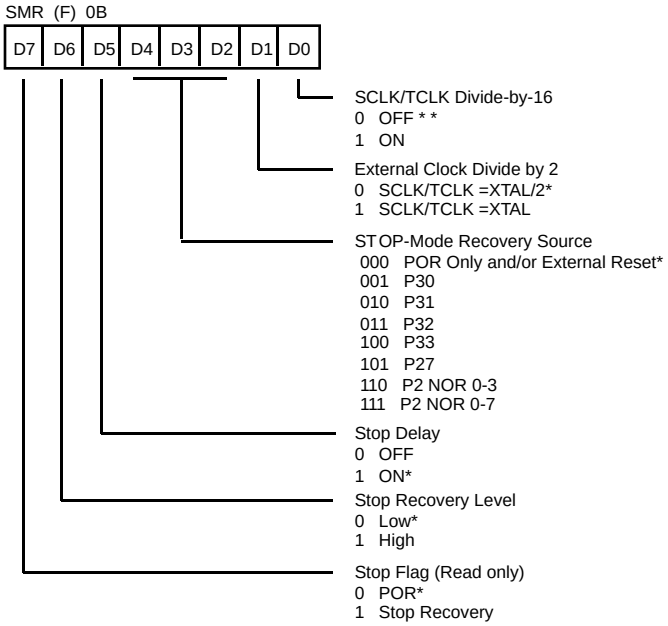


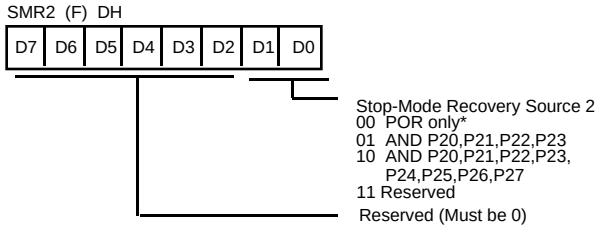
Figure 46. D/A 2 Data Register

EXPANDED REGISTER FILE CONTROL REGISTERS



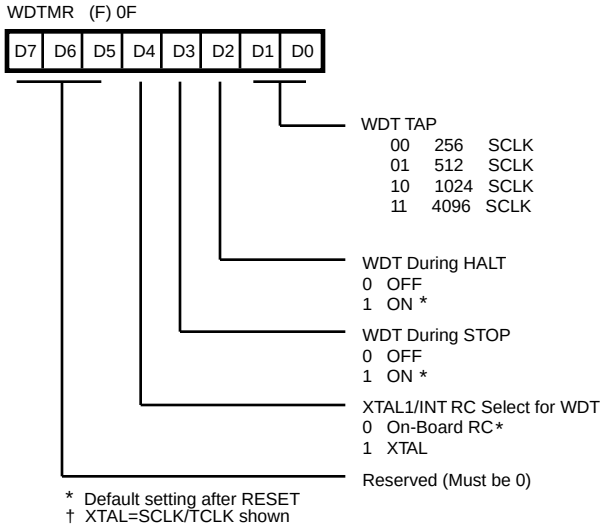
Note: Not used in conjunction with SMR2 Source
* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

Figure 47. Stop-Mode Recovery Register (Write-Only, except Bit 7 which is Read-Only)



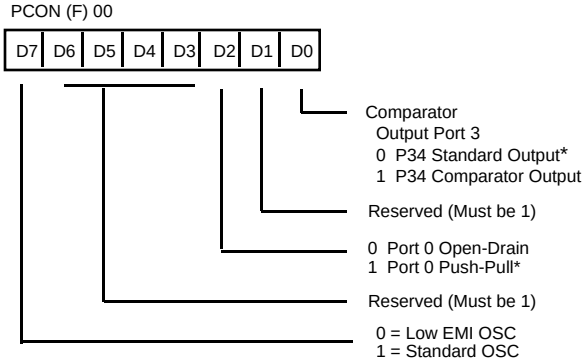
Note: Not used in conjunction with SMR Source

Figure 48. Watch-Dog Timer Mode Register 2



* Default setting after RESET
† XTAL=SCLK/TCLK shown

Figure 49. Watch-Dog Timer Mode Register (Write-Only)



* Default setting from Stop-Mode Recovery
Power-On Reset, and any WDT Reset.

Figure 50. Port Configuration Register (PCON) (Write-Only)

Z8 CONTROL REGISTERS

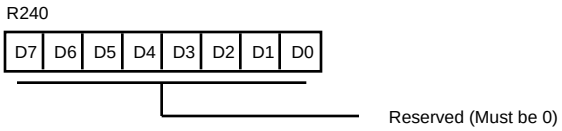


Figure 51. Reserved

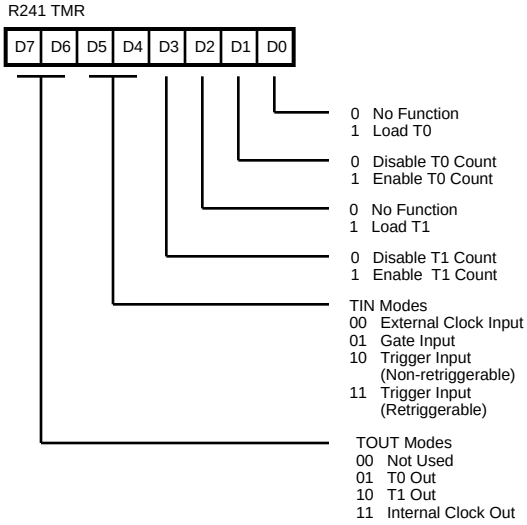


Figure 52. Timer Mode Register ($F1_H$: Read/Write)

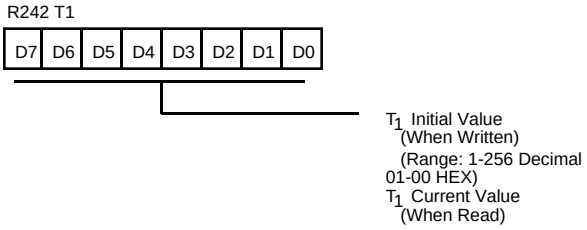


Figure 53. Counter/Timer 1 Register ($F2_H$: Read/Write)

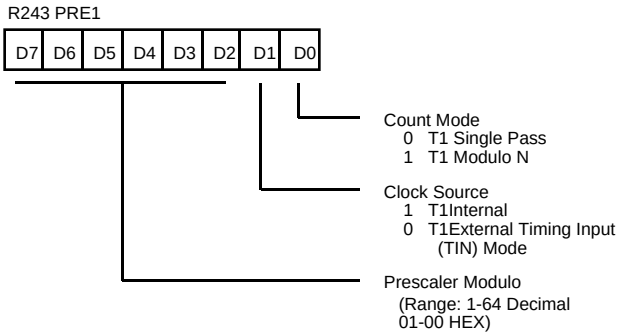


Figure 54. Prescaler 1 Register ($F3_H$: Write-Only)

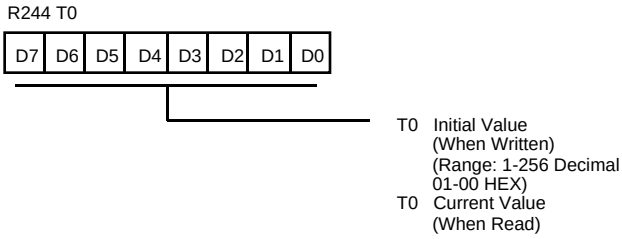


Figure 55. Counter/Timer 0 Register ($F4_H$: Read/Write)

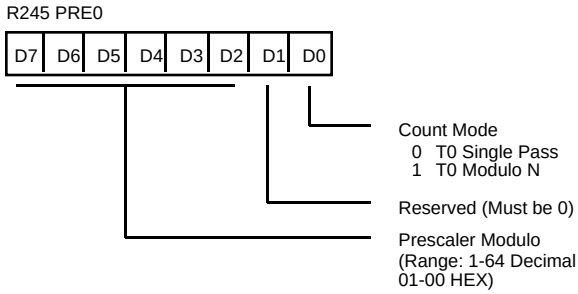


Figure 56. Prescaler 0 Register ($F5_H$: Write-Only)

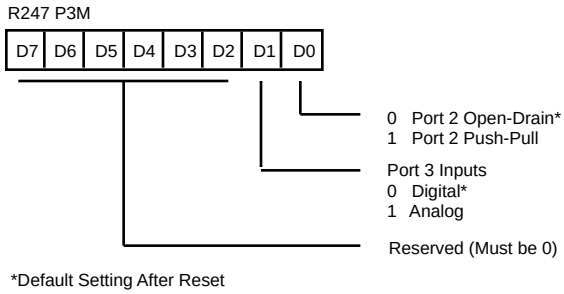


Figure 57. Port 3 Mode Register ($F7_H$: Write-Only)

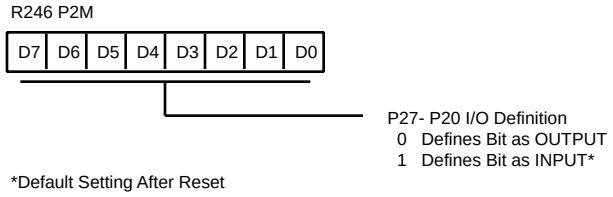


Figure 58. Port 2 Mode Register ($F6_H$: Write-Only)

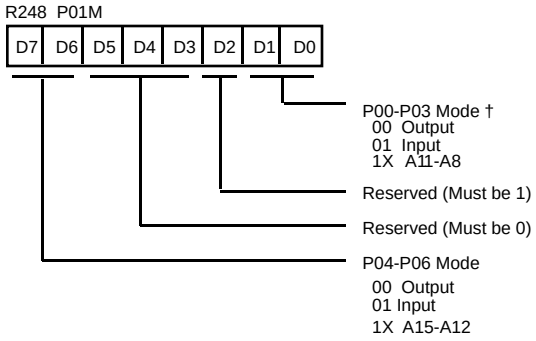


Figure 59. Port 0 and 1 Mode Register ($F8_H$: Write-Only)

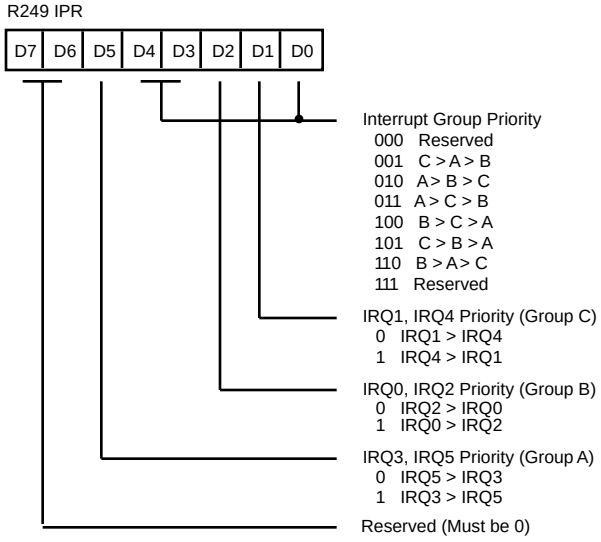


Figure 60. Interrupt Priority Register ($F9_H$: Write-Only)

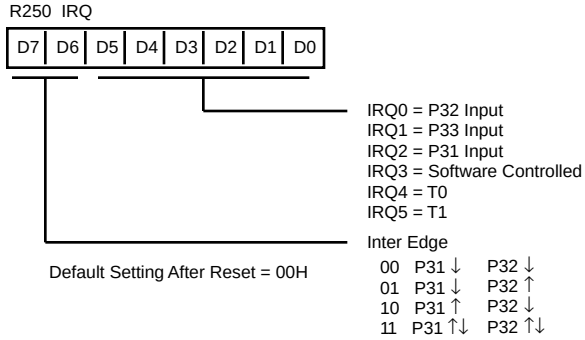


Figure 61. Interrupt Request Register (F_{AH}: Read/Write)

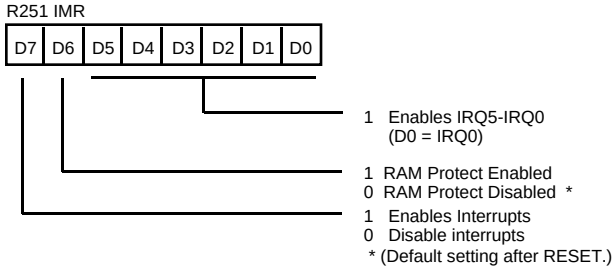


Figure 62. Interrupt Mask Register (F_{BH}: Read/Write)

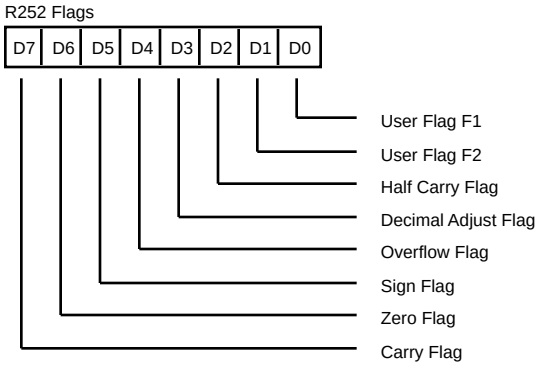


Figure 63. Flag Register (F_{CH}: Read/Write)

Z8 CONTROL REGISTERS (Continued)

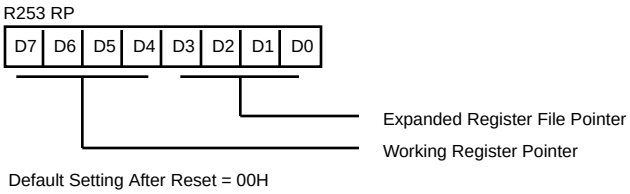


Figure 64. Register Pointer (F_{DH}: Read/Write)

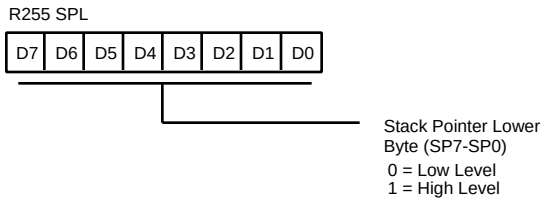


Figure 66. Stack Pointer (F_{FH}: Read/Write)

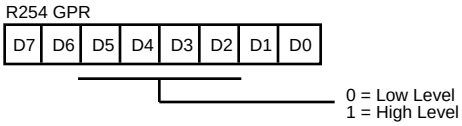


Figure 65. General-Purpose Register (F_{EH}: Read/Write)

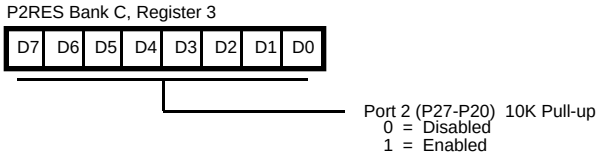
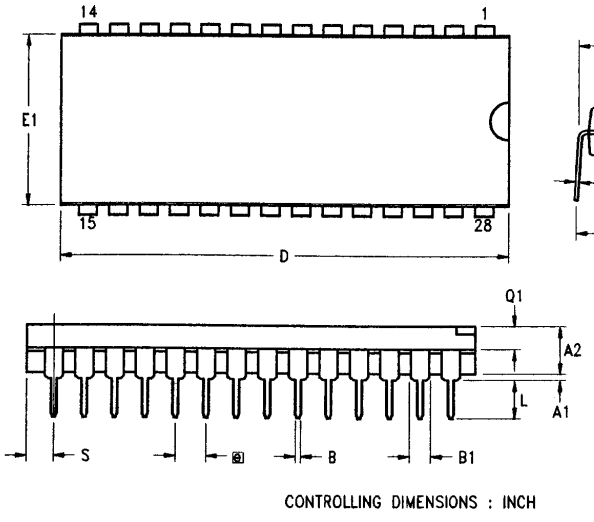


Figure 67. Port 2 Pull-up Register

PACKAGE INFORMATION



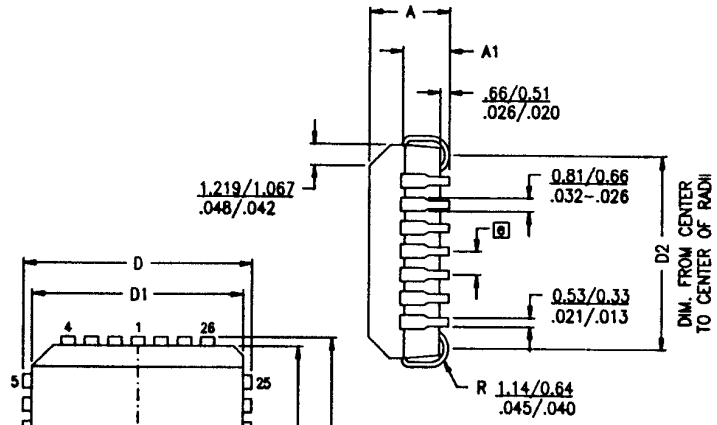
OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

Figure 68. 28-Pin DIP Package Diagram

Figure 69. 28-Pin SOIC Package Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
G	1.27 TYP		.050 TYP	

NOTES.
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 INCH.
3. DIMENSION : MM / INCH

Figure 70. 28-Pin PLCC Package Diagram

ORDERING INFORMATION

Z86C83 16 MHz			Z86E83 16 MHz		
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**	**28-Pin DIP**	**28-Pin SOIC**	**28-Pin PLCC**
Z86C8316PSC	Z86C8316SSC	Z86C8316VSC	Z86E8316PSC	Z86E8316SSC	Z86E8316VSC
Z86C8316PEC	Z86C8316SEC	Z86C8316VEC	Z86E8316PEC	Z86E8316SEC	Z86E8316VEC
Z86C84 16 MHz					
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**			
Z86C8416PSC	Z86C8416SSC	Z86C8416VSC			
Z86C8416PEC	Z86C8416SEC	Z86C8416VEC			

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Package

P = Plastic DIP
S = Plastic SOIC

Temperature

S = 0°C to + 70°C
E = -40°C to +105°C

Speed

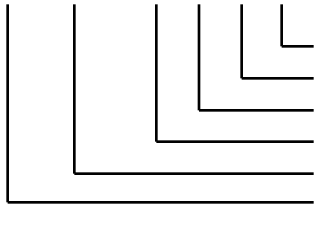
16 = 16 MHz

Environmental

C = Plastic Standard

Example:

Z 86C83 16 P S C is a Z86C83, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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