LAN7850

Hi-Speed USB 2.0 to 10/100/1000 Ethernet Controller with HSIC

Highlights

- Single Chip Hi-Speed (HS) USB 2.0 to 10/100/1000 Ethernet Controller
  - Integrated Gigabit PHY with HP Auto-MDIX
  - Integrated 10/100/1000 Ethernet MAC (Full-Duplex Support)
  - Integrated USB 2.0 Device Controller
  - Integrated USB PHY
- Low Power Consumption
  - Compliant with Energy Efficient Ethernet IEEE 802.3az
  - Wake on LAN support (WoL)
- Configuration via One Time Programmable (OTP) Memory
- NetDetach provides automatic USB attach/detach when Ethernet cable is connected/removed

Target Applications

- Automotive Infotainment
- Notebook/Tablet Docking Stations
- Detachable Laptops
- USB Port Replicators
- Standalone USB to Ethernet Dongles
- Embedded Systems / CE Devices
- Set-Top Boxes / Video Recorders
- Test Instrumentation / Industrial

System Considerations

- Power and I/Os
  - Multiple power management features
  - 12 GPIOs
  - Supports bus and self-powered operation
  - Variable voltage I/O supply (1.8V-3.3V)
- Software Support
  - Windows 7, 8, 8.1, and 10 drivers (Microsoft Certified)
  - Linux driver
  - OS X and macOS driver
  - uBoot support
  - UEFI support
  - PXE support
  - FreeBSD support
  - Windows OTP/EEPROM programming and testing utility
- Packaging
  - RoHS compliant 56-pin SQFN (8 x 8 mm)
- Environmental
  - Commercial temperature range (0°C to +70°C)
  - Industrial temperature range (-40°C to +85°C)

Key Benefits

- USB 2.0 Device Controller
  - Supports HS (480 Mbps), and FS (12 Mbps) modes
  - Four endpoints supported
  - Supports vendor specific commands
  - Remote wakeup supported
  - Integrated HSIC interface
- 10/100/1000 Ethernet Controller
  - Compliant with IEEE802.3/802.3u/802.3ab/802.3az
    - -10BASE-T/100BASE-TX/1000BASE-T support
    - -Full- and half-duplex capability (only full-duplex operation at 1000 Mbps)
  - Controller Modes
    - -Microsoft AOAC support (Always On Always Connected)
    - -Supports Microsoft NDIS 6.2 large send offload
    - -Full-duplex flow control
    - -Loop-back modes
    - -Supports IEEE 802.1q VLAN tagging
    - -VLAN tag based packet filtering (all 4096 tags)
    - -Flexible address filtering modes
      - -33 exact matches (unicast or multicast)
      - -512-bit hash filter for multicast frames
      - -Pass all multicast
      - -Promiscuous unicast/multicast modes
      - -Inverse filtering
      - -Pass all incoming with status report
    - -Supports various statistical counters
    - -PME pin support
  - Frame Features
    - -Supports 32 wake-up frame patterns
    - -Preamble generation and removal
    - -Automatic 32-bit CRC generation and checking
    - -9 KB jumbo frame support
    - -Automatic payload padding and pad removal
    - -Supports Rx/Tx checksum offloads (IPv4, IPv6, TCP, UDP, IGMP, ICMP)
    - -Ability to add and strip IEEE 802.1q VLAN tags

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
10BASE-T	10 Mbps Ethernet, IEEE 802.3 compliant
100BASE-TX	100 Mbps Fast Ethernet, IEEE802.3u compliant
1000BASE-T	100 Mbps Fast Ethernet, IEEE802.3ab compliant
ADC	Analog-to-Digital Converter
AFE	Analog Front End
ALR	Address Logic Resolution
AN	Auto-Negotiation
AOAC	Always on Always Connected
ARP	Address Resolution Protocol
BELT	Best Effort Latency Tolerance
BLW	Baseline Wander
Byte	8 bits
CPM	Clocks and Power Management
CSMA/CD	Carrier Sense Multiple Access/Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32 bits
EC	Embedded Controller
EEE	Energy Efficient Ethernet
EP	USB Endpoint
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FCT	FIFO Controller
FIFO	First In First Out buffer
FS	Full Speed
FSM	Finite State Machine
FW	Firmware
GMII	Gigabit Media Independent Interface
GPIO	General Purpose I/O
GPHY	Gigabit Ethernet Physical Layer
Host	External system (Includes processor, application software, etc.)
HS	High Speed
HW	Hardware. Refers to function implemented by digital logic.
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the device from the host
LDO	Linear Drop-Out Regulator
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true and the status bit is cleared by writing a zero.

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TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
LFPS	Low Frequency Periodic Signal
LFSR	Linear Feedback Shift Register
LPM	Link Power Management
lsb	Least Significant Bit
LSB	Least Significant Byte
LTM	Latency Tolerance Messaging
MAC	Media Access Controller
MDI	Medium Dependent Interface
MDIX	Media Dependent Interface with Crossover
MEF	Multiple Ethernet Frames
MII	Media Independent Interface
MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLD	Multicast Listening Discovery
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
OUI	Organizationally Unique Identifier
Outbound	Refers to data output from the device to the host
PCS	Physical Coding Sublayer
PHY	Physical Layer
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PMD	Physical Medium Dependent
PME	Power Management Event
PMIC	Power Management IC
POR	Power on Reset
PTP	Precision Time Protocol
QWORD	64 bits
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RFE	Receive Filtering Engine
RGMII	Reduced Gigabit Media Independent Interface
RMON	Remote Monitoring
RMII	Reduced Media Independent Interface
RST	Reset
RTC	Real-Time Clock

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TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
SA	Source Address
SCSR	System Control and Status Registers
SEF	Single Ethernet Frame
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SMNP	Simple Network Management Protocol
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
TMII	Turbo Media Independent Interface
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
URX	USB Bulk-Out Receiver
USB	Universal Serial Bus
UTX	USB Bulk-In Transmitter
UUID	Universally Unique IDentifier
VSM	Vendor Specific Messaging
WORD	16 bits
ZLP	Zero Length USB Packet

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1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
VIS	Variable voltage Schmitt-triggered input
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
HSIC	*High-Speed Inter-Chip (HSIC) USB Electrical Specification* compliant input/output
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog Input
AIO	Analog bidirectional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

1.3 Register Nomenclature

TABLE 1-3: REGISTER NOMENCLATURE

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
RS	**Read to Set:** This bit is set on read.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** Writing anything clears the value.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** This mode is used by the Ethernet PHY registers. Bits with this attribute will stay high until the bit is read. After it is read, the bit will remain high, but will change to low if the condition that caused the bit to go high is removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition.
NALR	**Not Affected by Lite Reset.** The state of NASR bits do not change on assertion of a lite reset.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros, unless otherwise indicated, to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

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2.0 INTRODUCTION

2.1 General Description

The LAN7850 is a high performance Hi-SpeedUSB 2.0 to 10/100/1000 Ethernet controller with an integrated 10/100/1000 Ethernet PHY and High-Speed Inter-Connect (HSIC) interface. With applications ranging from notebook/tablet docking stations, set-top boxes, and PVRs, to USB port replicators, USB to Ethernet dongles, embedded systems, and test instrumentation, the LAN7850 is a high performance and cost effective USB/HSIC to Ethernet connectivity solution.

The LAN7850 contains an integrated 10/100/1000 Ethernet MAC and PHY, Filtering Engine, USB PHY (with HSIC interface), Hi-Speed USB 2.0 device controller, TAP controller, EEPROM controller, and a FIFO controller with internal packet buffering.

The internal USB 2.0 device controller and USB PHY are compliant with the USB 2.0 Hi-Speed standard. The LAN7850 implements Control, Interrupt, Bulk-in, and Bulk-out USB Endpoints.

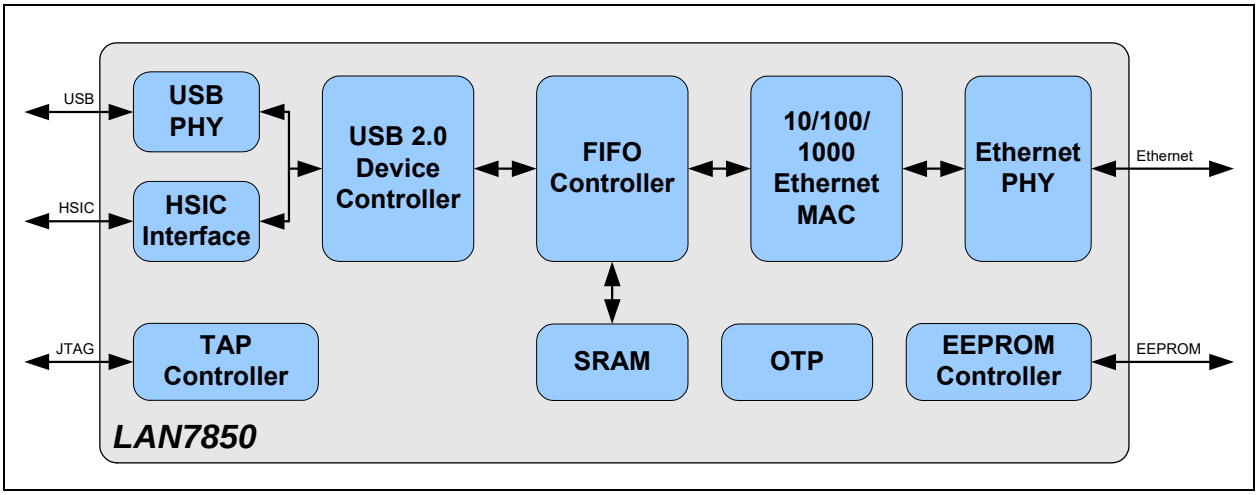
The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3, IEEE 802.3u, IEEE 802.3ab, and 802.3az (Energy Efficient Ethernet) standards. ARP and NS offload are also supported.

Multiple power management features are provided, including Energy Efficient Ethernet (IEEE 802.3az), support for Microsoft's Always On Always Connected (AOAC), and "Magic Packet", "Wake On LAN", and "Link Status Change" wake events. Wake events can be programmed to initiate a USB remote wakeup. Up to 32 different AOAC wake-up frame patterns are supported along with Microsoft's WPD (Whole Packet Detection).

An internal EEPROM controller exists to load various USB and Ethernet configuration parameters. For EEPROM-less applications, the LAN7850 provides 1K Bytes of OTP memory that can be used to preload this same configuration data before enumeration. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

The LAN7850 is available in commercial and industrial temperature range versions. An internal block diagram of the LAN7850 is shown in Figure 2-1.

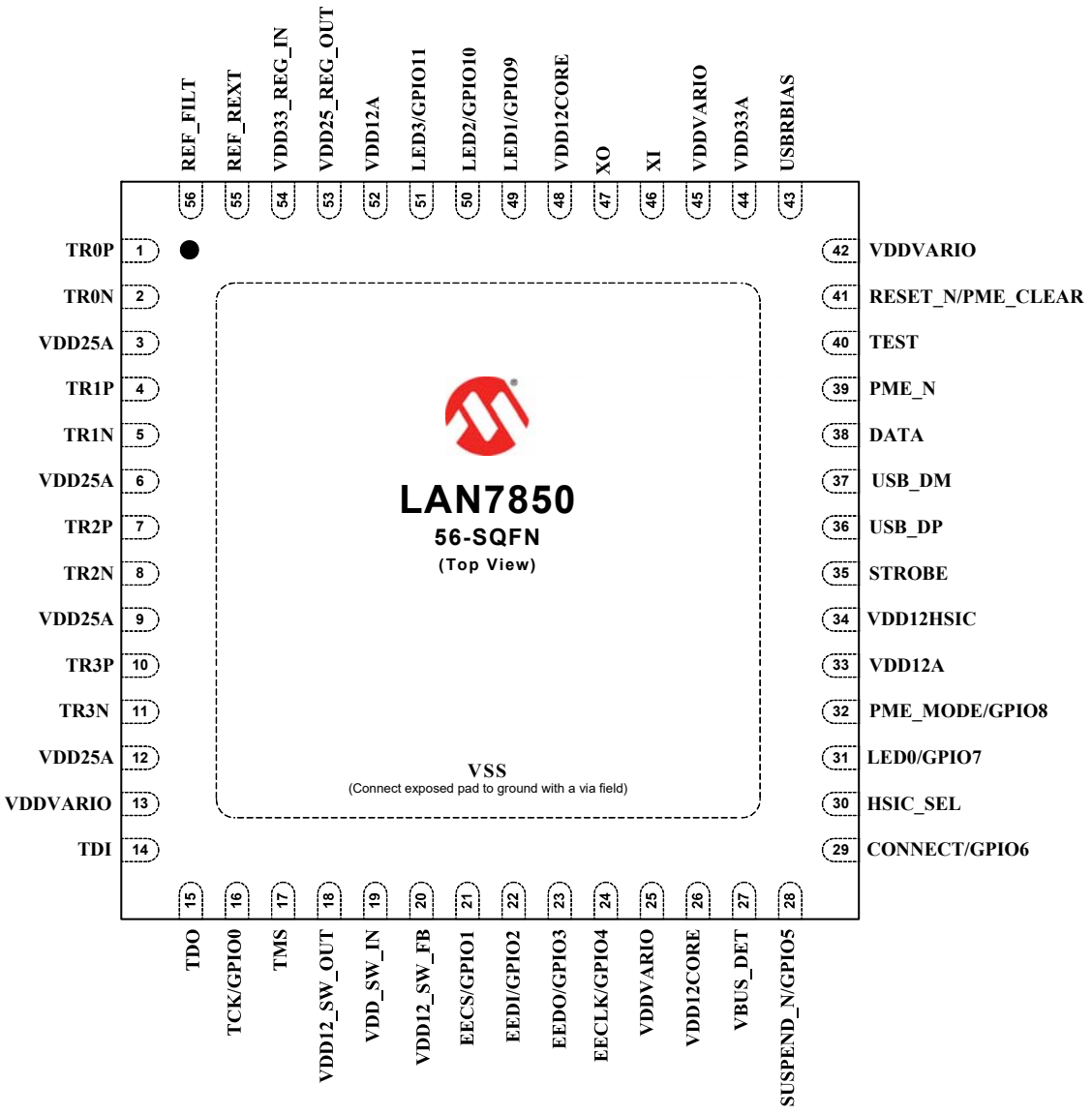
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

Note: When an "_N" is used at the end of the signal name, it indicates that the signal is active low. For example, **RESET_N** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.2, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

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TABLE 3-1: PIN ASSIGNMENTS

Pin Number	Pin Name	Pin Number	Pin Name
1	TR0P	29	CONNECT/GPIO6
2	TR0N	30	HSIC_SEL
3	VDD25A	31	LED0/GPIO7
4	TR1P	32	PME_MODE/GPIO8
5	TR1N	33	VDD12A
6	VDD25A	34	VDD12HSIC
7	TR2P	35	STROBE
8	TR2N	36	USB_DP
9	VDD25A	37	USB_DM
10	TR3P	38	DATA
11	TR3N	39	PME_N
12	VDD25A	40	TEST
13	VDDVARIO	41	RESET_N/PME_CLEAR
14	TDI	42	VDDVARIO
15	TDO	43	USBRBIAS
16	TCK/GPIO0	44	VDD33A
17	TMS	45	VDDVARIO
18	VDD12_SW_OUT	46	XI
19	VDD_SW_IN	47	XO
20	VDD12_SW_FB	48	VDD12CORE
21	EECS/GPIO1	49	LED1/GPIO9
22	EEDI/GPIO2	50	LED2/GPIO10
23	EEDO/GPIO3	51	LED3/GPIO11
24	EECLK/GPIO4	52	VDD12A
25	VDDVARIO	53	VDD25_REG_OUT
26	VDD12CORE	54	VDD33_REG_IN
27	VBUS_DET	55	REF_REXT
28	SUSPEND_N/GPIO5	56	REF_FILT
Exposed Pad (VSS) must be connected to ground			

3.2 Pin Descriptions

TABLE 3-2: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Gigabit Ethernet Pins			
Ethernet TX/RX Positive Channel 0	**TR0P**	AIO	Transmit/Receive Positive Channel 0.
Ethernet TX/RX Negative Channel 0	**TR0N**	AIO	Transmit/Receive Negative Channel 0.
Ethernet TX/RX Positive Channel 1	**TR1P**	AIO	Transmit/Receive Positive Channel 1.
Ethernet TX/RX Negative Channel 1	**TR1N**	AIO	Transmit/Receive Negative Channel 1.
Ethernet TX/RX Positive Channel 2	**TR2P**	AIO	Transmit/Receive Positive Channel 2.
Ethernet TX/RX Negative Channel 2	**TR2N**	AIO	Transmit/Receive Negative Channel 2.
Ethernet TX/RX Positive Channel 3	**TR3P**	AIO	Transmit/Receive Positive Channel 3.
Ethernet TX/RX Negative Channel 3	**TR3N**	AIO	Transmit/Receive Negative Channel 3.
External PHY Reference Filter	**REF_FILT**	AI	External PHY Reference Filter. Connect to an external 1uF capacitor to ground.
External PHY Reference Resistor	**REF_REXT**	AI	External PHY Reference Resistor. Connect to an external 2K 1.0% resistor to ground.
USB Pins			
USB 2.0 DPLUS	**USB_DP**	AIO	Hi-Speed USB data plus.
USB 2.0 DMINUS	**USB_DM**	AIO	Hi-Speed USB Speed data minus.
External USB Bias Resistor	**USBRBIAS**	AI	Used for setting HS transmit current level and on-chip termination impedance. Connect to an external 12K 1.0% resistor to ground.
HSIC STROBE	**STROBE**	HSIC	Bi-directional data strobe signal as defined in the *High-Speed Inter-Chip USB Electrical Specification.*
HSIC DATA	**DATA**	HSIC	Bi-directional Double Data Rate (DDR) data signal that is synchronous to the **STROBE** signal as defined in the *High-Speed Inter-Chip USB Electrical Specification*.
Miscellaneous Pins			
Detect Upstream VBUS Power	**VBUS_DET**	VIS (PD)	Detects the state of the upstream bus power. For bus powered operation, this pin must be tied to **VDD33A**. Refer to Section 4.0, "Power Connections" for additional information.
USB Connect	**CONNECT**	O12	This pin asserts when the device is attempting to attach to the USB host. This pin is intended to help address a known bug on existing HSIC host controllers where the HSIC connect signaling is missed.

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TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
HSIC Select	**HSIC_SEL**	VIS	When tied to VDD, the device HSIC interface is enabled. Otherwise, the USB 2.0 interface is enabled. **Note:** This is a static signal that may not be changed at run time.
PME	**PME_N**	O8/OD8	This pin is used to signal PME when the PME mode of operation is in effect.
PME Mode Select	**PME_MODE**	VIS	This pin serves as the PME mode selection input when the PME mode of operation is in effect.
PME Clear	**PME_CLEAR**	VIS	This pin may serves as PME clear input when the PME mode of operation is in effect.
USB Suspend	**SUSPEND_N**	O12	This pin is asserted when the device is in one of the suspend states as defined in Section 13.3, "Suspend States". This pin may be configured to place an external switcher into a low power state such as when the device is in SUSPEND2.
General Purpose I/O 0-11	**GPIO[0:11]**	VIS/O8/OD8 (PU)	These general purpose I/O pins are each fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. A programmable pull-up may optionally be enabled.
Indicator LEDs 0-3	**LED[0:3]**	OD12	These LEDs can be configured to indicate Ethernet link, activity, duplex, and collision. Refer to Section 9.3, "LED Interface," on page 92 for additional information.
System Reset	**RESET_N**	VIS	System reset. This pin is active low. If this signal is unused it must be pulled-up to VDD.
Test Pin	**TEST**	VIS	Active high test pin. JTAG test mode is selected when the TEST pin is asserted. For proper functional operation this pin should be connected to ground.
EEPROM			
EEPROM Chip Select	**EECS**	O12	This pin drives the chip select output of the external EEPROM.
EEPROM Data In	**EEDI**	VIS	This pin is driven by the EEDO output of the external EEPROM.
EEPROM Data Out	**EEDO**	O12	This pin drives the EEDI input of the external EEPROM.
EEPROM Clock	**EECLK**	O12	This pin drives the EEPROM clock of the external EEPROM.
JTAG			
JTAG Test Mode Select	**TMS**	VIS	JTAG test mode select.
JTAG Test Clock	**TCK**	VIS	JTAG test clock. The maximum operating frequency of this clock is half of the system clock.
JTAG Test Data Input	**TDI**	VIS	JTAG data input.
JTAG Test Data Output	**TDO**	O12	JTAG data output.

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TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Clock Interface			
Crystal Input	**XI**	ICLK	External 25 MHz crystal input. **Note:** This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected.
Crystal Output	**XO**	OCLK	External 25 MHz crystal output.
I/O Power pins, Core Power Pins, and Ground Pad			
Variable I/O Power Supply Input	**VDDVARIO**	P	+1.8V - +3.3V variable supply for I/Os. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
+3.3V Analog Power Supply Input	**VDD33A**	P	+3.3V analog power supply for USB 2.0 AFE. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
+2.5V Analog Power Supply Input	**VDD25A**	P	+2.5V analog power supply input for Gigabit Ethernet PHY. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
+1.2V Ethernet Port Power Supply Input	**VDD12A**	P	+1.2V analog power supply input for USB PLL/AFE. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
+1.2V Digital Core Power Supply Input	**VDD12CORE**	P	+1.2V digital core power supply input. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
+1.2V HSIC Power Supply Input	**VDD12HSIC**	P	+1.2V HSIC power supply input. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
+3.3V LDO Input Voltage	**VDD33_REG_IN**	P	+3.3V power supply input to the integrated LDO. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
+2.5V LDO Output	**VDD25_REG_OUT**	P	+2.5V power supply output from the integrated LDO. This is used to supply power to Gigabit Ethernet PHY AFE. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
Switcher Input Voltage	**VDD_SW_IN**	P	+3.3V input voltage for switching regulator. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
Switcher Feedback	**VDD12_SW_FB**	P	Feedback pin for the integrated switching regulator. Refer to Section 4.0, "Power Connections," on page 16 for connection information. **Note:** To disable the switcher, tie this pin to **VDD_SW_IN**.

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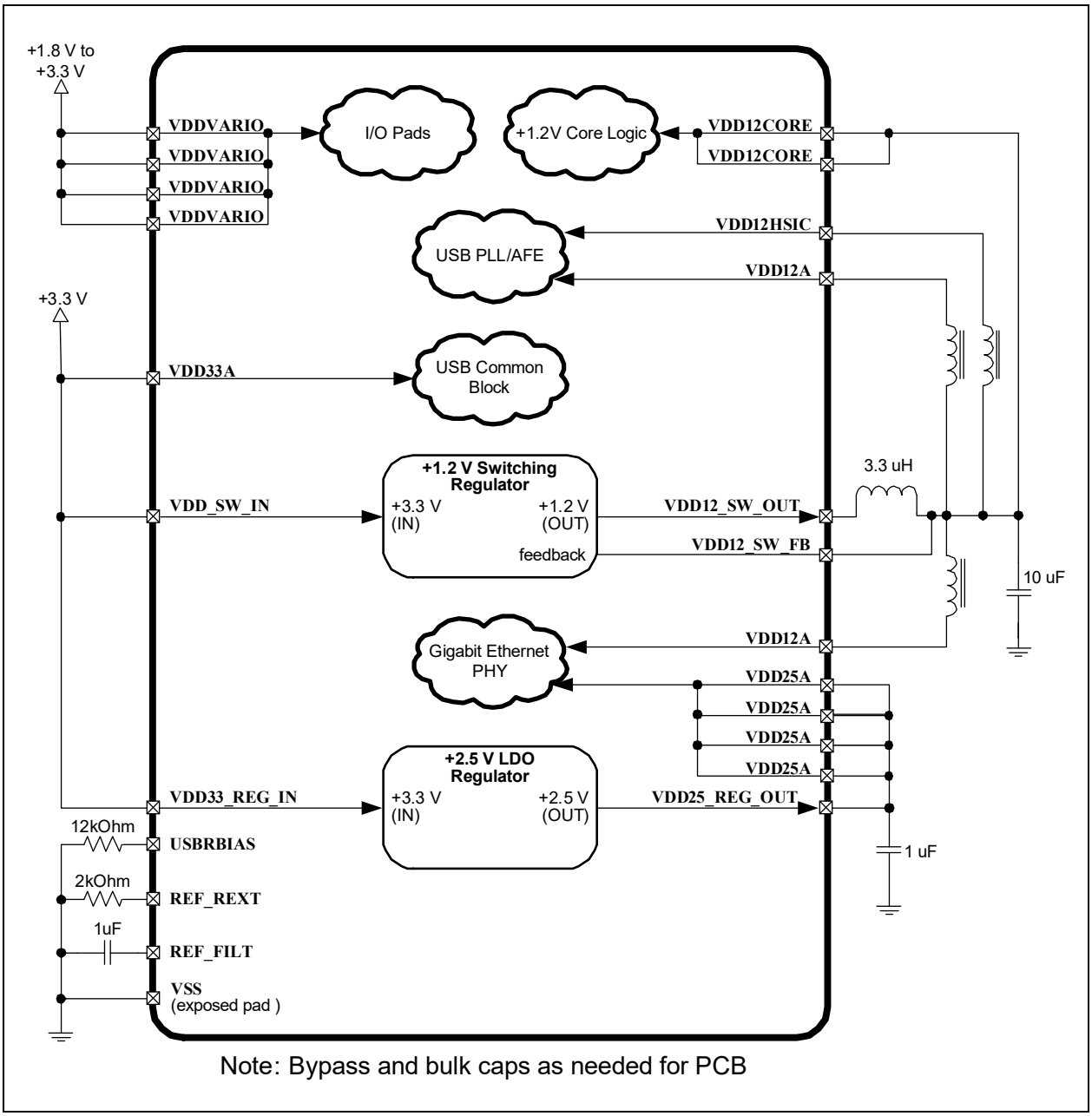
TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
+1.2V Switcher Output Voltage	VDD12_SW_OUT	P	+1.2V power supply output voltage for switching regulator. Refer to Section 4.0, "Power Connections," on page 16 for connection information.
Ground	VSS	P	Common Ground

4.0 POWER CONNECTIONS

Figure 4-1 illustrates the device power connections in a typical application. Refer to the device reference schematic for additional information. Refer to Section 3.0, "Pin Descriptions and Configuration," on page 10 for additional pin information.

FIGURE 4-1: POWER CONNECTION DIAGRAM



Note: Bypass and bulk caps as needed for PCB

Note: For 3.3V I/O operation, the **VDDVARIO** and +3.3V supplies may be connected together. To disable the internal switcher, tie the **VDD12_SW_FB** pin to 3.30V and ensure that all **VDD12** rails are connected to an external 1.20V supply.

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5.0 USB DEVICE CONTROLLER

5.1 Overview

The USB functionality consists of five major parts. The USB PHY, UDC (USB Device Controller), URX (USB Bulk Out Receiver), UTX (USB Bulk In Transmitter), and CTL (USB Control Block).

The UDC is configured to support one configuration, one interface, one alternate setting, and four endpoints. Streams are not supported in this device. The URX and UTX implement the Bulk-Out and Bulk-In endpoints respectively. The CTL manages Control and Interrupt endpoints.

Each USB Controller endpoint is unidirectional with even numbered endpoints handling the OUT (from the host, actually RX into the device) direction and odd numbered endpoints handling the IN (to the host, actually TX from the device) direction.

The UDC endpoint numbers start at 0 and increment. Endpoint numbers are not skipped and have a fixed mapping to the USB endpoint numbers. The corresponding USB endpoint is obtained by dividing the UDC endpoint number by 2 (rounding down). For example, single directional endpoint 0 indicates USB OUT endpoint 0, and single directional endpoint 1 corresponds to USB IN endpoint 0.

The mapping of the device's USB endpoints to the UDC endpoints is shown in Table 5-1. As can be seen, one IN and two OUT endpoints on the UDC are not utilized.

TABLE 5-1: DEVICE TO UDC ENDPOINT MAPPING

Endpoint Function	USB EP Number
Control OUT	0
Control IN	0
unused	NA
Bulk IN	1
Bulk OUT	2
unused	NA
unused	NA
Interrupt IN	3

5.2 Control Endpoint

The Control endpoint is handled by the CTL (USB Control) module. The CTL module is responsible for handling standard USB requests, as well as USB vendor commands. The UDC does not handle USB commands. These commands are passed to the CTL for completion.

5.2.1 USB STANDARD COMMAND PROCESSING

This section lists the supported USB standard device requests. The basic format of a device request is shown in section 9.3 of the USB 2.0 specification and the standard device requests are described in section 9.4. Valid values of the parameters are given below.

Per the USB specifications, if an unsupported or invalid request is made to a USB device, the device responds by returning STALL in the Data or Status stage of the request. Receipt of an unsupported or invalid request does NOT cause the optional Halt feature on the control pipe to be set.

For each request supported, the USB specifications provide details on the device behavior during the various configuration states and on the conditions which will return a Request Error. Some requests affect the state of the hardware.

In order to implement the Get Descriptor command, the CTL manages a 128x32 Descriptor RAM. The RAMs contents are initialized via the EEPROM or OTP, after a system reset occurs. The Descriptor RAM may also be programmed by the device driver to support EEPROM-Less mode.

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TABLE 5-2: STRING DESCRIPTOR INDEX MAPPINGS

INDEX	STRING NAME
0	Language ID
1	Manufacturer ID
2	Product ID
3	Serial Number
4	Configuration String
5	Interface String

When the UDC decodes a Get Descriptor command, it will pass a pointer to the CTL. The CTL uses this pointer to determine what the command is and how to fill it.

5.2.1.1 Clear Feature

bmRequestType - 00h for the device, 01h for interfaces and 02h for endpoints.

wValue - Specifies the feature, 1=Device_Remote_Wakeup and 0=Endpoint_Halt.

wIndex - Always 0 when the device is selected, specifies the interface number (always 0) when an interface is selected or the direction/endpoint number (0, 80h, 81h, 2 or 83h) when an endpoint is selected.

A ClearFeature(Endpoint_Halt) request will clear the USB 2.0 data toggle for the specified endpoint.

5.2.1.2 Get Configuration

All parameters are fixed per the USB specifications.

5.2.1.3 Get Descriptor

wValue - The high byte selects the descriptor type. The supported descriptors for this command are 1=Device, 2=Configuration (including Interface, Endpoint descriptors and Endpoint Companion descriptors (USB 2.1 LPM)), 3=String, 6=Device Qualifier (HS/FS), 7=Other Speed Configuration (USB2.0). The low byte selects the descriptor index and must be 0.

Note: Direct access to the Interface, Endpoint and Endpoint Companion (USB 2.1 LPM) descriptors are not supported by this command and will cause a USB stall.

wIndex - Specifies the Language ID for string descriptors or is 0 for other descriptors.

wLength - Specifies the number of bytes to return. If the descriptor is longer than the wLength field, only the initial bytes of the descriptor are returned. If the descriptor is shorter than the wLength field, the device indicates the end of the control transfer by sending a short packet when further data is requested. A short packet is defined as a packet shorter than the maximum payload size or a zero length data packet.

5.2.1.4 Get Interface

wIndex - Specifies the interface, always 0 for this device.

5.2.1.5 Get Status

bmRequestType - 00h for the device, 01h for interfaces and 02h for endpoints.

wIndex - Always 0 when the device is selected, specifies the interface number (always 0) when an interface is selected or the direction/endpoint number (0, 80h, 81h, 2 or 83h) when an endpoint is selected.

Note: Power Method (PWR_SEL) in Hardware Configuration Register (HW_CFG) is used as the source for the Self-Power bit (D0).

5.2.1.6 Set Address

wValue - Specifies the new device address.

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Per the USB specification, the USB device does not change its device address until after the Status stage of this request is completed successfully. This is a difference between this request and all other requests. For all other requests, the operation indicated must be completed before the Status stage.

5.2.1.7 Set Configuration

wValue - The lower byte specifies the configuration value.

The device supports only one configuration. A value of 1 places the device into the Configured state while a value of 0 places the device into the Address state.

The Halt feature is reset for *all* endpoints upon the receipt of this request with a valid configuration value.

The USB 2.0 data toggle for *all* endpoints are initialized upon the receipt of this request with a valid configuration value.

5.2.1.8 Set Descriptor

This optional request is not supported and the device responds by returning STALL.

5.2.1.9 Set Feature

bmRequestType - 00h for the device, 01h for interfaces and 02h for endpoints.

wValue - Specifies the feature, 1=Device_Remote_Wakeup, 2=device Test_Mode, 0=Endpoint_Halt.

Note:	Endpoint_Halt is not implemented for Endpoint 0.

wIndex - Specifies the interface number (always 0) when an interface is selected or the direction/endpoint number (81h, 2 or 83h) when an endpoint is selected. When the device is selected, this field is always 0 unless device Test_Mode is selected via wValue, in which case the upper byte is the Test Selector and the lower byte a 0.

5.2.1.10 Set Interface

wValue - Specifies the alternate setting (must be 0).

wIndex - Specifies the interface (always 0).

Only one interface with one setting is supported by the device. If the command is issued with an interface other than 00h, the device responds with a Request Error. If the command is issued with an interface setting of 00h but with an alternative setting other than 00h, the device responds with a STALL.

The Halt feature is reset for *all* endpoints upon the receipt of this request with valid interface and alternate setting values.

The USB 2.0 data toggle for *all* endpoints are initialized upon the receipt of this request with valid interface and alternate setting values.

5.2.1.11 Set Isochronous Delay

This command is not supported. The device will respond with a Stall to this request.

5.2.1.12 Set SEL

This command is not supported. The device will respond with a Stall to this request.

5.2.1.13 Sync Frame

There are no isochronous endpoints in this device. The device will respond with a Stall to this request.

5.2.2 USB VENDOR COMMANDS

The device implements several vendor specific commands in order to directly access CSRs and efficiently gather statistics. The memory map utilized by the address field is defined in Table 15-1, “Memory Map,” on page 138.

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5.2.2.1 Write Command

This command allows the Host to write a memory location. Burst writes are not supported. All writes are 32-bits.

TABLE 5-3: FORMAT OF WRITE SETUP STAGE

Offset	Field	Value
0h	bmRequestType	40h
1h	bRequest	A0h
2h	wValue	00h
4h	wIndex	{Address[12:0]}
6h	wLength	04h

TABLE 5-4: FORMAT OF WRITE DATA STAGE

Offset	Field
0h	Register Write Data [31:0]

5.2.2.2 Read Command

This command allows the Host to read a memory location. Burst reads are not supported. All reads return 32-bits.

TABLE 5-5: FORMAT OF READ SETUP STAGE

Offset	Field	Value
0h	bmRequestType	C0h
1h	bRequest	A1h
2h	wValue	00h
4h	wIndex	{Address[12:0]}
6h	wLength	04h

TABLE 5-6: FORMAT OF READ DATA STAGE

Offset	Field
0h	Register Read Data [31:0]

5.2.2.3 Get Statistics Command

The Get Statistics Command returns the entire contents of the RX and TX statistics counters. The statistics counters are snapshot when fulfilling the command request. The statistics counters rollover.

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Note: TX statistics counters are not affected by frames sent in response to NS/ARP requests when the device is suspended.

Good byte and received frame counters will count all frames that are delivered to the Host. If Store Bad Frames is set in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) any bad frames received will be counted as well.

The statistics counters are cleared by all reset events including LRST.

TABLE 5-7: FORMAT OF GET STATISTICS SETUP STAGE

Offset	Field	Value
0h	bmRequestType	C0h
1h	bRequest	A2h
2h	wValue	00h
4h	wIndex	00h
6h	wLength	BCh

TABLE 5-8: FORMAT OF GET STATISTICS DATA STAGE

Offset	Field
00h	RX FCS Errors
04h	RX Alignment Errors
08h	Rx Fragment Errors
0Ch	RX Jabber Errors
10h	RX Undersize Frame Errors
14h	RX Oversize Frame Errors
18h	RX Dropped Frames
1Ch	RX Unicast Byte Count
20h	RX Broadcast Byte Count
24h	RX Multicast Byte Count
28h	RX Unicast Frames
2Ch	RX Broadcast Frames
30h	RX Multicast Frames
34h	RX Pause Frames
38h	RX 64 Byte Frames
3Ch	RX 65 - 127 Byte Frames
40h	RX 128 - 255 Byte Frames
44h	RX 256 - 511 Bytes Frames
48h	RX 512 - 1023 Byte Frames
4Ch	RX 1024 - 1518 Byte Frames
50h	RX Greater 1518 Byte Frames
54h	EEE RX LPI Transitions
58h	EEE RX LPI Time
5Ch	TX FCS Errors
60h	TX Excess Deferral Errors
64h	TX Carrier Errors
68h	TX Bad Byte Count

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TABLE 5-8: FORMAT OF GET STATISTICS DATA STAGE (CONTINUED)

Offset	Field
6Ch	TX Single Collisions
70h	TX Multiple Collisions
74h	TX Excessive Collision
78h	TX Late Collisions
7Ch	TX Unicast Byte Count
80h	TX Broadcast Byte Count
84h	TX Multicast Byte Count
88h	TX Unicast Frames
8Ch	TX Broadcast Frames
90h	TX Multicast Frames
94h	TX Pause Frames
98h	TX 64 Byte Frames
9Ch	TX 65 - 127 Byte Frames
A0h	TX 128 - 255 Byte Frames
A4h	TX 256 - 511 Bytes Frames
A8h	TX 512 - 1023 Byte Frames
ACh	TX 1024 - 1518 Byte Frames
B0h	TX Greater 1518 Byte Frames
B4h	EEE TX LPI Transitions
B8h	EEE TX LPI Time

TABLE 5-9: STATISTICS COUNTER DEFINITIONS

Name	Description	Size (Bits)
RX FCS Errors	Number of frames received with CRC-32 errors or RX errors. **Note:** If a frame has a Jabber Error and FCS error, only the RX Jabber Errors counter will be incremented **Note:** If a frame is less than 64 bytes in length and has an FCS error, only the RX Fragment Errors counter will be incremented.	20
RX Alignment Errors	Number of RX frames received with alignment errors.	20
RX Fragment Errors	Number of frames received that are < 64 bytes in size and have an FCS error or RX error. **Note:** If a frame is less than 64 bytes in length and has an FCS error, only the RX Fragment Errors counter will be incremented.	20
RX Jabber Errors	Number of frames received with a length greater than Maximum Frame Size (MAX_SIZE) and have FCS errors or RX errors. **Note:** The existence of extra bits does not trigger a jabber error. A jabber error requires at least one full byte beyond the value specified by the Maximum Frame Size (MAX_SIZE) to be received. **Note:** If a frame has a Jabber Error and FCS error, only the RX Jabber Errors counter will be incremented.	20

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TABLE 5-9: STATISTICS COUNTER DEFINITIONS (CONTINUED)

Name	Description	Size (Bits)
RX Undersize Frame Errors	Number of frames received with a length less than 64 bytes. No other errors have been detected in the frame.	20
RX Oversize Frame Errors	Number of frames received with a length greater than the programmed maximum Ethernet frame size (Maximum Frame Size (MAX_SIZE) field of the MAC Receive Register (MAC_RX)). No other errors have been detected in the frame. **Note:** The VLAN Frame Size Enforcement (FSE) bit allows for the maximum legal size to be increased by 4-bytes to account for a single VLAN tag or 8-bytes to account for stacked VLAN tags. **Note:** The MAC determines a VLAN tag is present if the type field is equal to 8100h or the value programmed in the VLAN Type Register (VLAN_TYPE). **Note:** The existence of extra bits does not trigger an oversize error. An oversize error requires at least one full byte beyond the value specified by the Maximum Frame Size (MAX_SIZE) to be received.	20
RX Dropped Frames	Number of RX frames dropped by the FCT due to insufficient room in the RX FIFO. **Note:** If a frame to be dropped has an Ethernet error, it will be counted in the relevant bad frame counter. The RX Dropped Frames counter will be incremented for the errored frame only if Store Bad Frames is set in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL).	20
RX Unicast Byte Count	Total number of bytes received from unicast frames without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted. **Note:** The per frame byte count does not include the VLAN TAG and VID if the Enable VLAN Tag Stripping bit is set in the Receive Filtering Engine Control Register (RFE_CTL). It does not include the FCS if the FCS Stripping bit is set in the MAC Receive Register (MAC_RX).	32
RX Broadcast Byte Count	Total number of bytes received from broadcast frames without errors. This counter does not count broadcast frames received when the Accept Broadcast Frames (AB) bit is deasserted. Frames that are discarded from FIFO overflow are not counted. **Note:** The per frame byte count does not include the VLAN TAG and VID if the Enable VLAN Tag Stripping bit is set in the Receive Filtering Engine Control Register (RFE_CTL). It does not include the FCS if the FCS Stripping bit is set in the MAC Receive Register (MAC_RX).	32

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TABLE 5-9: STATISTICS COUNTER DEFINITIONS (CONTINUED)

Name	Description	Size (Bits)
RX Multicast Byte Count	Total number of bytes received from multicast frames without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted. **Note:** The per frame byte count does not include the VLAN TAG and VID if the Enable VLAN Tag Stripping bit is set in the Receive Filtering Engine Control Register (RFE_CTL). It does not include the FCS if the FCS Stripping bit is set in the MAC Receive Register (MAC_RX).	32
RX Unicast Frames	Number of unicast frames received without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	20
RX Broadcast Frames	Number of broadcast frames received without errors. This counter does not count broadcast frames received when the Accept Broadcast Frames (AB) bit is deasserted. Frames that are discarded from FIFO overflow are not counted.	20
RX Multicast Frames	Number of multicast frames received without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	20
RX Pause Frames	Number of pause frames received without errors. **Note:** This counter records pause frames that failed address filtering.	20
RX 64 Byte Frames	Number of frames received with a length of 64 bytes without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	20
RX 65 - 127 Byte Frames	Number of frames received with a length between 65 bytes and 127 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
RX 128 - 255 Byte Frames	Number of frames received with a length between 128 bytes and 255 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
RX 256 - 511 Bytes Frames	Number of frames received with a length between 256 bytes and 511 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20

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TABLE 5-9: STATISTICS COUNTER DEFINITIONS (CONTINUED)

Name	Description	Size (Bits)
RX 512 - 1023 Byte Frames	Number of frames received with a length between 512 bytes and 1023 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
RX 1024 - 1518 Byte Frames	Number of frames received with a length between 1024 bytes and 1518 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
RX Greater 1518 Byte Frames	Number of frames received with a length greater than 1518 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
EEE RX LPI Transitions	Number of times that the LPI indication from the PHY changes from de-asserted to asserted. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. This counters is required to operate during SUSPEND0, SUSPEND3 and Normal Configured Power states.	32
EEE RX LPI Time	The amount of time, in micro-seconds, that the PHY indicates LPI. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. This counters is required to operate during SUSPEND0, SUSPEND3 and Normal Configured Power states.	32
TX FCS Errors	Number of frames transmitted with an FCS error. The MAC can be forced to transmit frames with FCS errors by setting the Bad FCS (BFCS) bit.	20
TX Excess Deferral Errors	Number of frames that were excessively deferred. The frame has been deferred for more than two max-sized frame times + 16 bytes. The maximum frame length is defined by Maximum Frame Size (MAX_SIZE) in MAC Receive Register (MAC_RX) **Note:** Defer time is not cumulative. If the transmitter defers for 10,000 bit times, then transmits, collides, backs off, and then has to defer again after completion of back-off, the deferral timer resets to 0 and restarts. **Note:** The 16 bytes of margin is to account for the possibility of double VLAN tags.	20
TX Carrier Errors	Number of frames that had a carrier sense error occur during transmission. This error is caused by no carrier or loss of carrier.	20
TX Bad Byte Count	Total number of bytes sent from errored transmissions.	32
TX Single Collisions	Number of frames successfully transmitted after a single collision occurs.	20
TX Multiple Collisions	Number of frames successfully transmitted after multiple collisions occur.	20

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TABLE 5-9: STATISTICS COUNTER DEFINITIONS (CONTINUED)

Name	Description	Size (Bits)
TX Excessive Collision	Number of transmitted frames aborted due to excessive collisions. **Note:** 16 collisions results in an excessive collisions.	20
TX Late Collisions	Number of transmitted frames aborted because of a late collision.	20
TX Unicast Byte Count	Total number of bytes transmitted by unicast frames without errors. This counter does not count flow control frames. Bytes transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	32
TX Broadcast Byte Count	Total number of bytes transmitted by broadcast frames without errors. This counter does not count flow control frames. Bytes transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	32
TX Multicast Byte Count	Total number of bytes transmitted by multicast frames without errors. This counter does not count flow control frames. Bytes transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	32
TX Unicast Frames	Number of unicast TX frames transmitted without errors. This counter does not count flow control frames.	20
TX Broadcast Frames	Number of broadcast TX frames transmitted without errors. This counter does not count flow control frames.	20
TX Multicast Frames	Number of multicast TX frames transmitted without errors. This counter does not count flow control frames.	20
TX Pause Frames	Number of successfully transmitted pause frames.	20
TX 64 Byte Frames	Number of frames transmitted with a length of 64 bytes without error. This counter does not count flow control frames. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	20
TX 65 - 127 Byte Frames	Number of frames transmitted with a length between 65 bytes and 127 bytes without error. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	20
TX 128 - 255 Byte Frames	Number of frames transmitted with a length between 128 bytes and 255 bytes without error. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	20
TX 256 - 511 Bytes Frames	Number of frames transmitted with a length between 256 bytes and 511 bytes without error. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	20

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TABLE 5-9: STATISTICS COUNTER DEFINITIONS (CONTINUED)

Name	Description	Size (Bits)
TX 512 - 1023 Byte Frames	Number of frames transmitted with a length between 512 bytes and 1023 bytes without error. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	20
TX 1024 - 1518 Byte Frames	Number of frames transmitted with a length between 1024 bytes and 1518 bytes without error. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	20
TX Greater 1518 Byte Frames	Number of frames transmitted with a length greater than 1518 bytes without error. Frames transmitted as part of a partial packet transmission (half-duplex collision) are not counted.	20
EEE TX LPI Transitions	Number of times that the LPI request to the PHY changes from de-asserted to asserted. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. This counter is required to operate during SUSPEND0, SUSPEND3 and Normal Configured Power states.	32
EEE TX LPI Time	The amount of time, in microseconds, that the PHY is requested to send LPI. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. This counters is required to operate during SUSPEND0, SUSPEND3 and Normal Configured Power states.	32

5.2.3 DESCRIPTOR RAM

The Control Endpoint manipulates an internal Descriptor RAM which stores various configuration for the device including USB descriptors. The descriptor RAM is typically loaded from either an external EEPROM or the integrated OTP. However a mechanism exists, EEPROM-less mode, which allows the host software to directly configure the Descriptor RAM. It is described in Section 10.6, "Customized Operation Without EEPROM". The Descriptor RAM format is discussed in Section 10.6.3, "Descriptor RAM Initialization"

The Control EP first evaluates whether an external EEPROM is present by the successful recognition of the EEPROM signature. If an EEPROM exists, it shall be used to load the contents into the Descriptor RAM.

If an EEPROM does not exist, the Control EP considers whether the OTP is configured. If the OTP is configured it shall be used to load the Descriptor RAM.

In the event that the EEPROM does not exist and the OTP is not configured, the Control EP shall utilize the CSR and EEPROM defaults, as defined in Section 10.5, "EEPROM Defaults", for configuring the device.

EEPROM-Less operation may be invoked by host software. This mode shall take priority over an external EEPROM or configured OTP. This mode is described in Section 10.6, "Customized Operation Without EEPROM".

5.3 Bulk In Endpoint

The Bulk In Endpoint is controlled by the UTX (USB Bulk In Transmitter). The UTX is responsible for encapsulating Ethernet data into USB Bulk In packets. Ethernet frames are retrieved from the FCT's RX FIFO and passed to the UDC. The UTX manages an 8 KB UTX FIFO Buffer. USB packets from FCT are temporarily stored there to facilitate efficient bursting. In support for bursting, a USB Command FIFO is managed by the UTX to track packet lengths.

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5.3.1 USB TX DATA FIFO

The UTX Data FIFO RAM is a 2K x 32 (8 KB) dual port type. All USB packets are DWORD aligned in the USB TX Data FIFO. All Ethernet frames are DWORD aligned in USB packets. Within a USB transfer (assuming MEF mode is enabled), consecutive Ethernet frames are not concatenated into the same DWORD. The unused bytes (up to 3) in the DWORD at the end of an Ethernet frame (assuming it is not the last frame) are included in the USB packet and its length and are discarded by the host driver software. At the end of a USB transfer, the unused bytes (up to 3) are not included in the USB packet or it's length. The USB Device Controller will discard any unused bytes within a DWORD.

5.3.2 USB TX COMMAND FIFO

As Ethernet frames are transferred into the USB TX Data FIFO, the resulting USB packet lengths (including any zero length packets) are written into the USB TX Command FIFO. The USB Device Controller requires the packet lengths and number of packets available at the start of a USB transmission.

The size of the USB command FIFO allows up to 32 packets to be queued. This number is based on the 8K byte size of the USB TX Data FIFO divided by an average USB packet size of 256 bytes (e.g. 16 @ 512 byte packets and 16 zero length packets, etc.). Since it is possible for the USB TX Command FIFO to fill before the USB TX Data FIFO, the USB TX Command FIFO provides a full signal.

The head entry (USB packet length) and depth (number of entries) of the USB TX Command FIFO are passed as the USB packet length and number of available packets, respectively, to the USB Device Controller.

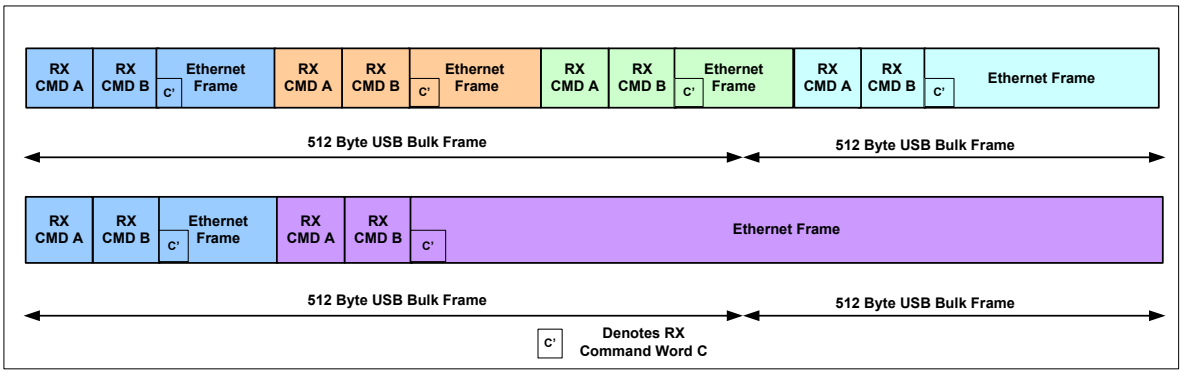
5.3.3 MEF/SEF OPERATION

The UTX supports the following two modes of operation: MEF and SEF, selected via the Multiple Ethernet Frames per USB Packet (MEF) bit of the Hardware Configuration Register (HW_CFG).

- MEF: Multiple Ethernet frames per Bulk In packet. This mode will maximize USB bus utilization by allowing multiple Ethernet frames to be packed into a USB packet. Frames greater than maximum USB packet size are split across multiple Bulk In packets.
- SEF: Single Ethernet frame per Bulk In packet. This mode will not maximize USB bus utilization, but simplifies the host software implementation and can potentially ease the burden on a low end Host processor. Frames greater than maximum USB packet size are split across multiple Bulk In packets.

Each Ethernet frame is pre-pended with three RX Command Words, RX Command A, RX Command B and RX Command C by the FCT. RX Command A contains the frame length that is used by the UTX to perform the encapsulation functions. The contents of the command words are generated by the MAC, RFE, and FCT.

FIGURE 5-1: MEF USB ENCAPSULATION



An Ethernet frame (starting with RX Command A) always begins on a DWORD boundary in the FCT. In MEF mode, UTX will not concatenate the end of the current frame and the beginning of the next frame into the same DWORD. Therefore, the last DWORD of an Ethernet frame may have unused bytes added to ensure DWORD alignment of the RX Command A of the next frame. The addition of pad bytes at the end of the frame depends on whether another frame is available for transmission after the current one. If the current frame is the last frame to be transmitted, no pad bytes will be added, as the USB protocol allows for termination of the packet on a byte boundary. If, however, another frame is available for transmission, the current frame will be padded out so that it ends on the DWORD boundary. This ensures the next frame to be transmitted, starting with RX Command A, will start on a DWORD boundary.

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Any unused bytes that were added to the last DWORD of a frame are not counted in the length field of RX Command A.

As noted in Section 5.3.1, UTX is responsible for storing USB packets into UTX Data FIFO. When calculating USB packet lengths DWORD padding between Ethernet frames is included.

In accordance with the USB protocol, UTX terminates a burst with either a ZLP or a Bulk In packet with a size of less than the Bulk In maximum packet size (512 for HS, 64 for FS). The ZLP is needed when the total amount of data transmitted is a multiple of a Bulk In maximum packet size. UTX monitors the UTX Data FIFO size to determine when a burst has ended.

The UTX monitors the RX FIFO size signal from the FCT and moves data into the UTX Data FIFO as complete Ethernet frames are received by the FCT and space is available. When the frame is moved its length is incorporated to packet length of the USB packet being formed. After a complete USB packet is created an entry is written into the UTX Command FIFO. If the Ethernet frame can not fit into the USB packet the remainder is moved into subsequent USB packet(s).

Note: In SEF mode, a ZLP is transmitted if the Ethernet frame is the same size as a maximum size Bulk In packet, or a multiple of the maximum Bulk In packet size.

The Host ignores unused bytes that exist in the last DWORD of an Ethernet frame.

When using SEF mode, there will never be any unused bytes added for end alignment padding. The USB transfer always ends on the last byte of the Ethernet frame.

If UTX receives a Bulk In token when the RX FIFO is empty, it will transmit a ZLP if Bulk-In Empty Response (BIR) is set otherwise it will NAK (FS/HS) or NRDY (SS) when cleared.

The UTX provides a mechanism for limiting the size of the USB burst per the burst cap function as described in Burst Cap Usage. This caps the amount of data that can be moved in a USB transfer before termination by a ZLP. The burst cap function applies for all operating speeds.

In order to more efficiently utilize USB bandwidth in MEF mode, the UTX has a mechanism for delaying the transmission of a short packet, or ZLP. This mode entails having the UTX wait a time defined by the Bulk-In Delay Register (BULK_IN_DLY) before terminating the burst. A value of zero in this register disables this feature. By default, a delay of 34 us is used.

After UTX transmits the last USB bMaxPacketSize packet in a burst, UTX enables an internal timer. When this timer is equal to Bulk In Delay, any Bulk In data in the UTX Data FIFO is transmitted upon next opportunity to the host.

In HS/FS mode, if enough data arrives before the timer elapses to build at least one maximum sized packet, then the UTX will transmit this packet when it receives the next Bulk In Token. After packet transmission, the UTX will reset its internal timer and delay the short packet, or ZLP, transmission until the Bulk In Delay time elapses or new data is received per above.

In the case where the UTX Data FIFO is empty and a single Ethernet packet less than USB bMaxPacketSize is then received, the UTX enables its internal timer. If enough data arrives before the timer elapses to build at least one maximum sized packet, the UTX will transmit this packet and reset the timer. Otherwise, FIFO data is sent after the timer expires.

In HS/FS mode, the UTX will NAK any Bulk In tokens while waiting for new data and Bulk In Delay to elapse.

Bulk In Delay is only intended for MEF operation and not appropriate for SEF mode.

5.3.4 USB ACKS AND RETRIES

In the case of an error condition, the UTX will issue a rewind to the FCT. This occurs when the UTX completes transmitting a Bulk In packet and does not receive an ACK from the Host. In this case, the next frame received by the UTX will be another In token and the Bulk In packet is retransmitted. When the ACK is finally received, the UTX notifies the FCT. The FCT will then advance the read head pointer to the next packet.

Both the USB TX Data and Command FIFOs handle USB retries. When a USB packet is acknowledged, its command information is popped from the USB TX Command FIFO and its storage can be release from the USB TX Data FIFO (note that zero length packets would not release any USB TX Data FIFO space).

Burst Cap Usage

The UTX, via the Burst Cap Register (BURST_CAP), is capable of prematurely terminating a burst. The Burst Cap Register (BURST_CAP) uses units of USB packet size (64/512/1024 bytes). To enable use of the Burst Cap register, the Burst Cap Enable (BCE) bit in the USB Configuration Register 0 (USB_CFG0) must be set.

For proper operation, the BURST_CAP field should be set by software so that the following relationships hold true:

For HS Operation, BURST_CAP * 512 >= Maximum Frame Size (MAX_SIZE)

For FS Operation, BURST_CAP * 64 >= Maximum Frame Size (MAX_SIZE)

Failure to set BURST_CAP values that obey the previous rules may result in untoward operation and may yield unpredictable results.

Note:	The first Ethernet frame of the burst is always sent without checking if it exceeds BURST_CAP.

Whenever Burst Cap enforcement is disabled and the RX FIFO, and UTX FIFO, are empty, the UTX will respond with a ZLP if Bulk-In Empty Response (BIR) = “0”. However, it will respond with NAK (FS/HS) when Bulk-In Empty Response (BIR) = “1”.

Whenever Burst Cap enforcement is enabled, the following holds:

- For HS Operation:
  $BURST_{Max}$ = BURST_CAP * 512
- For FS operation:
  $BURST_{Max}$ = BURST_CAP * 64

Let $BURST_{Cur}$ = Length of current burst = Summation of the lengths of frames in the current burst.

Let $LENGTH_{Next}$ = Length of the next frame available in the RX FIFO.

If the RX FIFO runs out of data, or a frame is available and $BURST_{Cur} + LENGTH_{Next} > BURST_{Max}$, then the burst is terminated with either a short USB packet or with a ZLP.

Otherwise, the next frame is able to fit in the current burst without exceeding BURST_CAP. The burst is continued and $BURST_{Cur}$ is incremented by $LENGTH_{Next}$.

Note:	If Store Bad Frames is set in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL), then the size of the transmitted burst may exceed the value specified by BURST_CAP. This can happen if an oversized frame is received that is larger than BURST_CAP. Ethernet frames are not fragmented across bursts when using Burst Cap Enforcement.

5.4 Bulk Out Endpoint

The Bulk Out Endpoint is controlled by the URX (USB Bulk Out Receiver). URX is responsible for receiving Ethernet data encapsulated over USB Bulk Out packet(s). Unlike the UTX, the URX does not explicitly track Ethernet frames. It views all received packets purely as USB data. The extraction of Ethernet frames is handled by the FCT. The URX always simultaneously supports MEF and SEF modes.

5.4.1 USB RX DATA FIFO

The URX manages an 8 KB Data FIFO. All USB packets start on DWORD boundaries. The format of the data within USB packets and across USB transactions ensures that Ethernet frames (including command headers) are DWORD aligned. Padding between Ethernet frames is added by the host driver and stripped by the TX FIFO.

5.4.2 RETRIES AND ERRORS

Packets from the USB Device Controller have the possibility of an error and subsequent retry. Based on the status of the packet, the packet may be either rejected or accepted. If the packet is rejected, the write pointers and free space is recovered from the data FIFO. If the packet is accepted, it can be made available to the FCT. Packet rejection or acceptance will occur before the start of the next packet, such that multiple outstanding packets need not be tracked.

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The FCT notifies the URX when it detects loss of sync. When this occurs, the URX stalls the Bulk Out pipe via the UDC. This is an appropriate response, as loss of sync is a catastrophic error (which can only be caused by a host software error. See Section 6.2.4, "TX Error Detection"). This behavior is configurable via the Stall Bulk-Out Pipe Disable (SBP) bit in the USB Configuration Register 0 (USB_CFG0).

5.5 Interrupt Endpoint

The Interrupt endpoint is responsible for indicating the device's status at each polling interval. The Interrupt endpoint is implemented via the CTL module. When the endpoint is accessed the following fields are presented to the host.

5.5.1 INTERRUPT PACKET FORMAT

TABLE 5-10: INTERRUPT PACKET FORMAT

Bits	Description
31:29	Reserved
28	OTP_WR_DONE_INT
27	Reserved
26	EEE_START_TX_LPI_INT
25	EEE_STOP_TX_LPI_INT
24	EEE_RX_LPI_INT
23	MACRTO_INT
22	RDFO_INT
21	TXE_INT
20	USB_STS_INT
19	TX_DIS_INT
18	RX_DIS_INT
17	PHY_INT
16	DP_INT
15	MAC_ERR_INT
14	TDFU
13	TDFO
12	UTX_FP
11:0	GPIOx_INT

If there is no interrupt status to report the device responds with a NAK unless Interrupt Endpoint Always On (INTEP_ON) in Interrupt Endpoint Control Register (INT_EP_CTL) is set in which case an interrupt packet of 0x0 is returned.

Note:	The polling interval is static and set through OTP or EEPROM. The polling interval can be changed by the host updating the contents of the EEPROM and resetting the part.

For an interrupt event to be reported via the Interrupt endpoint, the respective bit must be enabled in Interrupt Endpoint Control Register (INT_EP_CTL). The interrupt status can be cleared by writing to the Interrupt Status Register (INT_STS).

5.5.2 USB STATUS

USB_STS_INT bit is used to facilitate communication with the host software regarding OS programming of the device. The following are tracked by this mechanism.

- SET Select (SET_SEL) command issued
- Function Remote Wakeup Status
- Device Remote Wakeup Status

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The USB Status Register (USB_STATUS) includes both status change bits as well as the current value of the respective when appropriate.

APPLICATION NOTE: The majority of the above status information can also be obtained using the GET_STATUS USB request.

5.6 LPM Support

The USB device controller supports Link Power Management (LPM). It is fully capable of responding to LPM devices and placing the device into the L1 and L2 states or conversely moving the device to L0 via remote wakeup or Resume signaling.

Further details on LPM implementation can be found in Section 13.0, "Clocks and Power Management (CPM)," on page 124.

LPM is enabled by setting the LPM Capability (LPM_CAP) bit in USB Configuration Register 0 (USB_CFG0).

5.6.1 LPM L1

In L1 minimal components are powered down in order to ensure the device can quickly transition to L0 and not violate the pertinent USB specification parameters.

The device shall automatically transition the link from L1 to L0 after it receives a frame which passes any programmed filters in the RFE and MAC. Additionally, a scheduled interrupt EP packet shall also cause the device to transition out of L0.

5.6.2 LPM L2

The L2 state mimics the respective suspend mode programmed in the Suspend Mode (SUSPEND_MODE) of the Power Management Control Register (PMT_CTL).

5.7 USB Descriptors

In the event that the OTP is not configured or an external EEPROM is not available, the default values defined in the descriptor tables below are used - except in the case where EEPROM-less mode is enabled. In that case, the descriptors are programmed as defined in Section 10.6, "Customized Operation Without EEPROM".

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5.7.1 DEVICE DESCRIPTOR

The Device Descriptors are initialized based on values stored in OTP or EEPROM. Table 5-11 shows the default Device Descriptor values. These values are used for Full-Speed and High-Speed operation.

TABLE 5-11: DEVICE DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	12h	Note 5-1	Size of the Descriptor in Bytes (18 bytes)
01h	bDescriptorType	1	01h	Note 5-1	Device Descriptor (0x01)
02h	bcdUSB	2	Note 5-2	Yes	USB Specification Number which device complies to
04h	bDeviceClass	1	FFh	Yes	Class Code
05h	bDeviceSubClass	1	00h	Yes	Subclass Code
06h	bDeviceProtocol	1	FFh	Yes	Protocol Code
07h	bMaxPacketSize	1	Note 5-3	Yes	Maximum Packet Size for Endpoint 0
08h	IdVendor	2	0424h	Yes	Vendor ID
0Ah	IdProduct	2	7850h	Yes	Product ID
0Ch	bcdDevice	2	Note 5-4	Yes	Device Release Number
0Eh	iManufacturer	1	00h	Yes	Index of Manufacturer String Descriptor
0Fh	iProduct	1	00h	Yes	Index of Product String Descriptor
10h	iSerialNumber	1	00h	Yes	Index of Serial Number String Descriptor
11h	bNumConfigurations	1	01h	Note 5-5	Number of Possible Configurations

Note 5-1 The descriptor length and descriptor type for Device Descriptors specified in OTP or EEPROM are “don’t cares” and are always overwritten by hardware as 0x12 and 0x01, respectively.

Note 5-2 When operating in USB 2.0 mode the default value is 0210h (USB 2.10).

Note 5-3 When operating in full-speed or high-speed mode it should be set to 40h. If the OTP is not configured, or EEPROM is not present, the aforementioned values are returned.

Note 5-4 Default value is dependent on device release. The MSB matches the device release and the LSB is hard-coded to 00h. The initial release value is 01h. Subsequent versions will increment the value.

Note 5-5 Value is loaded from OTP, or EEPROM, but must be equal to the Default Value in order to comply with the USB Specification and provide for normal device operation. Specification of any other value will result in unwanted behavior and untoward operation.

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5.7.2 CONFIGURATION DESCRIPTOR

The Configuration Descriptor is initialized based on values stored in OTP or EEPROM. Table 5-12 shows the default Configuration Descriptor values. These values are used for Full-Speed and High-Speed operation.

TABLE 5-12: CONFIGURATION DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	09h	Note 5-6	Size of the Configuration Descriptor in bytes (9 bytes)
01h	bDescriptorType	1	02h	Note 5-7	Configuration Descriptor (0x02)
02h	wTotalLength	2	Note 5-8	Note 5-6	Total length in bytes of data returned
04h	bNumInterfaces	1	01h	Note 5-6	Number of Interfaces
05h	bConfigurationValue	1	01h	Note 5-6	Value to use as an argument to select this configuration
06h	iConfiguration	1	00h	Yes	Index of String Descriptor describing this configuration
07h	bmAttributes	1	E0h	Yes	Self powered and remote wakeup enabled.
08h	bMaxPower	1	Note 5-9	Yes	Maximum Power Consumption

Note 5-6 Value is loaded from OTP, or EEPROM, but must be equal to the Default Value in order to provide for normal device operation. Specification of any other value will result in unwanted behavior and untoward operation.

Note 5-7 The descriptor type for Configuration Descriptors specified in OTP, or EEPROM, is a “don’t care” and is always overwritten by hardware as 0x02.

Note 5-8 Default value is 0027h (39 bytes) when operating in USB 2.0 mode.

Note 5-9 Default value is 01h in Self Powered mode. In Bus Powered mode, default value is FAh (500mA).

Note: The Configuration Flags of the OTP, or EEPROM, may affect the default value of bmAttributes.

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5.7.3 INTERFACE DESCRIPTOR DEFAULT

Table 5-13 shows the default value for Interface Descriptor 0. This descriptor is initialized based on values stored in OTP or EEPROM.

TABLE 5-13: INTERFACE DESCRIPTOR 0

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	09h	Note 5-10	Size of Descriptor in Bytes (9 Bytes
01h	bDescriptorType	1	04h	Note 5-10	Interface Descriptor (0x04)
02h	bInterfaceNumber	1	00h	Note 5-10	Number identifying this Interface
03h	bAlternateSetting	1	00h	Note 5-10	Value used to select alternative setting
04h	bNumEndpoints	1	03h	Note 5-10	Number of Endpoints used for this interface (Less endpoint 0)
05h	bInterfaceClass	1	FFh	Yes	Class Code
06h	bInterfaceSubClass	1	00h	Yes	Subclass Code
07h	bInterfaceProtocol	1	FFh	Yes	Protocol Code
08h	iInterface	1	00h	Yes	Index of String Descriptor Describing this interface

Note 5-10 Value is loaded from OTP or EEPROM, but must be equal to the Default Value in order to comply with the USB Specification and provide for normal device operation. Specification of any other value will result in unwanted behavior and untoward operation.

5.7.4 ENDPOINT 1 DESCRIPTOR (BULK-IN)

Table 5-14 shows the default value for Endpoint Descriptor 1. This descriptor is not initialized from values stored in OTP or EEPROM.

TABLE 5-14: ENDPOINT 1 DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM	DESCRIPTION
00h	bLength	1	07h	No	Size of Descriptor in bytes
01h	bDescriptorType	1	05h	No	Endpoint Descriptor
02h	bEndpointAddress	1	81h	No	Endpoint Address
03h	bmAttributes	1	02h	No	Bulk Transfer Type
04h	wMaxPacketSize	2	Note 5-11	No	Maximum Packet Size this endpoint is capable of sending.
06h	bInterval	1	00h	No	Interval for polling endpoint data transfers. Ignored for bulk endpoints.

Note 5-11 64 bytes for full-speed mode, 512 bytes for high-speed mode.

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5.7.5 ENDPOINT 2 DESCRIPTOR (BULK-OUT)

Table 5-14 shows the default value for Endpoint Descriptor 2. This descriptor is not initialized from values stored in OTP or EEPROM.

TABLE 5-15: ENDPOINT 1 DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	07h	No	Size of Descriptor in bytes
01h	bDescriptorType	1	05h	No	Endpoint Descriptor
02h	bEndpointAddress	1	02h	No	Endpoint Address
03h	bmAttributes	1	02h	No	Bulk Transfer Type
04h	wMaxPacketSize	2	Note 5-12	No	Maximum Packet Size this endpoint is capable of sending.
06h	bInterval	1	00h	No	Interval for polling endpoint data transfers. Ignored for bulk endpoints.

Note 5-12 64 bytes for full-speed mode, 512 bytes for high-speed mode

5.7.6 ENDPOINT 3 DESCRIPTOR (INTERRUPT)

Table 5-16 shows the default value for Endpoint Descriptor 3. Only the bInterval field of this descriptor is initialized from OTP or EEPROM.

TABLE 5-16: ENDPOINT 2 DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	07h	No	Size of Descriptor in bytes
01h	bDescriptorType	1	05h	No	Endpoint Descriptor
02h	bEndpointAddress	1	83h	No	Endpoint Address
03h	bmAttributes	1	03h	No	Interrupt Transfer Type
04h	wMaxPacketSize	2	10h	No	Maximum Packet Size this endpoint is capable of sending.
06h	bInterval	1	Note 5-13	Yes	Interval for polling endpoint data transfers.

Note 5-13 This value is loaded from OTP, or EEPROM. A full-speed and high-speed polling interval exists. If OTP is not configured, and EEPROM does not exist, then this value defaults to 04h for HS, 01h for FS.

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5.7.7 OTHER SPEED CONFIGURATION DESCRIPTOR

The fields in this descriptor are derived from Configuration Descriptor information that is stored in OTP or EEPROM.

TABLE 5-17: OTHER SPEED CONFIGURATION DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	09h	Note 5-14	Size of Descriptor in bytes (9 bytes)
01h	bDescriptorType	1	07h	No	Other Speed Configuration Descriptor (0x07)
02h	wTotalLength	2	0027h	Note 5-14	Total length in bytes of data returned (39 bytes)
04h	bNumInterfaces	1	01h	Note 5-14	Number of Interfaces
05h	bConfigurationValue	1	01h	Note 5-14	Value to use as an argument to select this configuration
06h	iConfiguration	1	00h	Yes	Index of String Descriptor describing this configuration
07h	bmAttributes	1	E0h	Yes	Bus powered and remote wakeup enabled.
08h	bMaxPower	1	Note 5-15	Yes	Maximum Power Consumption

Note 5-14 Value is loaded from OTP or EEPROM, but must be equal to the Default Value in order to comply with the USB 2.x Specification and provide for normal device operation. Specification of any other value will result in unwanted behavior and untoward operation.

Note 5-15 Default value is 01h in Self Powered mode and FAh (500 mA) in Bus Powered mode.

Note: OTP or EEPROM values are obtained for the Configuration Descriptor at the other USB speed. I.e., if the current operating speed is FS, then the HS Configuration Descriptor values are used, and vice-versa.

The Configuration Flags of the OTP, or EEPROM, may affect the default value of bmAttributes

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5.7.8 DEVICE QUALIFIER DESCRIPTOR

The fields in this descriptor are derived from Device Descriptor information that is stored in the OTP or EEPROM.

TABLE 5-18: DEVICE QUALIFIER DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	0Ah	No	Size of Descriptor in bytes (10 bytes)
01h	bDescriptorType	1	06h	No	Device Qualifier Descriptor (0x06)
02h	bcdUSB	2	0210h	Yes	USB Specification Number which device complies to.
04h	bDeviceClass	1	FFh	Yes	Class Code
05h	bDeviceSubClass	1	00h	Yes	Subclass Code
06h	bDeviceProtocol	1	FFh	Yes	Protocol Code
07h	bMaxPacketSize0	1	40h	Note 5-16	Maximum Packet Size
08h	bNumConfigurations	1	01h	Note 5-16	Number of Other-Speed Configurations
09h	Reserved	1	00h	No	Must be zero

Note 5-16 .Value is loaded from OTP or EEPROM, but must be equal to the Default Value in order to comply with the USB 2.x Specification and provide for normal device operation.

Note: OTP or EEPROM values are from the Device Descriptor (including any EEPROM override) at the opposite HS/FS operating speed. I.e., if the current operating speed is HS, then Device Qualifier data is based on the FS Device Descriptor, and vice-versa.

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5.7.9 STRING DESCRIPTORS

5.7.9.1 String Index = 0 (LANGID)

TABLE 5-19: LANGID STRING DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	04h	No	Size of LANGID Descriptor in bytes (4 bytes)
01h	bDescriptorType	1	03h	No	String Descriptor (0x03)
02h	LANGID	2	None	Yes	Must be set to 0x0409 (US English).

Note: If there is no valid/enabled OTP or EEPROM, or if all string lengths in the OTP or EEPROM are 0, then there are no strings, so any Host attempt to read the LANGID string will return stall in the Data Stage of the Control Transfer.

If there is a valid/enabled OTP or EEPROM, and if at least one of the string lengths is not 0, then the value contained at addresses 0x23-0x24 shall be returned. These must be 0x0409 to allow for proper device operation.

Note: The device ignores the LANGID field in Control Read's of Strings, and will return the String (if it exists), regardless of whether the requested LANGID is 0x0409 or not.

5.7.9.2 String Indices 1-5

TABLE 5-20: STRING DESCRIPTOR (INDICES 1-5)

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	none	Yes	Size of the String Descriptor in bytes
01h	bDescriptorType	1	none	Yes	String Descriptor (0x03)
02h	Unicode String	2*N	none	Yes	2 bytes per unicode character, no trailing NULL.

Note: If there is no valid/enabled OTP or EEPROM, or if the corresponding String Length and offset for a given string index is zero, then that string does not exist, so any Host attempt to read that string will return stall in the Data Stage of the Control Transfer.

The device returns whatever bytes are in the designated OTP or EEPROM area for each of these strings. It is the responsibility of the OTP or EEPROM programmer to correctly set the bLength and bDescriptorType fields in the descriptor consistent with the byte length specified in the corresponding EEPROM locations.

5.7.10 BINARY DEVICE OBJECT STORE DESCRIPTOR

The Binary Device Object Store Descriptor is initialized based on values stored in OTP or EEPROM. Table 5-21 shows the default Binary Device Object Store Descriptor values.

TABLE 5-21: BINARY DEVICE OBJECT STORE DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	05h	Note 5-17	Size of Descriptor in bytes (5 bytes)
01h	bDescriptorType	1	0Fh	Note 5-17	BOS Descriptor (0x0F)
02h	wTotalLength	2	0016h	Yes	Total length of this descriptor and its sub-descriptors. (22 bytes)
04h	bNumDeviceCaps	1	02h	Yes	Number of Device Capability Descriptors in this BOS.

Note 5-17 The descriptor length and descriptor type for Binary Device Object Store Descriptors specified in OTP or EEPROM are “don’t cares” and are always overwritten by hardware as 0x05 and 0x0F, respectively.

5.7.11 USB 2.0 EXTENSION DESCRIPTOR

The USB 2.0 Extension Descriptor is initialized based on values stored in EEPROM. Table 5-22 shows the default USB 2.0 Extension Descriptor values.

TABLE 5-22: USB 2.0 EXTENSION DESCRIPTOR

OFFSET	FIELD	SIZE (BYTES)	DEFAULT VALUE	LOADED FROM EEPROM/ OTP	DESCRIPTION
00h	bLength	1	07h	Note 5-18	Size of Descriptor in bytes (7 bytes)
01h	bDescriptorType	1	10h	Note 5-18	Device Capability Descriptor (0x10)
02h	bDevCapabilityType	1	02h	Note 5-18	USB 2.0 Extension Capability (0x02)

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TABLE 5-22: USB 2.0 EXTENSION DESCRIPTOR (CONTINUED)

<table>
<tr><th>OFFSET</th><th>FIELD</th><th>SIZE (BYTES)</th><th>DEFAULT VALUE</th><th>LOADED FROM EEPROM/ OTP</th><th>DESCRIPTION</th></tr>
<tr><td>03h</td><td>bmAttributes</td><td>4</td><td>0006h</td><td>Yes</td><td>Bitmap encoding of number of supported device level features. A value of 1 in a bit location indicates a feature is supported. A value of 0 indicates it is not supported. Encodings are:
<table>
<tr><th>BIT</th><th>ENCODING</th></tr>
<tr><td>31:16</td><td>RESERVED (0)</td></tr>
<tr><td>15:12</td><td>Recommended Deep BESL value. Field shall be ignored by system software if bit[4] is zero.</td></tr>
<tr><td>11:8</td><td>Recommended Baseline BESL value. Field shall be ignored by system software if bit[3] is zero.</td></tr>
<tr><td>4</td><td>Recommended deep BESL valid.</td></tr>
<tr><td>3</td><td>Recommended baseline BESL valid.</td></tr>
<tr><td>2</td><td>BESL & Alternate HIRD definitions supported. The LPM bit must be set to a one when this bit is a one.</td></tr>
<tr><td>1</td><td>(LPM) Note 5-19
A value of 1 in this bit position indicates that this device supports the Link Power Management protocol.</td></tr>
<tr><td>0</td><td>RESERVED (0)</td></tr>
</table>
</td></tr>
</table>

Note 5-18 The descriptor length, descriptor type, and device capability type for USB 2.0 Extension Descriptors specified in OTP or EEPROM are “don’t cares” and are always overwritten by hardware as 0x07, 0x10, and 0x02, respectively.

Note 5-19 The value of this bit must match that of the LPM Capable (CFG0_LPM_CAPABLE) flag contained in Configuration Flags 0 of the OTP or EEPROM, if present. If the bit values disagree, unexpected results and untoward operation may result.

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6.0 FIFO CONTROLLER (FCT)

The FIFO controller uses internal RAMs to buffer RX and TX traffic. Bulk-Out packets from the URX are directly stored into the FCT TX FIFO. The FCT is responsible for extracting Ethernet frames from the USB packet data and passing the frames to the MAC.

Received Ethernet Frames are stored into the FCT RX FIFO and become the basis for bulk-in packets. The FCT passes the stored data to the UTX in blocks typically 1024, 512 or 64 bytes in size, depending on the current USB operating speed.

6.1 RX Path (Ethernet to USB)

The 12 KB RX FIFO buffers Ethernet frames received from the RFE. The UTX extracts these frames from the FCT to form USB Bulk In packets. Host software will ultimately reassemble the Ethernet frames from the USB packets.

FCT manages the writing of data into the RX FIFO through the use of two pointers - the rx_wr_ptr and the rx_wr_hd_ptr. The rx_wr_ptr is used to write Ethernet frame data into the FIFO. The rx_wr_hd_ptr points to two locations prior to the first FIFO location that holds frame data. The two DWORD space is used to write RX Command A and RX Command B upon completion of frame reception. Additionally, each Ethernet frame includes RX Command C which resides in the same DWORD that includes the first two bytes of frame data. The command words include information about the frame and status provided by the MAC, RFE, and FCT.

The rx_rd_ptr is used for reading data from the FIFO and passing it to the UTX. In order to support rewinds, the rx_rd_hd_ptr exists, as discussed in Section 6.1.1, "RX Error Detection". After an Ethernet frame is successfully read from the FIFO, the rx_rd_hd_ptr advances to point to the start of the next frame. Figure 6-1 illustrates how a frame is stored in the FIFO, along with pointer usage.

When the RFE signals that it has Data ready, the RFE controller starts passing the RX packet data to the FCT. The FCT updates the RX FIFO pointers as the data is written into the FIFO. The last information written into the FIFO are the Command Words.

Note:	RX Command C also serves the purpose of DWORD aligning the Ethernet frame TCP, IP and other protocol headers.

The RX FCT operates in store and forward mode. A received Ethernet frame is not visible to the UTX until the complete frame, including the Command Words, has been written into the RX FIFO. This is due to the fact that the frame may have to be removed via a rewind (pointer adjustment), in case of an error. Such is the case when a FIFO overflow condition is detected as the frame is being received. The FCT may be configured to discard errored frames and filtered frames through the use of a rewind operation. The automatic discard of errored and filtered frames is enabled/disabled by the Store Bad Frames bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL). Please refer to Section 6.1.1, "RX Error Detection," on page 43 for further details concerning errors which may result in the FCT performing rewind operation.

The FCT provides the UTX with an indication of how much data is available in the RX FIFO. This information is reflected in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL). In addition, internal signaling is used to inform the UTX that at least one entire frame has been received.

A RX FIFO overflow condition may be signaled via the RX Data FIFO Overflow Interrupt (RDFO_INT). The FCT RX Overflow bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) is also asserted when an overflow has occurred.

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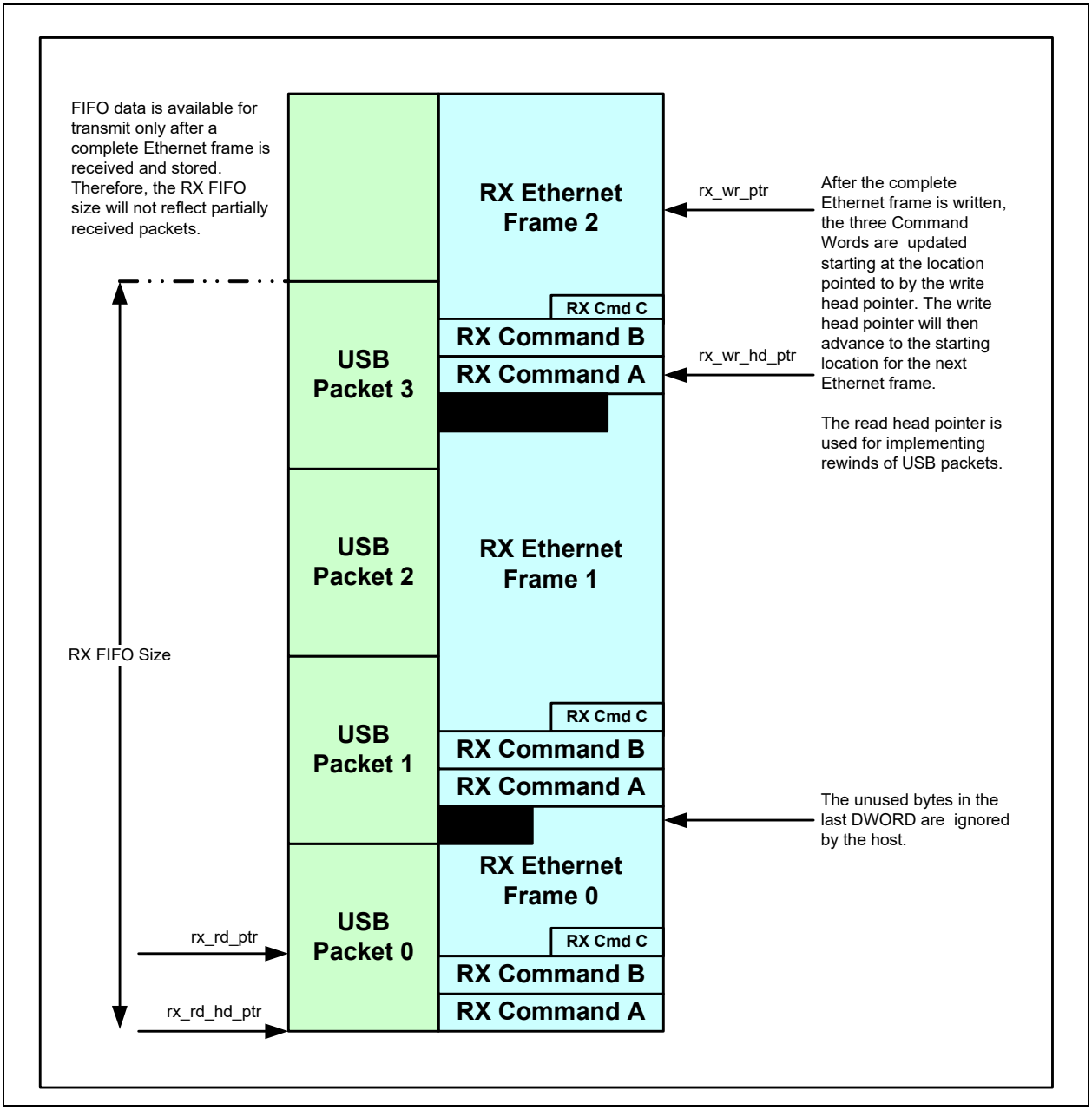
FIGURE 6-1: RX FIFO STORAGE



6.1.1 RX ERROR DETECTION

The FCT can be configured to drop Ethernet frames when certain error conditions occur. The setting of the Store Bad Frames bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) determines if the frame will be retained or dropped. Error conditions are indicated in RX Command A. Please refer to Table 5-9, “Statistics Counter Definitions,” on page 22 for more details on the error conditions tracked by the device.

Note:	The disposition of frames having checksum errors (IP/TCP/UDP) is not affected by Store Bad Frames. These frames are always passed to the Host Controller.

The FCT also drops frames when it detects a FIFO overflow condition. This occurs when the FIFO full condition occurs while a frame is being received. The FCT also maintains a count of the number of times a FIFO overflow condition has occurred.

Dropping an Ethernet frame is implemented by rewinding the received frame. A write side rewind is implemented by setting the rx_wr_ptr to be equal to the rx_wr_hd_ptr. Similarly, a read side rewind is implemented by setting the rx_rd_ptr to be equal to the rx_rd_hd_ptr.

For the case where the frame is dropped due to overflow, the FCT ignores the remainder of the frame. It will not begin writing into the RX FIFO again until the next frame is received.

In the read direction, the FCT also supports rewinds for the UTX. This is needed for the case where the USB Bulk Out packet is not successfully received by the Host and needs to be retransmitted.

6.1.2 RX COMMAND FORMAT

Every received Ethernet frame has Command Words concatenated to it that provide information about the frame. Table 6-1, "RX Command A", Table 6-2, "RX Command B" and Table 6-3, "RX Command C" define the contents of the Command Words.

RX Command A contains the frame length and has various status bits in regards to the frame. RX Command B provides the raw layer 3 checksum if enabled and the VLAN tag, if applicable. The raw checksum can be used to assist in the verification of checksums in unsupported layer 3 protocols. RX Command C provides additional information required for wakeup support.

TABLE 6-1: RX COMMAND A

BITS	SYMBOL	DESCRIPTION
31	ICE	**IP Checksum Error** When set, this bit indicates an error was detected in the IP checksum. **Note:** This field does not apply for IPv6 packets.
30	TCE	**TCP/UDP/ICMP/IGMP Checksum Error** When set, this bit indicates an error was detected in the TCP, UDP, ICMP or IGMP checksum.
29	IPV	**IP Version** When set, indicates the frame contains an IPv6 packet. Otherwise, the frame contains an IPv4 packet. **Note:** This field is not valid if the Protocol ID is set to 00b.
28:27	PID	**Protocol ID** Indicates the L3/L4 protocol of the received packet. 00b - None IP 01b - TCP and IP 10b - UDP and IP 11b - IP **Note:** 11b shall be used for ICMP and IGMP packets.
26	PFF	**Perfect Filter Passed** When set, this bit indicates the frame passed a perfect filter match of the MAC destination address. If this bit is not set, then the frame was passed due to the hash filter and needs to be further analyzed by the Host.
25	BAM	**Broadcast Frame** When set, this bit indicates that the received frame has a Broadcast address. **Note:** If the destination MAC address is 0xFFFF_FFFF_FFFF then the address is broadcast.

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TABLE 6-1: RX COMMAND A (CONTINUED)

BITS	SYMBOL	DESCRIPTION
24	MAM	**Multicast Frame** When set, this bit indicates that the received frame has a Multicast address. **Note:** If the least significant bit of the most significant byte of the destination MAC address is 1b, then the address is multicast. This bit is not set for a broadcast address.
23	FVTG	**Frame is VLAN tagged** When set, this bit indicates a VLAN tag was extracted from the frame. The tag is stored in the VLAN Tag field of RX Command B.
22	RED	**Receive Error Detected** When set, this bit indicates that an error was found in the received frame. One or more of the following fields will be set: FCS, ALN, RXE, LONG, RUNT, RWT, ICE, TCE.
21	RWT	**Receive Watchdog Timer Expired** When set, this bit indicates the received frame was longer than 11,264 bytes and was truncated by the MAC.
20	RUNT	**Short/Runt Frame** When set, this bit indicates that frame was prematurely terminated before the collision window (64 bytes). Runt frames are passed on to the Host only if the Store Bad Frames bit is set in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL). This bit is also set when a short frame has been received.
19	LONG	**Frame Too Long** When set, this bit indicates that the frame length exceeds the size specified in the Maximum Frame Size (MAX_SIZE) field of the MAC Receive Register (MAC_RX). This is only a frame too long indication and will not cause the frame reception to be truncated.
18	RXE	**RX Error** When set, this bit indicates that a receive error (internal PHY RX error signal asserted) was detected during frame reception.
17	ALN	**Alignment Error** When set, this bit indicates that the frame contained a non-integer multiple of 8 bits and the frame had an FCS Error. **Note:** Valid only for 10/100 mode.
16	FCS	**FCS Error** When set, this bit indicates that a FCS error was detected. This bit is also set when the internal PHY RX error signal is asserted during the reception of a frame even though the FCS may be correct. This bit is not valid if the received frame is a Runt frame or the Receive Watchdog Timer Expired.
15	UAM	**Unicast Frame** When set, this bit indicates that the received frame has a Unicast address.
14	ICSM	**Ignore TCP/UDP/ICMP/IGMP Checksum** When set, this bit indicates that the hardware was unable to calculate a UDP, TCP, ICMP or IGMP checksum for the packet. This implies that the value of TCE is “don’t care”.
13:0	LEN	**Frame Length** The size, in bytes, of the corresponding received frame. Size of the frame received from the network. **Note:** If the FCS Stripping bit of the MAC Receive Register (MAC_RX) is enabled, this value is decremented by four bytes.

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TABLE 6-2: RX COMMAND B

BITS	SYMBOL	DESCRIPTION
31:16	CSUM	**Raw L3 Checksum** This field contains the checksum computed for the frame over the L3 packet.
15:0	VTAG	**VLAN Tag** When the Frame is VLAN tagged bit is set, this field contains the frame's VLAN tag. Otherwise the contents of this field are undefined. [15:13] - PRI [12] - CFI [11:0] - VID

TABLE 6-3: RX COMMAND C

BITS	SYMBOL	DESCRIPTION
15	WAKE	**Wakeup Frame Received** When set, this field indicates that the corresponding frame is identified as the wakeup frame which cause remote wakeup over USB. This bit only has meaning when SUSPEND3 is used and Store Wakeup Frame (STORE_WAKE) is set.
14	RFE_FAIL	**RFE Filter Fail** When set, this field indicates that the received wakeup frame did not pass RFE filter rules. This bit only has meaning when both Always Pass Wakeup Frame (PASS_WKP) and Store Wakeup Frame (STORE_WAKE) are set and the device is in SUSPEND3. **Note:** This bit should never be set when Wakeup Frame Received is not set. It is not possible for a non-wake up frame to fail RFE filtering and still be transmitted to the host as they would have been discarded by the FCT RX FIFO.
13:0	-	**Reserved**

APPLICATION NOTE: It is possible for a received wakeup frame to cause a USB remote wakeup but not pass the filtering rules programmed in the RFE. In order to obviate the need for system software to implement the RFE filtering rules on a received wakeup frame, the RFE Filter Fail bit has been provided. This serves as an additional condition for dropping a frame such as ICE or TCE in RX Command A.

APPLICATION NOTE: Due to race conditions relating to when the device suspends relative to the reception of received data frames, the wakeup frame may have frame(s) preceding it in the FIFO. A pathological worst case can exist in which the RX FIFO is completely filled with data frames and drops the wakeup frame due to FIFO overflow error.

6.1.3 FLUSHING THE RX FIFO

The device allows for the Host to the flush the entire contents of the FCT RX FIFO. When a flush is activated, the read and write pointers of the RX FIFO are returned to their reset state.

Before flushing the RX FIFO, the device's receiver must be stopped, as specified in Section 6.1.3.1. Once the receiver stop completion is confirmed, the FCT RX Enable is cleared in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) to stop RX FIFO operation. The FCT RX Disabled bit and the RX Disabled Interrupt (RX_DIS_INT) (if enabled)

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assert when the RX FIFO hardware has completed the disabling process. The FCT RX RESET bit can then be set in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) to initiate the flush operation. This bit is cleared by the hardware when the flush operation has completed.

Note: RX Disabled Interrupt (RX_DIS_INT) will persist until the FCT RX Disabled status bit is cleared. The Receiver Disabled (RXD) status bit in the MAC Receive Register (MAC_RX) must also be cleared in order for RX_DIS_INT to de-assert. The RX Disabled Interrupt (RX_DIS_INT) is set in the Interrupt Status Register (INT_STS) and is also visible to the Host via the Interrupt Endpoint.

After the RX FIFO has been flushed, the receiver may be restarted, as specified in Section 6.1.3.1. RX FIFO operation may then be restarted by asserting the FCT RX Enable bit.

6.1.3.1 Stopping and Starting the Receiver

To stop the receiver, the Host must clear the Receiver Enable (RXEN) bit in the MAC Receive Register (MAC_RX). When the receiver is halted, the Receiver Disabled (RXD) bit and the RX Disabled Interrupt (RX_DIS_INT) (if enabled) will assert. Once stopped, the host software shall flush the RX FIFO. The Host must re-enable the receiver by setting the Receiver Enable (RXEN) bit.

Note: RX Disabled Interrupt (RX_DIS_INT) will persist until the Receiver Disabled (RXD) status bit is cleared. The FCT RX Disabled status bit in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) must also be cleared in order for RX_DIS_INT to de-assert. The RX Disabled Interrupt (RX_DIS_INT) is set in the Interrupt Status Register (INT_STS) and is also visible via the Interrupt Endpoint.

6.1.3.2 Flow Control

The FCT supports 802.3 flow control. The FCT can trigger the MAC to transmit a pause frame based upon programmable FIFO thresholds.

The FCT provides flow control on and flow control off signals to the MAC. These signals are asserted based upon the amount of data stored in the RX FIFO and the contents of the FCT Flow Control Threshold Register (FCT_FLOW).

When the amount of FIFO data exceeds the value specified by Flow Control On Threshold field of the FCT Flow Control Threshold Register (FCT_FLOW), the internal flow control on signal is asserted. The MAC may then (depending on the setting of the TX Flow Control Enable (TX_FCEN) of the Flow Control Register (FLOW)) transmit a Pause frame to instruct its link partner to halt transmission.

At some point in the future, the amount of FIFO data will fall below the value specified by Flow Control Off Threshold field of the FCT Flow Control Threshold Register (FCT_FLOW). This, in turn, causes the internal flow control off signal to the MAC to assert. The MAC may then (depending on the setting of TX_FCEN) transmit a Pause frame with a value of zero. Upon reception of the pause frame, the link partner resumes transmission.

APPLICATION NOTE: In order to avoid frame drops in the RX FIFO when using jumbo frames with flow control the maximum frame size should be restricted to 4 KB or less. Consider the scenario where the flow control threshold is set to 4 KB. The reception of the first 4 KB frame triggers the transmission of a Pause frame. However, the Pause frame may be blocked if the TX path is at that moment in the process of transmitting a 4 KB packet. While the transmitter is sending its jumbo a frame a second jumbo frame may be received followed by a third frame before the partner has processed the Pause frame. A larger jumbo frame can result in frame drops which would require retransmissions by a higher layer protocol in such a corner case.

6.2 TX Path (USB to Ethernet)

The 12 KB TX FIFO buffers USB Bulk Out packets received by the URX. The FCT is responsible for extracting the Ethernet frames embedded in the USB Bulk Out Packets and passing them to the MAC. The Ethernet frames are segmented across the USB packets by the host software.

The FCT receives valid USB bulk out packets from the URX and writes them into the TX FIFO. The write side of the FCT does not perform any processing on the USB packet data. No provisions for rewind of these packets on the write side is required, as the URX manages its own buffer RAM, URX FIFO, and performs rewinds in the event that the Bulk

Out Packet is errored and needs to be retransmitted by the Host. When the FCT writes the Ethernet frame into the FCT TX FIFO RAM, it prepends a DWORD in front of the TX Command Words, used for internal processing, that contains the length of the Ethernet frame.

The read side of the FCT TX FIFO is responsible for extracting the Ethernet frames.

The Ethernet frames may have been split across multiple USB buffers, as shown in Figure 6-2 which illustrates how frames are stored in the URX FIFO. Figure 6-3 illustrates how Ethernet frames are stored in the FCT TX FIFO after being read and assembled from the URX FIFO.

APPLICATION NOTE: Software shall not attempt to flush the FCT TX FIFO if there are pending IN transactions.

FIGURE 6-2: URX FIFO RAM

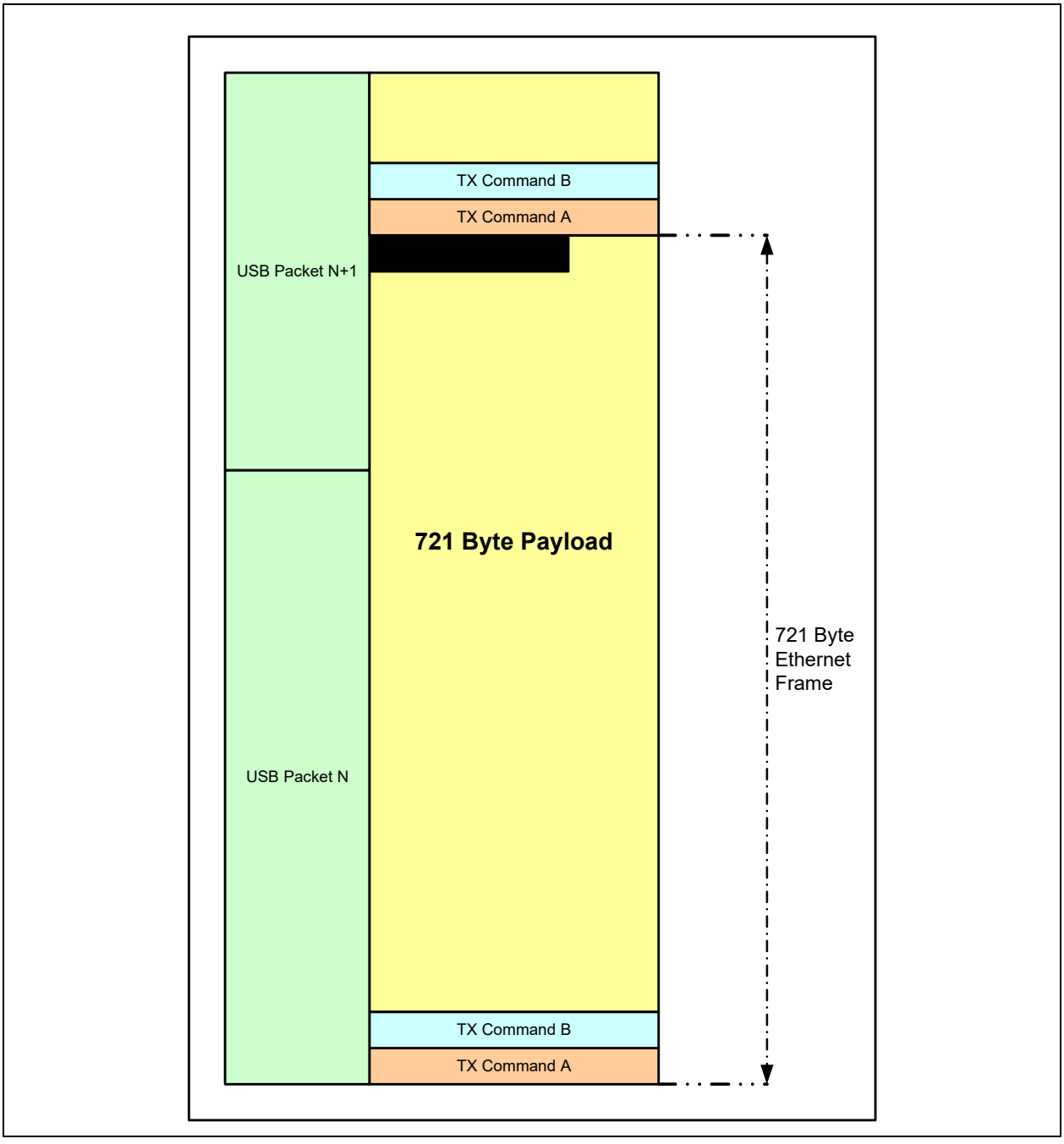

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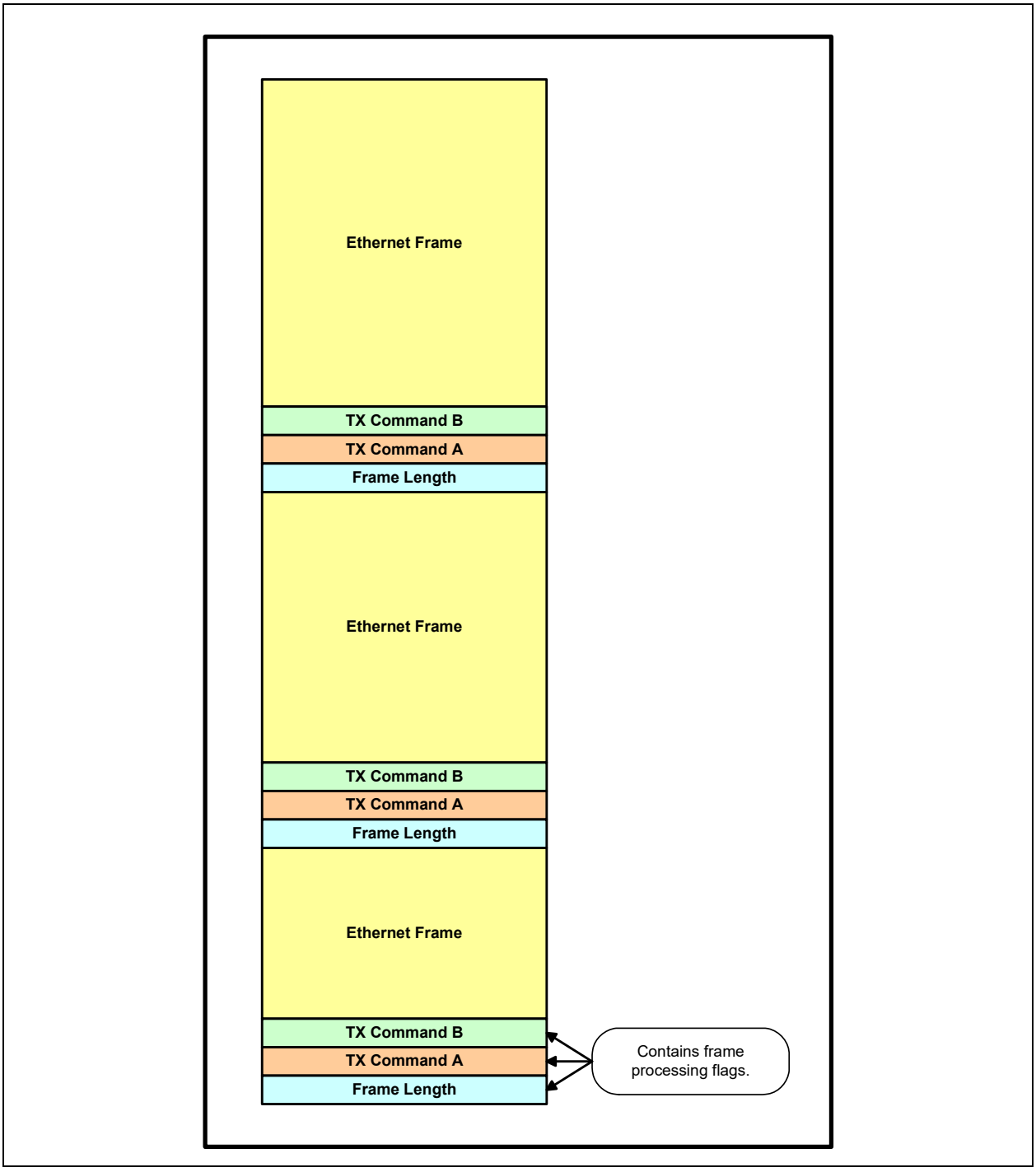
FIGURE 6-3: FCT TX FIFO RAM



6.2.1 TX COMMAND FORMAT

Each buffer starts with two TX Command DWORDs, TX Command A and TX Command B, which precede the data to be transmitted. The TX Commands instructs the FCT on the handling of the associated buffer.

The formats of TX Command A and TX Command B are shown in Table 6-4 and Table 6-5, respectively.

TX Command A contains the frame length and information to instruct how the frame must be processed. TX Command B provides the VLAN Tag and Maximum Segment Size. The former is needed when it is desired to have a VLAN ID inserted into the frame. The latter is used when Large Send Offload is specified. Please refer to Section 6.2.5, "VLAN Support," on page 52 and Section 6.2.8, "Large Send Offload (LSO)," on page 54 for further details on these features.

TABLE 6-4: TX COMMAND A

BITS	SYMBOL	DESCRIPTION
31:30	RESERVED	**RESERVED**
29	IGE	**IGMP Checksum Offload Enable** When set, the IGMP checksum will be calculated. **Note:** This bit has no meaning if LSO is enabled.
28	ICE	**ICMP/ICMPV6 Checksum Offload Enable** When set, the ICMP (IPV4)/ICMPV6(IPV6) checksum will be calculated. **Note:** This bit has no meaning if LSO is enabled.
27	LSO	**Large Send Offload Enable** When set, this bit enables TCP large send offload. The TCP packet will be segmented into blocks no larger than the amount specified by Maximum Segment Size.
26	IPE	**IP Checksum Offload Enable** When set, the IP checksum will be calculated. **Note:** This bit has no meaning if LSO is enabled.
25	TPE	**TCP/UDP Checksum Offload Enable** When set, the TCP/UDP will be calculated. **Note:** This bit has no meaning if LSO is enabled.
24	IVTG	**Insert VLAN Tag** When set, this bit instructs the FCT to insert a VLAN tag into the frame.
23	RVTG	**Replace VLAN Tag** This bit only applies if the TX frame has a pre-existing VLAN tag and the IVTG bit is set. When set, this bit causes the VLAN that exists in the frame to be overwritten by VLAN Tag. Otherwise, a second tag shall be inserted between the source address and the pre-existing tag.
22	FCS	**Insert FCS and Pad** When set, an FCS is generated and inserted for the frame.The MAC will insert padding if the frame is less than 64 bytes. If this bit is not set, then the MAC will never insert any padding and will assume the frame has an FCS. **Note:** It is not valid to enable checksum offloads or VLAN insertion when this bit is cleared. Doing so shall result in the frame being erroneous and at a minimum having an incorrect FCS. **Note:** Zero-es are always used for padding.
21:20	RESERVED	**RESERVED**

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TABLE 6-4: TX COMMAND A (CONTINUED)

BITS	SYMBOL	DESCRIPTION
19:0	LEN	**Frame Length [19:0]** This field indicates the size of the frame to be transmitted. **Note:** If Insert FCS and Pad is not set in this Command Word, then minimum transmit frame length must be at least 32 bytes. Values less than 32 bytes specified in this field when Insert FCS and Pad is clear may yield untoward operation and unexpected results. **Note:** During LSO operation this field defines the LSO packet size.

TABLE 6-5: TX COMMAND B

BITS	SYMBOL	DESCRIPTION
31:30	RESERVED	**RESERVED**
29:16	MSS	**Maximum Segment Size** When LSO is enabled, this 14-bit field specifies the maximum size of the TCP segments that are extracted from the TX IP packet. **Note:** The maximum jumbo frame size is 9 KB. **Note:** The minimum permissible value for this field is 8 bytes.
15:0	VTAG	**VLAN Tag** When the IVTG bit is set, a VLAN Tag will be inserted into the frame as defined by this field. [15:13] - PRI [12] - CFI [11:0] - VID

6.2.2 TX DATA FORMAT

The TX data section begins immediately after TX Command B. TX data is contiguous until the end of the buffer. The buffer may end on a byte boundary. Unused bytes at the end of the packet will not be sent to the MAC for transmission.

6.2.3 FCT ACTIONS ON TX FIFO READ

The FCT performs basic sanity checks on the correctness of the buffer configuration, as described in Section 6.2.4, "TX Error Detection," on page 52. Errors in this regard indicate the TX path is out of sync, which is catastrophic and requires a reinitialization of the TX path. A TX error can only be caused by a host software error.

The FCT performs the following steps when extracting an Ethernet frame from the TX FIFO:

- Strip out Frame Length DWORD
- Strip out TX Command A
- Strip out TX Command B
- Based upon the buffer size field of TX Command A, the FCT can numerically determine any unused bytes in the last word of the buffer. When transferring these respective DWORDs to the MAC, the FCT adjusts the byte enables accordingly.
- Configuration information required by the MAC from TX Command A is sent to it by the FCT through sideband channels.

Unlike the write side, the read side of the TX FIFO supports rewinds. The rewind_fr and release_fr signals from the MAC instruct the FCT on what actions to take on the TX FIFO buffer. The rewind_fr signal is asserted by the MAC when the frame must be re-transmitted due to a collision. When this signal is asserted, the FCT adjusts its internal read pointer to the start of the buffer to facilitate retransmission of the frame to the MAC. The release_fr signal is asserted by the MAC when the frame has been successfully transmitted or the maximum number of collisions has occurred. On assertion of release_fr, the FCT will purge the buffer from the TX FIFO through adjustment of its internal pointers.

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Errors are reported via the Transmitter Error (TXE) flag, which is visible to the Host via the Interrupt Endpoint and is also set in the Interrupt Status Register (INT_STS).

6.2.4 TX ERROR DETECTION

The following error conditions indicate that the TX path is out of sync and result in the Transmitter Error (TXE) flag being asserted:

- MSS is less than 8 and LSO is asserted or MSS is not 0 and LSO is not asserted
- LSO is asserted and detected template header size is more than 256 bytes
- TX Command A[19:16] is not 0 and LSO is not asserted
- TX Command A[15:0] is more than 2FF7h and LSO is not asserted (since extra 2 command words will be written to the TX FIFO as well)
- TX Command A Frame Length [19:0] field less than 32 bytes and Insert FCS and Pad is not asserted
- TX Command A[23] (Replace VLAN Tag (RVTG)) = 1 and TX Command A[24] (Insert VLAN Tag (IVTG)) = 0
- TX Command A[31:30] is not 0 (reserved bits)
- TX Command A[21:20] is not 0 (reserved bits)
- TX Command B[31:30] is not 0 (reserved bits)

Note:	The FCT can be configured to stall the Bulk Out pipe when a Transmit Error is detected. This is accomplished via the Stall Bulk-Out Pipe Disable (SBP) bit of the Hardware Configuration Register (HW_CFG).

Note:	A TX Error is a catastrophic condition that can only be caused by a host software error. The device should be reset in order to recover from it.

6.2.5 VLAN SUPPORT

The FCT supports insertion and manipulation of VLAN tags in transmitted frames. The FCT will insert a VLAN tag when the Insert VLAN Tag bit is set in TX Command A. In this case, the FCT will insert the tag specified by the VLAN Tag field in TX Command B. The type field used is the default VLAN type or 8100h. An additional VLAN type can be specified by the VLAN Type Register (VLAN_TYPE).

The FCT can also be instructed to replace a frame's VLAN tag. This occurs when the Replace VLAN Tag bit is set in TX Command A. In this case, the FCT will replace the existing tag with the one specified by the VLAN Tag field.

If the frame is already tagged, the FCT will insert a second VLAN tag if the Insert VLAN Tag is set and Replace VLAN Tag is clear. The new tag will be inserted between the source address and the original VLAN tag.

Note:	The Replace VLAN Tag bit has no meaning if the frame does not have a preexisting VLAN tag.

Note:	The VLAN insertion and replacement occurs as a frame is read out of the FIFO.

6.2.6 FCS GENERATION

The TX FCT shall generate an FCS for all transmitted frames when Insert FCS and Pad bit is set in TX Command A.

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6.2.7 TRANSMIT CHECKSUM OFFLOAD

The FCT is capable of offloading the generation of IP, ICMP/ICMPV6, IGMP, TCP, and UDP checksums for transmitted frames. The offload is enabled via the IP Checksum Offload Enable and TCP/UDP Checksum Offload Enable bits of TX Command A. Table 6-6 summarizes the transmit checksum offload capabilities.

TABLE 6-6: CHECKSUM OFFLOAD CAPABILITY SUMMARY

PACKET TYPE	IP CHECKSUM CAPABLE	TCP/UDP CHECKSUM CAPABLE	ICMP CHECKSUM CAPABLE	IGMP CHECKSUM CAPABLE
Type II Ethernet	Yes	Yes	Yes	Yes
SNAP Header	Yes	Yes	Yes	Yes
Single VLAN Tag	Yes	Yes	Yes	Yes
Stacked VLAN Tags	Yes	Yes	Yes	Yes
IPv4	Yes	Yes	Yes	Yes
IPv6	No	Yes	Yes	No
IP Fragment	Yes	No	No	No
IP Options	Yes	Yes	Yes	Yes
TCP or UDP Options	Yes	Yes	N/A	N/A
L4 protocol is not TCP or UDP	Yes	No	N/A	N/A
IPv6 with IP options next headers Note 6-1	No	Yes	Yes	No
IPv6 tunneled over IPv4	Yes (IPv4)	Yes	Yes	No
IPv4 tunneled over IPv4	No	No	No	No

Note 6-1 Fragmentation is not supported. Hop-by-Hop, Destination, and Routing options are supported.

Note: IPv6 does not have a header checksum.

Please refer to Section 7.2, "Checksum Offload," on page 66 for a discussion of the implementation of the checksum offload. Section 7.2 specifically addresses the receive checksum offload case. The pseudo header formats and scope of the checksum, however, are the same for both receive and transmit offload operations.

6.2.7.1 Configuration

In order to utilize the checksum offload, the host software performs the following steps:

1. Host software receives an IP packet from the application. The software must determine if a TCP or UDP packet is encapsulated.
2. The driver must indicate the checksum calculation to be offloaded by setting the proper bits in TX Command A. For IP checksum offload, the IP Checksum Offload Enable bit is set. For TCP or UDP checksum offload, the TCP/UDP Checksum Offload Enable bit is set. To enable ICMP and IGMP checksums the ICMP/ICMPV6 Checksum Offload Enable and IGMP Checksum Offload Enable bits are set respectively.

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6.2.8 LARGE SEND OFFLOAD (LSO)

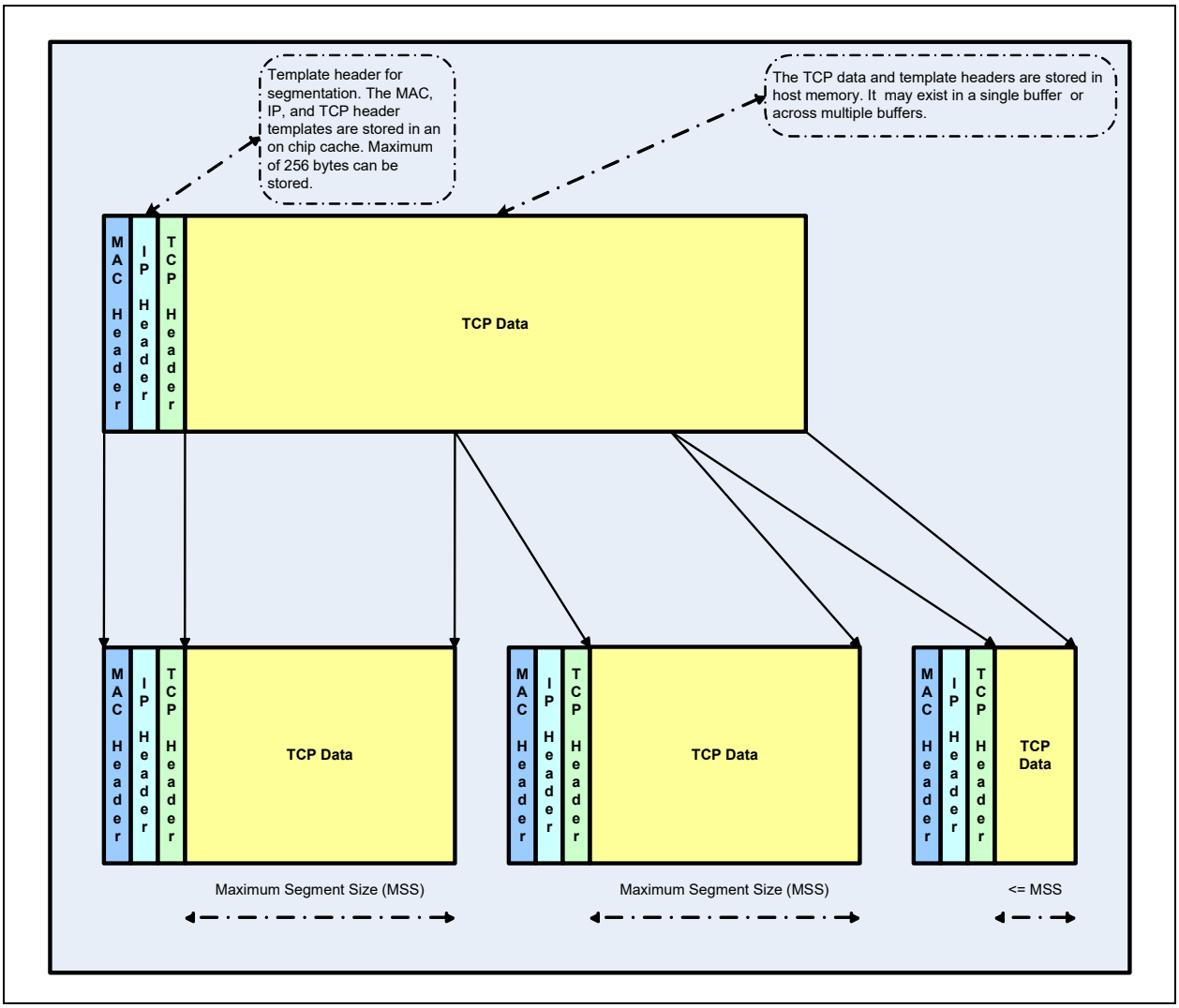
Large send offload (LSO), also known as TCP Segmentation, allows the TX FCT to segment a large TCP packet into multiple Ethernet frames. This feature relieves a significant burden on Host CPU resources.

The assertion of the Large Send Offload Enable bit in TX Command A enables this feature in the FCT. The size of the final Ethernet frames are determined by the Maximum Segment Size field in TX Command B, and the size of the encapsulating headers. Figure 6-4 illustrates a high level view of the TCP segmentation process.

The TX FCT performs the following operations:

- Breaks the large TCP packet into segments
- Creates the Ethernet Header
- Creates the IP Header
- Creates the TCP Header
- Calculates the IP checksum (IPv4 only)
- Calculates the TCP checksum

FIGURE 6-4: TCP SEGMENTATION



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The TCP payload stored in URX buffer RAM is preceded by template headers. They are composed of Ethernet, IP, and TCP headers. The template header may not exceed 256 bytes. The FCT copies the template headers and stores them in the LSO Template Header RAM. They are used as the basis for the headers of all future segments.

The following formats are supported for LSO.

- Ethernet 802.3
- IEEE 802.1q VLAN
- Ethernet Type II
- SNAP Header
- IPv4
- IPv6
- IP Options
- TCP Options
- IPv6 with next header options
  Hop-by-Hop supported
  Destination supported
  Routing supported
  Fragmentation not supported

Note:	LSO is not supported for UDP packets.

Note:	IP tunneling is not supported for LSO.

6.2.8.1 Configuration

In order to prepare the FCT for LSO, the following steps must be taken by the Host software.

Note:	Steps 1. and 2., with the exception of reservation of space for the TX Command Words, may be accomplished by the Host operating system.

1. The protocol stack receives a block of data from the application into its own local buffer. Sufficient space is reserved in the local buffer for the construction of the TX Command Words and template headers prior to the TCP payload.
2. Template headers are constructed and inserted in front of the TCP payload in the local buffer. Software must ensure the following requirements are met in the template headers:
   - The IPv4 MF bit is not set.
   - The IPv4 Fragment Offset field is zero.
   - The IPv4, or IPv6, packet length is set to zero.
   - The IPv4 Identification field is set appropriately.
   - The TCP Sequence Number field is set to identify the first byte of the TCP payload.
   - The TCP FIN bit is set as appropriate for the last packet of the segment.
   - The TCP PSH bit is set as appropriate for the last packet of the segment.
   - The TCP flags URG, RST, and SYN are not set. The urgent pointer is set to zero.
3. Software must then configure the TX Command Words as follows to enable Large Send Offload:
   - The Large Send Offload Enable bit is set in TX Command A.
   - The Maximum Segment Size field is set in TX Command A. The MSS indicates the size of the packet data that is being encapsulated. This value does not include the Ethernet header, IP header, or TCP header.
   - If VLAN operation is supported, then the Insert VLAN Tag bit, Replace VLAN Tag bit, and the VLAN Tag field must be set appropriately in TX Command B.
4. Software transmits the contents of its local buffer to the device via the USB interface. Subsequent data may be transmitted via the USB interface, depending on the size of the local buffer and the total size of the data to be transmitted from the application.

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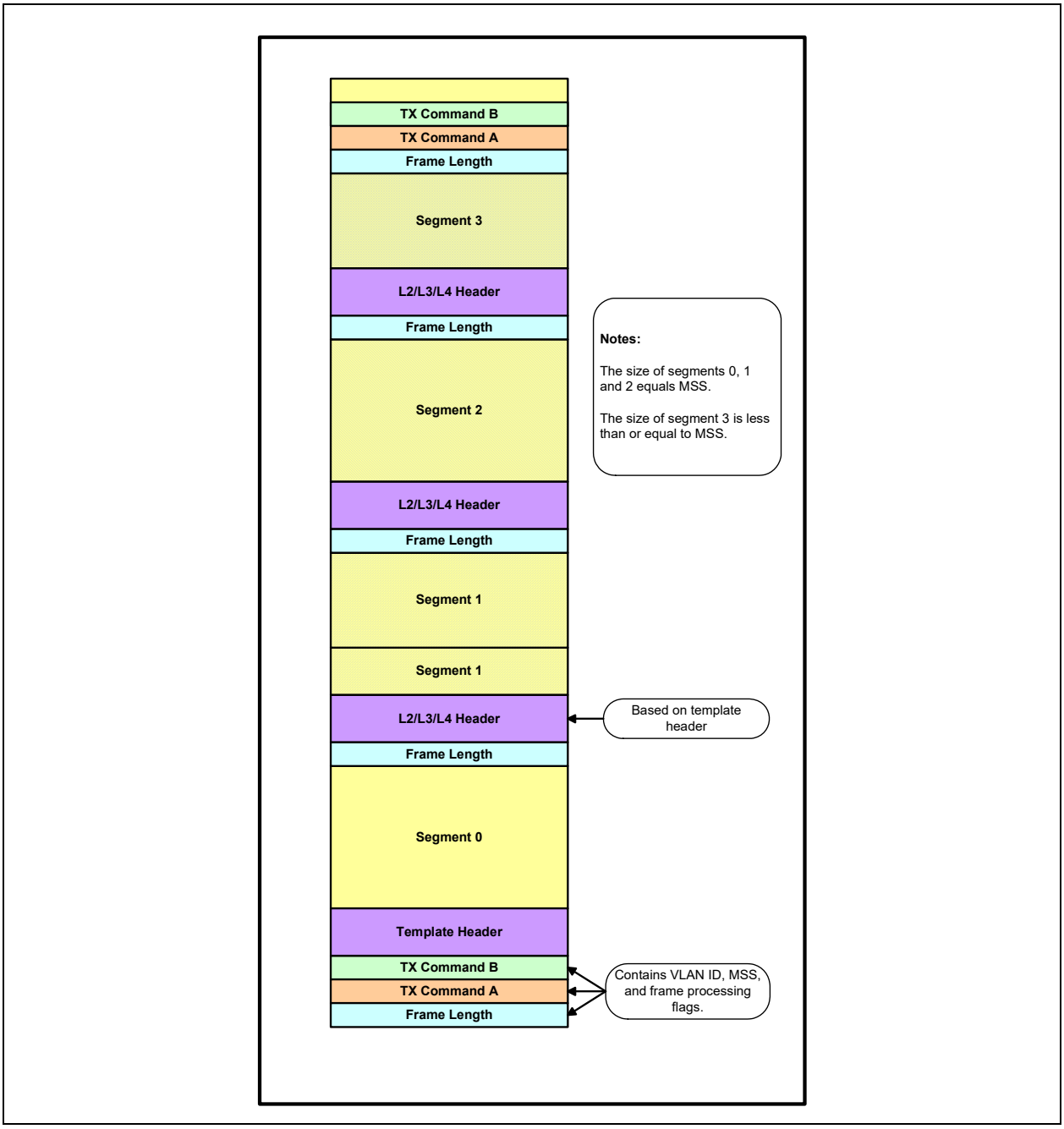
6.2.8.2 Processing

The FCT recognizes that it has received a frame for LSO by the assertion of the Large Send Offload Enable bit in TX Command A when it reads the command word out of URX Buffer RAM. The FCT copies and stores the template header. For subsequent segments, headers based upon the template header are inserted. Additionally, a frame length word is constructed for each segment. With the exception of the last segment, the length for all segments will equal to the Maximum Segment Size.

Figure 6-5 illustrates how frame data is stored in the TX FIFO when LSO is enabled. The total size of the packet requires four segments to be created. The last segment having a size less than the Maximum Segment Size.

FIGURE 6-5: LSO TX FIFO FRAME STORAGE



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The FCT is responsible for performing the following functions for the LSO:

1. Compute the IP checksum (IPv4)
2. Compute the IP pseudo-header
3. Compute the TCP checksum
4. Compute the IP packet length
5. Compute the IP Identification field (IPv4 only)
6. Compute the TCP Sequence Number field
7. If there are any IP options, the FCT copies them unmodified into each packet. Likewise, any TCP options are also copied unmodified into each TCP packet.
8. Set the TCP FIN and PSH bits accordingly
9. VLAN tag processing
10. Request the MAC to generate an FCS for each frame by setting the Insert FCS and Pad in the TX Command A it constructs for the frame.

If there is a SNAP header, the FCT must update the length field as required for an 802.3 frame.

Note: The FCT ignores the IP MF flag, NF flag, and fragment offset field. The FCT ignores the TCP URG, RST, and SYN flags. The TCP urgent pointer is also ignored.

The following sections break down the duties of the FCT on per segment basis for creating the frame's headers.

6.2.8.2.1 Initial Packet Generation

For the first packet of a segment, the FCT performs the following header calculations:

- IP Length = Maximum Segment Size + IP Header Size + TCP Header Size
- Total Frame Length = IP Length + L2 Header + VLAN
- Ethernet Length = IP Length
- Compute IP Checksum (IPv4)
- IP Identification = Value programmed in template IP header
- Compute TCP Checksum
- TCP Sequence Number = Value programmed in template TCP header
- TCP FIN flag = 0
- TCP PSH flag = 0

6.2.8.2.2 Intermediate Packet Generation

For the intermediary packets of a segment, the FCT performs the following header calculations:

- IP Length = Maximum Segment Size + IP Header Size + TCP Header Size
- Total Frame Length = IP Length + L2 Header + VLAN
- Ethernet Length = IP Length
- Compute IP Checksum (IPv4)
- IP Identification = Increment from value in previous IP packet
- Compute TCP Checksum
- TCP Sequence Number = Value of previous TCP header + Maximum Segment Size
- TCP FIN flag = 0
- TCP PSH flag = 0

6.2.8.2.3 Final Packet Generation

For the last packet of a segment, the FCT performs the following header calculations:

- Last frame TCP payload length = TCP payload length - N* Maximum Segment Size. (N is the number of previously transmitted segments.)
- IP Length = Last Frame TCP Payload Length + IP Header Size + TCP Header Size
- Total Frame Length = IP Length + L2 Header + VLAN
- Ethernet Length = IP Length

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- Compute IP Checksum (IPv4)
- IP Identification = Increment from value in previous IP packet
- Compute TCP Checksum
- TCP Sequence Number = Value of previous TCP header + Maximum Segment Size
- TCP FIN flag is set to the value specified in the TCP template header
- TCP PSH flag is set to the value specified in the TCP template header

6.2.9 FLUSHING THE TX FIFO

The device allows for the Host to the flush the entire contents of the FCT TX FIFO. When a flush is activated, the internal read and write pointers for the TX FIFO are returned to their reset state.

Before flushing the TX FIFO, the device's transmitter must be stopped, as specified in Section 6.2.10. Once the transmitter stop completion is confirmed, the FCT TX Enable bit is cleared in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) to stop TX FIFO operation. The FCT TX Disabled bit and the TX Disabled Interrupt (TX_DIS_INT) (if enabled) assert when the TX FIFO hardware has completed the disabling process. The FCT TX Reset bit shall then be set in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) to initiate the flush operation. This bit is cleared by the hardware when the flush operation has completed.

Note: TX Disabled Interrupt (TX_DIS_INT) will persist until both the FCT TX Disabled status bit and the Transmitter Disabled (TXD) status bit in the MAC Transmit Register (MAC_TX) are cleared.

After the TX FIFO has been flushed, the transmitter may be restarted as specified in Section 6.2.10. TX FIFO operation may then be restarted by asserting the FCT TX Enable bit.

APPLICATION NOTE: Software shall not attempt to flush the TX FIFO if there are pending URBs on the Bulk Out EP.

6.2.10 STOPPING AND STARTING THE TRANSMITTER

To stop the transmitter, the Host must perform the following steps:

1. Software clears the FCT TX Enable bit in the FIFO Controller TX FIFO Control Register (FCT_TX_CTL).
2. Software polls the FCT TX Disabled bit in the FIFO Controller TX FIFO Control Register (FCT_TX_CTL) to confirm the FCT TX is disabled.

Note: The MAC continues to read the frame currently being transmitted from the FCT until the frame is transmitted. After the frame is transmitted, the FCT TX Disabled bit will assert.

3. The FCT TX Disabled bit is set in the FIFO Controller TX FIFO Control Register (FCT_TX_CTL).
4. Software halts the MAC transmitter by clearing the Transmitter Enable (TXEN) bit in the MAC Transmit Register (MAC_TX).
5. Software polls the Transmitter Disabled (TXD) bit in the MAC Transmit Register (MAC_TX) to confirm the MAC transmitter is disabled.
6. The Transmitter Disabled (TXD) status bit is set to indicate that the MAC TX has halted.

APPLICATION NOTE: As an alternative to polling FCT TX Disabled and/or Transmitter Disabled (TXD), the TX Disabled Interrupt (TX_DIS_INT) bit in the Interrupt Status Register (INT_STS) may be used.

APPLICATION NOTE: When the device is configured for half-duplex operation, it is possible for a collision to happen after FCT TX Enable is cleared but before the frame has completed transmitted. In this case the MAC will assert abort signaling to the FCT and the frame shall be dropped by the FCT.

Once the TX path is stopped, the Host can optionally flush the TX FIFO as discussed in Section 6.2.9. The Host may re-enable the transmitter by setting the Transmitter Enable (TXEN) bit in the MAC Transmit Register (MAC_TX) followed by setting the FCT TX Enable bit in the FIFO Controller TX FIFO Control Register (FCT_TX_CTL).

If there are frames pending in the TX FIFO (i.e., the TX FIFO was not purged), the transmission will resume with this data.

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7.0 RECEIVE FILTERING ENGINE (RFE)

The RFE receives Ethernet frames from the Ethernet MAC, processes them, and passes them to the RX FCT. The RFE is responsible for filtering the received Ethernet frames, verifying the TCP/UDP/ICMP/IGMP and IP checksum, and removing the VLAN tag.

When receiving a frame from the MAC, the RFE will obtain the frame data and status information. Upon completion of frame processing, the RFE encapsulates its status with the status information obtained from the MAC, and passes this information (along with the frame data) on to the FCT in the form of RX Command A, RX Command B and RX Command C.

The RFE, if enabled, can remove a VLAN tag from the frame. VLAN tag stripping is controlled by the Enable VLAN Tag Stripping bit of the Receive Filtering Engine Control Register (RFE_CTL). If this bit is set, the tag will be stripped. If clear, the RFE will not modify the frame in any way.

Note:	If multiple VLAN tags are present in a frame, the RFE only removes the first tag (adjacent to the MAC source address).

The RFE provides the Layer 3 Checksum (if enabled) and VLAN ID via RX Command B, while RX Command A and RX Command C contain the frame's status.

When the RFE determines a frame has a checksum error, it sets the appropriate error bits in RX Command A to identify the error condition.

Note:	The FCT does not rewind frames that failed checksum validation from the FCT RX FIFO.

7.1 Frame Filtering

The RFE filters Ethernet frames by processing the Ethernet source address, Ethernet destination address, and VLAN ID.

The following frame filtering options are supported:

- Global Unicast (Receive all unicast frames)
- Global Multicast (Receive all multicast frames)
- Broadcast Filter (Discard all broadcast frames)
- Perfect Address Filtering
- Hash Address Filtering
- VLAN Filtering (Untagged/VID)

7.1.1 PERFECT ADDRESS FILTERING

The RFE provides for perfect address filtering. This represents the first level of frame filtering. There are 33 addresses available for this purpose, which are stored in the MAC Address Perfect Filter Registers (ADDR_FILTx). Each entry may be configured as either a destination or a source address. Table 7-1 illustrates an entry.

TABLE 7-1: PERFECT ADDRESS ENTRY FORMAT

BIT	DESCRIPTION
49	**Address Valid** When set, this bit indicates that the entry has valid data and is used in the perfect filtering.
48	**Address Type** When set, this bit indicates the MAC Address represents the MAC source address. Otherwise this entry applies to the MAC destination address.
47:0	**MAC Address** This field holds the 48-bit MAC address that will be matched by the RFE. The MAC address storage scheme matches that for the RXADDRH and RXADDRL registers, see Table 15-4, "RX_ADDRL, RX_ADDRH Byte Ordering".

Destination address filtering is enabled via the Enable Destination Address Perfect Filtering (DPF) bit of the Receive Filtering Engine Control Register (RFE_CTL). Source address filtering is enabled by the Enable Source Address Perfect Filtering (SPF) bit. If both source and destination address filtering are enabled, then a frame will be discarded if a match is not present for both fields. In this case, the destination address match may also occur via the hash filter.

After receiving a frame, the RFE will compare all 33 entries in the table, after parsing out the destination and source address. Filters are added and changed via the MAC Address Perfect Filter Registers (ADDR_FILTx). The entries may be changed during run time.

7.1.2 HASH ADDRESS FILTERING

The RFE supports imperfect filtering of the MAC destination address. This allows the number of address filters to exceed the number provided by the perfect filters.

Note: The hash filter can result in false positives. Therefore, the Host must validate the destination address.

By default, the hash filtering is enabled for both multicast and unicast destination addresses. Hash filtering never applies to broadcast addresses. The Enable Multicast Address Hash Filtering (MHF) and Enable Destination Address Hash Filtering (DHF) bits in the Receive Filtering Engine Control Register (RFE_CTL) enables the address hash filter for the respective frame type.

The RFE computes the hash on the destination address via a CRC-32 calculation. The hash result is used to index the Hash Address Filter table that is stored in the VHF. Figure 7-3 illustrates the layout of the VHF and the position of the Hash Address Filter table within it. The filter table is 16 DWORDS in length and holds up to 512 entries. Each entry is a single bit within the 16 DWORD array.

At the start of a new frame, the CRC-32 is initialized with the value FFFFFFFFh. The CRC-32 is then updated with each byte of the destination address.

The following algorithm is used to update the CRC-32 at that time:

Let:

^ denote the exclusive or operator.

Data [7:0] be the received data byte to be included in the checksum.

CRC[31:0] contain the calculated CRC-32 checksum.

F0 … F7 be intermediate results, calculated when a data byte is determined to be part of the CRC-32.

Calculate:

F0 = CRC[31] ^ Data[0]

F1 = CRC[30] ^ Data[1]

F2 = CRC[29] ^ Data[2]

F3 = CRC[28] ^ Data[3]

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F4 = CRC[27] ^ Data[4]

F5 = CRC[26] ^ Data[5]

F6 = CRC[25] ^ F0 ^ Data[6]

F7 = CRC[24] ^ F1 ^ Data[7]

The CRC-32 is updated as follows:

CRC[31] = CRC[23] ^ F2

CRC[30] = CRC[22] ^ F0 ^ F3

CRC[29] = CRC[21] ^ F0 ^ F1 ^ F4

CRC[28] = CRC[20] ^ F1 ^ F2 ^ F5

CRC[27] = CRC[19] ^ F2 ^ F3 ^ F6

CRC[26] = CRC[18] ^ F3 ^ F4 ^ F7

CRC[25] = CRC[17] ^ F4 ^ F5

CRC[24] = CRC[16] ^ F5 ^ F6

CRC[23] = CRC[15] ^ F0 ^ F6 ^ F7

CRC[22] = CRC[14] ^ F1 ^ F7

CRC[21] = CRC[13] ^ F2

CRC[20] = CRC[12] ^ F3

CRC[19] = CRC[11] ^ F0 ^ F4

CRC[18] = CRC[10] ^ F0 ^ F1 ^ F5

CRC[17] = CRC[9] ^ F0 ^ F1 ^ F2 ^ F6

CRC[16] = CRC[8] ^ F1 ^ F2 ^ F3 ^ F7

CRC[15] = CRC[7] ^ F0 ^ F2 ^ F3 ^ F4

CRC[14] = CRC[6] ^ F0 ^ F1 ^ F3 ^ F4 ^ F5

CRC[13] = CRC[5] ^ F1 ^ F2 ^ F4 ^ F5 ^ F6

CRC[12] = CRC[4] ^ F0 ^ F2 ^ F3 ^ F5 ^ F6 ^ F7

CRC[11] = CRC[3] ^ F0 ^ F1 ^ F3 ^ F4 ^ F6 ^ F7

CRC[10] = CRC[2] ^ F1 ^ F2 ^ F4 ^ F5 ^ F7

CRC[9] = CRC[1] ^ F0 ^ F2 ^ F3 ^ F5 ^ F6

CRC[8] = CRC[0] ^ F0 ^ F1 ^ F3 ^ F4 ^ F6 ^ F7

CRC[7] = F0 ^ F1 ^ F2 ^ F4 ^ F5 ^ F7

CRC[6] = F1 ^ F2 ^ F3 ^ F5 ^ F6

CRC[5] = F2 ^ F3 ^ F4 ^ F6 ^ F7

CRC[4] = F3 ^ F4 ^ F5 ^ F7

CRC[3] = F4 ^ F5 ^ F6

CRC[2] = F5 ^ F6 ^ F7

CRC[1] = F6 ^ F7

CRC[0] = F7

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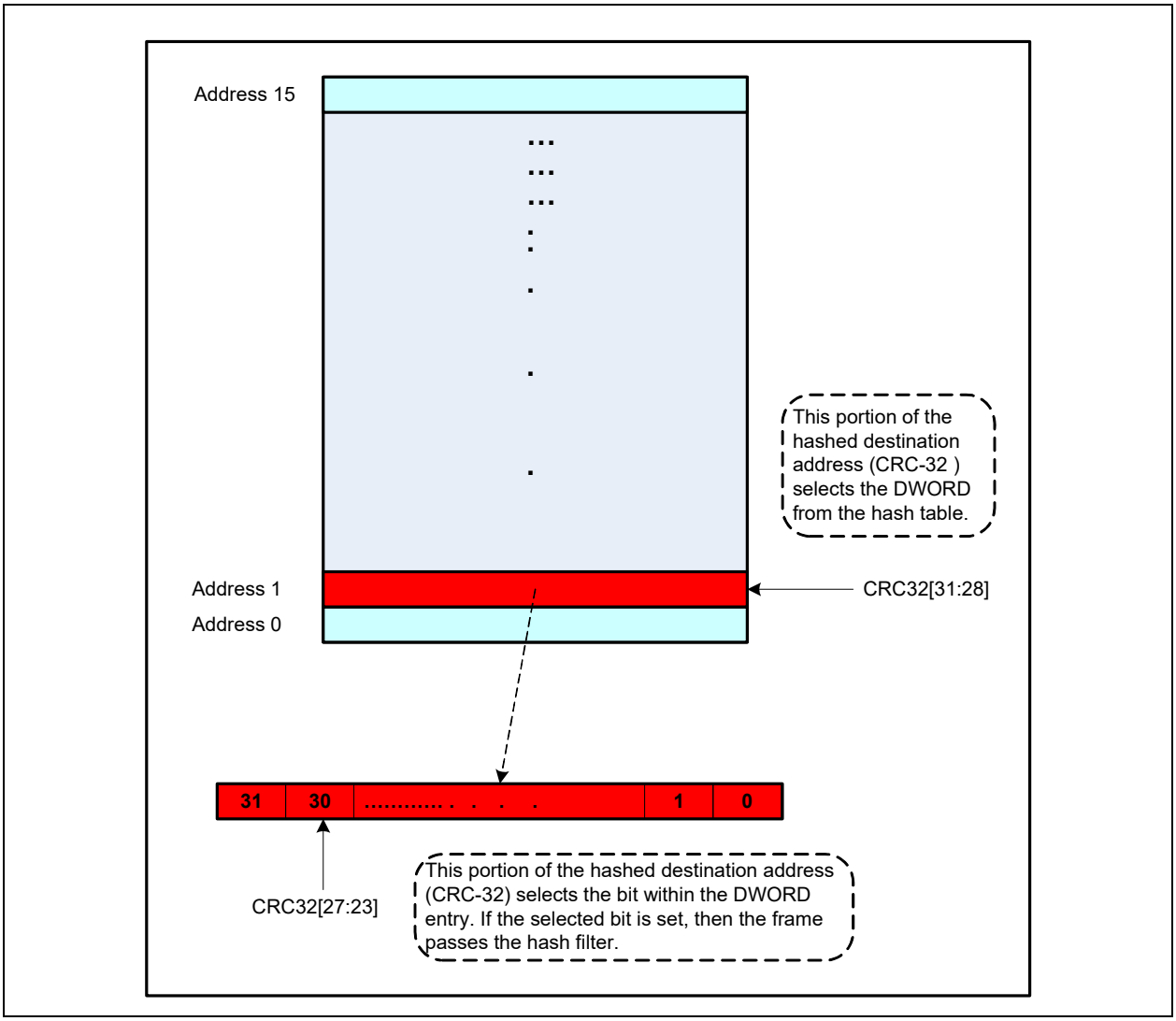
The upper 9-bits, [31:23] of the resultant CRC-32 is extracted by the RFE. This value provides the bit location in the filter table to be examined. If the respective bit is asserted, then the frame passes the hash filter. Bits 31:28 reference the DWORD within the table that is to be used, while bits 27:23 index the bit entry. Figure 7-1 illustrates this decoding.

FIGURE 7-1: HASH FILTER DECODING



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7.1.3 VLAN FILTERING

The RFE provides the ability to filter on the VLAN tag. A VLAN tag is present when the type field matches the value indicated by the VLAN Type Register (VLAN_TYPE) or 8100h.

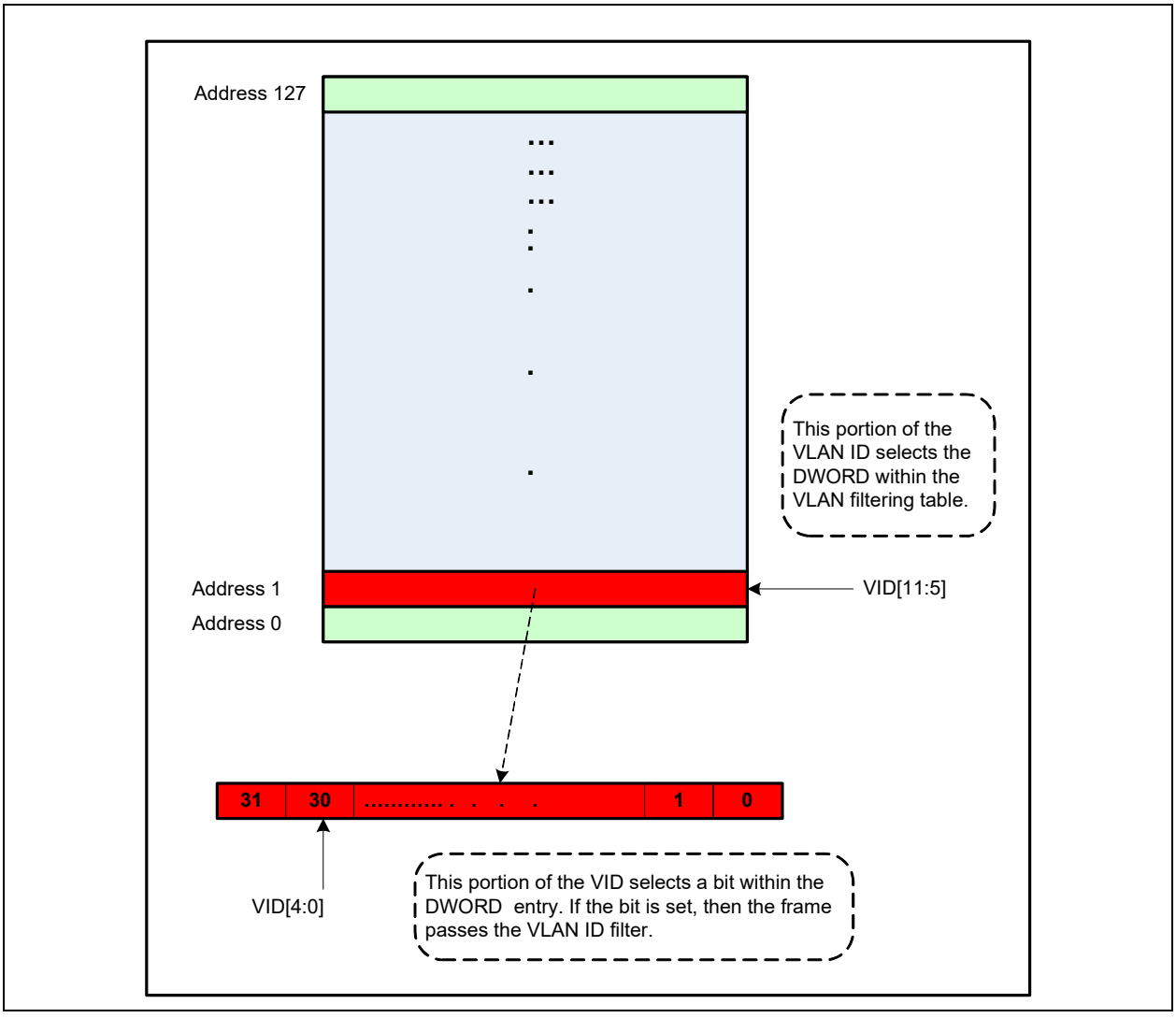
When multiple VLAN tags are present, the RFE only considers the first tag. This is defined as the tag immediately adjacent to the source address.

The RFE may be configured to discard frames or pass frames that do not have a VLAN tag. This is controlled by the Untagged Frame Filtering (UF) bit of the Receive Filtering Engine Control Register (RFE_CTL).

When the RFE encounters a tagged frame, the VLAN tag is stripped. The VLAN ID is placed into the VLAN Tag field of RX Command B and the Frame is VLAN tagged bit of RX Command A is set.

The 12-bit VID is extracted from the VLAN tag and used for VLAN filtering if the Enable VLAN Filtering (VF) bit of the Receive Filtering Engine Control Register (RFE_CTL) is set. The VID maps to a bit in the VLAN ID Filter Table contained in the VMF. Figure 7-2 illustrates the mapping. If the corresponding bit is set, then the frame passes the VLAN filtering. If filtering is enabled, and the VID is not present in the VLAN ID Filter Table (mapped bit is clear), then the frame is dropped.

FIGURE 7-2: VLAN ID FILTER DECODING



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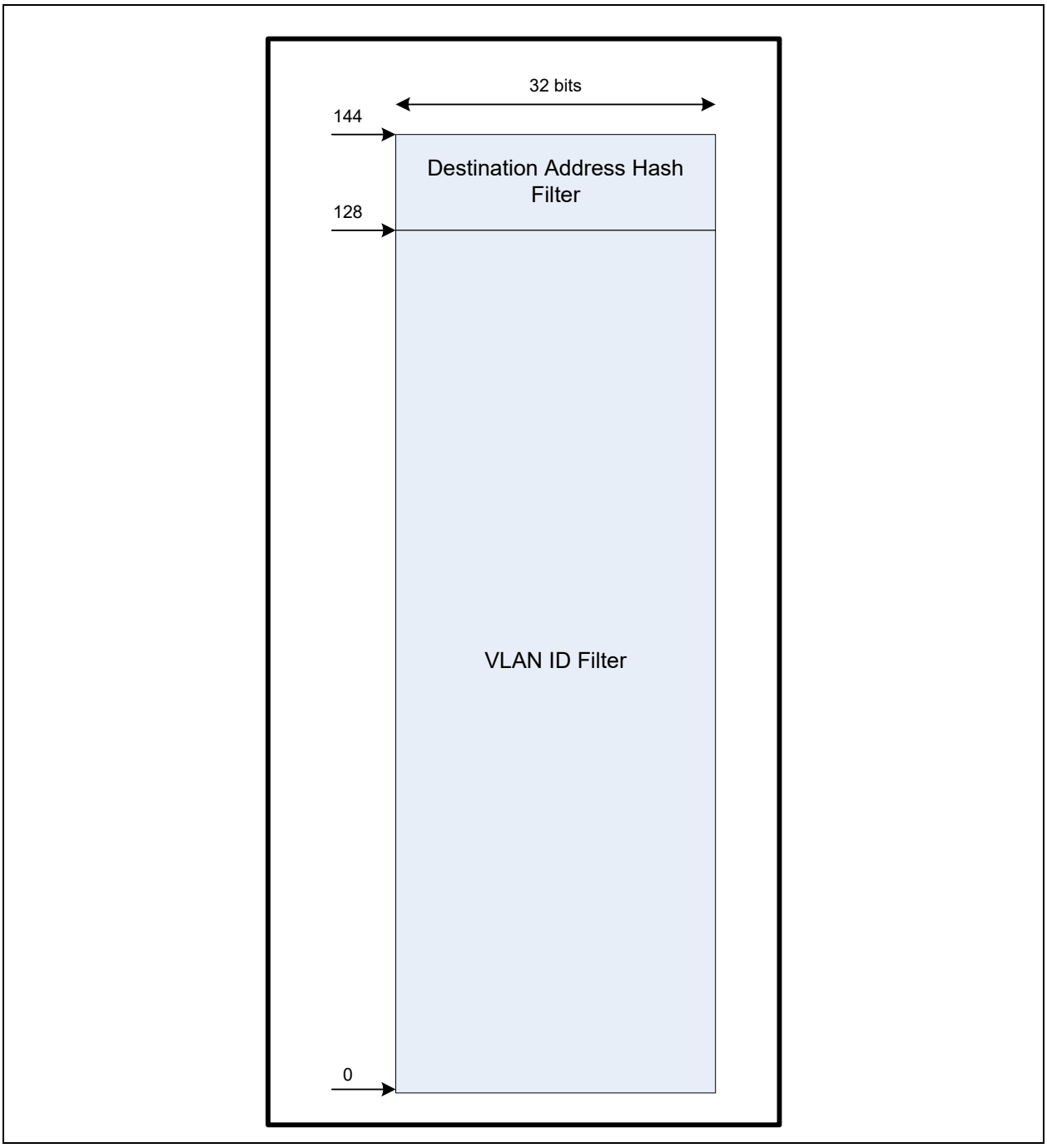
7.1.4 VHF ORGANIZATION

The VHF RAM contains the tables necessary to perform VLAN filtering and hash based destination address filtering. Figure 7-2 shows the locations of the VLAN filter table and the Hash filter table. The table's contents are addressed on a DWORD boundary.

FIGURE 7-3: VHF RAM LAYOUT



VHF entries are added and changed via the data port registers. The Data Port Select Register (DP_SEL) is used to specify the VHF RAM. The VHF entries may be changed during run time.

After a reset event, the RFE will automatically initialize the contents of the VHF to 0h. While the initialization is in progress, data port accesses to this RAM will be wait stated.

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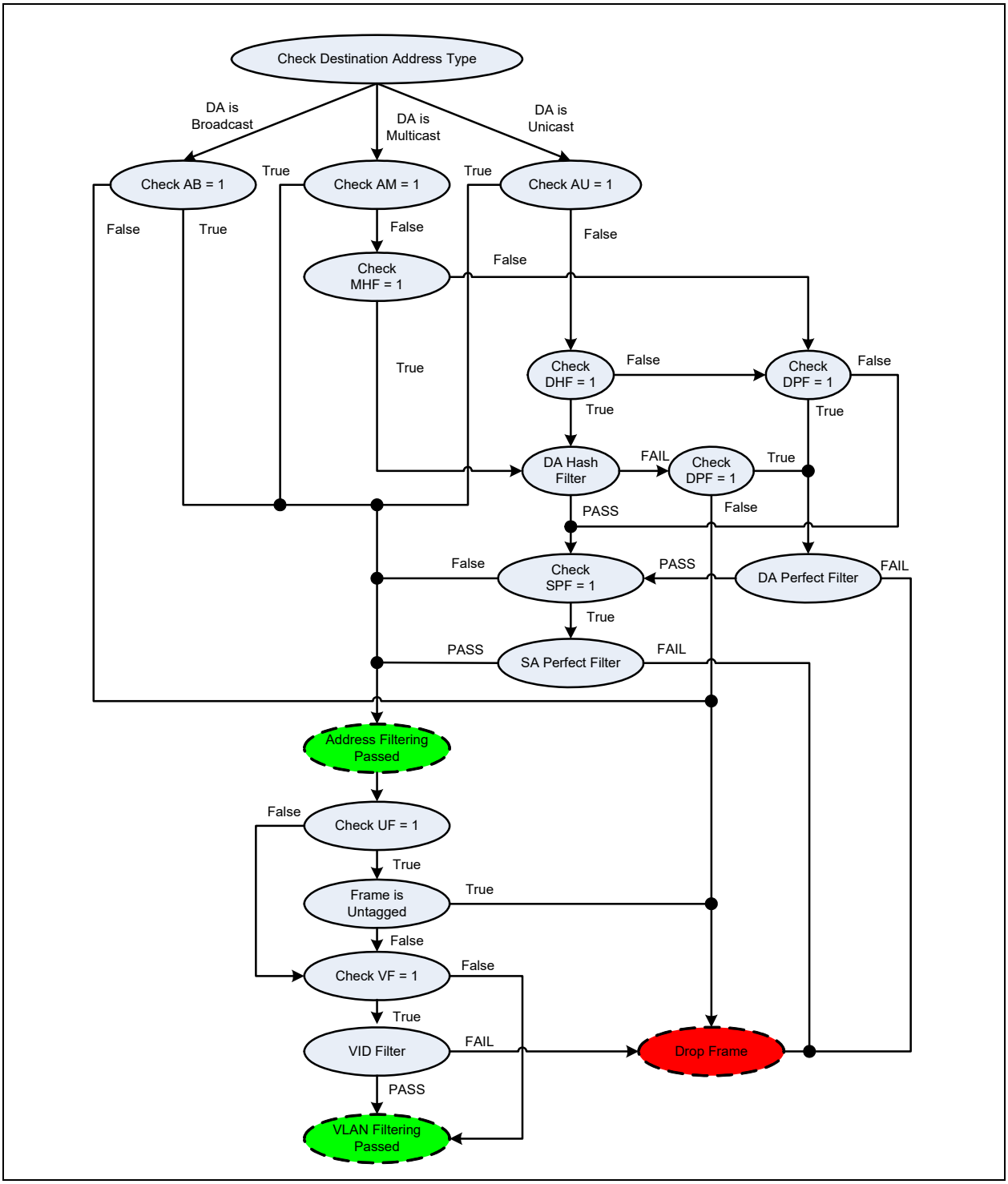
7.1.5 DETAILED FILTERING RULES

Figure 7-4 illustrates the exact filtering process performed by the RFE.

FIGURE 7-4: DETAILED FILTERING RULES



7.2 Checksum Offload

The RFE supports the offloading of the IP checksum, TCP/UDP checksum, and a L3 checksum. Both IPv4 and IPv6 are supported. The RFE supports the following IEEE 802.3 frame types:

- Type II Ethernet frames
- Ethernet SNAP frames

802.1q VLAN tags are supported. The RFE is capable of recognizing up to two VLAN tags and excludes them from the checksum calculations. The type used to recognize a VLAN tag is defined by the VLAN Type Register (VLAN_TYPE). This value defaults to 8100h.

7.2.1 IP CHECKSUM

A value of 0800h in the type field indicates the frame is IPv4. A value of 86DDh in the type field indicates the frame is IPv6.

IP checksum offload is enabled when the Enable IP Checksum Validation bit of the Receive Filtering Engine Control Register (RFE_CTL) is set. If an IP checksum is found to be erroneous, the IP Checksum Error bit in RX Command A is asserted and the RFE signals the FCT to abort the frame. The IP Checksum Error will also be asserted if the IP header is less than 20 bytes in size, as indicated by the IP Header Length.

Note:	The IP header may be larger than 5 DWORDs (20 bytes) if IP options are present. IPv6 does not have an IP checksum.

The IP checksum is the 16-bit one's complement of the one's complement sum of all 16-bit groups in the IP header. The checksum is verified by calculating he 16-bit one's complement sum across the IP header. This calculation includes the IP checksum itself. If the final result is FFFFh, then the packet has a valid IP checksum.

7.2.2 LAYER 3 CHECKSUM

The Layer 3 checksum and TCP/UDP checksum are enabled when the Enable TCP/UDP Checksum Validation bit of the Receive Filtering Engine Control Register (RFE_CTL) is set. The Layer 3 checksum and IGMP checksum are enabled when the Enable IGMP Checksum Validation bit of the Receive Filtering Engine Control Register (RFE_CTL) is set. Likewise the Layer 3 checksum and ICMP checksum are enabled when the Enable ICMP Checksum Validation bit of the Receive Filtering Engine Control Register (RFE_CTL) is set.

The Layer 3 checksum is the 16-bit one's complement sum of the entire layer 3 packet. The checksum is calculated 16 bits at a time. In the case of an odd sized frame, an extra byte of zero is used to pad up to 16 bits.

Consider the following packet: DA, SA, Type, B0, B1, B2 … BN, FCS

Let [A, B] = A*256 + B

If the packet has an even number of octets then:

checksum = [B1, B0] + C0 + [B3, B2] + C1 + … + [BN, BN-1] + CN-1

Where C0, C1,... CN-1 are the carry out results of the intermediate sums.

If the packet has an odd number of octets then:

checksum = [B1, B0] + C0 + [B3, B2] + C1 + … + [0, BN] + CN-1

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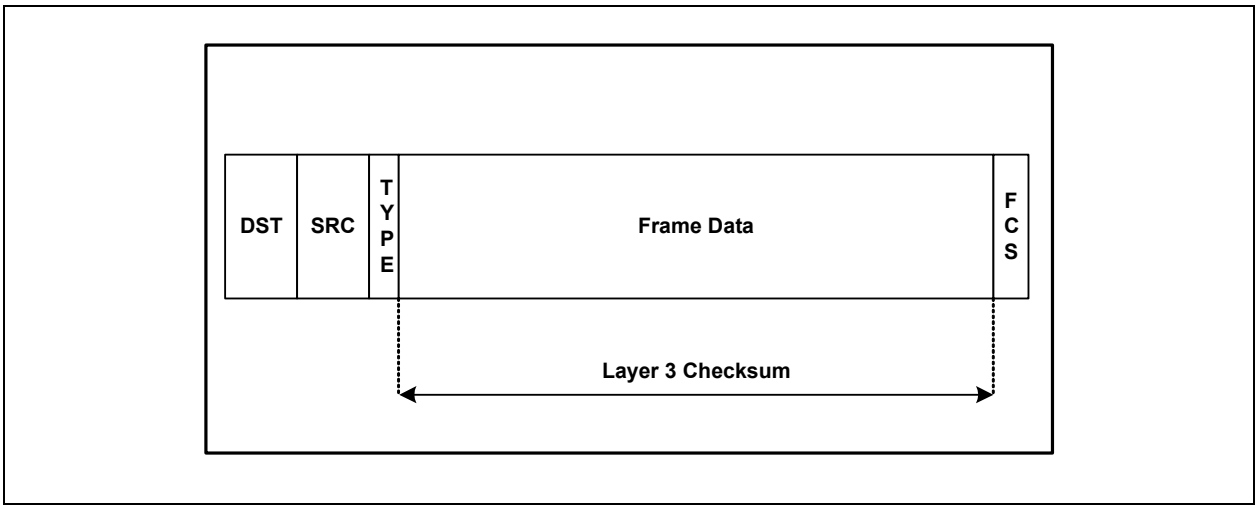
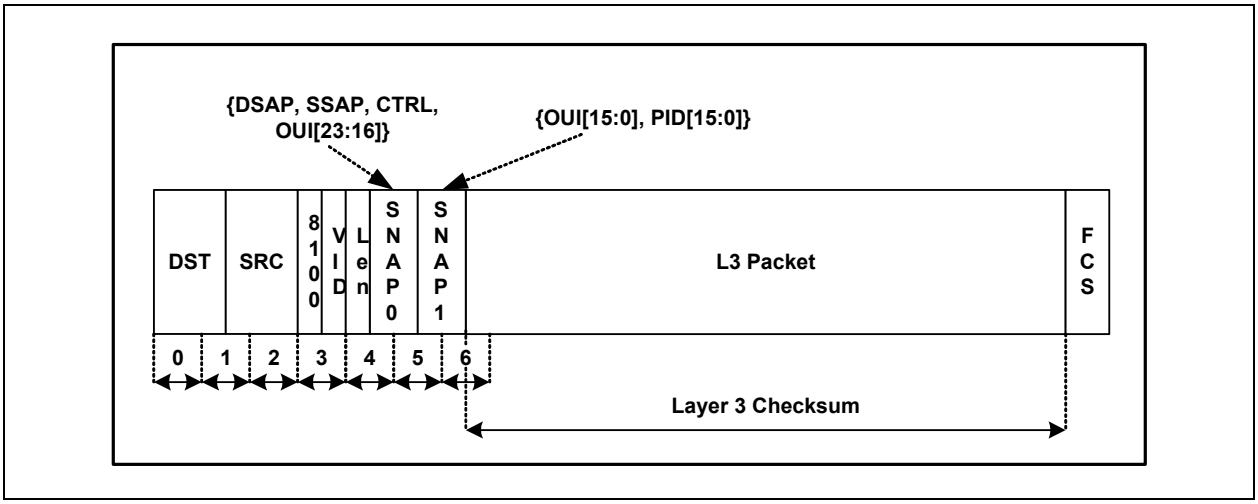
Figure 7-5 illustrates the scope of the Layer 3 checksum over a type II Ethernet frame. The calculation starts after the type field and does not include the FCS.

FIGURE 7-5: LAYER 3 CHECKSUM - TYPE II ETHERNET



Consider the case where the frame is a 802.3 Ethernet frame with a VLAN tag. The RFE bypasses DA, SA, VLAN tag, SNAP header, and type fields. The calculation begins at the byte immediately following the type field. The calculation does not include the FCS.

FIGURE 7-6: LAYER 3 CHECKSUM - 802.3 FRAME



The checksum is placed in the Raw L3 Checksum field in RX Command B. This raw checksum is useful in cases such as when the layer 3 protocol is not IP or IP fragmented packets.

Note: If neither the Enable TCP/UDP Checksum Validation, Enable ICMP Checksum Validation nor Enable IGMP Checksum Validation bits of the Receive Filtering Engine Control Register (RFE_CTL) are set, then the value of the Raw L3 Checksum field is undefined.

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7.2.3 TCP CHECKSUM

If the RFE detects a TCP header, it will attempt to verify the TCP checksum when the Enable TCP/UDP Checksum Validation bit in the Receive Filtering Engine Control Register (RFE_CTL) is set. TCP is indicated when the IP Protocol is 6.

The TCP checksum covers the TCP header, TCP data, and pseudo header. The pseudo header consists of the Source IP Address, Destination IP Address, IP Protocol Number, and the total number of bytes in the TCP header and data. The latter field is calculated as follows:

Total Bytes in TCP Header and Data = IP Total Length - 4*(IP Header Length)

Note:	There is no length field in the TCP header that can be used. This must be calculated via the IP header.

Because the checksum is done in 16-bit quantities, a pad byte of zero may need to be placed adjacent to the last data byte. This is required in the case where the total number of bytes is odd. Figure 7-7 (IPv4) and Figure 7-8 (IPv6) illustrate the scope of the TCP checksum.

The RFE calculates a 16-bit one's complement sum over the TCP header, TCP data, and pseudo header. If the final result is FFFFh, then the packet passes the TCP checksum. If the final result is not FFFFh, then the checksum fails and the TCP/UDP/ICMP/IGMP Checksum Error bit is set.

If the IP packet is fragmented, the TCP checksum is not validated. A fragmented packet is determined by the following conditions.

- The first fragment is indicated by the IP header's MF flag being set and fragment offset having a value of zero.
- Subsequent fragments are determined by the IP Fragment Offset field having a value greater than zero.

Note:	See RFC 1624 for further details on checksum computation.

FIGURE 7-7: TCP CHECKSUM - IPV4

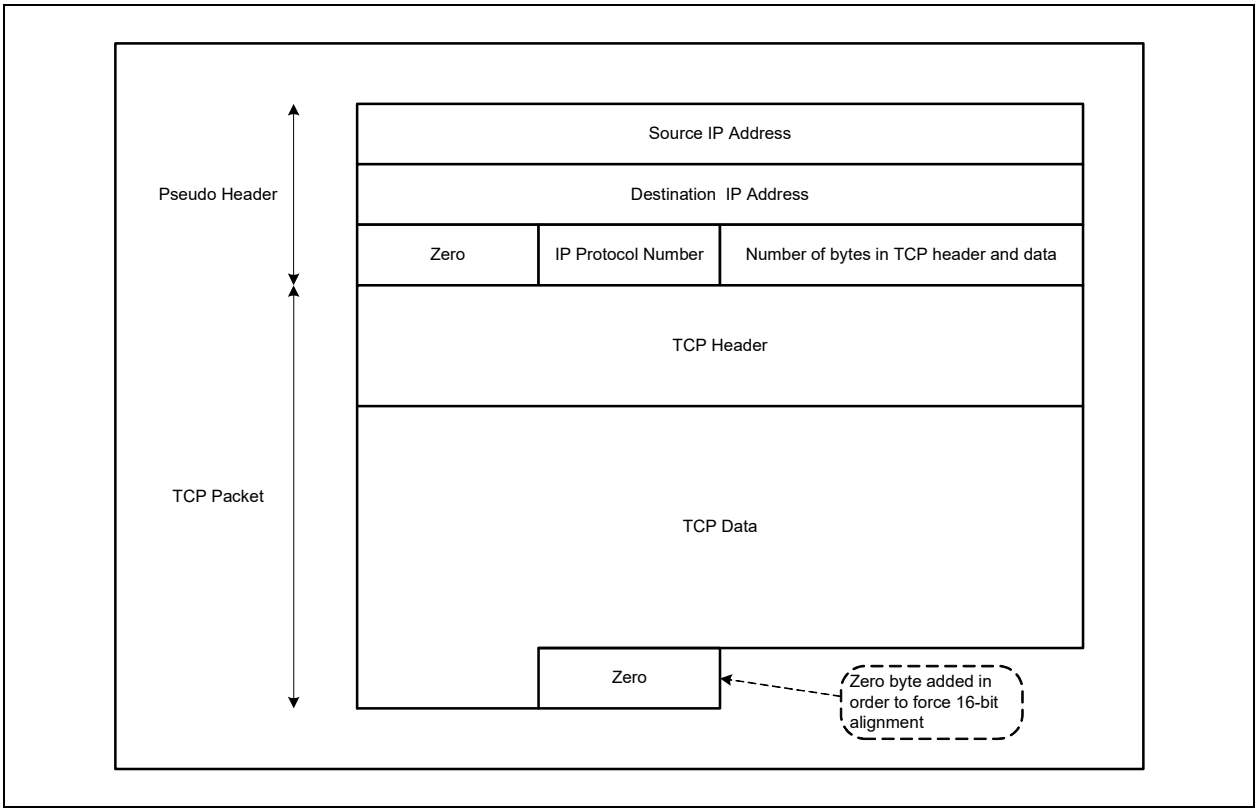

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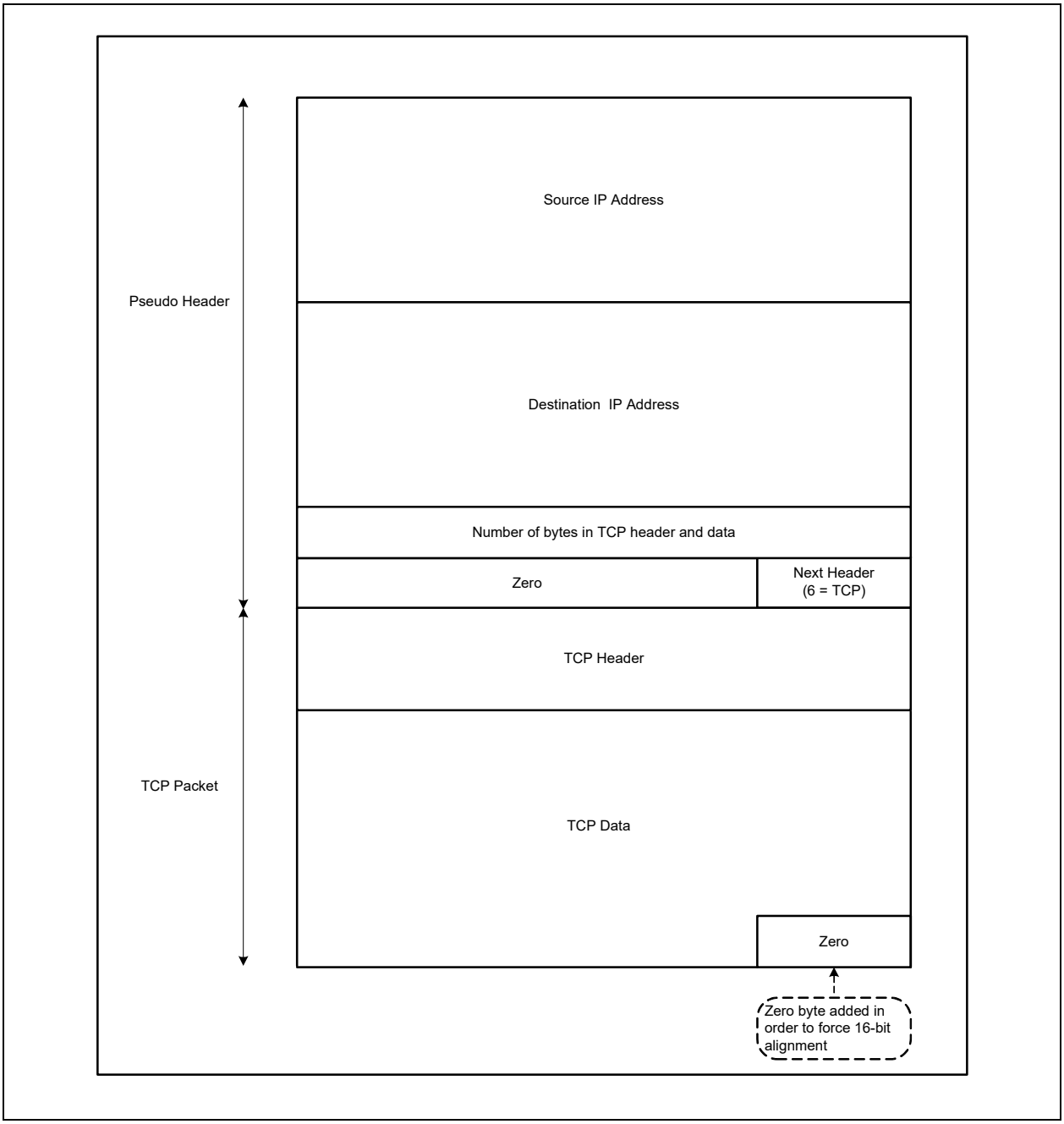
FIGURE 7-8: TCP CHECKSUM - IPV6



7.2.4 UDP CHECKSUM

If the RFE detects a UDP header, it will attempt to verify the UDP checksum when the Enable TCP/UDP Checksum Validation bit in the Receive Filtering Engine Control Register (RFE_CTL) is set. UDP is indicated when the IP protocol is 17. The UDP checksum calculation is nearly identical to the TCP checksum procedure. The scope of the UDP checksum is shown in Figure 7-9 (IPv4) and Figure 7-10 (IPv6).

Note:	The UDP Length field in the pseudo header is equivalent to the UDP message length in the UDP header. Therefore, unlike the TCP case, the length does not have to be calculated numerically from the IP header.

The UDP checksum is optional for IPv4. A value of 0000h indicates that the checksum is not used. If IPv4 is used, then the TCP/UDP/ICMP/IGMP Checksum Error status bit is not asserted after encountering this condition.

A zero UDP checksum is not valid for IPv6. When IPv6 is used, a checksum of 0000h results in the assertion of the TCP/UDP/ICMP/IGMP Checksum Error bit.

Note:	Typically, when the UDP checksum generation results in 0000h, a value of FFFFh (0-) is inserted into the UDP checksum field.

If the IP packet is fragmented, the UDP checksum is not validated. See Section 7.2.3 for further details on how to identify a fragmented packet.

FIGURE 7-9: UDP CHECKSUM - IPV4

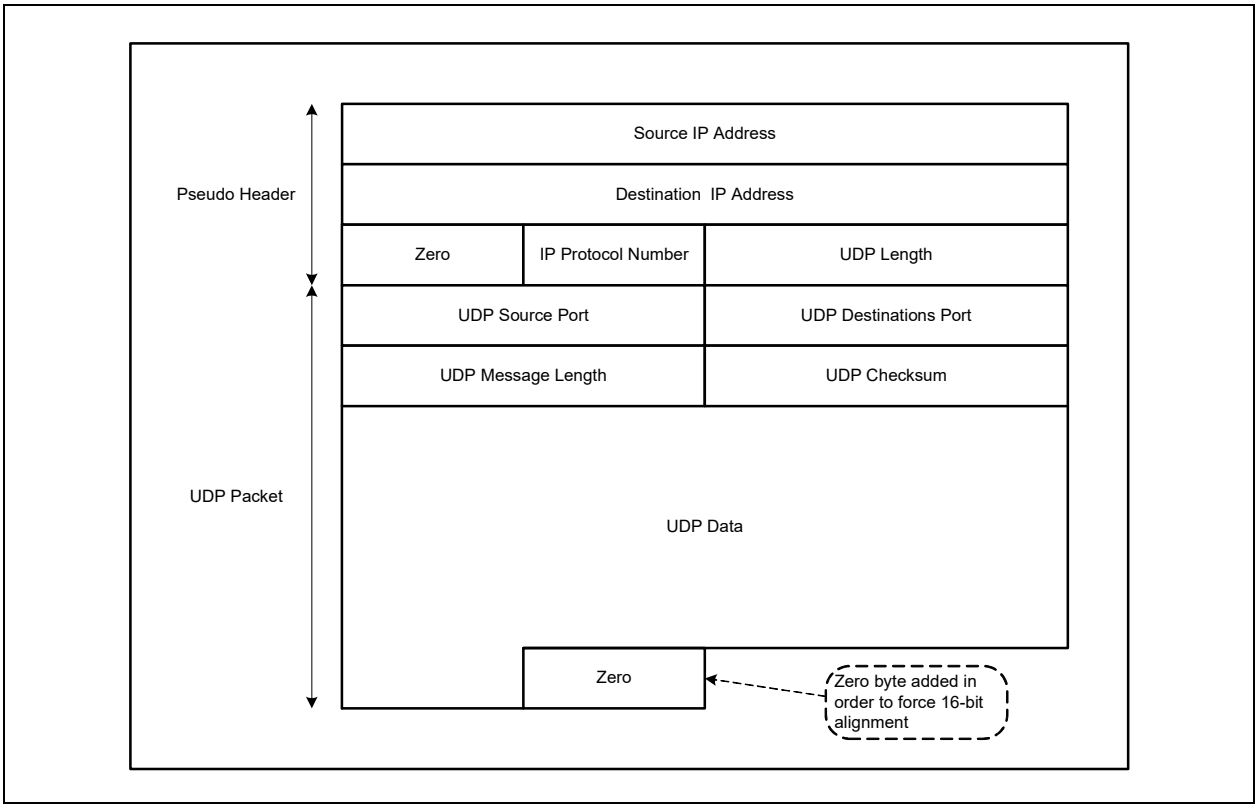


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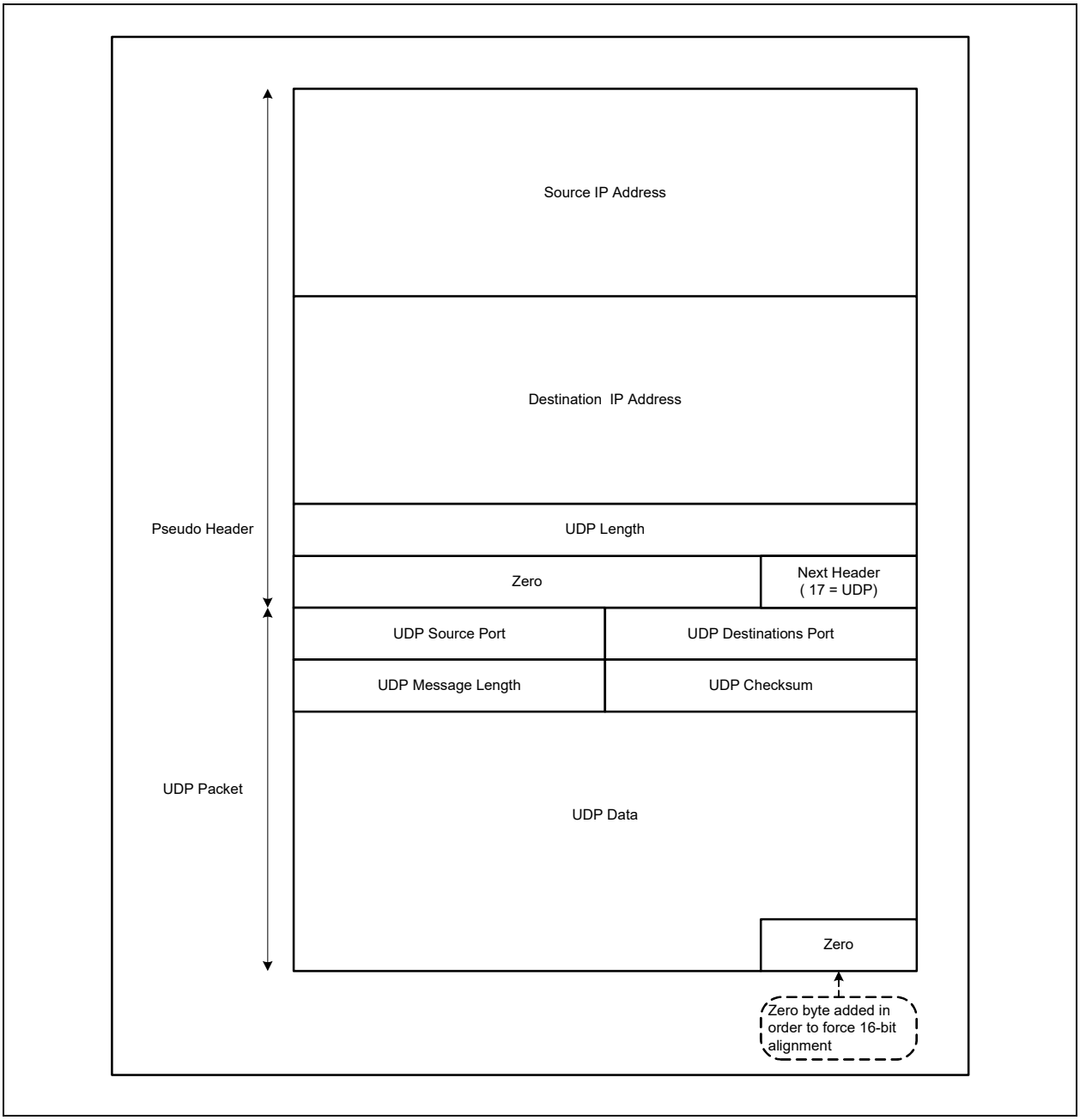
FIGURE 7-10: UDP CHECKSUM - IPV6



7.2.5 ICMP CHECKSUM

If the RFE detects an ICMP header, it will attempt to verify the ICMP checksum when configured. ICMP is indicated when the IP protocol is 1 for an IPv4 datagram. The ICMP checksum is the 16-bit ones complement of the one's complement sum of the ICMP message starting with the ICMP Type field.

ICMPv6 is utilized with IPv6. This is indicated by a next header value of 58. In this case the checksum is the 16-bit one's complement of the one's complement sum of the entire ICMPv6 message, starting with the ICMPv6 message type field, and prepended with a “pseudo-header” of IPv6 header fields. The inclusion of a pseudo-header in the ICMPv6 checksum is a change from IPv4. See Figure 7-8 for a definition of the IPv6 pseudo-header. The Next Header value used in the pseudo-header is 58.

ICMP checksum validation is enabled by setting the Enable ICMP Checksum Validation bit in the Receive Filtering Engine Control Register (RFE_CTL).

If the IP packet is fragmented, the ICMP checksum is not validated. See Section 7.2.3 for further details on how to identify a fragmented packet.

7.2.6 IGMP CHECKSUM

If the RFE detects an IGMP header, it will attempt to verify the IGMP checksum when configured. IGMP is indicated when the IP protocol is 2. The checksum is the 16-bit one's complement of the one's complement sum of the whole IGMP message (the entire IP payload).

IGMP checksum validation is enabled by setting the Enable IGMP Checksum Validation bit in the Receive Filtering Engine Control Register (RFE_CTL).

If the IP packet is fragmented, the IGMP checksum is not validated. See Section 7.2.3 for further details on how to identify a fragmented packet.

7.2.6.1 Checksum Summary

Table 7-2 summarizes the checksum offload ability of the RFE for various L3 and L4 configurations.

TABLE 7-2: CHECKSUM OFFLOAD CAPABILITY SUMMARY

PACKET TYPE	IP CHECKSUM CAPABLE	TCP/UDP CHECKSUM CAPABLE	ICMP CHECKSUM CAPABLE	IGMP CHECKSUM CAPABLE	RAW CHECKSUM
Type II Ethernet	Yes	Yes	Yes	Yes	Yes
SNAP Header	Yes	Yes	Yes	Yes	Yes
Single VLAN Tag	Yes	Yes	Yes	Yes	Yes
Stacked VLAN Tags	Yes	Yes	Yes	Yes	Yes
IPv4	Yes	Yes	Yes	Yes	Yes
IPv6	No	Yes	Yes	No	Yes
IP Fragment	Yes	No	No	No	Yes
IP Options	Yes	Yes	Yes	Yes	Yes
TCP or UDP Options	Yes	Yes	N/A	N/A	Yes
L4 protocol is not TCP or UDP	Yes	No	N/A	N/A	Yes
L3 protocol is not IP	No	No	No	No	Yes

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TABLE 7-2: CHECKSUM OFFLOAD CAPABILITY SUMMARY (CONTINUED)

PACKET TYPE	IP CHECKSUM CAPABLE	TCP/UDP CHECKSUM CAPABLE	ICMP CHECKSUM CAPABLE	IGMP CHECKSUM CAPABLE	RAW CHECKSUM
IPv6 with next header options Note 7-1	No	Yes	Yes	No	Yes
IPv6 tunneled over IPv4	Yes (IPv4)	Yes	Yes	No	Yes
IPv4 tunneled over IPv4	No	No	No	No	Yes

Note 7-1 Fragmentation is not supported. Hop-by-Hop, Destination, and Routing extension headers are supported.

8.0 10/100/1000 ETHERNET MAC

The Ethernet Media Access controller (MAC) incorporates the essential protocol requirements for operating an Ethernet/IEEE 802.3-compliant node and provides an interface to the Ethernet PHY. The MAC can operate in full-duplex 1000 Mbps or half/full-duplex 10/100 Mbps mode.

When operating in half-duplex mode, the MAC complies fully with Section 4 of ISO/IEC 8802-3 (ANSI/IEEE standard) and ANSI/IEEE 802.3 standards. When operating in full-duplex mode, the MAC complies with IEEE 802.3x full-duplex operation standard.

The MAC provides programmable enhanced features designed to minimize Host supervision, bus utilization, and pre- or post-message processing. These features include the ability to disable retries after a collision, dynamic FCS (Frame Check Sequence) generation on a frame-by-frame basis, automatic pad field insertion and deletion to enforce minimum frame size attributes, and automatic retransmission and detection of collision frames.

The primary attributes of the MAC Function are:

- Interfaces to Ethernet PHY
- Transmit and receive message data encapsulation
- Framing (frame boundary delimitation, frame synchronization)
- Error detection (physical medium transmission errors)
- FCS checking/stripping/generation
- Preamble stripping/generation
- Media access management
- Medium allocation (collision detection, except in full-duplex operation)
- Contention resolution (collision handling, except in full-duplex operation)
- Flow control during full-duplex mode
- Decoding of control frames (PAUSE command) and disabling the transmitter
- Generation of control frames (PAUSE command)
- Maintains minimum inter packet gap (IPG)
- Magic packet/Wake-On-LAN (WOL) detection
- Remote wakeup frame detection
- Neighbor Solicitation offload
- ARP offload
- Implements Simple Network Management Protocol (SNMP) and Remote Monitoring (RMON) management counter sets

The transmit and receive data paths are separate within the device from the MAC to the USB interface, allowing the highest performance, especially in full-duplex mode.

On the backend, the MAC interfaces with the PHY via internal GMII and MII ports. The GMII port is used for 1000 Mbps operation, while the MII port is used for 10/100 Mbps operation. The device's registers also provide a mechanism for accessing the PHY's registers through the internal SMI (Serial Management Interface) bus.

The FCT RX and TX FIFO, as well as the URX FIFO and UTX FIFO, allow increased packet buffer storage to the MAC. The FIFOs are a conduit between the USB interface and the MAC through which all transmitted and received data and various command/status information is passed. Deep FIFOs allow a high degree of latency tolerance relative to the various transport and OS software stacks, reducing and minimizing overrun conditions.

8.1 Collision Handling

When a collision is detected, the transmission of data is halted and a Jam pattern is transmitted. After a collision, the MAC will attempt to retransmit the frame. The time the frame is retransmitted is determined by the "truncated binary exponential back-off" algorithm. The back-off limit is selected by the Back Off Limit (BOLMT) field of the Hardware Configuration Register (HW_CFG). The units of the delay is slot times, where a slot time is equivalent to a 512-bit time. The MAC also controls the rewind_fr and release_fr signals to the FCT. The rewind_fr signal is used to support frame retransmission after a collision occurs. After a frame has been successfully transmitted or aborted due to excessive collisions or late collisions, the release_fr signal asserts to indicate the MAC is done processing the current frame and is ready for the next frame.

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Note: Half-duplex operation is not supported in 1000 Mbps mode.

8.2 Flow Control

The device's Ethernet MAC supports full-duplex flow control using the pause operation and control frame. Full-duplex flow control is also supported based on manual transmission of flow control frames or via automatic transmission of flow control frames, as determined by high and low watermark threshold levels in the RX FIFO.

8.2.1 FULL-DUPLEX FLOW CONTROL

The pause operation inhibits data transmission of data frames for a specified period of time. A Pause operation consists of a frame containing the globally assigned multicast address (01-80-C2-00-00-01) or the programmed unicast address, the PAUSE opcode, and a parameter indicating the quantum of slot time (512 bit times) to inhibit data transmissions. The PAUSE parameter may range from 0 to 65,535 slot times.

The RX Flow Control Enable (RX_FCEN) bit of the Flow Control Register (FLOW) enables the receive MAC flow control function. When this bit is set, the Ethernet MAC logic, on receiving a frame with the reserved multicast address or unicast address and PAUSE opcode, inhibits data frame transmissions for the length of time indicated. If a Pause request is received while a transmission is in progress, then the pause will take effect after the transmission is complete. Control frames are received and processed by the MAC. The setting of the Forward Pause Frames (FPF) bit of the Flow Control Register (FLOW) determines whether or not they are passed on.

Transmit pause frames may be generated manually, or automatically, based on RX FIFO threshold levels. Setting the Force Transmission of TX Flow Control Frame (FORCE_FC) bit of the Flow Control Register (FLOW) will initiate the transmission of a Pause Control Frame. The Pause time is specified in the Pause Time (FCPT) field of the Flow Control Register (FLOW).

The TX Flow Control Enable (TX_FCEN) bit of the Flow Control Register (FLOW) enables automatic generation of transmit pause frames. When this bit is set, the MAC uses the internal flow control on/off signals generated by the FCT to trigger pause frame transmission. The FCT signals the MAC whenever the threshold values programmed in the Flow Control Register (FLOW) are crossed. When the RX FIFO reaches the level set in the Flow Control On Threshold field of FCT Flow Control Threshold Register (FCT_FLOW), the FCT asserts the internal flow control on signal, which causes the MAC to transmit a pause frame containing the pause time specified in the Pause Time (FCPT) field of the FLOW register. When the RX FIFO drops below the level set in the Flow Control Off Threshold field of FCT_FLOW, the FCT asserts the internal flow control off signal, which causes the MAC to transmit a pause frame with a pause time of zero. The device will only send another pause frame when the RX FIFO level falls below the Flow Control Off Threshold and then exceeds the Flow Control On Threshold again.

8.3 Wake On LAN (WOL) Event Detection

8.3.1 OVERVIEW

The following bits of the Wakeup Control and Status Register 1 (WUCSR1), when enabled, may allow a WOL event detected by the Ethernet MAC to be asserted:

- Perfect DA Frame Received (PFDA_FR)
- Wakeup Frame Enable (WUEN)
- Magic Packet Enable (MPEN)
- Broadcast Wakeup Enable (BCAST_EN)

Similarly, the following bits of the Wakeup Control and Status Register 2 (WUCSR2), when enabled, may allow the assertion of a WOL event:

- IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN)
- IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN)

Whenever Wake-On-LAN Enable (WOL_EN) is set in the Power Management Control Register (PMT_CTL) and at least one of the previously listed enable bits is set, and the device is in the SUSPEND0 state, the following occurs when encountering a packet whose characteristics match those specified by the enable bit(s):

- Store frame in RX FIFO when in SUSPEND3
- The appropriate status bits are set in Wakeup Control and Status Register 1 (WUCSR1) and Wakeup Source Register (WK_SRC), depending of the settings of the enable bits and the characteristics of the packet.

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- A wakeup event is signaled to the host.
- The Host sends resume signaling.
- All wakeup status bits are cleared in Wakeup Control and Status Register 1 (WUCSR1) and Wakeup Control and Status Register 2 (WUCSR2) if the Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) bit is set in the Power Management Control Register (PMT_CTL).
- All wakeup enable bits in Wakeup Control and Status Register 1 (WUCSR1) and Wakeup Control and Status Register 2 (WUCSR2) are cleared if the Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) bit is set in the Power Management Control Register (PMT_CTL).
- The device transitions to the Normal state.
- The Host then examines data within the device's registers and memory to determine what occurred.

Note: Multiple status bits may be set in WUCSR and WUCSR2 for the packet. I.e., assume Perfect DA Frame Received (PFDA_FR) and IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN) are set. Then Perfect DA Frame Received (PFDA_FR) and IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) will be set when an IPv4 TCP SYN packet matching the parameters set by the SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC), SYN IPv4 Destination Address Register (SYN_IPV4_ADDR_DEST), and SYN IPv4 TCP Ports Register (SYN_IPV4_TCP_PORTS) is received.

Note: If Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set in Power Management Control Register (PMT_CTL), no status bits will be available for examination. To get this information Wakeup Source Register (WK_SRC) may be consulted.

8.3.2 DETECTION OF WOL EVENTS

The following sections describe, in general terms, each of the WOL events that may be enabled. They assume the following:

- Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) and Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) bits **are NOT set** in the Power Management Control Register (PMT_CTL).

8.3.2.1 Perfect DA Detection

Setting the Perfect DA Wakeup Enable (PFDA_EN) bit in the Wakeup Control and Status Register 1 (WUCSR1) and entering SUSPEND0, SUSPEND1 or SUSPEND3 states places the MAC in the Perfect DA detection mode. In this mode, normal data reception is disabled, and detection logic within the MAC examines the destination address of each received frame. When a frame whose destination address matches that specified by the MAC Receive Address High Register (RX_ADDRH) and MAC Receive Address Low Register (RX_ADDRL) is received, the Perfect DA Frame Received (PFDA_FR) bit in WUCSR1 is set, and remote wakeup is issued. The Host will then resume the device. The Host may read WUSCR1 and WUSCR2 registers to determine the characteristics of the received packet and the condition(s) that caused the remote wakeup.

Note: More than just the Perfect DA Frame Received (PFDA_FR) bit may be set for the packet in WUCSR1 and WUCSR2, depending on the setting of the enable bits and the packet's characteristics.

The Perfect DA Wakeup Enable (PFDA_EN) bit, as well as all other enable bits in WUCSR1 and WUCSR2 must be cleared in order to permit the MAC to resume normal receive operation. The Host must also clear all status bits in WUCSR1 and WUCSR2 before entering the SUSPEND0, SUSPEND1 or SUSPEND3 state to monitor for the next WOL event.

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8.3.2.2 Wakeup Frame Detection

Thirty two programmable wakeup frame filters are supported. Each filter has a 128-bit byte mask that indicates which bytes of the frame should be compared by the MAC. A CRC-16 is calculated over these bytes. The result is then compared with the filter's respective CRC-16 to determine if a match exists.

Setting the Wakeup Frame Enable (WUEN) bit in the Wakeup Control and Status Register 1 (WUCSR1), places the MAC in the Wakeup Frame detection mode. In this mode, normal data reception is disabled, and detection logic within the MAC examines receive data for the pre-programmed Wakeup Frame patterns. When a wakeup pattern is received, the Remote Wakeup Frame Received (WUFR) bit in the WUCSR is set, the device places itself in a fully operational state, and remote wakeup is issued. The Host will then resume the device and read the WUSCR1 and WUCSR2 registers to determine the condition(s) that caused the remote wakeup.

Note:	More than just the Remote Wakeup Frame Received (WUFR) bit may be set for the packet in WUCSR1 and WUCSR2, depending on the setting of the enable bits and the packet's characteristics.

The Wakeup Frame Enable (WUEN) bit, as well as all other enable bits in WUCSR1 and WUCSR2 must be cleared in order to permit the MAC to resume normal receive operation. The Host must also clear all status bits in WUCSR1 and WUCSR2 before entering the SUSPEND0, SUSPEND1 or SUSPEND3 state to monitor for the next WOL event.

Before putting the MAC into the Wakeup Frame detection state, the application program must provide the detection logic with a list of sample frames and their corresponding byte masks. This information is provided by writing the Wakeup Filter x Configuration Register (WUF_CFGx), and the Wakeup Filter x Byte Mask Registers (WUF_MASKx) for all enabled filters. Please refer to the indicated sections for additional information on these registers.

The MAC provides 32 programmable filters that support many different receive packet patterns. Whether or not a filter is enabled, and the destination address type of an enabled filter, is determined by the Filter Enable and Filter Address Type fields, respectively, of the Wakeup Filter x Configuration Register (WUF_CFGx).

If remote wakeup mode is enabled, the remote wakeup function receives all frames addressed to the MAC. It then checks each frame against the enabled filters and recognizes the frame as a remote Wakeup Frame if it passes an enabled filter's address filtering and CRC value match.

In order to determine which bytes of the frames should be checked by the CRC module, the MAC uses a programmable byte mask and a programmable pattern offset for each of the eight supported filters.

The pattern offset defines the location of the first byte that should be checked in the frame. The byte mask is a 128-bit field that specifies whether or not each of the 128 contiguous bytes within the frame, beginning with the pattern offset, should be checked. If bit j in the byte mask is set, the detection logic checks byte (pattern offset + j) in the frame, otherwise, byte (pattern offset + j) is ignored.

At the completion of the CRC-16 checking process, the CRC-16 calculated using the pattern offset and byte mask is compared to the expected CRC-16 value associated with the filter. If a match occurs, a remote wakeup event is signaled.

The pattern offset and expected CRC-16 for a particular filter is determined by the Filter Pattern Offset and Filter CRC-16 fields, respectively, of the Wakeup Filter x Configuration Register (WUF_CFGx). The byte mask for a particular filter is set by the Host by writing the four DWORD mask registers associated with the filter in the Wakeup Filter x Byte Mask Registers (WUF_MASKx) block.

CRC-16 is calculated as follows:

At the start of a frame, CRC-16 is initialized with the value FFFFh. CRC-16 is updated when the pattern offset and mask indicate the received byte is part of the checksum calculation. The following algorithm is used to update the CRC-16 at that time:

Let:

^ denote the exclusive or operator.

Data [7:0] be the received data byte to be included in the checksum.

CRC[15:0] contain the calculated CRC-16 checksum.

F0 … F7 be intermediate results, calculated when a data byte is determined to be part of the CRC-16.

Calculate:

F0 = CRC[15] ^ Data[0]

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F1 = CRC[14] ^ F0 ^ Data[1]

F2 = CRC[13] ^ F1 ^ Data[2]

F3 = CRC[12] ^ F2 ^ Data[3]

F4 = CRC[11] ^ F3 ^ Data[4]

F5 = CRC[10] ^ F4 ^ Data[5]

F6 = CRC[09] ^ F5 ^ Data[6]

F7 = CRC[08] ^ F6 ^ Data[7]

The CRC-16 is updated as follows:

CRC[15] = CRC[7] ^ F7

CRC[14] = CRC[6]

CRC[13] = CRC[5]

CRC[12] = CRC[4]

CRC[11] = CRC[3]

CRC[10] = CRC[2]

CRC[9] = CRC[1] ^ F0

CRC[8] = CRC[0] ^ F1

CRC[7] = F0 ^ F2

CRC[6] = F1 ^ F3

CRC[5] = F2 ^ F4

CRC[4] = F3 ^ F5

CRC[3] = F4 ^ F6

CRC[2] = F5 ^ F7

CRC[1] = F6

CRC[0] = F7

Table 8-1 indicates the cases that produce a wakeup event when the Wakeup Frame Enable (WUEN) bit in the Wakeup Control and Status Register 1 (WUCSR1) is set. All other cases do not generate a wakeup event.

TABLE 8-1: WAKEUP GENERATION CASES

FILTER ENABLED (Note 8-1)	CRC MATCH (Note 8-2)	PASS REGULAR RECEIVE FILTER	ADDRESS TYPE (Note 8-3)	WAKEUP PACKET TYPE SUPPORTED
Yes	Yes	Yes	Multicast (=10b)	Multicast
Yes	Yes	Yes	Unicast (=00b)	Unicast
Yes	Yes	Yes	Passed Receive Filter (=x1b)	Broadcast, Multicast, Unicast

Note 8-1 As determined by the Filter Enable bit of the respective Wakeup Filter x Configuration Register (WUF_CFGx).

Note 8-2 CRC matches Filter *x* CRC-16, as determined by the Filter CRC-16 field of the respective Wakeup Filter x Configuration Register (WUF_CFGx).

Note 8-3 As determined by the Filter Address Type field of the Wakeup Filter x Configuration Register (WUF_CFGx).

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Note: x indicates “don’t care”.

8.3.2.3 Magic Packet Detection

Setting the Magic Packet Enable (MPEN) bit in the Wakeup Control and Status Register 1 (WUCSR1) places the MAC in the “Magic Packet” detection mode. In this mode, normal data reception is disabled, and detection logic within the MAC examines receive data for a Magic Packet.

When a Magic Packet is received, the Magic Packet Received (MPR) bit in the WUCSR is set, the device places itself in a fully operational state, and remote wakeup is issued. The Host will then resume the device and read the WUSCR1 and WUCSR2 registers to determine the condition(s) that caused the remote wakeup.

Note: More than just the Magic Packet Received (MPR) bit may be set for the packet in WUCSR1 and WUCSR2, depending on the setting of the enable bits and the packet’s characteristics.

The Magic Packet Enable (MPEN) bit, as well as all other enable bits in WUCSR1 and WUCSR2 must be cleared in order to permit the MAC to resume normal receive operation. The Host must also clear all status bits in WUCSR1 and WUCSR2 before entering the SUSPEND0, SUSPEND1 or SUSPEND3 state to monitor for the next WOL event.

In Magic Packet mode, logic within the MAC constantly monitors each frame addressed to the node for a specific Magic Packet pattern. It checks packets with the MAC’s address or a multicast address (which includes the broadcast address) to meet the Magic Packet requirement.

Note: The MAC’s address is specified by the MAC Receive Address High Register (RX_ADDRH) and the MAC Receive Address Low Register (RX_ADDRL).

The MAC checks each received frame for the pattern 48‘hFF_FF_FF_FF_FF_FF synchronization stream after the destination and source address field. Then the MAC inspects the frame for 16 repetitions of the MAC address without any breaks or interruptions. In case of a break in the 16 address repetitions, the MAC scans for the 48‘hFF_FF_FF_FF_FF_FF pattern again in the incoming frame.

The 16 repetitions may be anywhere in the frame but must be preceded by the synchronization stream. The device will also accept a multicast frame, as long as it detects the 16 duplications of the MAC address. If the MAC address of a node is 00h 11h 22h 33h 44h 55h, then the MAC scans for the following data sequence in an Ethernet frame:

Destination Address Source Address ……FF FF FF FF FF FF

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

…FCS

8.3.2.4 Broadcast Detection

Setting the Broadcast Wakeup Enable (BCAST_EN) bit in the Wakeup Control and Status Register 1 (WUCSR1) and entering SUSPEND0, SUSPEND1 or SUSPEND3 states places the MAC in the Broadcast detection mode. In this mode, normal data reception is disabled, and detection logic within the MAC examines the destination address of each received frame. When a frame whose destination address is FF FF FF FF FF FF is received, the Broadcast Frame Received (BCAST_FR) bit in the WUCSR is set, the device places itself in a fully operational state, and remote wakeup is issued. The Host will then resume the device and read the WUSCR1 and WUCSR2 registers to determine the condition(s) that caused the remote wakeup.

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Note:	More than just the Broadcast Frame Received (BCAST_FR) bit may be set for the packet in WUCSR1 and WUCSR2, depending on the setting of the enable bits, the packet's characteristics, and the programming of the MAC Receive Address High Register (RX_ADDRH) and the MAC Receive Address Low Register (RX_ADDRL). I.e., if, for some reason, RX_ADDRH and RX_ADDRL retain their default values, then Broadcast Frame Received (BCAST_FR), as well as Perfect DA Frame Received (PFDA_FR) would be set on reception of a Broadcast frame.

The Broadcast Wakeup Enable (BCAST_EN) bit, as well as all other enable bits in WUCSR1 and WUCSR2 must be cleared in order to permit the MAC to resume normal receive operation. The Host must also clear all status bits in WUCSR1 and WUCSR2 before entering the SUSPEND0, SUSPEND1 or SUSPEND3 states to monitor for the next WOL event.

8.3.3 TCP SYN DETECTION

The device supports wakeup on receiving a TCP SYN packet over a IPv4 or a IPv6 frame. The Wakeup Control and Status Register 2 (WUCSR2) contains the bits that control this and other Windows 7 Power Management features. Two sets of registers are used to control TCP SYN Detection - one set for IPv4 and another for IPv6. Their use is discussed in the following sections.

Note:	TCP SYN Detection should be enabled for use when the device is being programmed to enter the SUSPEND0, SUSPEND1 or SUSPEND3 states, in anticipation of generating a WOL event. Its use in any state other than SUSPEND0, SUSPEND1 or SUSPEND3, may result in untoward operation and unexpected results.

The following sections describe, in general terms, each of the TCP SYN events that may be enabled. They assume that Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) and Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) bits **are NOT set** in the Power Management Control Register (PMT_CTL).

8.3.3.1 IPv4 TCP SYN Detection

The following registers are dedicated for use in detecting a TCP SYN packet within an IPv4 frame:

- SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC)
- SYN IPv4 Destination Address Register (SYN_IPV4_ADDR_DEST)
- SYN IPv4 TCP Ports Register (SYN_IPV4_TCP_PORTS)

Note:	The registers can be set to force a match to occur with the field its contents are being compared to. Please refer to the register definition for details.

IPv4 TCP SYN detection occurs when the IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN) bit is set in Wakeup Control and Status Register 2 (WUCSR2) and the device is in the SUSPEND0, SUSPEND1 or SUSPEND3 states. When these conditions are met, logic within the MAC will process IPv4 frames whose destination address is the device's MAC address, a multi-cast address, or the broadcast address as follows:

A check is made for a TCP protocol match within the IPv4 header. Valid TCP packets whose SYN bit is asserted, having an IPv4 header whose source address and destination address match those specified in the SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC) and the SYN IPv4 Destination Address Register (SYN_IPV4_ADDR_DEST), respectively, and whose source port and destination port match those specified by the SYN IPv4 TCP Ports Register (SYN_IPV4_TCP_PORTS), will cause a wakeup. Upon detecting a wakeup condition, the IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) bit is set in WUSCR2, the device places itself in a fully operational state, and remote wakeup is issued.

The Host will then resume the device and read the WUSCR1 and WUCSR2 registers to determine the condition(s) that caused the remote wakeup.

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Note:	More than just the IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) bit may be set for the packet in WUCSR1 and WUCSR2, depending on the setting of the enable bits and the packet's characteristics.

The IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN) bit, as well as all other enable bits in WUCSR1 and WUCSR2 must be cleared in order to permit the MAC to resume normal receive operation. The Host must also clear all status bits in WUCSR and WUCSR2 before entering the SUSPEND0, SUSPEND1 or SUSPEND3 states to monitor for the next WOL event.

Note:	The IPv4 TCP SYN packet must be valid in order for packet detection to be signaled. The header checksum, TCP checksum, and FCS are calculated and all must agree with the packet contents, in order for the packet to be considered for detection analysis.

8.3.4 IPV6 TCP SYN DETECTION

The following registers are dedicated for use in detecting a TCP SYN packet within an IPv6 frame:

- SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC)
- SYN IPv6 Destination Address Register (SYN_IPV6_ADDR_DEST)
- SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS)

Note:	The registers can be set to force a match to occur with the protocol field its contents is being compared to. Please refer to the register definition for details.

IPv6 TCP SYN detection occurs when the IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN) bit is set in WUCSR2 and the device is in the SUSPEND0, SUSPEND1 or SUSPEND3 states. When these conditions are met, logic within the MAC will process IPv6 frames whose destination address is the device's MAC address, a multi-cast address, or the broadcast address as follows:

A check is made for a TCP protocol match within the IPv6 header (or an extension header). Valid TCP packets whose SYN bit is asserted, having an IPv6 header whose source address and destination address match those specified in the SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC) and the SYN IPv6 Destination Address Register (SYN_IPV6_ADDR_DEST), respectively, and whose TCP ports in the IPv6 payload (TCP packet) match those specified by the SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS), will cause a wakeup. Upon detecting a wakeup condition, the IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) bit is set in WUSCR2, the device places itself in a fully operational state, and remote wakeup is issued.

The Host will then resume the device and read the WUSCR1 and WUCSR2 registers to determine the condition(s) that caused the remote wakeup.

Note:	More than just the IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) bit may be set for the packet in WUCSR1 and WUCSR2, depending on the setting of the enable bits and the packet's characteristics.

The IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN) bit, as well as all other enable bits in WUCSR1 and WUCSR2 must be cleared in order to permit the MAC to resume normal receive operation. The Host must also clear all status bits in WUCSR1 and WUCSR2 before entering the SUSPEND0, SUSPEND1 or SUSPEND3 states to monitor for the next WOL event.

Note:	The IPv6 TCP SYN packet must be valid in order for packet detection to be signaled. The TCP checksum and FCS are calculated and must agree with the packet contents, in order for the packet to be considered for detection analysis.

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8.4 Always on Always Connected (AOAC)

This device supports the Connected Standby state of Microsoft's instant-on and always-connected power model, similar to smart-phone devices. The intent of Connected Standby is to enable a PC to resume from sleep extremely quickly - typically less than 500 milliseconds. The performance of a resume from Connected Standby is almost always faster than the traditional Sleep (S3) state and significantly faster than a resume from Hibernate (S4) or Shutdown (S5).

Note:	AOAC and Connected Standby were introduced for Windows 8.X operating systems.

In Connected Standby certain networking tasks are offloaded from the host CPU by the device to conserve system power and to enable the network to maintain basic L2 connectivity. For this device, ARP and NS offloads are enabled to minimize host wake ups. Additionally, the device is configured to detect a wakeup event and upon detection awakens the CPU.

In the case the wake event is a wakeup frame, it is stored in the FCT RX FIFO. This is required to maintain higher layer protocol connections and enable the host software to determine the cause of the wake up. Any frames received after the wakeup event are also stored in the FCT RX FIFO. This coalescing of packets allows windows to process batches of packets in a single pass without potentially breaking any protocols.

The following wake events are supported in Connected Standby.

- WOL (Wakeup Frame, Magic Packet)
- Broadcast Frame
- Perfect DA
- Link Status Connected
- Link Status Disconnected
- GPIO Assertion
- TCP SYN

The steps for AOAC support are as follows.

1. An extended period of time expires with out an Ethernet packet or transmission or reception. The timescale is typically in the order of seconds.
2. Driver enables SUSPEND3 in Power Management Control Register (PMT_CTL).
3. Driver enables NS Offload and ARP Offload.
4. Driver configures desired wakeup events.
5. Driver enables wakeup packet storage in FCT RX FIFO via the Store Wakeup Frame (STORE_WAKE) bit in the Wakeup Control and Status Register 1 (WUCSR1).
6. Device is suspended by host.

8.5 Neighbor Solicitation (NS) Offload

NS Offload is a power management feature that permits the device to respond to a NS request by generating and transmitting the required NA response packet. It will not result in the generation of a wake event.

The following registers are used to facilitate NS offload:

- NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST)
- NSx IPv6 Source Address Register (NSx_IPV6_ADDR_SRC)
- NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0)
- NSx ICMPv6 Address 1 Register (NSx_ICMPV6_ADDR1)

Note:	For all registers, 0<=x<=1

Note:	The registers can be set to force a match to occur with the protocol field its contents is being compared to. Please refer to the register definition for details.

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These registers are used when the NS Offload Enable (NS_OFFLOAD_EN) bit is set in Wakeup Control and Status Register 2 (WUCSR2). When enabled, logic within the MAC shall examine all IPv6 frames whose Ethernet destination address matches either the device's MAC address, a multi-cast address, or is the broadcast address. Frames not meeting this criteria shall be ignored.

The headers of all IPv6 frames matching the aforementioned criteria are further checked as follows. IPv6 DA is compared to NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST) and NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0) and NSx ICMPv6 Address 1 Register (NSx_ICMPV6_ADDR1). One of the three compares must match. IPv6 SA is compared to NSx IPv6 Source Address Register (NSx_IPV6_ADDR_SRC).

When NSx IPv6 Source Address Register (NSx_IPV6_ADDR_SRC) is set to 0h, the IPv6 SA check is ignored. A match is yielded.

In the event that the IPv6 header destination address is a solicited node multicast address (i.e. it has a prefix that matches FF02.1:FF00:0/104), only the upper three bytes (NSx_IPv6_ADDR_DEST_3 [127:104]) of NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST) are compared against the last 24 bits of the IPv6 header destination address.

If both IPv6 DA and SA checks pass, and the Next Header field of the IPv6 header (or any extension headers) specify ICMPv6 (58), then a check is made to determine whether an NS (Neighbor Solicitation) request is being made (ICMP type = 135 and code = 0 within the ICMPv6 header).

If so, the target address specified in the NS request is compared to the addresses contained in the NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0) and NSx ICMPv6 Address 1 Register (NSx_ICMPV6_ADDR1). If a match occurs on either comparison, and the ICMPv6 checksum is good, and no other errors occurred in the frame, then the MAC shall transmit an NA response frame to the sender.

The NS frame must be validated per the checks defined in section 7.1.1 of RFC 4861. Frames that fail the validation checks are discarded.

NA response frames have the following characteristics:

Frame header:

- DA = SA from frame header of the NS packet
- SA = device's MAC address
- Type = 86DDh

IPv6 header:

- SA = When NA SA Select (NA_SA_SEL) of Wakeup Control and Status Register 2 (WUCSR2) is cleared, the Target address from the NS packet is used. When set, the value in NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST) is used.
- DA = SA of NS packet, if specified. If NS packet contained an unspecified address (0::0) in its IPv6 SA, then DA = FF02:0:0:0:0:0:0:1
- Hop limit = 255

ICMPv6:

- Type = 136
- Code = 0
- Checksum = set to the checksum - 16-bit 1's complement of the 1's complement sum calculated over the entire message starting with a "pseudo-header" of the IPv6 header fields (next header is 58)
- Router flag = 0
- Solicited flag = 1 if Destination Address is not equal to FF02:0::1, otherwise 0
- Override flag = 1
- Reserved = 0 (This is a 29 bit field)
- Target address = target address from the NS packet
- Option = device's MAC address (same as frame header)

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Note: The IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) bit in Wakeup Control and Status Register 2 (WUCSR2) is set whenever a NS packet is received during the time interval between NS Offload Enable (NS_OFFLOAD_EN) being set and subsequently cleared. This bit, and all other status bits contained in Wakeup Control and Status Register 1 (WUCSR1) and Wakeup Control and Status Register 2 (WUCSR2) should be cleared prior to entering a SUSPEND state. NS Packet Received (NS_RCD) will be automatically cleared when exiting a SUSPEND state whenever the Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) bit is set in the Power Management Control Register (PMT_CTL).

8.6 ARP Offload

ARP Offload is a power management feature that permits the device to respond to an ARP request by generating and transmitting the required response packet.

The following registers are used to facilitate ARP offload:

- ARP Sender Protocol Address Register (ARP_SPA)
- ARP Target Protocol Address Register (ARP_TPA)

Note: The registers can be set to force a match to occur with the protocol field its contents is being compared to. Please refer to the register definition for details.

These registers are used when the ARP Offload Enable (ARP_OFFLOAD_EN) bit is set in WUCSR2. When enabled, logic within the MAC will examine the frame type of all received Ethernet frames. ARP frames (those having a frame type of 0806h) whose destination address matches the device's MAC address or is the broadcast address will further be examined. Frames that are not ARP frames or frames that are ARP frames, but whose destination address did not fit the selection criteria, will be ignored.

The following fields of the ARP header are checked to ensure they are set to the indicated values. if a mismatch occurs, the frame is ignored.

- Hardware Type (HTYPE) - 0x0001 for Ethernet
- Protocol Type (PTYPE) - 0x0800 for IPv4
- Hardware Address Length (HLEN) - 0x06 for Ethernet
- Protocol Address Length (PLEN) - 0x04 for IPv4
- Opcode (OP) - 0x0001 for Request

The contents of the ARP Sender Protocol Address Register (ARP_SPA) and ARP Target Protocol Address Register (ARP_TPA) are compared to the SPA and TPA fields, respectively, of the ARP message. If the contents of both registers match the contents of the message, then the MAC TX is signaled to transmit an ARP response frame to the sender.

ARP response frames have the following characteristics:

Frame header:

- DA = SA from frame header of the ARP packet
- SA = device's MAC address
- Type = 0806h

ARP message:

- Hardware type = 1
- Protocol type = 0800h
- Hardware length = 6
- Protocol length = 4
- Sender HA = device's MAC address
- Sender IP = TPA field from the ARP request packet
- Target HA = SHA field from the ARP request packet
- Target IP = SPA field from the ARP request packet

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Note: The ARP Packet Received (ARP_RCD) bit in WUCSR2 is set whenever a ARP request is received during the time interval between ARP Offload Enable (ARP_OFFLOAD_EN) being set and subsequently cleared. This bit, and all other status bits contained in WUCSR1 and WUCSR2 should be cleared prior to entering a SUSPEND state. ARP Packet Received (ARP_RCD) will be automatically cleared when exiting a SUSPEND state whenever the Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) bit is set in the Power Management Control Register (PMT_CTL).

Note: The ARP Offload Enable (ARP_OFFLOAD_EN) bit of the WUCSR2 register must be cleared in order for the MAC to resume normal receive and transmit operation. Failure to clear this bit and all other enable bits contained in WUCSR1 and WUCSR2 upon returning to the Normal state, or setting this bit during normal operation, will result in untoward operation and unexpected results.

8.7 Automatic Speed and Duplex Detection

The device permits manual or automatic control of speed and duplex operation.

The Automatic Speed Detection (ASD) bit in the MAC Control Register (MAC_CR) controls whether or not the MAC operational speed is determined automatically or is manually set. When ASD is set, the MAC ignores the setting of the MAC Configuration (CFG) field of the MAC Control Register (MAC_CR) and automatically determines the speed of operation. The MAC samples an internal receive clock signal to accomplish speed detection and reports the last determined speed via the MAC Configuration (CFG) field. When ASD is zero, the setting of the MAC Configuration (CFG) field determines operational speed.

The Automatic Duplex Detection (ADD) bit in the MAC Control Register (MAC_CR) controls whether or not the MAC operates in manual or automatic duplex mode of operation. When this bit is set, the MAC ignores the setting of the Duplex Mode (DPX) bit in the MAC Control Register (MAC_CR) and automatically determines the duplex operational mode. The MAC uses the PHY status signal to accomplish mode detection and reports the last determined status via the Duplex Mode (DPX) bit. When ADD is zero, the setting of the Duplex Mode (DPX) bit determines Duplex operation.

See Section 9.1, "Category 5 Twisted Pair Media Interface" for additional information.

On loss of SYNC, the MAC will commence automatic speed and/or duplex detection, depending on the setting of ASD/ADD.

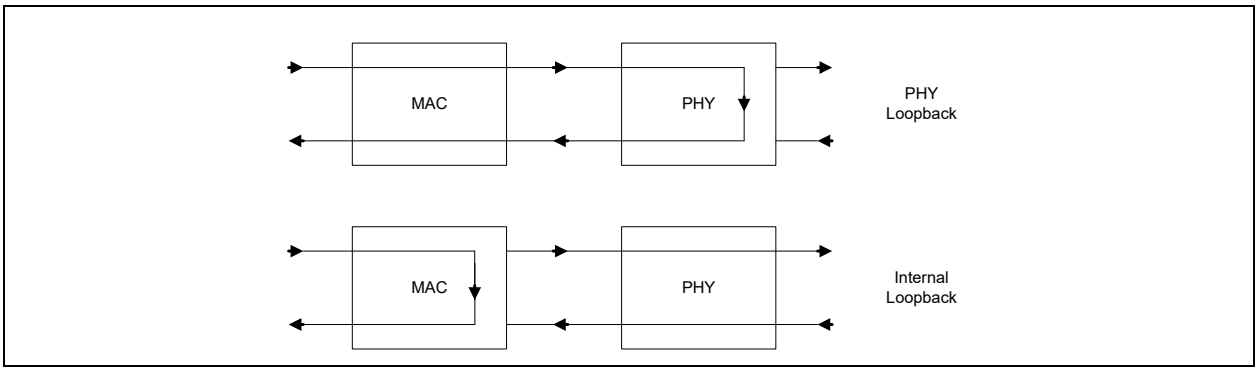
8.8 Loopback Operation

The following Loopback modes are available:

- PHY Loopback Mode
- MAC Internal Loopback Mode

This mode is configured via the Internal Loopback Operation Mode (INT_LOOP) bit of the MAC Control Register (MAC_CR). It is only valid in full-duplex mode of operation. In this loopback mode, the TX frame is received by the Internal GMII interface and is sent back to the MAC without being sent to the PHY.

FIGURE 8-1: LOOPBACK OPERATIONAL MODES



8.9 802.3az EEE Support

The device supports Energy Efficient Ethernet as defined in revision IEEE 802.3az-2012 of the standard. EEE support is enabled by the Energy Efficient Ethernet Enable (EEEEN) bit of the MAC Control Register (MAC_CR).

8.9.1 TX LPI GENERATION

The process of when the MAC should indicate LPI requests to the PHY is divided into two sections.

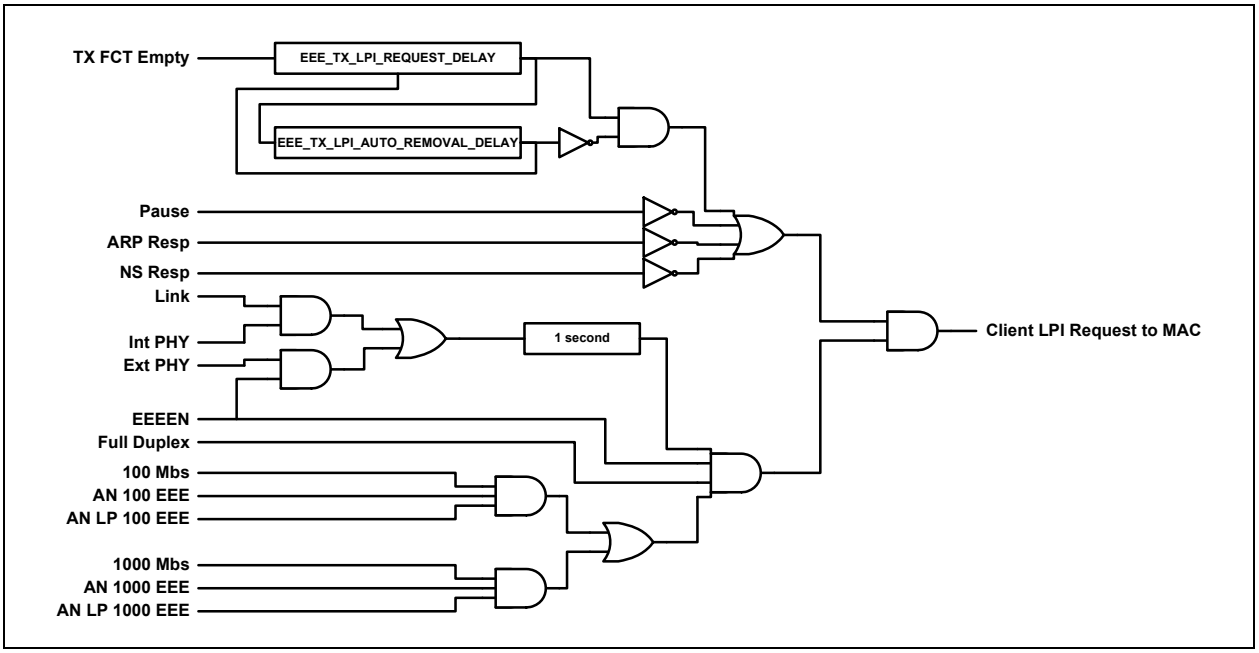
First is the concept of the “Client”, which is basically any source of data that the MAC needs to transmit. This includes packet data via the TX FCT, pause frames request via the RX FCT and ARP and NS offload frames internally generated by the MAC due to the reception of certain frames.

The second section is the MAC low level FSM, which includes the concepts of IDLE, DEFERRAL, IFG, PREAMBLE and DATA / FCS.

8.9.1.1 Client LPI Requests to MAC

The Client to MAC LPI request process is shown in Figure 8-2.

FIGURE 8-2: CLIENT LPI REQUEST GENERATION



When the TX FCT is empty for a time (in microseconds) specified in EEE TX LPI Request Delay Count Register (EEE_TX_LPI_REQUEST_DELAY_CNT) a TX LPI request is asserted to the MAC. This is managed by the internal FCT TX Empty Timer. A setting of 0 us is possible for this time. If the TX FCT becomes not empty while the timer is running, the timer will reset (i.e. empty time is not cumulative). Once TX LPI is requested and the TX FCT becomes not empty, the TX LPI request is negated. The Client shall return to waiting for the TX FCT to be empty. Note that it is conceivable for the TX LPI request to the MAC to only be asserted for a single clock cycle.

The TX LPI request can optionally be automatically removed after the time specified in the EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY) in anticipation of periodic transmissions. This function is enabled with the Energy Efficient Ethernet TX LPI Automatic Removal Enable (EEE_TX_LPI_AUTO_REMOVAL_EN) bit. The TX FCT Empty timer is reset and the client returns to waiting for the TX FCT to be empty for the request delay time as above.

TX LPI requests are asserted only if the Energy Efficient Ethernet Enable (EEEEN) bit is set in the MAC Control Register (MAC_CR), the current speed is 100 Mbps or 1000 Mbps, the current duplex is full and the auto-negotiation result indicates that both the local and partner device support EEE at the current operating speed. In order to prevent an unstable link condition, the PHY link status also must indicate “up” for one second before LPI is requested.

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TX LPI requests are asserted even if the Transmitter Enable (TXEN) bit in the MAC Transmit Register (MAC_TX) is cleared.

When TX LPI is requested to the MAC, the Energy Efficient Ethernet Start TX Low Power Interrupt (EEE_START_TX_LPI_INT) bit will be set. This bit may generate a USB interrupt if Energy Efficient Ethernet Start TX Low Power Enable (EEE_START_TX_LPI_EN) is set.

When the TX LPI request is de-asserted, due to the expiration of the above EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY) timer, the Energy Efficient Ethernet Stop TX Low Power Interrupt (EEE_STOP_TX_LPI_INT) bit is set. This bit may then generate a USB interrupt if Energy Efficient Ethernet Stop TX Low Power Enable (EEE_STOP_TX_LPI_EN) is set.

Also when the TX LPI request is de-asserted due to the same automatic removal, the Energy Efficient Ethernet TX Wake (EEE_TX_WAKE) bit is set if Energy Efficient Ethernet TX Wake Enable (EEE_TX_WAKE_EN) is set. Energy Efficient Ethernet TX Wake (EEE_TX_WAKE) being set causes EEE WAKE-UP Status (EEE_WUPS) to set. EEE WAKE-UP Status (EEE_WUPS), in turn, may generate a USB remote wake-up event if EEE WAKE-UP Enable (EEE_WAKE-UP_EN) is set. EEE TX Wake is required to operate during the SUSPEND3 Power state, however the hardware should not intentionally enforce the power state mapping since it is left to the S/W driver to properly match wake events and power states.

8.9.1.1.1 Flow Control, ARP Response and NS Response Packet Interaction

It is possible that a pause frame (automatically generated based on the RX FCT levels or RX FCT overflow or manual generated via the FORCE_FC bit in the FLOW register) or an ARP or NS response packet needs to be transmitted while waiting for the TX FCT empty timer to expire. When such packets are necessary, the TX FCT empty timer is not restart or paused. If such a packet is started while waiting for TX FCT empty timer but finishes following the wait time, TX LPI is requested following the packet (i.e. the LPI request is delayed). If the TX FCT becomes not empty while the packet is being transmitted, the TX FCT empty timer is reset, as normally would happen, and TX LPI is not requested.

It is also possible that a pause frame or an ARP or NS response packet needs to be transmitted while the TX LPI request is asserted. When such packets are necessary, the TX LPI request is de-asserted and the packet is presented to the MAC for transmission. The MAC, as described below, will defer until the appropriate wake timer has expired before transmitting the packet. Once the packet is sent to the MAC, TX LPI is immediately reasserted, assuming that the FCT empty timer is still expired and that the EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY) timer has not expired. The MAC, as described below, will finish the packet transmission before signaling LPI to the PHY

Removal of the LPI request, due to flow control or ARP or NS response packets does, not reset the FCT empty timer nor does it reset or pause the EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY) timer.

8.9.1.2 MAC LPI Request to PHY

The MAC will always finish the current packet before signaling TX LPI to the PHY. It is possible that the TX LPI request from the Client is asserted and de-asserted during a packet. This will not result in a TX LPI request to the PHY nor will it trigger the wake timer described below.

The MAC will generate TX LPI requests to the PHY even if the Transmitter Enable (TXEN) bit in the MAC Transmit Register (MAC_TX) is cleared.

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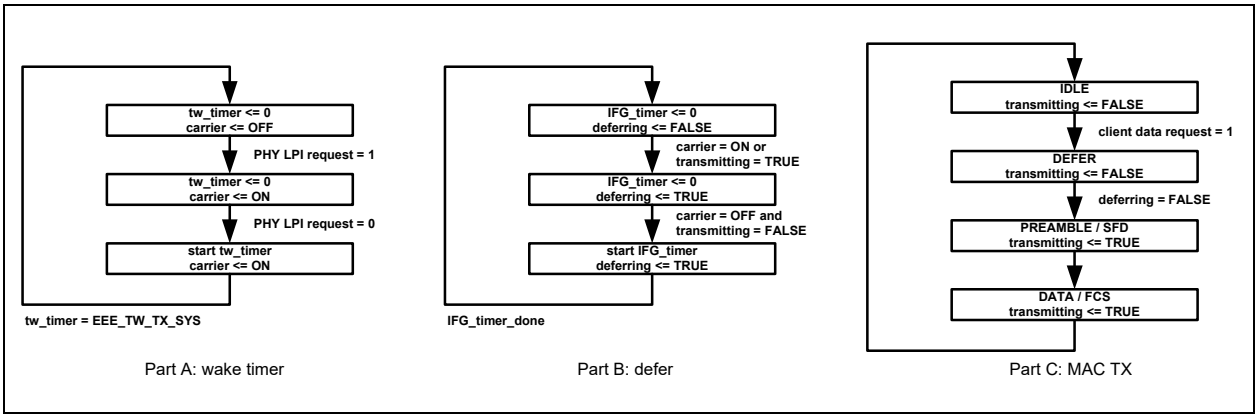
802.3az specifies the usage of a simplified full duplex MAC with carrier sense deferral. Basically this means that once the TX LPI request to the PHY is de-asserted, the MAC will defer the time specified in EEE Time Wait TX System Register (EEE_TW_TX_SYS) in addition to the normal IPG before sending a frame. This is shown in Figure 8-3.

FIGURE 8-3: TX LPI WAKE TIMER



In part A of the figure, a carrier indicator is set when the TX LPI request to the PHY is asserted. The wake timer (tw_timer) is triggered when the TX LPI request to the PHY is de-asserted and once the wake timer is satisfied, the carrier indicator is cleared. Note that there are separate TX wait values depending on the speed of operation.

Part B of the figure shows that a deferring indicator is set when either a frame is transmitted or the carrier indicator is active. Once the frame transmission is finished or (logically an “and”) the carrier indicator is cleared, the IFG timer is triggered and once the IFG timer is satisfied, the deferring indicator is cleared.

Part C of the figure shows that the MAC transmitter waits for the clearing of the deferring indicator before transmitting a frame. This is unchanged.

8.9.1.2.1 Selecting the source of transmit data Following wake

Currently, when presented with a simultaneous request to transmit FCT data, ARP or NS responses or pause packets, the MAC prioritizes pause packets over the other sources. In order to minimize the impact of the wake time on the latency of transmitting a pause packet, the choice of data source must not be made until the expiration of the wake time.

As an example, assume that during the TX LPI, a maximum size transmit packet is written into the TX FCT. Also assume that during the wake time, the RX FCT FIFO level reaches the pause threshold and a request is made for a pause packet to be transmitted. At the expiration of the wake time, if the packet from the TX FCT was selected and transmitted, the eventual pause packet would have waited the wake time portion plus the maximum packet transmit time. The additional of the wake time may not have been accounted for in the RX FCT threshold level setting and an overflow might occur as a result. To alleviate this issue, the pause packet should be selected at the expiration of the wake time.

8.9.1.2.2 Halting GMII TX Clock

Once the TX LPI request is asserted, the MAC, optionally based on the Energy Efficient Ethernet TX Clock Stop Enable (EEE_TX_CLK_STOP_EN) bit in the MAC Control Register (MAC_CR), may halt the GMII GTX_CLK output. The MAC provides at least 9 clock cycles of GTX_CLK following the assertion of the TX LPI request before halting the clock. The MAC provides at least 1 clock cycle of GTX_CLK before the de-assertion of the TX LPI request.

8.9.1.2.3 TX LPI Counters

The MAC maintains a counter, EEE TX LPI Transitions, that counts the number of times that TX LPI request to the PHY changes from de-asserted to asserted. The counter is not writable and does not clear on read.

The MAC maintains a counter, EEE TX LPI Time, that counts (in microseconds) the amount of time that TX LPI is asserted. Note that this counter does not include the time specified in the EEE Time Wait TX System Register (EEE_TW_TX_SYS). The counter is not writable and does not clear on read.

Both counters are required to operate during SUSPEND0, SUSPEND3 and Normal Configured Power states.

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8.9.2 RX LPI DETECTION

In order to provide robustness, RX LPI is seen active from the PHY for 3 RX clocks in order to be considered valid active and is seen inactive from the PHY for 4 RX clocks in order to be considered valid inactive.

8.9.2.1 LPI Affect on Automatic Speed Detection

It is possible for the PHY to halt RX_CLK after indicating LPI but at least 9 RX clocks of LPI will occur before the RX_CLK is stopped. When RX_CLK is restarted, due to wake signaling, at least 1 RX clock of RX LPI will occur before the PHY indicates normal IDLE.

8.9.2.2 Decoding LPI

The MAC will decode the start of the RX LPI indication and set the Energy Efficient Ethernet RX Low Power Interrupt (EEE_RX_LPI_INT) bit. This bit may generate a USB interrupt if Energy Efficient Ethernet RX Low Power Enable (EEE_RX_LPI_EN) is set.

The MAC will decode the end of the RX LPI indication and, if Energy Efficient Ethernet RX Wake Enable (EEE_RX-_WAKE_EN) is set, the MAC will set Energy Efficient Ethernet RX Wake (EEE_RX_WAKE). Energy Efficient Ethernet RX Wake (EEE_RX_WAKE) being set causes EEE WAKE-UP Status (EEE_WUPS) to set. EEE WAKE-UP Status (EEE_WUPS), in turn, may generate a USB remote wake-up event if EEE WAKE-UP Enable (EEE_WAKEUP_EN) is set. EEE RX Wake is required to operate during SUSPEND0 and SUSPEND3 Power states, however the hardware will not intentionally enforce the power state mapping since it is left to the software driver to properly match wake events and power states.

The MAC will decode the LPI indication only when the Energy Efficient Ethernet Enable (EEEEN) bit is set in the MAC Control Register (MAC_CR), the current speed is 100Mbs or 1000Mbs, the current duplex is full and the auto-negotiation result indicates that both the local and partner device supports EEE at the current operating speed. In order to prevent an unstable link condition, the PHY link status also must indicate “up” for one second before LPI is decoded.

The MAC will decode the LPI indication even if Receiver Enable (RXEN) in the MAC Receive Register (MAC_RX) is cleared.

8.9.2.3 RX LPI Counters

The MAC maintains a counter, EEE RX LPI Transitions, that counts the number of times that the LPI indication from the PHY changes from de-asserted to asserted. The counter is not writable and does not clear on read.

The MAC maintains a counter, EEE RX LPI Time, that counts (in microseconds) the amount of time that the PHY indicates LPI. The counter is not writable and does not clear on read.

Both counters are required to operate during SUSPEND0, SUSPEND3 and Normal Configured Power states.

8.10 MAC Reset Watchdog Timer

A portion of the MAC operates on clocks generated by the Ethernet PHY. During a PHY reset event, this portion of the MAC is designed to not be taken out of reset until the PHY clocks are operational, such that the respective MAC resets can be de-asserted synchronously. In the event of an error condition in which the MAC’s RX and TX clocks are not enabled, a watchdog timer is provided to detect this condition. The duration of the timer is 8 ms.

The below scenarios utilize the watchdog timer:

- System level reset events.
- PHY Reset (PHY_RST) results in resetting the portion of the MAC operating on the PHY receive and transmit clocks and therefore they also enable the watchdog timer.
- The Ethernet PHY is held in reset while in SUSPEND2. If the device transitions to Normal-Configured, the PHY must be taken out of reset as well as the affected portions of the MAC. This likewise enables the watchdog timer.

The expiration of the timer causes MAC Reset Time Out (MACRTO_INT) in Interrupt Status Register (INT_STS) to assert.

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9.0 GIGABIT ETHERNET PHY (GPHY)

The device incorporates a low-power Gigabit Ethernet PHY (GPHY) transceiver that is fully compliant with the IEEE 802.3, 802.3u, 802.3ab, and 802.3az (Energy Efficient Ethernet) standards. It provides a low electromagnetic interference (EMI) line driver, and integrated line side termination resistors that conserve both power and printed circuit board (PCB) space.

The mixed signal and digital signal processing (DSP) architecture of the Ethernet PHY assures robust performance even under less-than-favorable environmental conditions. It supports both half-duplex and full-duplex 10BASE-T, 100BASE-TX, and 1000BASE-T communication speeds over Category 5 (Cat5) unshielded twisted pair (UTP) cable at distances greater than 100m, displaying excellent tolerance to NEXT, FEXT, echo, and other types of ambient environment and system electronic noise. The Ethernet PHY implements auto-negotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or cross-over LAN cables.

The Ethernet PHY supports Wake on LAN (WoL), providing a mechanism to trigger an interrupt upon reception of a perfect DA, broadcast, magic packet, or wakeup frame. This feature allows filtering of packets at the PHY layer, without requiring MAC intervention.

Per IEEE 802.3-2005 standards, all digital interface pins are tolerant to 3.6V. Additional power savings can be achieved by utilizing the integrated Energy Efficient Ethernet (EEE) function and Enhanced ActiPHY power saving mode, resulting in significant power savings during low link utilizations.

The Ethernet PHY is configurable via the Ethernet PHY Control and Status Registers. These registers are accessed indirectly through the Ethernet MAC via the MII Access Register (MII_ACCESS) and MII Data Register (MII_DATA).

9.1 Category 5 Twisted Pair Media Interface

9.1.1 VOLTAGE-MODE LINE DRIVER

The Ethernet PHY uses a patented voltage-mode line driver that allows it to fully integrate the series termination resistors (required to connect the PHY's Category 5 interface to an external 1:1 transformer). Also, the interface does not require the user to place an external voltage on the center tap of the magnetic.

9.1.2 CATEGORY 5 AUTO-NEGOTIATION AND PARALLEL DETECTION

The Ethernet PHY supports twisted pair auto-negotiation as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az. The auto-negotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-T. Also, auto-negotiation allows the internal MAC to communicate with its link partner MAC through the Ethernet PHY using optional "next pages," which set attributes that may not otherwise be defined by the IEEE standard.

If the Category 5 link partner does not support auto-negotiation, the Ethernet PHY automatically uses parallel detection to select the appropriate link speed.

Auto-negotiation is disabled by clearing the Auto-Negotiation Enable bit of the Ethernet PHY Mode Control Register. If auto-negotiation is disabled, the state of the Ethernet PHY Mode Control Register bits Speed Select[0], Speed Select[1], and Duplex Mode determine the device operating speed and duplex mode. While 10BASE-T and 100BASE-T do not require auto-negotiation, clause 40 has defined 1000BASE-T to require auto-negotiation.

9.1.3 1000BASE-T FORCED MODE SUPPORT

The device provide support for a 1000BASE-T forced test mode. In this mode, the Ethernet PHY can be forced into 1000BASE-T mode and does not require manual setting of master/slave at the two ends of the link. This mode is for test purposes only, and should not be used in normal operation. To configure a PHY in this mode, set the Enable 1000BASE-T Force Mode bit of the Ethernet PHY Page 2 EEE Control Register to 1b, and the Ethernet PHY Mode Control Register bits Speed Select[1] and Speed Select[0] to 10b.

9.1.4 AUTOMATIC CROSSOVER AND POLARITY DETECTION

For trouble-free configuration and management of Ethernet links, the Ethernet PHY includes a robust automatic cross-over detection feature for all three speeds on the twisted-pair interface (10BASE-T, 100BASE-T, and 1000BASE-T). Known as HP Auto-MDIX, the function is fully compliant with clause 40 of the IEEE standard 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs, a useful capability that exceeds the requirements of the standard.

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Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. The default settings can be changed via the Disable Auto-MDI/MDI-X Correction and Disable Polarity Inversion Correction bits of the Ethernet PHY Bypass Control Register. The status bits for each of these functions are located in the Ethernet PHY Auxiliary Control and Status Register.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in Table 9-1.

TABLE 9-1: SUPPORTED MDI PAIR COMBINATIONS

RJ-45 Pin Pairings				Mode
1,2	3,6	4,5	7,8	
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

9.1.5 MANUAL MDI/MDI-X SETTING

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using the MDI/MDI-X Force Enable bits of the Ethernet PHY Page 1 LED and Crossover Control Register. Setting these bits to 10b forces MDI and setting to 11b forces MDI-X. Leaving the bits 00b enables the MDI/MDI-X setting to be based on the Disable Auto-MDI/MDI-X in Forced 10/100 Mode and Disable Auto-MDI/MDI-X Correction bits of the Ethernet PHY Bypass Control Register.

9.1.6 LINK SPEED DOWNSHIFT

For operation in cabling environments that are incompatible with 1000BASE-T, the Ethernet PHY provides an automatic link speed “downshift” option. When enabled, the device automatically changes its 1000BASE-T auto-negotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state if a subsequent link partner with 1000BASE-T support is connected.

This is useful in setting up in networks using older cable installations that may include only pairs A and B and not pairs C and D. The two-pair Cable Detection and Auto Downshift Operation enables link-up at 10/100BASE-T speeds in this scenario.

To configure and monitor link speed downshifting, set the Enable Cable Impairment Auto-Downshift, Link Speed Auto-Downshift Control, and Apply Downshift bits of the Ethernet PHY Page 1 Extended PHY Control 3 Register.

9.1.7 ENERGY EFFICIENT ETHERNET

The Ethernet PHY supports the IEEE 802.3az Energy Efficient Ethernet standard. This standard provides a method for reducing power consumption on an Ethernet link during times of low utilization. It uses Low Power Idles (LPI) to achieve this objective.

Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization.

The Ethernet PHY uses LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T modes of operation. In addition, the IEEE 802.3az standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5Vpeak-to-peak to approximately 3.3Vpeak-to-peak. This mode reduces power consumption in 10Mb/s link speed and can fully inter-operate with legacy 10BASE-T compliant PHYs over 100m Category 5 cable or better.

To configure the Ethernet PHY in 10BASE-Te mode, set the Enable Energy Efficient (802.3az) 10BASE-Te Operating Mode bit in the Ethernet PHY Page 2 EEE Control Register to 1b. Additional Energy Efficient Ethernet features are controlled through the MMD control and status registers EEE Advertisement (EEE_ADVERTISEMENT) and EEE Link Partner Advertisement (EEE_LP_ADVERTISEMENT).

9.2 Ethernet PHY Power Management

9.2.1 PHY POWER DOWN

The Ethernet PHY can be powered down via the IEEE-specified Power Down bit in the Ethernet PHY Mode Control Register.

9.2.2 ENHANCED PHY POWER MANAGEMENT

In addition to the IEEE-specified power-down control bit, the device also includes an enhanced PHY power management mode. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY "wakes up" at a programmable interval and attempts to "wake-up" the link partner PHY by sending a burst of FLP over copper media.

The enhanced PHY power management mode is enabled during normal operation at any time by setting the Enhanced PHY Enable bit of the Ethernet PHY Auxiliary Control and Status Register to 1b.

The enhanced PHY power management mode helps conserve power in the following cases:

- An unplugged PHY port
- A PHY port, plugged into a cable with no link partner on the other end
- A PHY port, plugged into a cable with a link partner PHY not transmitting link pulses because it is un-powered, in reset, or other reasons that prevent it from linking.

The enhanced PHY power management mode can be used in conjunction with all suspend states with the exception of SUSPEND2, since the PHY is disabled. Moreover, Enhanced PHY mode can be enabled while in Normal-Configured, NetDetach and PME mode by setting the Enhanced PHY Enable bit of the Ethernet PHY Auxiliary Control and Status Register to 1b. It is desirable to do so in all these cases.

For PME mode, EEPROM/OTP settings are available to enable the Enhanced PHY mode to be enabled by default.

9.3 LED Interface

The Ethernet PHY provides four LED pins, **LED[0:3]**. Each LED can be configured to display different status information that can be selected by setting the corresponding LED Configuration field of the Ethernet PHY LED Mode Select Register. The modes in Table 9-2 are equivalent to the settings used in the Ethernet PHY LED Mode Select Register to configure each LED pin. The default LED state is active low and can be changed by modifying the Invert LED Polarity field of the Ethernet PHY Page 2 EEE Control Register. The blink/pulse-stretch and other LED settings can be configured via the Ethernet PHY LED Behavior Register. The LED pins can also be configured via EEPROM or OTP (LED Configuration 0, LED Configuration 1, LED Configuration 2, LED Configuration 3, LED Configuration 4).

TABLE 9-2: LED MODE AND FUNCTION SUMMARY

Mode	Name	Description
0	Link/Activity	**1** = No link in any speed on any media interface. **0** = Valid link at any speed on any media interface. **Blink or pulse stretch** = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	**1** = No link at 1000BASE-T. **0** = Valid link at 1000BASE-T. **Blink or pulse stretch** = Valid link at 1000BASE-T with activity present.
2	Link100/Activity	**1** = No link at 100BASE-TX. **0** = Valid link at 100BASE-TX. **Blink or pulse stretch** = Valid link at 100BASE-TX with activity present.
3	Link10/Activity	**1** = No link at 10BASE-T. **0** = Valid link at 10BASE-T. **Blink or pulse stretch** = Valid link at 10BASE-T with activity present.
4	Link100/1000/Activity	**1** = No link at 100BASE-TX or 1000BASE-T. **0** = Valid link at 100BASE-TX or 1000BASE-T. **Blink or pulse stretch** = Valid link at 100BASE-TX or 1000BASE-T, with activity present.

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TABLE 9-2: LED MODE AND FUNCTION SUMMARY (CONTINUED)

Mode	Name	Description
5	Link10/1000/Activity	**1** = No link at 10BASE-T or 1000BASE-T. **0** = Valid link at 10BASE-T or 1000BASE-T. **Blink or pulse stretch** = Valid link at 10BASE-T or 1000BASE-T, with activity present.
6	Link10/100/Activity	**1** = No link at 10BASE-T or 100BASE-TX. **0** = Valid link at 10BASE-T or 100BASE-TX. **Blink or pulse stretch** = Valid link at 10BASE-T or 100BASE-TX, with activity present.
7	RESERVED	RESERVED
8	Duplex/Collision	**1** = Link established in half-duplex mode, or no link established. **0** = Link established in full-duplex mode. **Blink or pulse stretch** = Link established in half-duplex mode but collisions are present.
9	Collision	**1** = No collisions detected. **Blink or pulse stretch** = Collision detected.
10	Activity	**1** = No activity present. **Blink or pulse stretch** = Activity present. (becomes TX activity present if the LED Activity Output Select bit in the Ethernet PHY LED Behavior Register is set to 1.)
11	RESERVED	RESERVED
12	Auto-negotiation Fault	**1** = No auto-negotiation fault present. **0** = Auto-negotiation fault occurred.
13	RESERVED	RESERVED
14	Force LED Off	**1** = De-asserts the LED.
15	Force LED On	**0** = Asserts the LED.

9.3.1 LED BEHAVIOR

Using the Ethernet PHY LED Behavior Register, the following LED behaviors can be configured.

9.3.1.1 LED Combine

Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin via the LED Combination Disables field of the Ethernet PHY LED Behavior Register. For example, a copper link running in 1000BASE-T mode with activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display if the combine feature is disabled.

9.3.1.2 LED Blink or Pulse-Stretch

This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin via the LED Pulse Stretch Enables field of the Ethernet PHY LED Behavior Register. Activity and collision events can occur randomly and intermittently throughout the link-up period. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin. Pulse-stretch guarantees that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured, as detailed in Section 9.3.1.3, "Rate of LED Blink or Pulse-Stretch".

9.3.1.3 Rate of LED Blink or Pulse-Stretch

This behavior controls the LED blink rate or pulse-stretch length when the blink/pulse-stretch is enabled (LED Pulse Stretch Enables) on an LED pin. This can be uniquely configured for each LED pin via the LED Blink / Pulse-Stretch Rate field of the Ethernet PHY LED Behavior Register. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms.

9.3.1.4 LED Pulsing Enable

To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz, 20% duty cycle, by setting the LED Pulsing Enable bit of the Ethernet PHY LED Behavior Register.

9.4 Test Features

The Ethernet PHY includes several testing features designed to facilitate system-level debugging and production testing. These are detailed in the following sub-sections.

9.4.1 ETHERNET PACKET GENERATOR

The Ethernet Packet Generator (EPG) can be used at each of the 10/100/1000BASE-T speed settings for Copper Category 5 media to isolate problems between the MAC and PHY, or between a locally connected PHY and its remote link partner. Enabling the EPG feature effectively disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface.

Note:	The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the device is connected to a live network.

To enable the EPG feature, set the EPG Enable bit to 1b in the Ethernet PHY Page 1 Ethernet Packet Generator (EPG) Control 1 Register. When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output pins to the MAC are still active when the EPG is enabled.

When the EPG Run/Stop bit of the Ethernet PHY Page 1 Ethernet Packet Generator (EPG) Control 1 Register is set to 1b, the PHY begins transmitting Ethernet packets based on the settings in the Ethernet PHY Page 1 Ethernet Packet Generator (EPG) Control 1 Register and Ethernet PHY Page 1 Ethernet Packet Generator (EPG) Control 2 Register. These registers set:

- Source and destination addresses for each packet
- Packet size
- Inter-packet gap
- FCS state
- Transmit duration
- Payload pattern

If the Transmission Duration bit of the Ethernet PHY Page 1 Ethernet Packet Generator (EPG) Control 1 Register is set to 0, the EPG Run/Stop bit is cleared automatically after 30,000,000 packets are transmitted.

9.4.2 CRC COUNTERS

A set of Cyclical Redundancy Checking (CRC) counters are available to monitor traffic on the copper interface. Two separate CRC counters are available:

- Good packet Counter (Packet Counter field in the Ethernet PHY Page 1 Receive Good Counter Register)
- Bad Packet Counter (Receive Packet CRC Error Counter field in the Ethernet PHY Page 1 Extended PHY Control 4 Register)

The good CRC counters highest value is 9,999 packets. After this value is reached, the counter clears on the 10,000th packet and continues to count additional packets beyond that value. The bad CRC counter stops counting when it reaches its maximum counter limit of 255 packets.

The device CRC counters operate in the 10/100/1000BASE-T mode as follows:

- After receiving a packet on the media interface, the Packet Counter Active bit of the Ethernet PHY Page 1 Receive Good Counter Register is set and cleared after being read.

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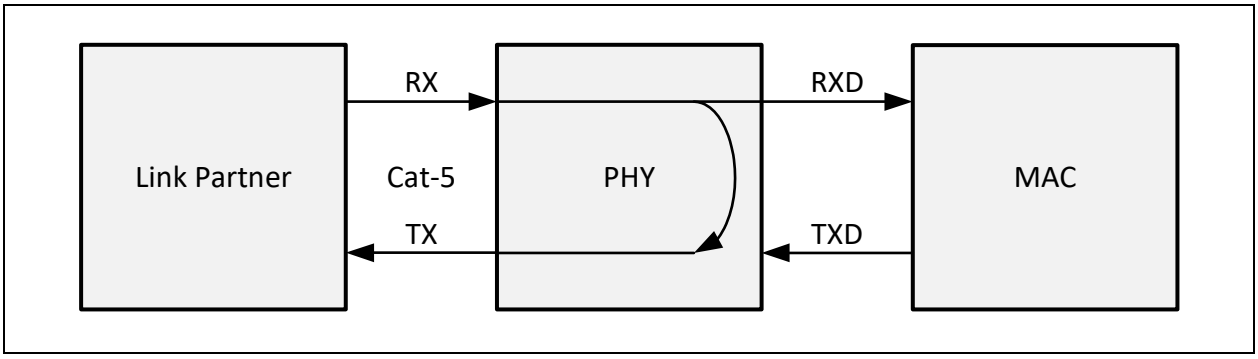
- The packet then is counted by either the good CRC counter (Packet Counter field in the Ethernet PHY Page 1 Receive Good Counter Register) or the bad CRC counter (Receive Packet CRC Error Counter field in the Ethernet PHY Page 1 Extended PHY Control 4 Register).
- Both CRC counters are also automatically cleared when read.

9.4.3 FAR-END LOOPBACK

The far-end loopback testing feature is enabled by setting the Far-End Loopback Enable bit of the Ethernet PHY Extended PHY Control 1 Register to 1b. When enabled, it forces incoming data from a link partner on the current media interface, into the MAC interface of the PHY, to be retransmitted back to the link partner on the media interface as shown in Figure 9-1. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

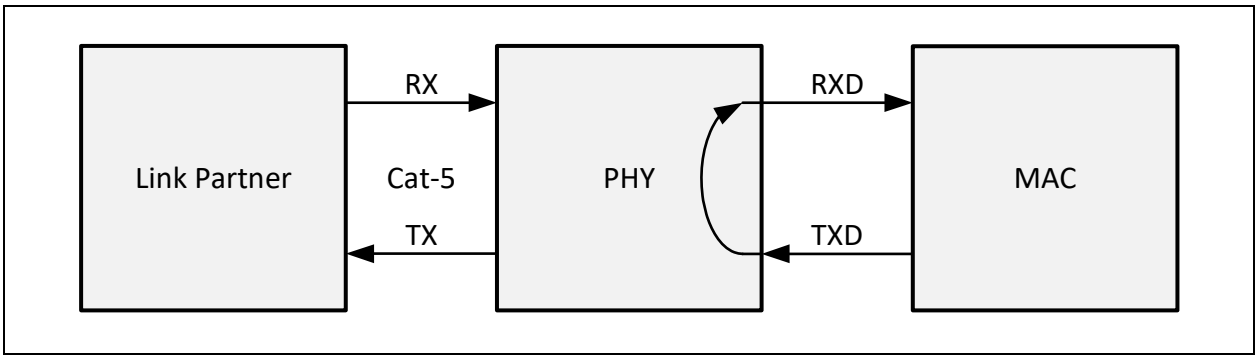
FIGURE 9-1: FAR-END LOOPBACK DIAGRAM



9.4.4 NEAR-END LOOPBACK

When the near-end loopback testing feature is enabled (by setting the Digital Loopback bit of the Ethernet PHY Mode Control Register to 1b), data on the transmit data pins (**TXD**) is looped back in the PCS block, onto the device receive data pins (**RXD**), as shown in Figure 9-2. When using this testing feature, no data is transmitted over the network.

FIGURE 9-2: NEAR-END LOOPBACK DIAGRAM



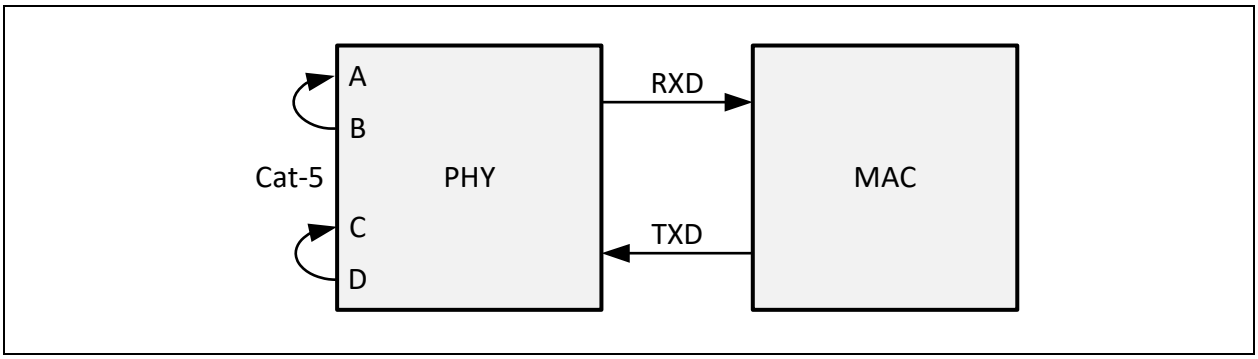
9.4.5 CONNECTOR LOOPBACK

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B, and pair C to pair D, as shown in Figure 9-3. The connector loopback feature functions at all available interface speeds.

When using the connector loopback testing feature, the device auto-negotiation, speed, and duplex configuration is set using the Ethernet PHY Mode Control Register, Ethernet PHY Device Auto-Negotiation Advertisement Register, and Ethernet PHY 1000BASE-T Control Register. For 1000BASE-T connector loopback, the following additional writes are required to be executed in the following order:

1. Enable the 1000BASE-T connector loopback. Set the Cable Loopback Mode Enable bit of the Ethernet PHY Extended PHY Control 2 Register to 1b.
2. Disable pair swap correction. Set the Disable Auto-MDI/MDI-X Correction bit of the Ethernet PHY Bypass Control Register to 1b.

FIGURE 9-3: CONNECTOR LOOPBACK DIAGRAM



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10.0 EEPROM CONTROLLER (EEP)

The device may use an external EEPROM to store the default values for the USB descriptors and the MAC address. The EEPROM controller supports most “93C56 or 93C66” type 256/512 byte EEPROMs. A total of nine address bits are used.

After a system-level reset occurs, the device will load the default values from EEPROM. The device will not accept USB transactions from the Host until this process is completed.

The EEPROM controller also allows the Host to read, write and erase the contents of the Serial EEPROM.

Note:	A 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation must be used.

10.1 EEPROM and OTP Relationship

A detected external EEPROM shall always take precedence over OTP. When determining the source to configure the device, the following order is used:

1. EEPROM Configuration
2. OTP Configuration
3. CSR defaults

The CSR defaults are used if the OTP is determined to be unconfigured.

10.2 EEPROM Auto-Load

Certain system level resets (USB Reset, Power-On Reset (POR), External Chip Reset (RESET_N), and Soft Reset (SRST)) cause the EEPROM contents to be loaded into the device. After a reset, the EEPROM controller attempts to read the first byte of data from the EEPROM. If the value A5h is read from the first address, then the EEPROM controller will assume that a programmed external Serial EEPROM is present.

Note:	The USB reset only loads the MAC address.

The EEPROM Controller will then load contents of the EEPROM into an internal 512 byte Descriptor SRAM. The contents of the RAM are accessed by the USB EP0 Control Block as needed (i.e., to fill Get Descriptor commands). A detailed explanation of the EEPROM byte ordering with respect to the MAC address is given in Section 15.1.45, "MAC Receive Address Low Register (RX_ADDRL)," on page 189.

If A5h is not read from the first address, the EEPROM controller will end initialization. The default values, as specified in the associated registers and USB descriptors, shall be assumed unless a configured OTP is present.

Where there is no EEPROM or OTP it is the responsibility of the Host LAN driver software to set the IEEE 802.3 address by writing to the MAC Receive Address High Register (RX_ADDRH) and MAC Receive Address Low Register (RX_ADDRL).

The device will not respond to the USB Host until the EEPROM loading sequence has completed. Therefore, after reset, the USB PHY is kept in the disconnect state until the EEPROM load has completed.

10.3 EEPROM Host Operations

After the EEPROM controller has finished reading (or attempting to read) the EEPROM after a system-level reset, the Host is free to perform other EEPROM operations. EEPROM operations are performed using the EEPROM Command (E2P_CMD) and EEPROM Data (E2P_DATA) registers. Section 15.1.12, "EEPROM Command Register (E2P_CMD)," on page 158 provides an explanation of the supported EEPROM operations.

If the EEPROM operation is the “write location” (WRITE) or “write all” (WRAL) commands, the Host must first write the desired data into the E2P_DATA register. The Host must then issue the WRITE or WRAL command using the E2P_CMD register by setting the EPC_CMD field appropriately. If the operation is a WRITE, the EPC_ADDR field in E2P_CMD must also be set to the desired location. The command is executed when the Host sets the EPC_BSY bit high. The completion of the operation is indicated when the EPC_BSY bit is cleared.

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If the EEPROM operation is the “read location” (READ) operation, the Host must issue the READ command using the E2P_CMD register with the EPC_ADDR set to the desired location. The command is executed when the Host sets the EPC_BSY bit high. The completion of the operation is indicated when the EPC_BSY bit is cleared, at which time the data from the EEPROM may be read from the E2P_DATA register.

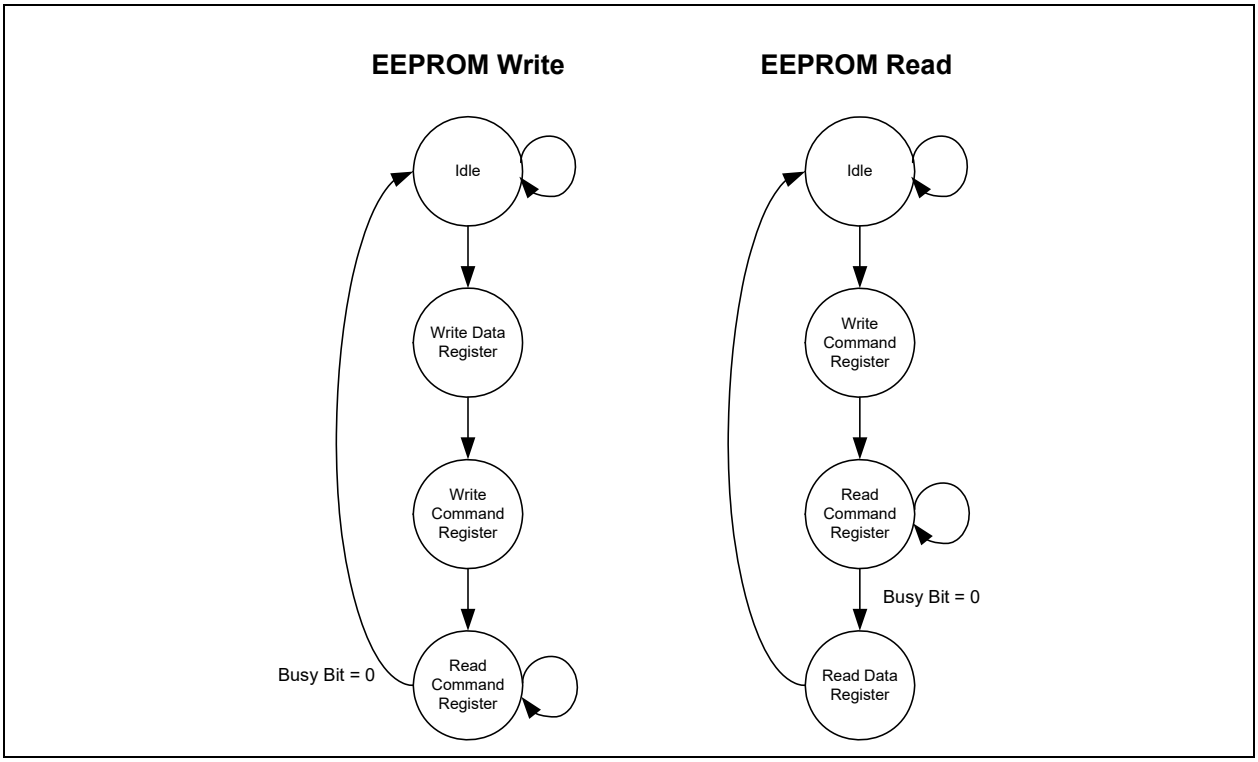
Other EEPROM operations are performed by writing the appropriate command to the E2P_CMD register. The command is executed when the Host sets the EPC_BSY bit high. The completion of the operation is indicated when the EPC_BSY bit is cleared. In all cases, the Host must wait for EPC_BSY to clear before modifying the E2P_CMD register.

Note:	The EEPROM device powers-up in the erase/write disabled state. To modify the contents of the EEPROM, the Host must first issue the EWEN command.

If an operation is attempted, and an EEPROM device does not respond within 30 ms, the device will timeout, and the EPC Time-out bit (EPC_TO) in the E2P_CMD register will be set.

Figure 10-1 illustrates the Host accesses required to perform an EEPROM Read or Write operation.

FIGURE 10-1: EEPROM ACCESS FLOW DIAGRAM



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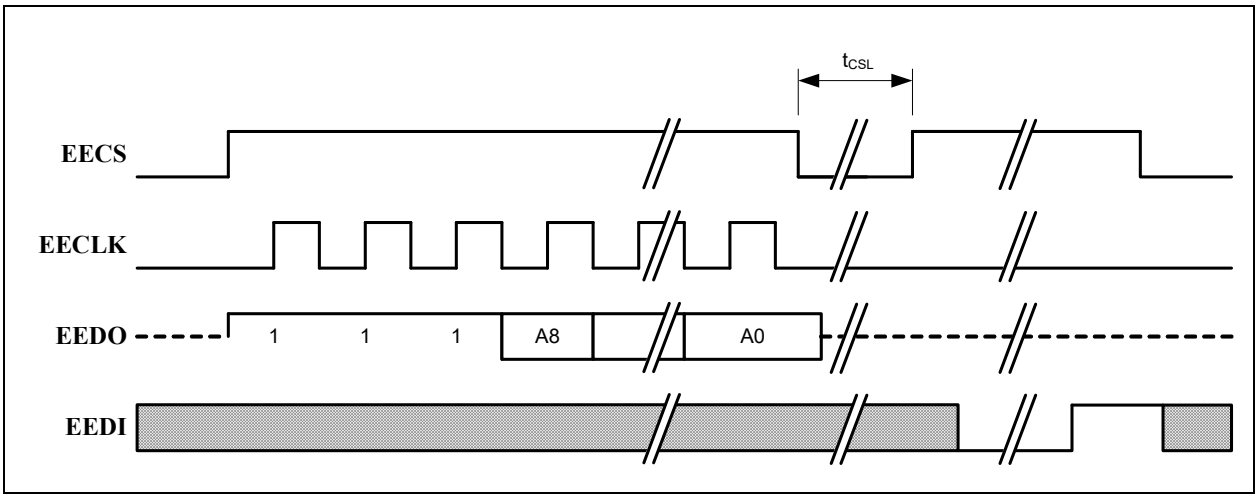
10.3.1 SUPPORTED EEPROM OPERATIONS

The EEPROM controller supports the following EEPROM operations under Host control via the E2P_CMD register. The operations are commonly supported by “93C46” EEPROM devices. A description and functional timing diagram is provided below for each operation. Please refer to the E2P_CMD register description in Section 15.1.12, "EEPROM Command Register (E2P_CMD)," on page 158 for E2P_CMD field settings for each command.

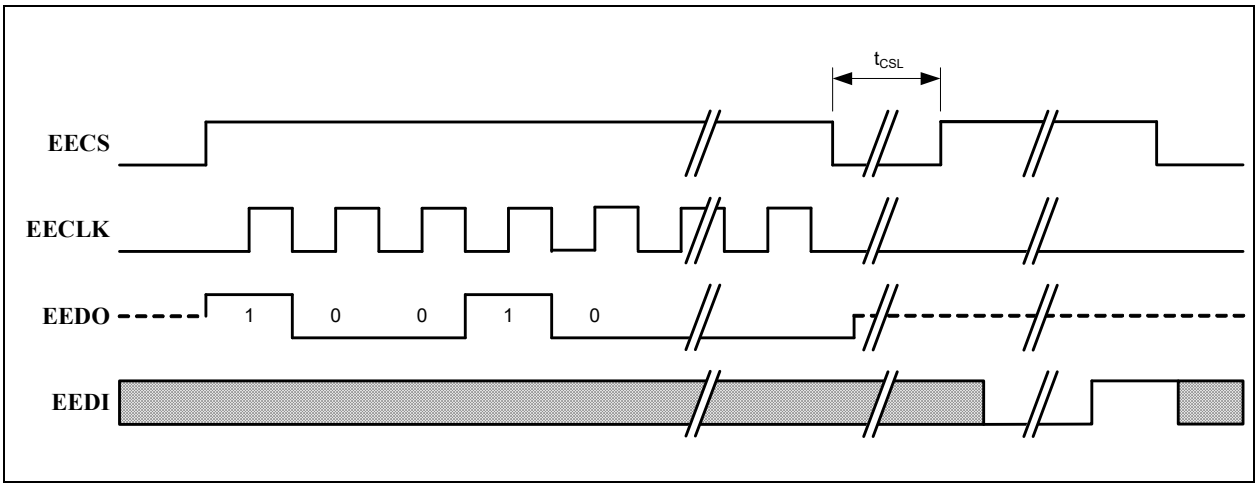
ERASE (Erase Location): If erase/write operations are enabled in the EEPROM, this command will erase the location selected by the EPC Address field (EPC_ADDR). The EPC_TO bit is set if the EEPROM does not respond within 30 ms.

FIGURE 10-2: EEPROM ERASE CYCLE



ERAL (Erase All): If erase/write operations are enabled in the EEPROM, this command will initiate a bulk erase of the entire EEPROM.The EPC_TO bit is set if the EEPROM does not respond within 30 ms.

FIGURE 10-3: EEPROM ERAL CYCLE



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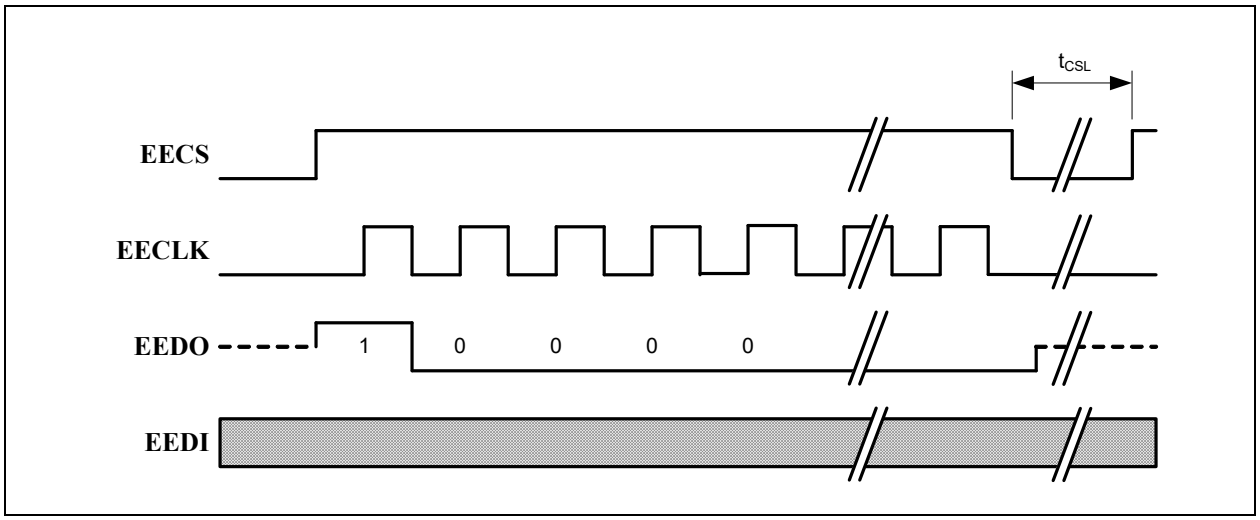
EWDS (Erase/Write Disable): After issued, the EEPROM will ignore erase and write commands. To re-enable erase/write operations issue the EWEN command.

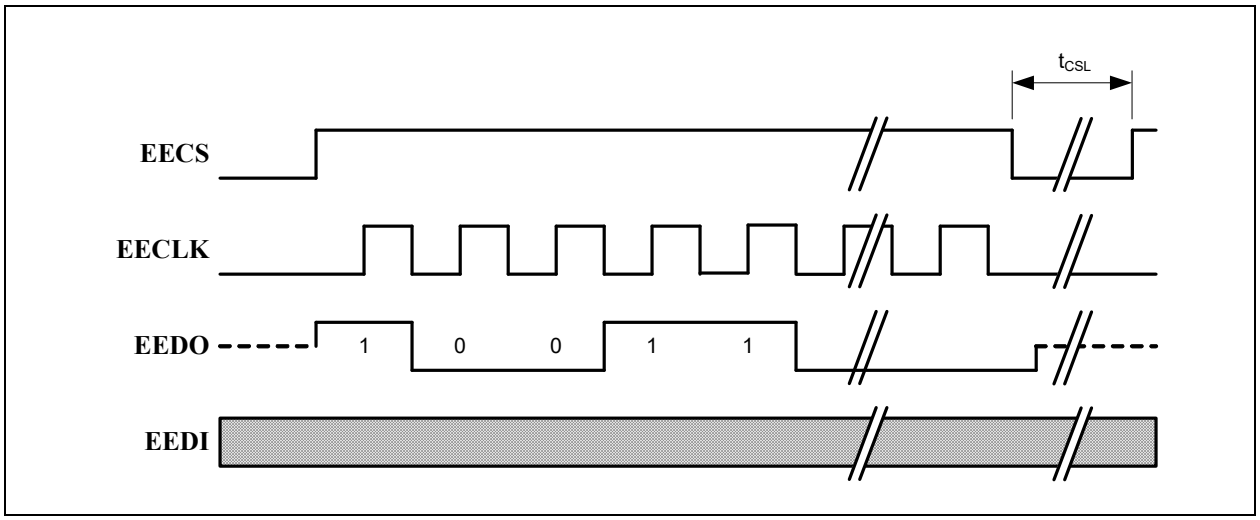
FIGURE 10-4: EEPROM EWDS CYCLE



EWEN (Erase/Write Enable): Enables the EEPROM for erase and write operations. The EEPROM will allow erase and write operations until the “Erase/Write Disable” command is sent, or until power is cycled.

The EEPROM device will power-up in the erase/write-disabled state. Any erase or write operations will fail until an Erase/Write Enable command is issued.

FIGURE 10-5: EEPROM EWEN CYCLE



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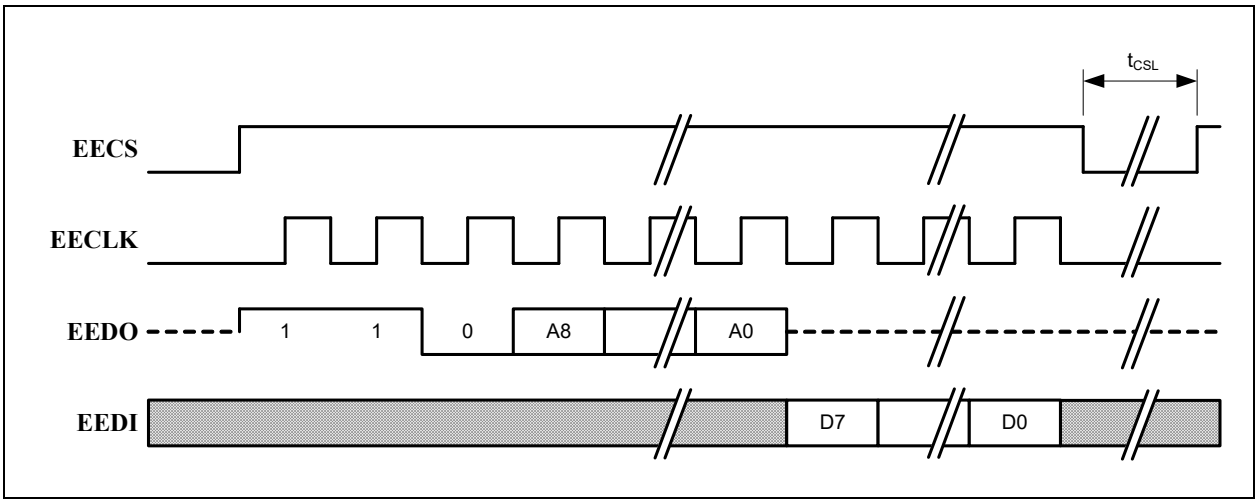
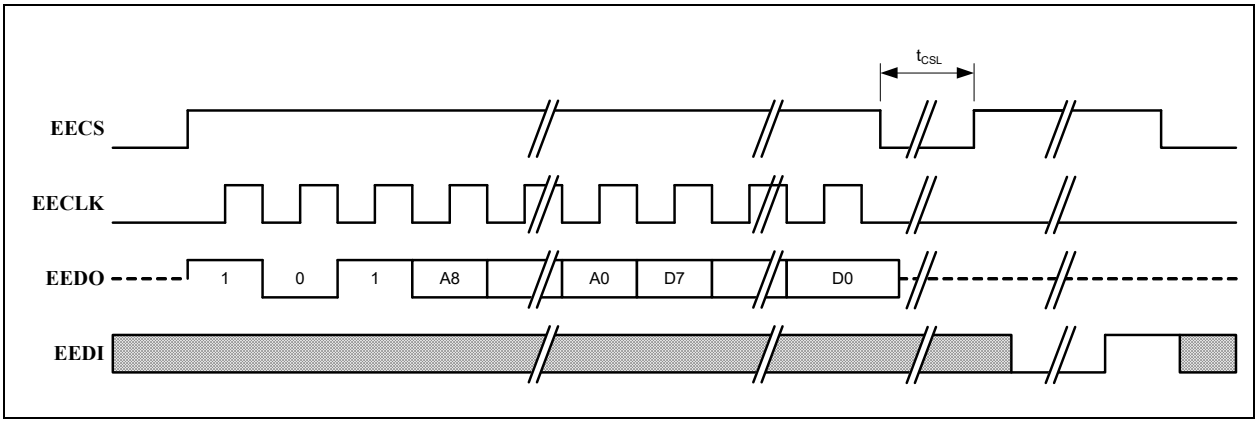
READ (Read Location): This command will cause a read of the EEPROM location pointed to by EPC Address (EPC_ADDR). The result of the read is available in the E2P_DATA register.

FIGURE 10-6: EEPROM READ CYCLE



WRITE (Write Location): If erase/write operations are enabled in the EEPROM, this command will cause the contents of the E2P_DATA register to be written to the EEPROM location selected by the EPC Address field (EPC_ADDR). The EPC_TO bit is set if the EEPROM does not respond within 30 ms.

FIGURE 10-7: EEPROM WRITE CYCLE



WRAL (Write All): If erase/write operations are enabled in the EEPROM, this command will cause the contents of the E2P_DATA register to be written to every EEPROM memory location. The EPC_TO bit is set if the EEPROM does not respond within 30 ms.

FIGURE 10-8: EEPROM WRAL CYCLE

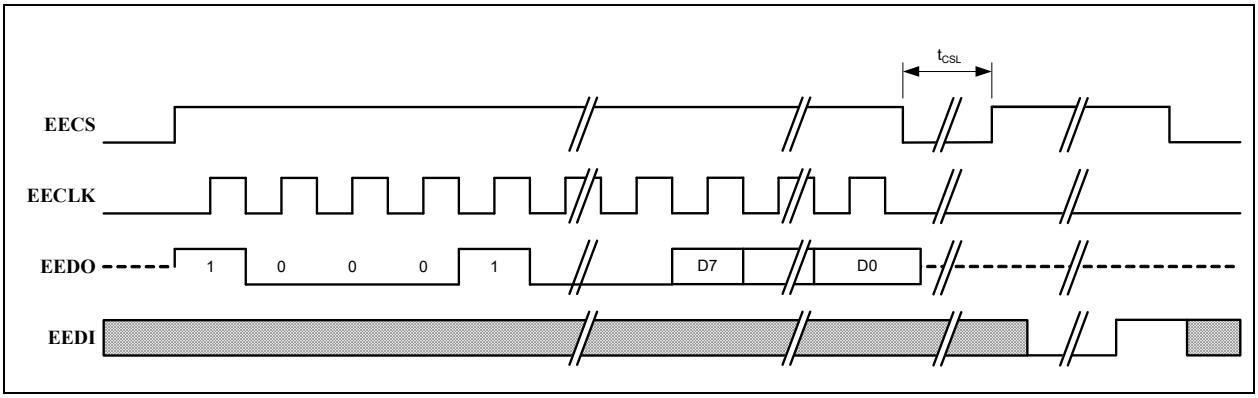


Table 10-1 details the number of EECLK cycles required for each EEPROM operation.

TABLE 10-1: REQUIRED EECLK CYCLES

Operation	Required EECLK Cycles
ERASE	10
ERAL	10
EWDS	10
EWEN	10
READ	18
WRITE	18
WRAL	18

10.3.2 HOST INITIATED EEPROM RELOAD

The Host can initiate a reload of the EEPROM by issuing the RELOAD command via the EEPROM Command Register (E2P_CMD). If the first byte read from the EEPROM is not 0xA5, it is assumed that the EEPROM is not present, or not programmed, and the reload will fail. The Data Loaded bit of the EEPROM Command Register (E2P_CMD) indicates a successful reload of the EEPROM.

Note:	It is not recommended that the RELOAD command be used as part of normal operation, as race conditions can occur with USB Commands that access descriptor data. It is recommended that the Host driver issue a Soft Reset (SRST) to reload the EEPROM data.

10.3.3 EEPROM COMMAND AND DATA REGISTERS

Refer to Section 15.1.12, "EEPROM Command Register (E2P_CMD)," on page 158 and Section 15.1.13, "EEPROM Data Register (E2P_DATA)," on page 160 for a detailed description of these registers. Supported EEPROM operations are described in these sections.

10.3.4 EEPROM TIMING

Refer to Section 16.6.4, "EEPROM Timing," on page 264 for detailed EEPROM timing specifications.

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10.4 EEPROM Format

Table 10-2 illustrates the format in which data is stored inside of the EEPROM.

The EEPROM offsets are given in units of 16-bit word offsets. A length field with a value of zero indicates that the field does not exist in the EEPROM. The device will use the field's hardware default value in this case.

Note: For the device descriptor the only valid values for the length are 0 and 18.

For the configuration and interface descriptor the only valid values for the length are 0 and 18.

For the Binary Object Store (BOS) Block, the length varies and is dependent on block components.

The EEPROM programmer must ensure that if a string descriptor does not exist in the EEPROM, the referencing descriptor must contain 00h for the respective string index field.

If all string descriptor lengths are zero, then a Language ID will not be supported.

All reserved EEPROM bits must be set to 0.

TABLE 10-2: EEPROM FORMAT

EEPROM offset	EEPROM Contents
00h	0xA5 (EEPROM Programmed Indicator)
01h	MAC Address [7:0]
02h	MAC Address [15:8]
03h	MAC Address [23:16]
04h	MAC Address [31:24]
05h	MAC Address [39:32]
06h	MAC Address [47:40]
07h	GPIO[7:0] Wakeup Enables Used to load LSB of the GPIO Wake 0-11 (GPIOWK[11:0]) field of the General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE)
08h	GPIO[11:8] Wakeup Enables Used to load bits 11:8 of the GPIO Wake 0-11 (GPIOWK[11:0]) field of the General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE)
09h	GPIO PME Flags 0
0Ah	GPIO PME Flags 1
0Bh	LED Configuration 0
0Ch	LED Configuration 1
0Dh	LED Configuration 2
0Eh	GPIO[7:0] Wakeup Polarity Used to load LSB of the GPIO Polarity 0-11 (GPIOPOL[11:0]) field of General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE)

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TABLE 10-2: EEPROM FORMAT (CONTINUED)

EEPROM offset	EEPROM Contents
0Fh	GPIO[11:8] Wakeup Polarity Used to load bits 11:8 of the GPIO Polarity 0-11 (GPIOPOL[11:0]) field of General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE)
10h	Full-Speed Polling Interval for Interrupt Endpoint
11h	High-Speed Polling Interval for Interrupt Endpoint
12h	RESERVED (write as 0)
13h	Configuration Flags 0 [7:0]
14h	Configuration Flags 0 [15:8]
15h	Configuration Flags 0 [23:16]
16h	Configuration Flags 0 [31:24]
17h	Configuration Flags 1 [7:0]
18h	Configuration Flags 1 [15:8]
19h	Configuration Flags 1 [23:16]
1Ah	Configuration Flags 1 [31:24]
1Bh	Configuration Flags 2 [7:0]
1Ch	Configuration Flags 2 [15:8]
1Dh	Configuration Flags 2 [23:16]
1EH	Configuration Flags 2 [31:24]
1Fh	Configuration Flags 3 [7:0]
20h	Configuration Flags 3 [15:8]
21h	Configuration Flags 3 [23:16]
22h	Configuration Flags 3 [31:24]
23h	Language ID [7:0]
24h	Language ID [15:8]
25h	Manufacturer ID String Descriptor Length (bytes)
26h	Manufacturer ID String Descriptor EEPROM Word Offset
27h	Product Name String Descriptor Length (bytes)
28h	Product Name String Descriptor EEPROM Word Offset
29h	Serial Number String Descriptor Length (bytes)
2Ah	Serial Number String Descriptor EEPROM Word Offset
2Bh	Configuration String Descriptor Length (bytes)
2Ch	Configuration String Descriptor Word Offset
2Dh	Interface String Descriptor Length (bytes)

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TABLE 10-2: EEPROM FORMAT (CONTINUED)

EEPROM offset	EEPROM Contents
2Eh	Interface String Descriptor Word Offset
2Fh	Binary Object Store (BOS) Block Length (Bytes) (See Note 10-1)
30h	Binary Object Store (BOS) Block Word Offset (See Note 10-1)
31h - 34h	RESERVED (Must be written as 0000_0000h)
35h	High-Speed Device Descriptor Length (bytes)
36h	High-Speed Device Descriptor Word Offset
37h	High-Speed Configuration and Interface Descriptor Length (bytes)
38h	High-Speed Configuration and Interface Descriptor Word Offset
39h	Full-Speed Device Descriptor Length (bytes)
3Ah	Full-Speed Device Descriptor Word Offset
3Bh	Full-Speed Configuration and Interface Descriptor Length (bytes)
3Ch	Full-Speed Configuration and Interface Descriptor Word Offset
3Dh	Wake Frame Filter 0 Configuration and Mask Length (bytes) (See Note 10-2)
3Eh	Wake Frame Filter 0 Configuration and Mask Word Offset (See Note 10-3)
3Fh - 40h	RESERVED (Must be written as 0000h)
41h	Common Test Bus In Length (bytes) (See Note 10-4)
42h	Common Test Bus In Word Offset (bytes)
43h - 44h	RESERVED (Must be written as 0200h)
45h	RESERVED (Must be written as 00h)
46h	SW Descriptor Length (bytes)
47h	SW Descriptor Word Offset (bytes)
48h - 4Fh	GPIO Configuration
50h - 57h	RESERVED (Must be written as 00h)
58h	LED Configuration 3
59h	LED Configuration 4
5Ah - 61h	RESERVED (Must be written as ***TBD***)

Note 10-1 This block may include Binary Object Store (BOS) Descriptor, USB 2.0 Extension Descriptor, and Container ID Descriptor.

Note 10-2 The length shall always be 20 bytes when this feature is used.

Note 10-3 The first four bytes specified at this address contains the WUF configuration data. The next subsequent 16 bytes are allocated to the mask. This data is used to set filter 0 in Wakeup Filter x Configuration Register (WUF_CFGx) and Wakeup Filter x Byte Mask Registers (WUF_MASKx).

Note 10-4 The length shall always be 4 bytes when this feature is used.

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10.4.1 GPIO PME FLAGS 0

Table 10-3 describes the GPIO PME Flags 0 byte.

TABLE 10-3: GPIO PME FLAGS 0

BIT	DESCRIPTION
7	**GPIO PME Enable** Setting this bit enables the assertion of the **PME_N** pin, as a result of a Wakeup (GPIO) pin, Packet, WUFF, Perfect DA or PHY Link Change. 0 = The device does not support GPIO PME signaling. 1 = The device supports GPIO PME signaling. **Note:** When this bit is 0, the remaining GPIO PME parameters in this flag byte are ignored.
6	**GPIO PME Configuration** This bit selects whether the GPIO PME is a level or a pulse on the **PME_N** pin. If pulse is selected, the duration of the pulse is determined by the setting of the GPIO PME Length bit of this flag byte. The level of the signal or the polarity of the pulse is determined by the GPIO PME Polarity bit of this flag byte. 0 = GPIO PME is signaled via a level. 1 = GPIO PME is signaled via a pulse. **Note:** If GPIO PME Enable is 0, this bit is ignored.
5	**GPIO PME Length** When the GPIO PME Configuration bit of this flag byte indicates that the GPIO PME is signaled by a pulse on the **PME_N** pin, this bit determines the duration of the pulse. 0 = GPIO PME pulse length is 1.5 ms. 1 = GPIO PME pulse length is 150 ms. **Note:** If GPIO PME Enable is 0, this bit is ignored. **Note:** The pulse length is relative to the first wakeup event received by the device. In the event that additional wake events are received during the duration of the PME pulse the assertion length shall not be affected.
4	**GPIO PME Polarity** Specifies the level of the signal or the polarity of the pulse used for GPIO PME signaling. 0 = GPIO PME signaling polarity is low. 1 = GPIO PME signaling polarity is high. **Note:** If GPIO PME Enable is 0, this bit is ignored.
3	**GPIO PME Buffer Type** This bit selects the output buffer type for the **PME_N** pin. 0 = Open drain driver 1 = Push-Pull driver **Note:** If GPIO PME Enable is 0, this bit is ignored.
2	**PHY Link Change Enable** This bit selects whether PHY Link Change wakeup event is supported. 0 = PHY link change wakeup not supported 1 = PHY link change wakeup supported **Note:** If GPIO PME Enable is 0, this bit is ignored.
1	**PME Packet Enable** This bit enables/disables Packet detection and wakeup. 0 = Packet event wakeup disabled. 1 = Packet event wakeup enabled. **Note:** If GPIO PME Enable is 0, this bit is ignored.

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TABLE 10-3: GPIO PME FLAGS 0 (CONTINUED)

BIT	DESCRIPTION
0	**PME Perfect DA Enable** This bit enables/disables Perfect DA detection and wakeup. 0 = Perfect DA event wakeup disabled. 1 = Perfect DA event wakeup enabled. **Note:** If GPIO PME Enable is 0, this bit is ignored.

Note: The contents of this field defines several defaults for the Flag Attributes Register (FLAG_ATTR).

10.4.2 GPIO PME FLAGS 1

Table 10-4 describes the GPIO PME Flags 1 byte.

TABLE 10-4: GPIO PME FLAGS 1

BIT	DESCRIPTION
7	**RESERVED**
6	**GPIO CONNECT Buffer Type** This bit selects the output buffer type for the CONNECT pin. 0 = Open drain driver 1 = Push-Pull driver **Note:** If GPIO CONNECT Enable is 0, this bit is ignored.
5	**GPIO CONNECT Enable** Setting this bit enables the assertion of the CONNECT pin, when the USB device controller is ready to attach to the host. 0 = The device does not support GPIO CONNECT signaling. 1 = The device supports GPIO CONNECT signaling.
4	**GPIO CONNECT Polarity** Specifies the level of the signal or the polarity of the CONNECT pin. 0 = GPIO CONNECT signaling polarity is low. 1 = GPIO CONNECT signaling polarity is high. **Note:** If GPIO CONNECT Enable is 0, this bit is ignored.
3:2	**RESERVED**
1	**PME Broadcast Packet Enable** When set this bit enables/disables Broadcast Packet detection and wakeup. 0 = Broadcast Packet event wakeup disabled. 1 = Broadcast Packet event wakeup enabled.
0	**PME WUFF Enable** When set this bit enables/disables wakeup frame detection and wakeup. When enabled wakeup frame filter 0 is configured from EEPROM/OTP. 0 = Wakeup Frame detection disabled. 1 = Wakeup Frame detection enabled.

Note: The contents of this field defines several defaults for the Flag Attributes Register (FLAG_ATTR).

Note: The **CONNECT** pin function is only supported when the device is enabled for HSIC operation.

10.4.3 LED CONFIGURATION 0

TABLE 10-5: LED CONFIGURATION 0

BIT	DESCRIPTION
7:4	**RESERVED**
3	**LED3 Enable (LED3_EN)** When set, the **LED3** pin is enabled.
2	**LED2 Enable (LED2_EN)** When set, the **LED2** pin is enabled.
1	**LED1 Enable (LED1_EN)** When set, the **LED1** pin is enabled.
0	**LED0 Enable (LED0_EN)** When set, the **LED0** pin is enabled.

Note: The contents of this field defines several defaults for the Hardware Configuration Register (HW_CFG).

10.4.4 LED CONFIGURATION 1

TABLE 10-6: LED CONFIGURATION 1

BIT	DESCRIPTION
7:4	**LED1 Control** This field determines the function displayed on the **LED1** pin. The value specified here is loaded into the LED1 Configuration field of the Ethernet PHY LED Mode Select Register.
3:0	**LED0 Control** This field determines the function displayed on the **LED0** pin. The value specified here is loaded into the LED0 Configuration field of the Ethernet PHY LED Mode Select Register.

Note: The contents of this field defines several defaults for the Ethernet PHY LED Mode Select Register.

APPLICATION NOTE: In order to implement EEPROM-Less operation, the Ethernet PHY LED Mode Select Register supports reset protection via Reset Protection (RST_PROTECT) in the Hardware Configuration Register (HW_CFG).

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10.4.5 LED CONFIGURATION 2

TABLE 10-7: LED CONFIGURATION 2

BIT	DESCRIPTION
7:4	**LED3 Control** This field determines the function displayed on the **LED3** pin. The value specified here is loaded into the LED3 Configuration field of the Ethernet PHY LED Mode Select Register.
3:0	**LED2 Control** This field determines the function displayed on the **LED2** pin. The value specified here is loaded into the LED2 Configuration field of the Ethernet PHY LED Mode Select Register.

Note: The contents of this field defines several defaults for the Ethernet PHY LED Mode Select Register.

APPLICATION NOTE: In order to implement EEPROM-Less operation, the Ethernet PHY LED Mode Select Register supports reset protection via Reset Protection (RST_PROTECT) in the Hardware Configuration Register (HW_CFG).

10.4.6 LED CONFIGURATION 3

TABLE 10-8: LED CONFIGURATION 3

BIT	DESCRIPTION
7:0	**LED Behavior [7:0]** The value specified here is loaded into bits [7:0] of the Ethernet PHY LED Behavior Register.

Note: The contents of this field defines several defaults for the Ethernet PHY LED Behavior Register.

APPLICATION NOTE: In order to implement EEPROM-Less operation, the Ethernet PHY LED Behavior Register supports reset protection via Reset Protection (RST_PROTECT) in the Hardware Configuration Register (HW_CFG).

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10.4.7 LED CONFIGURATION 4

TABLE 10-9: LED CONFIGURATION 4

BIT	DESCRIPTION
7:0	**LED Behavior [15:8]** The value specified here is loaded into bits [15:8] of the Ethernet PHY LED Behavior Register.

Note:	The contents of this field defines several defaults for the Ethernet PHY LED Behavior Register.

APPLICATION NOTE:	In order to implement EEPROM-Less operation, the Ethernet PHY LED Behavior Register supports reset protection via Reset Protection (RST_PROTECT) in the Hardware Configuration Register (HW_CFG).

10.4.8 CONFIGURATION FLAGS 0

Table 10-10 describes Configuration Flags 0. If a configuration descriptor exists in the EEPROM, its values must agree with analogous values contained in the Configuration Flags 0. If they do not, unexpected results and untoward operation may occur.

TABLE 10-10: CONFIGURATION FLAGS 0

BIT	DESCRIPTION
31	**HSIC 50ohm Driver Data and Strobe Enable (HSIC_DS_EN50)** Refer to the HSIC 50ohm Driver Data and Strobe Enable (HSIC_DS_EN50) field of the HSIC Enable Register (HSIC_EN) for permissible values.
30	**HSIC Slew Tune Test Bit Data and Strobe (HSIC_DS_SLEW_TUNE)** Refer to the HSIC Slew Tune Test Bit Data and Strobe (HSIC_DS_SLEW_TUNE) field of the HSIC Enable Register (HSIC_EN) for permissible values.
29:27	**Squelch Threshold (CFG0_SQU_THR)** Refer to the Squelch Tune (USB2_SQU_TUNE) field of the USB 2.0 AFE Upstream Control Register (USB2_AFE_CTRL) for permissible values.
26:22	**RESERVED**
21	**HSIC Pin Swap (HSIC_PIN_SWAP)** Refer to the HSIC Pin Swap (HSIC_PIN_SWAP) field of the HSIC Enable Register (HSIC_EN) for permissible values.
20	**Suspend Enable (SUSP_EN)** Refer to the Suspend Enable (SUSP_EN) bit of the USB Configuration Register 0 (USB_CFG0) for permissible values.
19:18	**SUSPEND_N Select (CFG0_SUSPEND_N_SEL)** Refer to the SUSPEND_N Pin Select (SUSPEND_N_SEL) bit of the Hardware Configuration Register (HW_CFG) for permissible values.
17	**SUSPEND_N Polarity (CFG0_SUSPEND_N_POL)** Refer to the SUSPEND_N Pin Polarity (SUSPEND_N _POL) bit of the Hardware Configuration Register (HW_CFG) for permissible values.

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TABLE 10-10: CONFIGURATION FLAGS 0 (CONTINUED)

BIT	DESCRIPTION
16	**Automatic Duplex Detection (CFG0_ADD)** Refer to the Automatic Duplex Detection (ADD) bit of the MAC Control Register (MAC_CR) for permissible field values.
15	**Automatic Speed Detection (CFG0_ASD)** Refer to the Automatic Speed Detection (ASD) bit of the MAC Control Register (MAC_CR) for permissible field values.
14:13	**Enhanced PHY Sleep Timer (PHY_SLEEP_TIMER)** The field sets the value for the Enhanced PHY Sleep Timer which is controlled by the Enhanced PHY Sleep Timer field of the Ethernet PHY Page 1 Extended PHY Control 3 Register.
12:11	**Enhanced PHY Wake Timer (PHY_WAKE_TIMER)** The field sets the value for the Enhanced PHY Wake Timer which is controlled by the Enhanced PHY Wake Timer field of the Ethernet PHY Page 1 Extended PHY Control 3 Register.
10:9	**Link Time Out Control (LINK_TIME_OUT_CTRL)** The field sets the value for the status timeout control which is controlled by the Link Status Timeout Control [1] and Link Status Timeout Control [0] fields of the Ethernet PHY Auxiliary Control and Status Register.
8	**Enhanced PHY Enable (ACT_PHY_EN)** When set, the Enhanced PHY mode is enabled by default. This sets the value of the Enhanced PHY Enable bit of the Ethernet PHY Auxiliary Control and Status Register.
7	**Enable Link Power Management Mode (COM_PLL_LPM_MODE)** Refer to the Enable Link Power Management Mode (COM_PLL_LPM_MODE) bit of the Common Block Test Register (COM_TEST) for permissible values.
6:4	**PHY Boost (CFG0_PHY_BOOST)** Refer to the HS Output Current (PHY_BOOST) field of the USB 2.0 AFE Test Register (USB2_TEST) for permissible values.
3	**Port Swap (CFG0_PORT_SWAP)** Refer to the Port Swap (PORT_SWAP) bit of the USB Configuration Register 0 (USB_CFG0) for permissible values.
2	**LPM Capable (CFG0_LPM_CAPABLE)** Refer to the LPM Capability (LPM_CAP) bit of the USB Configuration Register 0 (USB_CFG0) for permissible values.
1	**Remote Wakeup (CFG0_RMT_WKP)** Refer to the Remote Wakeup Support (RMT_WKP) bit of the USB Configuration Register 0 (USB_CFG0) for permissible values.
0	**Power Method (CFG0_PWR_SEL)** Refer to the Power Method (PWR_SEL) bit of the USB Configuration Register 0 (USB_CFG0) for permissible values.

Note: Power Method, Remote Wakeup, LPM Enable and other such fields specified in Configuration Flags 0 must agree with analogous quantities specified in descriptors. If they do not, unexpected results and untoward operation may occur.

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10.4.9 CONFIGURATION FLAGS 1

Table 10-11 describes Configuration Flags 1.

TABLE 10-11: CONFIGURATION FLAGS 1

BITS	DESCRIPTION
31:17	**RESERVED**
16	**Crystal Suspend Disable (XTAL_SUSP_DIS)** Refer to the Crystal Suspend Disable (XTAL_SUSP_DIS) bit of the Power Management Control Register (PMT_CTL) for permissible values.
15:7	**RESERVED**
6	**TX Swing (TxSwing)** TX Swing (TxSwing) bit of the PIPE Control Register (PIPE_CTL). Refer to Table 5-3 of the PIPE3 specification for details.
5:3	**TX Margin (TxMargin)** TX Margin (TxMargin) bit of the PIPE Control Register (PIPE_CTL). Refer to table 5-3 of the PIPE3 specification.
2:1	**TX Deemphasis (TxDeemphasis)** TX Deemphasis (TxDeemphasis) bit of the PIPE Control Register (PIPE_CTL). Refer to table 5-3 of the PIPE3 specification.
0	**Elasticity Buffer Mode (ElasticityBufferMode)** Elasticity Buffer Mode (ElasticityBufferMode) bit of the PIPE Control Register (PIPE_CTL). **Note:** Refer to table 5-3 of the PIPE3 specification.

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10.4.10 CONFIGURATION FLAGS 2

Table 10-12 describes Configuration Flags 2.

TABLE 10-12: CONFIGURATION FLAGS 2

BITS	DESCRIPTION
31:14	**RESERVED**
13	**Automatic Duplex Polarity (ADP)** See Section 15.1.38, "MAC Control Register (MAC_CR)," on page 182
12	**EEE PHY Link Up Speed Up (EEE_PHY_LINK_CHANGE_SPEED_UP)** See Section 15.1.3, "Hardware Configuration Register (HW_CFG)," on page 144
11	**Energy Efficient Ethernet TX Clock Stop Enable (EEE_TX_CLK_STOP_EN)** See Section 15.1.38, "MAC Control Register (MAC_CR)," on page 182
10	**Energy Efficient Ethernet Enable (EEEEN)** See Section 15.1.38, "MAC Control Register (MAC_CR)," on page 182
9	**Energy Efficient Ethernet TX LPI Automatic Removal Enable (EEE_TX_LPI_AUTO_REMOVAL_EN)** See Section 15.1.38, "MAC Control Register (MAC_CR)," on page 182
8	**Duplex Mode (DPX)** See Section 15.1.38, "MAC Control Register (MAC_CR)," on page 182
7:6	**MAC Configuration (CFG)** See Section 15.1.38, "MAC Control Register (MAC_CR)," on page 182
5:3	**HS Timeout Calibration (HS_TOutCal)** See Section 15.1.22, "USB Configuration Register 1 (USB_CFG1)," on page 169
2:0	**FS Timeout Calibration (FS_TOutCal)** See Section 15.1.22, "USB Configuration Register 1 (USB_CFG1)," on page 169

10.4.11 CONFIGURATION FLAGS 3

Table 10-13 describes Configuration Flags 3.

TABLE 10-13: CONFIGURATION FLAGS 3

BITS	DESCRIPTION
31:16	**RESERVED**
15:0	**HS Detach Time (HS_DETACH)** See Section 15.1.23, "USB Configuration Register 2 (USB_CFG2)," on page 170

10.4.12 GPIO CONFIGURATION

Table 10-13 describes the GPIO configuration field of the EEPROM (Table 10-2). These bits define the defaults for the respective fields in Section 15.1.5, "General Purpose IO Configuration 0 Register (GPIO_CFG0)" and Section 15.1.6, "General Purpose IO Configuration 1 Register (GPIO_CFG1)".

TABLE 10-14: GPIO CONFIGURATION

BITS	DESCRIPTION
63:60	**RESERVED**
59:48	**GPIO 0-11 Enable**
47:44	**RESERVED**
43:32	**GPIO 0-11 Buffer**
31:28	**RESERVED**
27:16	**GPIO 0-11 Direction**
15:12	**RESERVED**
11:0	**GPIO 0-11 Data**

10.5 EEPROM Defaults

The signature value of 0xA5 is stored at address 0. A different signature value indicates to the EEPROM controller that no EEPROM is attached to the device. In this case, and where the OTP is likewise not configured, the defaults values are specified in the respective CSR loaded from the EEPROM. EEPROM fields not loaded into CSRs (e.g. Vendor ID, Product ID) have their defaults defined in the respective descriptors in Section 5.7, "USB Descriptors".

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10.6 Customized Operation Without EEPROM

The device provides the capability to customize operation without the use of an EEPROM. Descriptor information and initialization quantities normally fetched from EEPROM and used to initialize descriptors and elements of the System Control and Status Registers may be specified via an alternate mechanism. This alternate mechanism involves the use of the Descriptor RAM in conjunction with the Attribute Registers and select elements of the System Control and Status Registers. The software device driver orchestrates the process by performing the following actions in the order indicated:

- Initialization of SCSR Elements in Lieu of EEPROM Load
- Attribute Register Initialization
- Descriptor RAM Initialization
- Enable Descriptor RAM and Attribute Registers as Source
- Inhibit Reset of Select SCSR Elements

The following subsections explain these actions. The attribute registers must be written prior to initializing the Descriptor RAM. Failure to do this will prevent the PWR_SEL and RMT_WKUP flags from being overwritten by the bmAttributes of the Configuration Descriptor.

10.6.1 INITIALIZATION OF SCSR ELEMENTS IN LIEU OF EEPROM LOAD

During EEPROM operation, the following register fields are initialized by the hardware using the values contained in the EEPROM. In the absence of an EEPROM, or configured OTP, the software device driver must initialize these quantities as required for the application.

- MAC Receive Address High Register (RX_ADDRH) and MAC Receive Address Low Register (RX_ADDRL)
- SUSPEND_N Pin Select (SUSPEND_N_SEL) bit of the Hardware Configuration Register (HW_CFG)
- SUSPEND_N Pin Polarity (SUSPEND_N _POL) bit of the Hardware Configuration Register (HW_CFG)
- Device Speed to Connect (DEV_SPEED) bit of the USB Configuration Register 0 (USB_CFG0)
- HS Output Current (PHY_BOOST) field of the USB 2.0 AFE Test Register (USB2_TEST)
- LPM Capability (LPM_CAP) field of the USB Configuration Register 0 (USB_CFG0)
- Remote Wakeup Support (RMT_WKP) field of the USB Configuration Register 0 (USB_CFG0)
- Power Method (PWR_SEL) field of the USB Configuration Register 0 (USB_CFG0)
- Automatic Duplex Detection (ADD) bit of the MAC Control Register (MAC_CR)
- Automatic Speed Detection (ASD) bit of the MAC Control Register (MAC_CR)
- GPIO Enable (GPIOEN), GPIO Buffer Type (GPIOBUF), GPIO Direction (GPIODIR) and GPIO Data (GPIOD) of the General Purpose IO Configuration 0 Register (GPIO_CFG0)
- GPIO Enable (GPIOEN), GPIO Buffer Type (GPIOBUF), GPIO Direction (GPIODIR) and GPIO Data (GPIOD) of the General Purpose IO Configuration 1 Register (GPIO_CFG1)
- **GPIO Wake 0-11 (GPIOWK[11:0])** of the General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE)
- **GPIO Polarity 0-11 (GPIOPOL[11:0])** of the General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE)
- TX Swing (TxSwing), TX Margin (TxMargin), TX Deemphasis (TxDeemphasis), Elasticity Buffer Mode (ElasticityBufferMode) of PIPE Control Register (PIPE_CTL)
- LED3 Enable (LED3_EN) bit of the Hardware Configuration Register (HW_CFG), if desired
- LED2 Enable (LED2_EN) bit of the Hardware Configuration Register (HW_CFG), if desired
- LED1 Enable (LED1_EN) bit of the Hardware Configuration Register (HW_CFG), if desired
- LED0 Enable (LED0_EN) bit of the Hardware Configuration Register (HW_CFG), if desired
- LED3 Configuration, LED2 Configuration, LED2 Configuration, LED1 Configuration, LED0 Configuration of the Ethernet PHY LED Mode Select Register
- All fields of the Ethernet PHY LED Behavior Register

For a description of PME operation see Section 14.0, "Power Management Event (PME) Operation" and the Flag Attributes Register (FLAG_ATTR).

10.6.2 ATTRIBUTE REGISTER INITIALIZATION

The Attribute Registers are as follows:

- BOS Descriptor Attributes Register (BOS_ATTR)
- HS Descriptor Attributes Register (HS_ATTR)
- FS Descriptor Attributes Register (FS_ATTR)
- String Attributes Register 0 (STRNG_ATTR0)
- String Attributes Register 1 (STRNG_ATTR1)
- Flag Attributes Register (FLAG_ATTR)

All of these registers contain fields defining the lengths of the descriptors or block contents written into the Descriptor RAM. If an item is not written into the Descriptor RAM, the associated entry in the Attributes Register must be written as 0. Writing an erroneous or illegal length will result in untoward operation and unexpected results.

Note:	The software device driver must initialize these registers prior to initializing the Descriptor RAM. The bmAttributes field of the HS, and FS descriptors in descriptor RAM (if present) must be consistent with the contents of the Power Method (PWR_SEL) field of the USB Configuration Register 0 (USB_CFG0).

10.6.3 DESCRIPTOR RAM INITIALIZATION

The Descriptor RAM contents are initialized using the Data Port registers. The Data Port registers are used to select the Descriptor RAM and write the descriptor elements into it. The Descriptor RAM is 512 bytes in length. Every descriptor/block written into the Descriptor RAM must be DWORD aligned. The Attribute Registers discussed in Section 10.6.2 must be written with the length of the descriptors written into the Descriptor RAM. If a descriptor/block is not used, hence not written into Descriptor RAM, its length must be written as 0 into the associated Attribute Register.

Note:	The Attribute Registers must be initialized before the Descriptor RAM. Address 0 of the Descriptor RAM is always reserved for the Language ID, even if it will not be supported.

The descriptors/blocks must be written in the following order, starting at address 0 of the RAM and observing the DWORD alignment rule:

- Language ID (2 bytes)
- Manufacturing String Descriptor (String Index 1)
- Product Name String Descriptor (String Index 2)
- Serial Number String Descriptor (String Index 3)
- Configuration String Descriptor (String Index 4)
- Interface String Descriptor (String Index 5)
- BOS Block
- HS Device Descriptor
- HS Configuration Descriptor
- FS Device Descriptor
- FS Configuration Descriptor

An example of Descriptor RAM use is illustrated in Figure 10-9. In it, the BOS Block contains the BOS Descriptor (5 bytes), and a USB 2.0 Extension Descriptor (7 bytes) and a reserved 10 bytes for a total length of 22 bytes.

As in the case of descriptors specified in EEPROM, the following restrictions apply to descriptors written into Descriptor RAM:

1. For Device Descriptors, the only valid values for the length are 0 and 18. The descriptor size for the Device Descriptors specified in the Descriptor RAM is a don't care and always overwritten by HW to 0x12 when transmitting the descriptor to the host.
2. The descriptor type for Device Descriptors specified in the Descriptor RAM is a don't care and is always overwritten by HW to 0x1 when transmitting the descriptor to the host.

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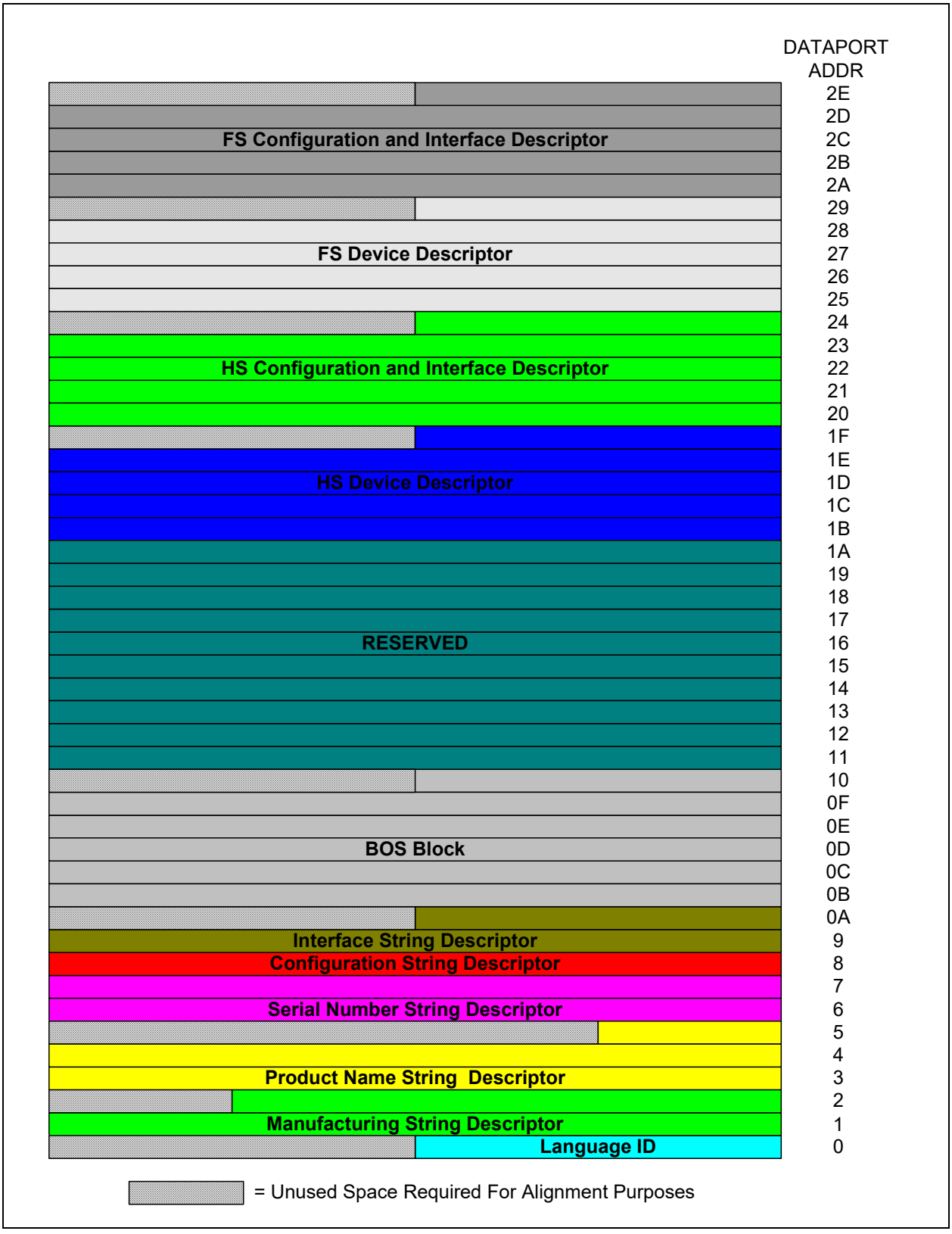
3. For the Configuration and Interface descriptor, the only valid values for the length are 0 and 18. The descriptor size for the Configuration Descriptors specified in the Descriptor RAM is a don't care and always overwritten by HW to 0x12 when transmitting the descriptor to the host.
4. The descriptor type for the Configuration Descriptors specified in the Descriptor RAM is a don't care and always overwritten by HW to 0x2 when transmitting the descriptor to the host.
5. If a string descriptor does not exist in the Descriptor RAM, the referencing descriptor must contain 00h for the respective string index field.
6. If all string descriptor lengths are zero, then a Language ID will not be supported.

Note: The first entry in the Descriptor RAM is always reserved for the Language ID, even if it will not be supported.

Descriptors having bMaxPacketSize other than 40h when operating in Full-Speed or High-Speed mode will result in unwanted behavior and untoward results. Descriptors having bNumConfigurations with values other than 1 will result in unwanted behavior and untoward results.

FIGURE 10-9: DESCRIPTOR RAM EXAMPLE



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10.6.4 ENABLE DESCRIPTOR RAM AND ATTRIBUTE REGISTERS AS SOURCE

The EEPROM Emulation Enable (EEM) bit of the Hardware Configuration Register (HW_CFG) must be set by the software device driver to use the Descriptor RAM and the Attribute Registers for custom operation. Upon assertion of EEPROM Emulation Enable (EEM), the hardware will utilize the Descriptor information contained in the Descriptor RAM, the Attributes Registers, and the values of the items listed in Section 10.6.1 to facilitate custom operation.

10.6.5 INHIBIT RESET OF SELECT SCSR ELEMENTS

The software device driver must take care to ensure that the contents of the Descriptor RAM and SCSR register content critical to custom operation using Descriptor RAM are preserved across reset operations other than POR. The driver must configure the Reset Protection (RST_PROTECT) bit of the Hardware Configuration Register (HW_CFG) in order to accomplish this.

The following registers have contents that can be preserved across all resets other than POR. Consult the register's description for additional details.

- Descriptor RAM (Section 10.6.3)
- Attribute Registers (Section 10.6.2)
- MAC Receive Address High Register (RX_ADDRH) and MAC Receive Address Low Register (RX_ADDRL)
- Hardware Configuration Register (HW_CFG)
- USB Configuration Register 0 (USB_CFG0)
- USB Configuration Register 1 (USB_CFG1)
- USB Configuration Register 2 (USB_CFG2)
- MAC Control Register (MAC_CR)
- Flag Attributes Register (FLAG_ATTR)
- General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE)
- Ethernet PHY LED Mode Select Register
- PIPE Control Register (PIPE_CTL)

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11.0 ONE TIME PROGRAMMABLE (OTP) MEMORY

The device integrates a 1K One Time Programmable (OTP) memory to store various configuration data and serve as an EEPROM replacement to reduce bill of material costs. OTP programming is supported over USB to facilitate end user customization. Microchip provides a comprehensive software programming tool, Pro-Touch, for configuring the device's OTP memory. All OTP configuration is to be performed via the Pro-Touch programming tool. For additional information on the Pro-Touch programming tool, refer to www.microchip.com.

OTP may potentially co-exist with an external EEPROM. Refer to Section 10.1, "EEPROM and OTP Relationship," on page 97 for details.

11.1 OTP Format

The OTP format is based upon the format specified for the EEPROM. See Section 10.4, "EEPROM Format," on page 103 for details.

As with the EEPROM, a signature is required to define whether or not the OTP has been programmed. If the value 0xF3 or 0xF7 is found at byte 0, the OTP shall be determined to be programmed.

A signature of 0xF3 indicates that the device is configured using values (Mac Address and subsequent as per EEPROM Contents) from byte offset 1 in the OTP. A value of 0xF7 indicates that the device is configured loading values (Mac Address and subsequent as per EEPROM Contents) from byte offset 0x101 in the OTP.

APPLICATION NOTE: The dual signatures enable a mechanism for the OTP to be programmed twice. This may prove useful for initial bring up of the device where inadvertently mis-programming the device could render it non-functional. This scheme requires that when an offset of 0xF3 is used that only the first 255 bytes of the OTP are programmed. In the event that the OTP was mis-configured the device can be "saved" by changing the signature on byte 0 from 0xF3 to 0xF7 and writing the new content starting at byte 0x101.

APPLICATION NOTE: Software must ensure that the offsets are appropriately configured to support the dual 256 byte partitioning when this mode of operation is desired. Even when using 0xF7 the offsets are still from 0x0.

As with the EEPROM, if a valid signature is not present at byte 0, the OTP shall be deemed to not be programmed and the device will not use it for configuration.

11.2 OTP Interrupt

The OTP module's interrupt has been mapped into the Interrupt Endpoint as well as the Interrupt Status Register (INT_STS).

OTP program operations take a significant amount of time and therefore are posted. A general rule of thumb is 5 ms/bit. The completion of a program operation is signified by the OTP Write Done Interrupt (OTP_WR_DONE_INT).

11.3 OTP System Reset

Certain system reset events cause the contents of the OTP to be re-loaded, as detailed in Section 12.0, "Resets". The OTP is powered up initially after a reset event and its contents automatically loaded into the device's Descriptor RAM and various configuration CSRs. See Section 12.0, "Resets" for further details.

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12.0 RESETS

The device provides the following chip-level reset sources:

- Power-On Reset (POR)
- External Chip Reset (RESET_N)
- Lite Reset (LRST)
- Soft Reset (SRST)
- USB Reset
- VBUS_DET

Additionally, the device provides a non-chip-level Ethernet PHY Software Reset.

12.1 Power-On Reset (POR)

A Power-On Reset (POR) occurs whenever power is initially applied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset for approximately 20 ms. EEPROM/OTP contents are loaded by this reset.

The POR is a combination of five separate POR circuits that measure the voltage on the following domains:

- Ethernet PHY 1.2 V
- Ethernet PHY 2.5 V
- USB PHY 1.2 V
- USB PHY 3.3 V
- VDDVARIO

After power up, the POR initially de-asserts after the Rising Threshold is passed. In the event that the supply drops below the Falling Threshold the POR asserts. The POR stays asserted until the Rising Threshold is once again crossed. The rising and falling thresholds are listed in Table 12-1.

TABLE 12-1: POR THRESHOLDS

POR	RISING THRESHOLD	FALLING THRESHOLD
Ethernet PHY 1.2V	0.9 V	0.8 V
Ethernet PHY 2.5V	2.0 V	1.8 V
USB PHY 1.2V	0.9 V	0.8 V
USB PHY 3.3V	2.7 V	2.35 V
VDDVARIO	1.45 V	1.25 V

APPLICATION NOTE: The POR on **VDDVARIO** targets 1.8 V I/O operation. If a higher voltage is used, than an external POR may be required to provide full brown out detection on the I/O domain.

12.2 External Chip Reset (RESET_N)

A hardware reset will occur when the **RESET_N** pin is driven low. Assertion of **RESET_N** is not required at power-on. However, if used, **RESET_N** must be driven low for a minimum period as defined in Section 16.6.2, "RESET_N Timing," on page 263. The **RESET_N** pin is pulled-high internally but must be connected externally to **VDDVARIO** if unused.

Note: If configured, the EEPROM/OTP contents are reloaded by this reset.

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12.3 Lite Reset (LRST)

This reset is initiated via the Soft Lite Reset (LRST) bit in the Hardware Configuration Register (HW_CFG). It will reset the entire device with the exception of the USB Device Controller and the USB PHY. The PLL is not turned off during a Lite Reset.

Note:	This reset does not cause the USB contents from the EEPROM/OTP to be reloaded. This reset does not place the device into the Unconfigured state. The Soft Lite Reset (LRST) bit does not clear control register bits marked as NALR.

APPLICATION NOTE: Prior to issuing an LRST, system software shall stop activity on the device's USB pipes. After the LRST is issued, the system software shall restart the pipes. This process includes sending CLEAR_FEATURE(ENDPOINT_HALT) for the device pipes, which causes data toggle on the device side to be reset. The data toggle must also be reset for each pipe on the host side.

12.4 Soft Reset (SRST)

Software initiated reset is accomplished by setting the Soft Reset (SRST) bit of Hardware Configuration Register (HW_CFG). After this bit is set, the device soft detaches from the USB bus. The duration of the detachment is typically 10 ms for HS/FS. Upon expiration of this time, the device will completely reset itself and re-attach to the USB bus.

Note:	If configured, the EEPROM/OTP contents are reloaded by this reset.

APPLICATION NOTE: The detachment time is programmable via the HS Detach Time (HS_DETACH) fields in USB Configuration Register 2 (USB_CFG2).

12.5 USB Reset

A USB reset causes a reset of the entire device with the exception of the USB Device Controller and the USB PHY. The USB PLL is not turned off. After a USB reset, the Device Ready (READY) bit in the Power Management Control Register (PMT_CTL) can be read by the Host and will read back a '0' until the EEPROM/OTP contents are loaded (provided one is present). The device than can be configured via its control registers.

Note:	This reset does not cause the entire contents from the EEPROM or OTP to be reloaded. Only the MAC address is reloaded.

12.6 VBUS_DET

The removal of USB power causes the device to transition to the UNPOWERED state. The chip is held in reset while in the UNPOWERED state.

Note:	After **VBUS_DET** is asserted, the contents of the EEPROM/OTP are reloaded, if configured.

Note:	After transitioning out of the UNPOWERED state, the internal Ethernet PHY remains in reset to minimize power.

12.7 Ethernet PHY Software Reset

An Ethernet PHY software reset is provided via the PHY Reset (PHY_RST) bit in the Power Management Control Register (PMT_CTL). This reset is not a chip-level reset and resets only the Ethernet PHY. When asserted, the Gigabit Ethernet PHY is reset for a minimum of 2 ms.

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The Device Ready (READY) bit in the Power Management Control Register (PMT_CTL) asserts when the Ethernet PHY is functional. It may take over 100 ms for the device to become operational after this reset, depending on the state of Disable Wait Analog Voltage Reference Stable (DIS_WAIT_ANA_REF) in Power Management Control Register (PMT_CTL).

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13.0 CLOCKS AND POWER MANAGEMENT (CPM)

The Clocks and Power Management (CPM) block is responsible for generating the device clocks and controlling the power management logic. CPM functions include:

- Enabling the host to place the device in a reduced power state, e.g. suspend state, by disabling internal clocks and powering down various device blocks, including PLLs.
- Providing detection of various wakeup events.
- Providing a host-readable READY flag which is set when the device is in the NORMAL state.
- Controlling the loading of OTP or EEPROM values after a system reset.
- Supporting USB 2.0 Suspend
- Supporting LPM extensions

These functions are detailed in the following sub-sections:

- Device Clocking
- Power States
- Suspend States
- Wake Events

13.1 Device Clocking

The device requires a fixed-frequency 25 MHz clock source. This is typically provided by attaching a 25 MHz crystal to the **XI** and **XO** pins. The clock can optionally be provided by driving the **XI** input pin with a single-ended 25 MHz clock source. If a single-ended source is selected, the clock input must run continuously for normal device operation.

Internally, the device generates its required clocks with a phase-locked loop (PLL). It reduces its power consumption in several of its operating states by disabling its internal PLL and derivative clocks. The 25 MHz clock remains operational in all states where power is applied.

Refer to Section 16.7, "Clock Circuit," on page 265 for additional clocking requirements.

13.2 Power States

The following power states are supported:

- UNPOWERED
- NORMAL (Unconfigured and Configured)
- Suspend States (SUSPEND0, SUSPEND1, SUSPEND2, and SUSPEND3)

Figure 13-1 details the device power states and transitions. In order to simplify Figure 13-1, the USB Suspend and USB Resume transitions are a superset of the following conditions:

- **USB Suspend:** USB 2.0 Suspend
- **USB Resume:** USB 2.0 Resume, transition to LPM L0

Additionally, only a subset of wake events are shown, due to space constraints. A detailed wakeup description is provided in the following sub-sections.

Note:	It is not possible to transition from SUSPEND2 to NORMAL Configured if SUSPEND2 was entered via a transition from NORMAL Unconfigured. When the device is bus powered, **VBUS_DET** is externally tied to 1b. Therefore, the UNPOWERED state only has meaning for self powered operation.

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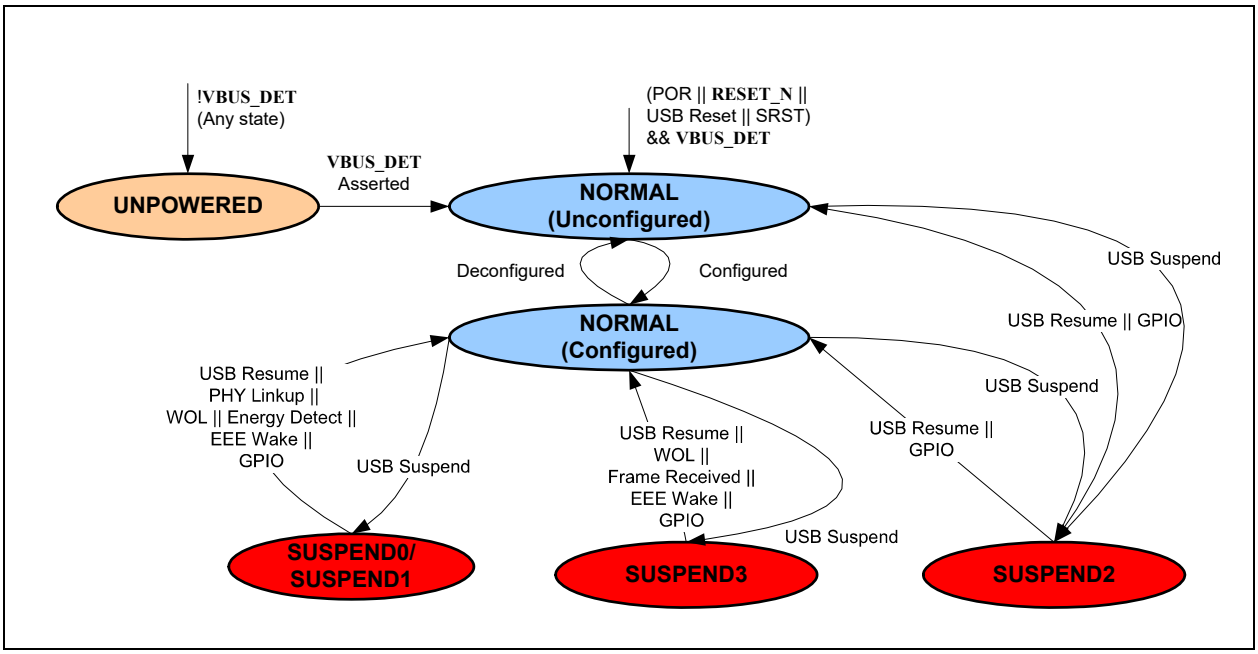
FIGURE 13-1: POWER STATES



13.2.1 UNPOWERED STATE

The UNPOWERED state provides a mechanism for the device to conserve power when **VBUS_DET** is not connected and the device is self powered.

The device initially enters the UNPOWERED state when a system reset occurs and USB power is not detected. This state persists until the **VBUS_DET** is asserted. The UNPOWERED state is alternatively entered whenever **VBUS_DET** de-asserts.

In the UNPOWERED state, the crystal oscillator and PLLs are turned off and the Ethernet PHY is disabled. Assertion of **VBUS_DET** causes the device to enable the crystal oscillator and PLLs. When PLLs are stable, the device transitions to the NORMAL-Unconfigured state.

In order to make the device fully operational, the host must configure the device, which places it in the NORMAL Configured state.

13.2.2 NORMAL STATE

The NORMAL state is the functional state of the device. The are two versions of this state, NORMAL-Configured and NORMAL-Unconfigured. In the configured variation all modules are enabled. The Unconfigured variation has only a subset of the modules enabled to allow for power savings.

The NORMAL state is entered by any of the following methods.

- A system reset and **VBUS_DET** is asserted
- The device is in the UNPOWERED state and **VBUS_DET** is asserted
- The device is in a SUSPEND*x* state and the host issues resume signaling.
- The device is in a SUSPEND*x* state and a wake event is detected.

13.2.2.1 NORMAL-Unconfigured

Upon initially entering the NORMAL-Unconfigured state, the device is not configured. While unconfigured, the device will only draw up to 100 mA per the USB 2.0 Specification. After being configured, an additional 400 mA may be consumed when operating in USB 2.0 mode.

In order to maximize power savings in NORMAL-Unconfigured mode, the Gigabit Ethernet PHY is held in reset.

The device moves from the Normal-Unconfigured to Normal-Configured when directed by the host via the SetConfiguration request. Likewise, the host can move the device back into the Normal-Unconfigured state with this request.

13.2.2.2 NORMAL-Configured

This is the fully operational state of the device where all clocking resources and analog blocks are enabled and functional.

13.2.2.3 Reset Operation

After a system reset, the device is moved into the NORMAL-Unconfigured state (unless the device is self-powered and **VBUS_DET** = 0). The host must then configure the device.

The following steps illustrate the process for a POR. The steps vary depending on the reset and the initial state of the device.

13.2.2.4 Suspend Operation

When returning to the NORMAL state from a SUSPEND*x* state, the USB context is maintained. After entering the NORMAL-Configured state, the Device Ready (READY) bit in the Power Management Control Register (PMT_CTL) is asserted after the PHY is operational.

Note:	If the originating suspend state is SUSPEND2, then the host is required to reinitialize the Ethernet PHY registers.

13.3 Suspend States

The suspend state is entered after the USB Host places the device in low power state as defined below:

- USB 2.0 Suspend (LPM L2)

There are several variations of the suspend state available. Each state offers different options in terms of power consumption and remote wakeup support.

A suspend state can only be entered via a transition from the NORMAL state. The Suspend Mode (SUSPEND_MODE) field of the Power Management Control Register (PMT_CTL) indicates which suspend state is to be used. A transfer back to the NORMAL state occurs when requested by the host (e.g. USB Resume signaling) or a configured wakeup event is detected by the device.

When the device is in the NORMAL-Unconfigured state, it is only possible to transition to the SUSPEND2 state. After being taken out of suspend, the device transitions back to NORMAL-Unconfigured.

Note:	If the device is deconfigured, then Suspend Mode (SUSPEND_MODE) resets to 10b.

13.3.1 RESET FROM SUSPEND

All suspend states must respond to USB Reset and **RESET_N** pin assertion. The application of these resets result in the device being re-initialized and placed into the NORMAL-Unconfigured state.

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13.3.2 SUSPEND0

This state is selected when the Suspend Mode (SUSPEND_MODE) field of the Power Management Control Register (PMT_CTL) is set to 00b.

In this state the device can optionally be programmed to detect GPIO wake, Wake-On-LAN event, Magic Packet, PHY Link Status, EEE wake, etc.. Refer to Section 13.4.2, "Enabling Wake Events," on page 131 for details on how to program events that cause resumption from the SUSPEND0 state.

To maximize power savings the PLLs are shutdown. The 25 MHz crystal oscillator remains operational to clock the MAC and the Gigabit Ethernet PHY.

The detection of a WOL event causes the PLL, as required for the established USB link, to be turned on and all output clocks to be enabled.

Note: Software may optionally enable ARP offload or NS offload in this state.

APPLICATION NOTE: Additional power savings can be gained if the Ethernet Link is forced to negotiate to a lower speed. However, this may have additional drawbacks. Studies done with drivers for prior controllers have shown latencies in excess of four seconds.

13.3.3 SUSPEND1

This state is logically equivalent to SUSPEND0 and is selected when the Suspend Mode (SUSPEND_MODE) field of the Power Management Control Register (PMT_CTL) is set to 00b.

13.3.4 SUSPEND2

This state is selected when the Suspend Mode (SUSPEND_MODE) field of the Power Management Control Register (PMT_CTL) is set to 10b. SUSPEND2 is the default suspend mode.

SUSPEND2 consumes the least power of the suspend state options. It is the only option that meets the USB 2.5 mA suspend power consumption requirement. In this state, GPIO assertion is the only remote wakeup source supported.

13.3.5 SUSPEND3

This state is selected when the Suspend Mode (SUSPEND_MODE) field of the Power Management Control Register (PMT_CTL) is set to 11b.

In this suspend state, most clocks in the device are enabled and power consumption is similar to the NORMAL-Configured state. Power savings is realized only in powering down the USB AFEs which happens automatically after the host software moves the device into USB Suspend. The target for power savings in this state is the host CPU. This suspend state shall be used for AOAC support and/or whenever the packet event that caused the wake event must be saved.

Refer to Section 13.4.2.1, "Enabling GPIO Wake Events," on page 131, Section 13.4.2.4, "Enabling “GOOD Frame” Wake Events," on page 132, Section 13.4.2.2, "Enabling WOL Wake Events," on page 131, and Section 13.4.2.5, "Enabling “AOAC” Wake events" for detailed instructions on how to program events that cause resumption from the SUSPEND3 state. SUSPEND3 can also be exited when Energy Efficient Ethernet RX Wake (EEE_RX_WAKE) is set with Energy Efficient Ethernet RX Wake Enable (EEE_RX_WAKE_EN) set or when Energy Efficient Ethernet TX Wake (EEE_TX_WAKE) is set with Energy Efficient Ethernet TX Wake Enable (EEE_TX_WAKE_EN) set.

Unlike other suspend states, there is the capability to store the frame that triggered the wakeup into the RX FIFO. This is discussed further in Section 13.4.2.5, "Enabling “AOAC” Wake events". After the wakeup frame is received, all subsequent frames that pass the filtering constraints in the MAC and Receive Filtering Engine (RFE) are written into the RX FIFO as well. This feature allows the OS to determine the cause of the wake event and report the packet and any following ones that were received while the USB bus has not yet been resumed.

To enable an aggressive suspend policy by the host, SUSPEND3 supports the concept of “Good Frame” wake-ups. In this scenario any non-errored receive frame that passes the RFE filters causes a wakeup and is stored in the RX FIFO. All subsequent frames are also written into the FIFO. Utilizing the RFE filter rules in the context of a wakeup is enabled by the RFE Wakeup Frame Received (RFE_WAKE_FR) bit.

Note: It is appropriate to enable ARP offload and NS offload in this state, though it is completely under software control and not enforced by hardware. For AOAC support, that is mandatory, and normally executed by the operating system.

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13.3.6 NETDETACH

NetDetach is a mode of operation where the device detaches from the USB bus after the Ethernet cable is disconnected. It is typically used in environments that cannot implement selective suspend when the link is down (such Windows OS prior to Windows 8). This is advantageous for mobile devices, as an attached USB device prevents the host CPU from entering the C3 state. Allowing the CPU to enter the C3 state maximizes battery life.

When detached, the device power state is essentially the same as the SUSPEND0 state. After the Ethernet cable is reconnected, or a programmed GPIO pin asserts, the device automatically attaches to the USB bus.

NetDetach requires assistance of the host software driver. The driver will monitor the link status of the Ethernet PHY and program the part appropriately to detach and re-attach to the USB bus upon link change. The following steps illustrate this process:

1. Ethernet cable is not detected.
2. Driver detects assertion of the PHY_INT bit via the interrupt control endpoint. The driver may also detect PHY interrupt assertion by polling the Interrupt Status Register (INT_STS). It is also valid to only poll the PHY's link status bit without looking at interrupt endpoint or interrupt status.
3. Driver reads the respective Ethernet PHY CSRs and determines that the link has been lost.
4. Driver programs the device and Ethernet PHY to detect Link Status Change from link down to link up.
5. Driver sets the NetDetach Enable (NETDET_EN) bit in the Hardware Configuration Register (HW_CFG). The **CONNECT** function may also be enabled via the Hardware Configuration Register (HW_CFG).
6. The device then detaches from the USB bus and disables the PLLs. The driver is unloaded at this point and can no longer communicate with the device.
7. At some point in the future, the Ethernet cable is reconnected and link is regained, or an appropriately configured GPIO pin is asserted.
8. The device enables the USB PLLs and AFEs.
9. The device attaches to the USB bus.
10. The driver is loaded and the device is configured by the driver. The driver examines the NetDetach Status (NETDET_STS) bit in the Hardware Configuration Register (HW_CFG) to determine if it was reloaded as a result of coming back from a NetDetach operation or for some other event. The driver may also disable the **CONNECT** function if previously enabled.

APPLICATION NOTE: In order to maximize power savings it is recommended that the driver utilize the Enhanced PHY power down feature of the Ethernet PHY (via Configuration Flags 0). Further power savings may be obtained by forcing the link to 100 Mbps.

APPLICATION NOTE: GPIO wakes are supported in this state.

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13.4 Wake Events

The following events can wake up/enable the device.

- USB Host Resume
- **VBUS_DET** assertion
- Wakeup Frame
- Magic Packet
- PHY Link Change
- EEE Wake
- Global Unicast frame
- Broadcast frame
- Perfect DA Match
- TCP SYN Packet
- “Good” Frame
- GPIO[11:0]

Table 13-1 illustrates the wake events permitted in each of the power states.

TABLE 13-1: POWER STATUS/WAKE EVENT MAPPING

Wake Event	SUSPEND0/ SUSPEND1	SUSPEND2	SUSPEND3	Unpowered	PME Mode	NetDetach
USB Host Resume Signaling	YES	YES	YES	NO	NO	NO
VBUS Detection	NO	NO	NO	YES	NO	NO
Magic Packet	YES	NO	YES	NO	YES	NO
Wakeup Frame	YES	NO	YES	NO	YES	NO
Broadcast Frame	YES	NO	YES	NO	YES	NO
Perfect DA Match of Physical Address	YES	NO	YES	NO	YES	NO
Good Frame	NO	NO	YES	NO	NO	NO
TCP SYN	YES	NO	YES	NO	NO	NO
EEE RX Wake	YES	NO	YES	NO	NO	NO
EEE TX Wake	YES	NO	YES	NO	NO	NO
PHY Link Change (Internal PHY)	YES	NO	YES	NO	YES	YES
GPIO[10:0]	YES	YES	YES	NO	YES	YES

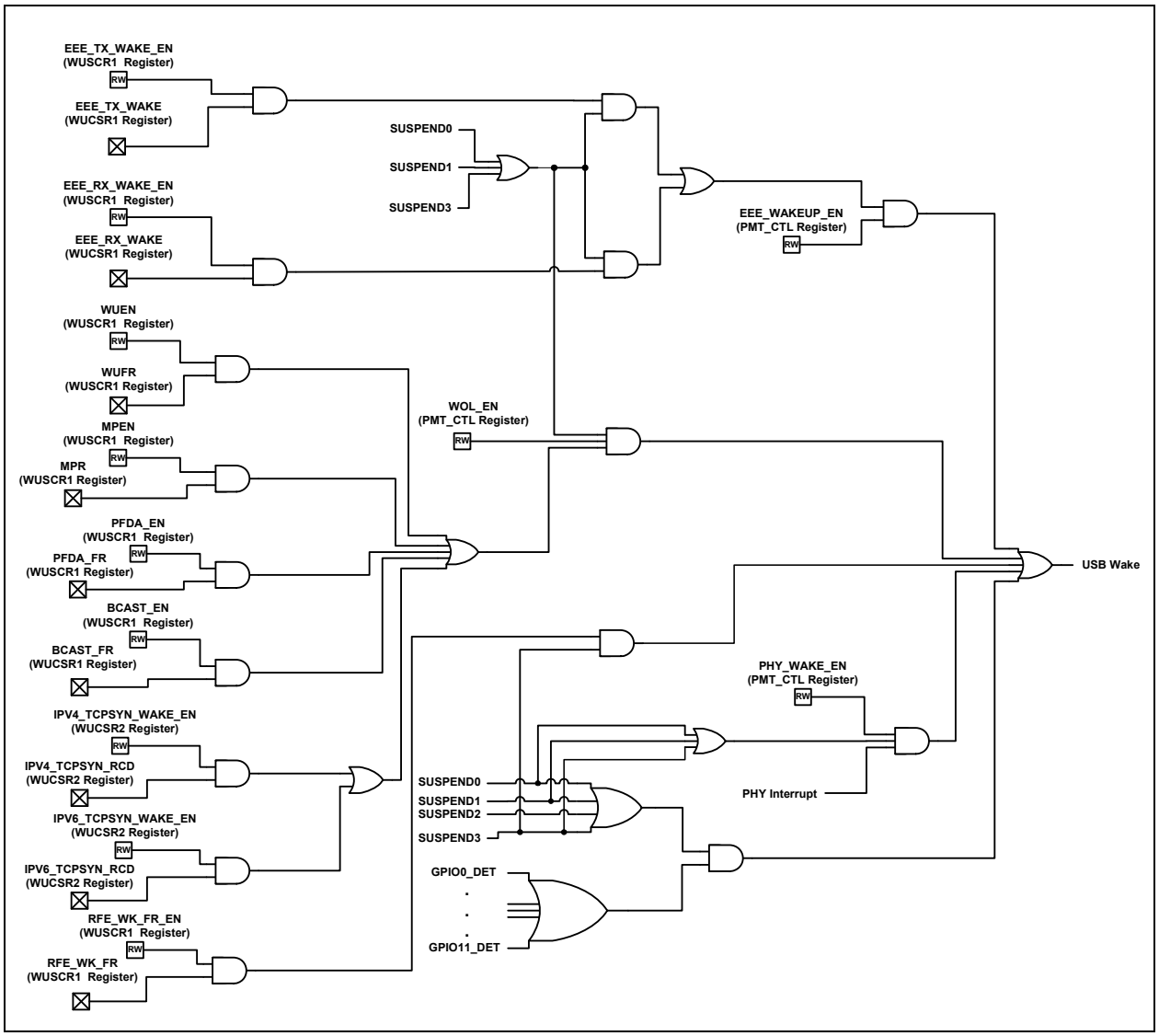
The occurrence of a GPIO wake event causes the corresponding bit in the Interrupt Status Register (INT_STS) to be set. Before suspending the device, the host must ensure that any pending wake events are cleared. Otherwise, the device will immediately be awakened after being suspended.

13.4.1 DETECTING WAKEUP EVENTS

The device supports the ability to generate remote wakeup events. A simplified diagram of the wake event detection logic is shown in Figure 13-2.

When an enabled remote wake event is detected, the USB Device Controller notifies the host. For HS mode, remote wakeup signaling is issued. The device can also de-assert the **SUSPEND_N** pin, depending on its configuration.

FIGURE 13-2: WAKE EVENT DETECTION BLOCK DIAGRAM



In addition to the above, the device also supports remote wakeup. In HS/FS mode the DEVICE_REMOTE_WAKEUP feature must be set.

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13.4.2 ENABLING WAKE EVENTS

The following sub-sections detail the procedure for enabling various wake events:

- Enabling GPIO Wake Events
- Enabling WOL Wake Events
- Enabling Link status Change Wake Events
- Enabling “GOOD Frame” Wake Events
- Enabling “AOAC” Wake events

13.4.2.1 Enabling GPIO Wake Events

The Host system shall perform the following steps to enable the device to issue a remote wake event on detection of a GPIO wake.

1. The GPIO pin is programmed to facilitate generation of the wake event.The respective GPIO must be enabled via GPIO Enable (GPIOEN) of General Purpose IO Configuration 0 Register (GPIO_CFG0) or GPIO Enable (GPIOEN) of General Purpose IO Configuration 1 Register (GPIO_CFG1).
2. The GPIO pin must be enabled for wakeup and its desired polarity specified in the **GPIO Wake 0-11 (GPIOWK[11:0])** and **GPIO Polarity 0-11 (GPIOPOL[11:0])** fields, respectively, of the General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE).
3. The Host places the device in the any one of the SUSPEND states by setting the Suspend Mode (SUSPEND_MODE) field of the Power Management Control Register (PMT_CTL) to indicate the desired suspend state, then sends suspend signaling.
4. On detection of an enabled GPIO wake event, the device will transition back to the NORMAL state and signal a remote wake event. The Host may then examine the GPIO [11:0] (GPIOx_INT_WK) status bits of the Wakeup Source Register (WK_SRC) to determine the source of the wakeup.

13.4.2.2 Enabling WOL Wake Events

The Host system shall perform the following steps to enable the device to assert a remote wake event on detection of a Wake on LAN event.

1. All transmit and receive operations must be halted: All pending Ethernet TX and RX operations must be completed. The MAC RX and TX paths are disabled.
2. The MAC must be configured to detect the desired wake event. This process is explained in Section 8.3.2.2, "Wakeup Frame Detection," on page 77 for Wakeup Frames and in Section 8.3.2.3, "Magic Packet Detection," on page 79 for Magic Packets. Configuring Perfect DA and Broadcast Frame wakeup detection is analogous and requires the Perfect DA Frame Received (PFDA_FR) or Broadcast Wakeup Enable (BCAST_EN) bit to be set in the Wakeup Control and Status Register 1 (WUCSR1).
3. Bit 1 of the Wakeup Status (WUPS[1]) in the Power Management Control Register (PMT_CTL) must be cleared since a set bit will cause the immediate assertion of wake event when the Wake-On-LAN Enable (WOL_EN) bit is set. The WUPS[1] bit will not clear if the internal MAC wakeup event is asserted.
4. Set the Wake-On-LAN Enable (WOL_EN) bit in the Power Management Control Register (PMT_CTL).
5. The MAC RX path is re-enabled.
6. The Host places the device in SUSPEND0 or SUSPEND3 state by appropriately setting the Suspend Mode (SUSPEND_MODE) field in the Power Management Control Register (PMT_CTL), to indicate the desired suspend state. The host then sends suspend signaling.

On detection of an enabled event, the device will transition back to the NORMAL state and signal a wake event. Upon discovering wakeup occurred, the status bits of the Wakeup Source Register (WK_SRC) may be examined to determine the particular event that caused the wakeup.

13.4.2.3 Enabling Link status Change Wake Events

The Host system must perform the following steps to enable the device to assert a remote_wake event on detection of an Ethernet link status change or Energy Detection.

1. Ethernet cable is not detected or has become disconnected.
2. All transmit and receive operations must be halted: All pending Ethernet TX and RX operations must be completed. The MAC RX and TX paths are disabled.
3. The appropriate CSRs are configured in the PHY to enable the Energy and Link Status Change detection. The Link State-Change Interrupt Mask is unmasked and the PHY asserts its interrupt when the condition is detected.
4. Bit 0 of the Wakeup Status (WUPS[0]) in the Power Management Control Register (PMT_CTL) must be cleared, since a set bit will cause the immediate assertion of wake event when PHY Interrupt Enable (PHY_WAKE_EN) is set. The WUPS[0] bit will not clear if the internal PHY interrupt is asserted.
5. Set the PHY Interrupt Enable (PHY_WAKE_EN) bit in the Power Management Control Register (PMT_CTL).
6. The Host places the device in SUSPEND0 or SUSPEND1 state by appropriately setting the Suspend Mode (SUSPEND_MODE) field in the Power Management Control Register (PMT_CTL), to indicate the desired suspend state, then sends suspend signaling.
7. On detection of Ethernet activity, the device will signal a remote wake event and transition back to the NORMAL state upon examining the Wakeup Source Register (WK_SRC) the software can know the source was a link change and process it accordingly.

13.4.2.4 Enabling “GOOD Frame” Wake Events

The Host system must perform the following steps to enable the device to initiate a remote wake event on detection of a “Good Frame”. A “Good Frame” being an Ethernet frame that is not corrupted and passes the RFE filter rules as enabled by the Receive Filtering Engine Control Register (RFE_CTL).

After reception of the “Good Frame” all valid subsequent frames received are placed in the Receive FIFO. The frame that caused the “Good Frame” wake may also be stored in the FIFO if Store Wakeup Frame (STORE_WAKE) is set.

1. All transmit and receive operations must be halted: All pending Ethernet TX and RX operations must be completed. The MAC RX and TX paths are disabled.
2. Frame filtering is configured by setting the desired constraints in the Receive Filtering Engine Control Register (RFE_CTL). The RFE Wake Enable (RFE_WAKE_EN) is set in Wakeup Control and Status Register 1 (WUCSR1) as well as Wake-On-LAN Enable (WOL_EN) bit of the Power Management Control Register (PMT_CTL) shall be set to zero.
3. The device may be configured to store the wakeup frame in the FCT RX FIFO by setting Store Wakeup Frame (STORE_WAKE) in the Wakeup Control and Status Register 1 (WUCSR1).
4. Bit 1 of the Wakeup Status (WUPS[1]) in the Power Management Control Register (PMT_CTL) must be cleared since a set bit will cause the immediate assertion of a wake event. The WUPS[1] bit will not clear if the internal MAC wakeup event is asserted.
5. The MAC RX path is re-enabled.
6. The Host places the device in the SUSPEND3 state by setting the Suspend Mode (SUSPEND_MODE) field in the Power Management Control Register (PMT_CTL), to indicate the desired suspend state, and then sends suspend signaling.
7. On detection of a “Good Frame”, the device transitions back to the NORMAL state and signals a remote wake event.
8. Upon discovering a wakeup occurred software shall examine the Wakeup Source Register (WK_SRC). Host software shall perform the desired processing as a result of receiving the “Good Frame” which typically includes passing the received packet up the normal receive path of the software stack.

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13.4.2.5 Enabling “AOAC” Wake events

This section describes how to configure the device for AOAC operation.

After an extended period of idle time, as defined by the host OS, it is desirable to place the system in a deep sleep state. In order to maximize the duration in which the system can stay in sleep the network interfaces, in this case Ethernet, are configured to offload several tasks that would normally awaken the host. The host is only awakened when a pre-programmed wakeup pattern is received. The wakeup frame is stored in the RX FIFO to allow the OS to evaluate the cause of the wakeup as well as pass it up the normal receive path (i.e. so that TCP socket connections can be maintained without retries).

The driver may consult Wakeup Frame Received bit of RX Command C to determine which packet in the RX FIFO instigated the wakeup event. It is not guaranteed that the first packet written into the FIFO caused the wakeup. It is possible for a data frame to have been written into the FIFO while the part is being suspended.

All frames received after wakeup frame are also stored in the FIFO. However these frames must also pass any additional filtering rules programmed into the MAC and RFE as well a frame corruption checks (e.g. FCS).

APPLICATION NOTE: In order to minimize system latency to the full operational state, and allow an aggressive suspend/resume policy, the Ethernet link should not be change (i.e. 100 Mbps mode when Gigabit link exists).

1. All transmit and receive operations must be halted: All pending Ethernet TX and RX operations must be completed. The MAC RX and TX paths are disabled.
2. The MAC must be configured to detect the desired wake event. The wakeup filters are appropriately configured by the host via the Wakeup Filter x Configuration Register (WUF_CFGx) and Wakeup Filter x Byte Mask Registers (WUF_MASKx). This process is explained in Section 8.3.2.2, "Wakeup Frame Detection," on page 77 for Wakeup Frames. Other wake events such as TCP SYN or Magic Packet may also be enabled.
3. Bit 1 of the Wakeup Status (WUPS[1]) in the Power Management Control Register (PMT_CTL) must be cleared since a set bit will cause the immediate assertion of wake event when the Wake-On-LAN Enable (WOL_EN) bit is set. The WUPS[1] bit will not clear if the internal MAC wakeup event is asserted.
4. Set the Wake-On-LAN Enable (WOL_EN) bit in the Power Management Control Register (PMT_CTL).
5. The device shall be configured to store the wakeup frame in the FCT RX FIFO by setting Store Wakeup Frame (STORE_WAKE) in the Wakeup Control and Status Register 1 (WUCSR1).
6. The device shall be configured to disable RFE filtering on wakeup frames by setting Always Pass Wakeup Frame (PASS_WKP) in Receive Filtering Engine Control Register (RFE_CTL).
7. The device is configured to enable ARP and NS offloads. See Section 8.6, "ARP Offload," on page 84 and Section 8.5, "Neighbor Solicitation (NS) Offload," on page 82 for details on how to configure these functions.
8. The MAC RX and TX paths are re-enabled.
9. The Host places the device in the SUSPEND3 state by setting the Suspend Mode (SUSPEND_MODE) field in the Power Management Control Register (PMT_CTL) to 11b, to indicate the desired suspend state, then sends suspend signaling.
10. On detection of an enabled wake event, the device transitions back to the NORMAL state and signals a remote wake event. The software will then examine the Wakeup Source Register (WK_SRC) and perform the desired processing which may include passing the packet up to the operating system if the wake event was due to reception of a WOL packet.

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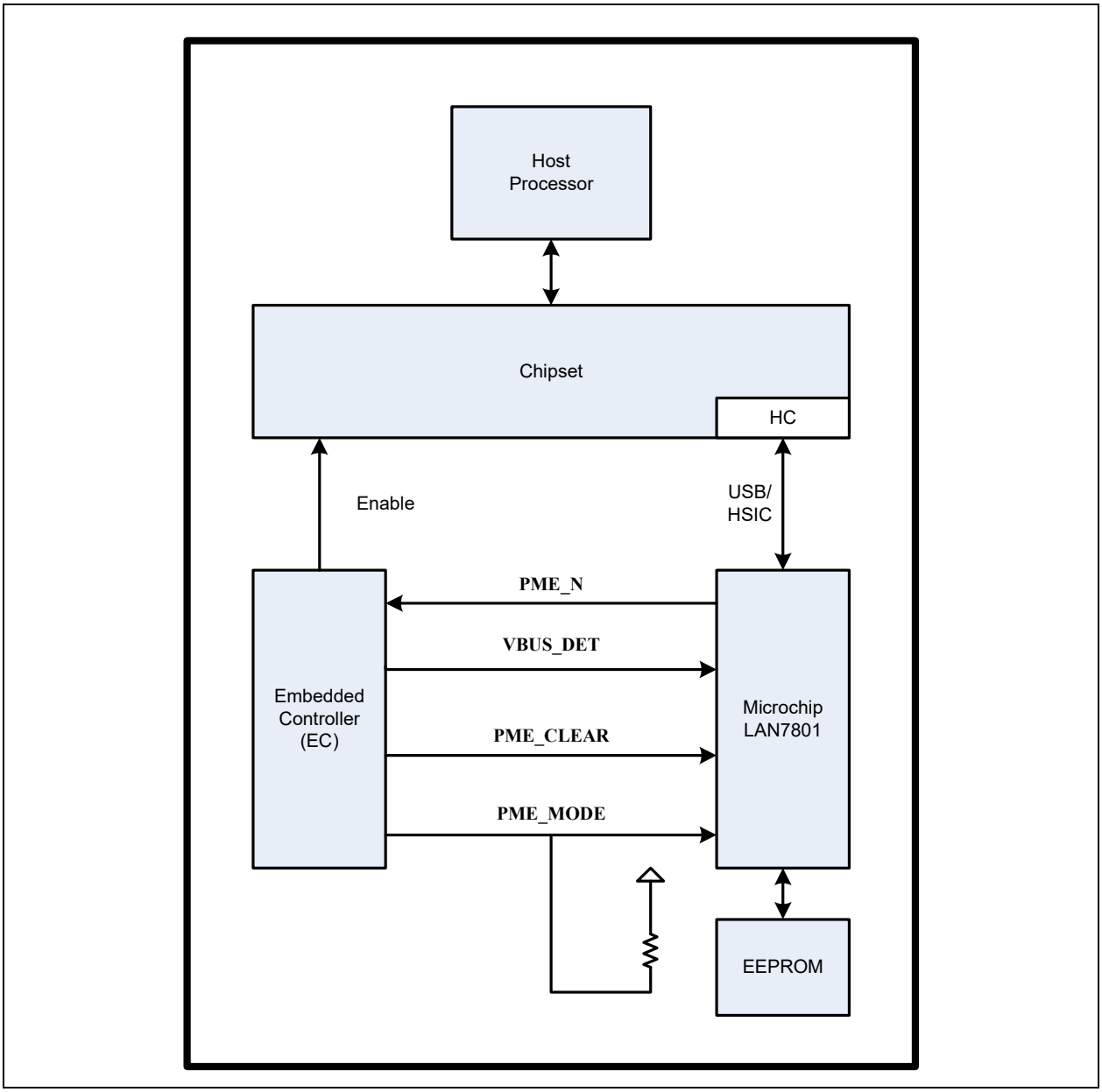
14.0 POWER MANAGEMENT EVENT (PME) OPERATION

The device provides a mechanism for waking up a host system via the Power Management Event (PME) mode of operation. PME signaling is only available while the device is operating in the self powered mode and a properly configured EEPROM is attached. Figure 14-1 illustrates a typical application.

FIGURE 14-1: TYPICAL APPLICATION



The Host Processor is connected to a Chipset containing the Host USB Controller (HC). The USB Host Controller interfaces to the device via the USB signals. An Embedded Controller (EC) signals the Chipset and the Host processor to power up via an Enable signal. The EC interfaces to the device via four signals. The **PME_N** signal is an input to the EC from the device that indicates the occurrence of a wakeup event. The **VBUS_DET** output of the EC is used to indicate bus power availability. The **PME_CLEAR** (**RESET_N**) signal is used to clear the PME. The **PME_MODE** signal is sampled by the device when **PME_CLEAR** (**RESET_N**) is de-asserted and is used by the device to determine whether it should remain in PME mode or resume normal operation.

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The application scenario in Figure 14-1 assumes that the Host Processor and the Chipset are powered off, the EC is operational, and the device is in PME mode, waiting for a wake event to occur. A wake event will result in the device signaling a PME event to the EC, which will then wake up the Host Processor and Chipset via the Enable signal. The EC asserts **VBUS_DET** after the USB bus is powered, sets **PME_MODE** to determine whether the device is to begin normal operation or continue in PME mode, and asserts **PME_CLEAR** (**RESET_N**) to clear the PME.

APPLICATION NOTE: After de-assertion of **PME_CLEAR**, the device is configured. Configuration may entail loading data from EEPROM or OTP if EEPROM-less mode is not used. The EC should not sample **PME_N** during this time, which is dependent on the amount of data programmed in OTP/EEPROM, as the polarity and behavior of **PME_N** has not yet been configured. For EEPROM-less or OTP mode, the PME shall be valid within 1 ms. For an external EEPROM this will be a function of the amount of data programmed in the EEPROM. If all 512 bytes are programmed, the maximum delay is under 16 ms. Refer to Section 16.6.4, "EEPROM Timing," on page 264 for additional details.

APPLICATION NOTE: If EEPROM-less mode is used, out-of-box wake is not supported. PME can only support wakes with no EEPROM/OTP if the desired device's wakes mentioned below are configured by system software over USB before entering PME mode.

The following wake events are supported:

- Wakeup Pin(s)
  The GPIO pins not reserved for PME handling have the capability to wake up the device when operating in PME mode. In order for a GPIO to generate a wake event, it's enable bit must be set in the GPIO[7:0] Wakeup Enables and GPIO[11:8] Wakeup Enables fields of the EEPROM (or OTP). The polarity may also be set with GPIO[7:0] Wakeup Polarity and GPIO[11:8] Wakeup Polarity.
- Magic Packet
  Reception of a Magic Packet when in PME mode will result in a PME being asserted.
- WUFF
  Reception of a packet matching the WUFF when in PME mode will result in a PME being asserted.
- Perfect DA match of Physical address
  Reception of an Ethernet frame whose Destination address matches the device's MAC address will result in a PME being asserted.
- Broadcast Packet
  Reception of a Broadcast Packet when in PME mode will result in a PME being asserted.
- PHY Link Change
  Detection of a PHY link partner when in PME mode will result in a PME being asserted.

In order to facilitate PME mode of operation, the GPIO PME Enable bit in the GPIO PME Flags 0 field must be set and all remaining GPIO PME Flags 0 and GPIO PME Flags 1 bits must be appropriately configured for pulse or level signaling, buffer type, and GPIO PME WoL selection.

The **PME_MODE** pin must be driven to the value that determines whether or not the device remains in PME mode of operation (1) or resumes normal operation (0) when the PME is recognized and cleared by the EC via **PME_CLEAR** (**RESET_N**) assertion.

When in PME mode, **RESET_N** (**PME_CLEAR**) or POR will always cause the contents of the EEPROM to be reloaded.

Figure 14-2 flowcharts PME operation while Magic Packet is enabled with a configured EEPROM/OTP in place. The following conditions hold for OTP/EEPROM Configuration:

- GPIO PME Enable = 1 (enabled)
- GPIO PME Configuration = 0 (PME signaled via level)
- GPIO PME Length = 0 (NA)
- GPIO PME Polarity = 1 (high level signals event)
- GPIO PME Buffer Type = 1 (Push-Pull)
- PME Packet Enable = 1
- PME Perfect DA Enable = 0
- PME WUFF Enable = 0
- Power Method (CFG0_PWR_SEL) = 1 (self powered)
- MAC address for Magic Packet

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Note: If utilizing PME mode the system software must appropriately configure the Flag Attributes Register (FLAG_ATTR).

A POR occurring when **PME_MODE** = 1 and GPIO PME Enable is set in EEPROM/OTP, results in the device entering PME Mode.

In this mode the Ethernet interface operates at the negotiated speed.

Optionally, the Enhanced PHY feature of the Gigabit Ethernet PHY may be enabled during PME operation to further save power. This is controlled by following Configuration Flags 0 fields:

- Enhanced PHY Sleep Timer (PHY_SLEEP_TIMER)
- Enhanced PHY Wake Timer (PHY_WAKE_TIMER)
- Link Time Out Control (LINK_TIME_OUT_CTRL)
- Enhanced PHY Enable (ACT_PHY_EN)

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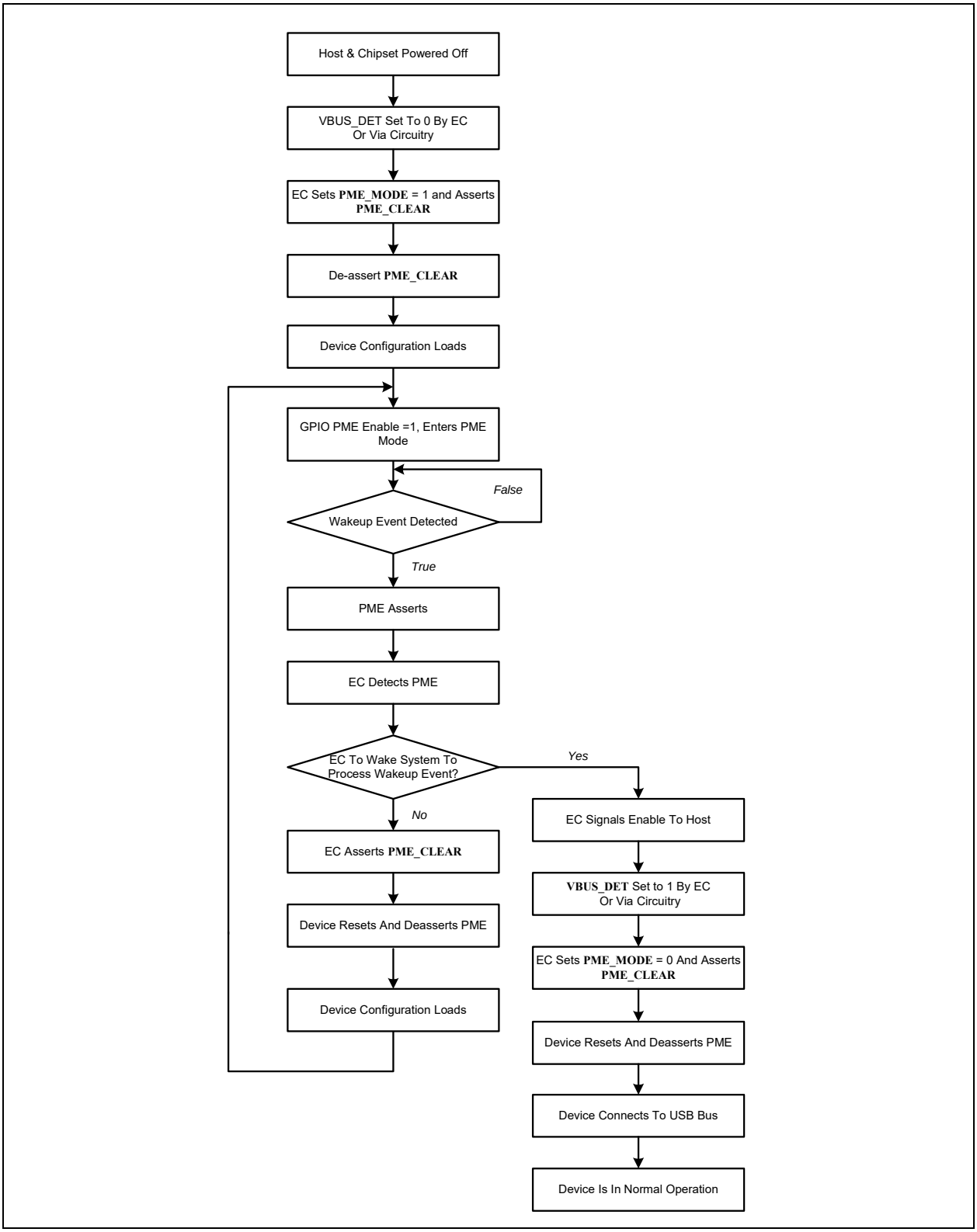
FIGURE 14-2: PME OPERATION



15.0 REGISTER DESCRIPTIONS

This section details the device register descriptions and memory map. The directly addressable memory map is detailed in Table 15-1. Additional indirectly addressable registers are detailed in the following sub-sections.

TABLE 15-1: MEMORY MAP

Address	Data Space
0x0000-0x0FFF	System Control and Status Registers
0x1000-0x11FF	Reserved
0x1200-0x15FF	USB PHY Control and Status Registers
0x1200-0x1FFF	Reserved

Note: For additional information on the device's OTP memory, refer to Section 11.0, "One Time Programmable (OTP) Memory," on page 120.

Directly Addressable Registers

- Section 15.1, "System Control and Status Registers," on page 139
- Section 15.2, "USB PHY Control and Status Registers," on page 214

Indirectly Addressable Registers

- Section 15.3, "Ethernet PHY Control and Status Registers," on page 221
- Section 15.4, "MDIO Manageable Device (MMD) Control and Status Registers," on page 255

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15.1 System Control and Status Registers

Note: Any access to register offsets 0B0h and above will be STALLed in the Unconfigured state, hence unavailable. As a result of this all MAC, FIFO Controller (FCT), and Receive Filtering Engine (RFE) registers will not be available in the Unconfigured state.

Note: RESERVED address space in the System Control and Status Registers Map must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

TABLE 15-2: SYSTEM CONTROL AND STATUS REGISTERS MAP

OFFSET	REGISTER NAME
000h	Device ID and Revision Register (ID_REV)
004h – 008h	Reserved
00Ch	Interrupt Status Register (INT_STS)
010h	Hardware Configuration Register (HW_CFG)
014h	Power Management Control Register (PMT_CTL)
018h	General Purpose IO Configuration 0 Register (GPIO_CFG0)
01Ch	General Purpose IO Configuration 1 Register (GPIO_CFG1)
020h	General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE)
024h	Data Port Select Register (DP_SEL)
028h	Data Port Command Register (DP_CMD)
02Ch	Data Port Address Register (DP_ADDR)
030h	Data Port Data Register (DP_DATA)
034h – 03Ch	Reserved
040h	EEPROM Command Register (E2P_CMD)
044h	EEPROM Data Register (E2P_DATA)
048h – 04Fh	Reserved
050h	BOS Descriptor Attributes Register (BOS_ATTR)
054h	Reserved
058h	HS Descriptor Attributes Register (HS_ATTR)
05Ch	FS Descriptor Attributes Register (FS_ATTR)
060h	String Attributes Register 0 (STRNG_ATTR0)
064h	String Attributes Register 1 (STRNG_ATTR1)
068h	Flag Attributes Register (FLAG_ATTR)
06Ch – 077h	Software General Purpose Register x (SW_GPx)
078h – 07Fh	Reserved
080h	USB Configuration Register 0 (USB_CFG0)
084h	USB Configuration Register 1 (USB_CFG1)
088h	USB Configuration Register 2 (USB_CFG2)
090h	Burst Cap Register (BURST_CAP)
094h	Bulk-In Delay Register (BULK_IN_DLY)
098h	Interrupt Endpoint Control Register (INT_EP_CTL)
09Ch	PIPE Control Register (PIPE_CTL)
0A0h – 0A4h	Reserved
0A8h	USB Status Register (USB_STATUS)
0ACh	Reserved
0B0h	Receive Filtering Engine Control Register (RFE_CTL)

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TABLE 15-2: SYSTEM CONTROL AND STATUS REGISTERS MAP (CONTINUED)

OFFSET	REGISTER NAME
0B4h	VLAN Type Register (VLAN_TYPE)
0B8h – 0BFh	Reserved
0C0h	FIFO Controller RX FIFO Control Register (FCT_RX_CTL)
0C4h	FIFO Controller TX FIFO Control Register (FCT_TX_CTL)
0C8h	FCT RX FIFO End Register (FCT_RX_FIFO_END)
0CCh	FCT TX FIFO End Register (FCT_TX_FIFO_END)
0D0h	FCT Flow Control Threshold Register (FCT_FLOW)
0D4h	RX Datapath Storage (RX_DP_STOR)
0D8h	TX Datapath Storage (TX_DP_STOR)
0DCh – 0FFh	Reserved
100h	MAC Control Register (MAC_CR)
104h	MAC Receive Register (MAC_RX)
108h	MAC Transmit Register (MAC_TX)
10Ch	Flow Control Register (FLOW)
110h	Random Number Seed Value Register (RAND_SEED)
114h	Error Status Register (ERR_STS)
118h	MAC Receive Address High Register (RX_ADDRH)
11Ch	MAC Receive Address Low Register (RX_ADDRL)
120h	MII Access Register (MII_ACCESS)
124h	MII Data Register (MII_DATA)
128h - 12Fh	Reserved
130h	EEE TX LPI Request Delay Count Register (EEE_TX_LPI_REQUEST_DELAY_CNT)
134h	EEE Time Wait TX System Register (EEE_TW_TX_SYS)
138h	EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY)
13Ch - 13Fh	Reserved
140h	Wakeup Control and Status Register 1 (WUCSR1)
144h	Wakeup Source Register (WK_SRC)
148h – 14Fh	Reserved
150h - 1CC	Wakeup Filter x Configuration Register (WUF_CFGx)
1D0h – 1Fh	Reserved
200h – 3FCh	Wakeup Filter x Byte Mask Registers (WUF_MASKx)
400h – 504h	MAC Address Perfect Filter Registers (ADDR_FILTx)
508h – 5FFh	Reserved
600h	Wakeup Control and Status Register 2 (WUCSR2)
610h – 61Ch	NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST)
620h – 62Ch	NSx IPv6 Source Address Register (NSx_IPV6_ADDR_SRC)
630h – 63Ch	NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0)
640h – 64Ch	NSx ICMPv6 Address 1 Register (NSx_ICMPV6_ADDR1)
650h – 65Ch	NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST)
660h – 66Ch	NSx IPv6 Source Address Register (NSx_IPV6_ADDR_SRC)
670h – 67Ch	NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0)
680h – 68Ch	NSx ICMPv6 Address 1 Register (NSx_ICMPV6_ADDR1)
690h	SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC)
694h	SYN IPv4 Destination Address Register (SYN_IPV4_ADDR_DEST)
698h	SYN IPv4 TCP Ports Register (SYN_IPV4_TCP_PORTS)
69Ch – 6A8h	SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC)
6ACh – 6B8h	SYN IPv6 Destination Address Register (SYN_IPV6_ADDR_DEST)
6BCh	SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS)

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TABLE 15-2: SYSTEM CONTROL AND STATUS REGISTERS MAP (CONTINUED)

OFFSET	REGISTER NAME
6C0h	ARP Sender Protocol Address Register (ARP_SPA)
6C4h	ARP Target Protocol Address Register (ARP_TPA)
6C8h – 6FFh	Reserved
700h	PHY Device Identifier (PHY_DEV_ID)
704h – FFFh	Reserved

15.1.1 DEVICE ID AND REVISION REGISTER (ID_REV)

Offset: 000h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Chip ID** This read-only field identifies the device model.	RO	7850h
15:0	**Chip Revision** This is the revision of the device.	RO	Note 15-1

Note 15-1 Default value is dependent on device revision.

15.1.2 INTERRUPT STATUS REGISTER (INT_STS)

.

Offset: 00Ch Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:29	**RESERVED**	RO	-
28	**OTP Write Done Interrupt (OTP_WR_DONE_INT)** OTP write operation has completed. **Note:** The source of this interrupt is a level. The interrupt persists until it is cleared in the OTP.	R/WC	0b
27	**RESERVED**	RO	-
26	**Energy Efficient Ethernet Start TX Low Power Interrupt (EEE_START_TX_LPI_INT)** This interrupt is asserted when the transmitter enters low power idle mode, due to the expiration of the time specified in EEE TX LPI Request Delay Count Register (EEE_TX_LPI_REQUEST_DELAY_CNT) This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low. **Note:** The source of this interrupt is a pulse.	R/WC	0b
25	**Energy Efficient Ethernet Stop TX Low Power Interrupt (EEE_STOP_TX_LPI_INT)** This interrupt is asserted when the transmitter exits low power idle mode, due to the expiration of the time specified in the EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY). This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low. **Note:** The source of this interrupt is a pulse.	R/WC	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
24	**Energy Efficient Ethernet RX Low Power Interrupt (EEE_RX_LPI_INT)** This interrupt is asserted when the receiver enters low power idle mode. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low. **Note:** The source of this interrupt is a pulse.	R/WC	0b
23	**MAC Reset Time Out (MACRTO_INT)** This interrupt signifies that the 8 ms reset watchdog timer has timed out. This means that the Ethernet PHY is not supplying RX and TX clocking to the MAC. After the timer times out, the MAC reset is deasserted asynchronously. **Note:** The source of this interrupt is a pulse.	R/WC	0b
22	**RX Data FIFO Overflow Interrupt (RDFO_INT)** This interrupt is set when the receive logic attempts to place data into the RX Data FIFO after it has been completely filled. When set, newly received data is discarded. **Note:** The source of this interrupt is a level.	R/WC	0b
21	**Transmitter Error Interrupt (TXE_INT)** This interrupt indicates that the transmitter has encountered an error. Refer to Section Section 6.2.4, "TX Error Detection", for a description of the conditions that will cause a TXE. **Note:** The source of this interrupt is a level.	R/WC	0b
20	**USB Status Interrupt (USB_STS_INT)** This interrupt is issued after a USB status event. This interrupt persists until the asserted event(s) is cleared in USB Status Register (USB_STATUS). **Note:** The source of this interrupt is a level.	R/WC	0b
19	**TX Disabled Interrupt (TX_DIS_INT)** This interrupt is issued after the TX FIFO or MAC transmitter has been successfully disabled. This interrupt persists when either the FCT TX Disabled bit of the FIFO Controller TX FIFO Control Register (FCT_TX_CTL) or the Transmitter Disabled (TXD) bit of the MAC Transmit Register (MAC_TX) is set. **Note:** The source of this interrupt is a level.	R/WC	0b
18	**RX Disabled Interrupt (RX_DIS_INT)** This interrupt is issued after the RX FIFO or MAC receiver has been successfully disabled. This interrupt persists when either the FCT RX Disabled bit of the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) or the Receiver Disabled (RXD) bit of the MAC Receiver Register (MAC_RX) is set. **Note:** The source of this interrupt is a level.	R/WC	0b
17	**PHY Interrupt (PHY_INT)** Indicates an Ethernet PHY Interrupt event. **Note:** The source of this interrupt is a level. The interrupt persists until it is cleared in the PHY.	R/WC	0b
16	**Data Port Interrupt (DP_INT)** Indicates that a pending data port operation has been completed. **Note:** The source of this interrupt is a pulse.	R/WC	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
15	**MAC Error Interrupt (MAC_ERR_INT)** This interrupt is set whenever any error condition tracked in the MAC's Error Status Register (ERR_STS) occurs. The application program can determine the specific error(s) that occurred by examining the Error Status Register (ERR_STS). **Note:** This is a level-triggered interrupt event that remains asserted until all the error event bits in the Error Status Register (ERR_STS) are cleared.	R/WC	0b
14:13	**RESERVED**	RO	-
12	**UTX Frame Pending (UTX_FP)** Indicates the USB TX FIFO has at least one frame pending.	RO	0b
11:0	**GPIO [11:0] (GPIOx_INT)** Interrupts are generated from the GPIOs. **Note:** The sources for these interrupts are a level.	R/WC	Note 15-2

Note 15-2 The default depends on the state of the GPIO pin. The clearing of a GPIOx_INT bit also clears the corresponding GPIO wake event

15.1.3 HARDWARE CONFIGURATION REGISTER (HW_CFG)

Offset: 010h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23	**LED3 Enable (LED3_EN)** When set, the **LED3** pin function is enabled. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-6
22	**LED2 Enable (LED2_EN)** When set, the **LED2** pin function is enabled. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-6
21	**LED1 Enable (LED1_EN)** When set, the **LED1** pin function is enabled. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-6
20	**LED0 Enable (LED0_EN)** When set, the **LED0** pin function is enabled. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-6
19:16	**RESERVED**	RO	-
15	**NetDetach Status (NETDET_STS)** After the driver loads, this bit is checked to determine whether a NetDetach event occurred.	R/WC	Note 15-7

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BITS	DESCRIPTION	TYPE	DEFAULT
14	**NetDetach Enable (NETDET_EN)** When this bit is set, the device detaches from the USB bus. This results in the driver unloading and no further communication with the device. The device remains detached until PHY link is detected, or a properly configured GPIO pin is asserted. Occurrence of either event causes the device to attach to the USB bus, the driver to be loaded, and the NETDET_STS bit to be asserted. **Note:** The $\overline{\text{CONNECT}}$ pin may be enabled to assert in support of this function.	SC	0b
13	**EEPROM Emulation Enable (EEM)** This bit is used to select the source of descriptor information and configuration flags when no EEPROM is present. 0 = HW generates descriptor based upon CSR defaults. 1 = Use Descriptor RAM and Attributes Registers. **Note:** This bit affects operation only when an EEPROM is not present and OTP is not configured. This bit has no effect when an EEPROM is present or OTP is configured. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	0b
12	**Reset Protection (RST_PROTECT)** Setting this bit protects select fields of certain registers from being affected by resets other than POR. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	0b
11	**RESERVED**	RO	-
10	**CONNECT Pin Buffer Type (CONNECT_BUF)** This bit selects the output buffer type for $\overline{\text{CONNECT}}$. 0 = Open drain driver 1 = Push-Pull driver **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-3
9	**Connect Pin Enable (CONNECT_EN)** This bit enables the $\overline{\text{CONNECT}}$ pin. When enabled the pin asserts when the device is attempting to attach to the USB bus. **Note:** The $\overline{\text{CONNECT}}$ pin is also functional for NetDetach. **Note:** This bit only has meaning when configured for HSIC operation. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-4
8	**Connect Pin Polarity (CONNECT _POL)** This bit selects the polarity of the $\overline{\text{CONNECT}}$ pin. 0 = Active low 1 = Active high **Note:** This bit only has meaning when configured for HSIC operation. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-5

BITS	DESCRIPTION	TYPE	DEFAULT
7:6	**SUSPEND_N Pin Select (SUSPEND_N_SEL)** This bit specifies the modes of operation during which the SUSPEND_N pin will be asserted. 00b: SUSPEND_N asserted in SUSPEND2. 01b: SUSPEND_N asserted in SUSPEND2, SUSPEND1 and NetDetach. 10b: SUSPEND_N asserted in SUSPEND2, SUSPEND1, SUSPEND0 and NetDetach. 11b: SUSPEND_N asserted in SUSPEND3, SUSPEND2, SUSPEND1, SUSPEND0 and NetDetach. **Note:** This field is protected by Reset Protection (RST_PROTECT). **Note:** The usage of this bit is not gated by the EEPROM Emulation Enable (EEM) bit or the lack of an EEPROM.	R/W	Note 15-8
5	**SUSPEND_N Pin Polarity (SUSPEND_N _POL)** This bit selects the polarity of the SUSPEND_N pin. 0 = Active low. 1 = Active high **Note:** This field is protected by Reset Protection (RST_PROTECT). **Note:** The usage of this bit is not gated by the EEPROM Emulation Enable (EEM) bit or the lack of an EEPROM.	R/W	Note 15-9
4	**Multiple Ethernet Frames per USB Packet (MEF)** This bit enables the USB transmit direction to pack multiple Ethernet frames per USB packet whenever possible. 0 = Support no more than one Ethernet frame per USB packet 1 = Support packing multiple Ethernet frames per USB packet	R/W	0b
3	**EEPROM Time-out Control (ETC)** This bit controls the length of time used by the EEPOM controller to detect a time-out. 0 = Time-out occurs if no response received from EEPROM after 30 ms. 1 = Time-out occurs if no response received from EEPROM after 1.28 us. **Note:** When a timeout occurs it is indicated via EPC Time-out (EPC_TO) in EEPROM Command Register (E2P_CMD).	R/W	0b
2	**RESERVED**	RO	-
1	**Soft Lite Reset (LRST)** Writing 1 generates the lite software reset of the device. A lite reset will not affect the USB controller and will not cause the USB PHY to disconnect. Additionally, the contents of the EEPROM will not be reloaded. This bit clears after the reset sequence has completed.	SC	0b
0	**Soft Reset (SRST)** Writing 1 generates a software initiated reset of the device. A software reset will result in the contents of the EEPROM being reloaded. While the reset sequence is in progress, the USB PHY will be disconnected. After the device has been re-initialized, it will take the PHY out of the disconnect state and be visible to the Host.	SC	0b

Note 15-3 The default value of this bit is determined by the value of the respective GPIO CONNECT Buffer Type field of GPIO PME Flags 1 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed than 0b is the

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default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

Note 15-4 The default value of this bit is determined by the value of the respective GPIO CONNECT Enable field of GPIO PME Flags 0 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

Note 15-5 The default value of this bit is determined by the value of the respective GPIO CONNECT Polarity field of GPIO PME Flags 0 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

Note 15-6 The default value of this bit is determined by the value of the respective LED_EN field of LED Configuration 0 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

Note 15-7 The default value of this bit depends on whether a NetDetach event occurred. If set, the event occurred.

Note 15-8 The default value of this bit is determined by the value of the SUSPEND_N Select (CFG0_SUSPEND_N_SEL) bit of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 00b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 00b if neither is available.

Note 15-9 The default value of this field is determined by the value of the **SUSPEND_N** Polarity (CFG0_**SUSPEND_N**_POL) bit of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Light Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

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15.1.4 POWER MANAGEMENT CONTROL REGISTER (PMT_CTL)

Offset: 014h Size: 32 bits

This register controls the power management features.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15	**Disable Wait Analog Voltage Reference Stable (DIS_WAIT_ANA_REF)** This bit disables waiting for the analog voltage reference to stabilize when the Ethernet PHY is placed in reset to maximize power savings. When this bit is set the analog reference is not disabled when the PHY is reset. When the reference is disabled a delay in the order of 100 ms is required for the PHY to stabilize. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	0b
14	**Crystal Suspend Disable (XTAL_SUSP_DIS)** 0 - Normal Crystal driver operation 1 - Crystal is never suspended **Note:** When asserted, this bit prevents the crystal oscillator from being disabled in SUSPEND2 and UNPOWERED modes. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-10
13	**EEE WAKE-UP Enable (EEE_WAKEUP_EN)** Enables EEE WAKE-UP Status (EEE_WUPS) as a wakeup event. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b
12	**EEE WAKE-UP Status (EEE_WUPS)** This field indicates if the cause of the current wake-up event is due to EEE. It is used along with WAKE-UP Status (WUPS). See the WUPS field for the encoding. This bit will set regardless of the value in EEE WAKE-UP Enable (EEE_WAKEUP_EN). If the Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) bit is set, this bit will clear upon completion of a resume. See the RES_CLR_WKP_STS bit for further details. **Note:** It is not valid to simultaneously clear the EEE_WUPS bit and change the contents of the Suspend Mode (SUSPEND_MODE) field.	R/WC	0b
11	**MAC Soft Reset (MAC_SRST)** The MAC RX/TX clock domains will be held in reset when this bit is high. This bit must then be cleared to resume normal operation. MAC RX/TX resets will be deasserted only if RX/TX clocks are running.	R/W	0b
10	**RESERVED**	RO	-

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BITS	DESCRIPTION	TYPE	DEFAULT
9	**Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS)** When set, the following status signals in WUCSR1 and WUCSR2 will clear upon the completion of a resume sequence: WUCSR1: RFE Wakeup Frame Received (RFE_WAKE_FR) Perfect DA Frame Received (PFDA_FR) Remote Wakeup Frame Received (WUFR) Magic Packet Received (MPR) Broadcast Frame Received (BCAST_FR) Energy Efficient Ethernet TX Wake (EEE_TX_WAKE) Energy Efficient Ethernet RX Wake (EEE_RX_WAKE) WUCSR2: IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD) IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD) When set, this bit also affects the WUPS field. WUPS[1] and EEE_WUPS will clear upon completion of a resume event. Only resume sequences initiated by the above listed wake events wakeup frame or magic packet are affected by RES_CLR_WKP_STS. Resumes initiated by the host do not clear the wakeup statuses. When cleared, the wakeup status signals are not cleared after a resume.	R/W	0b
8	**Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN)** When asserted, all wakeup enable bits in WUCSR and WUCSR2 are cleared after a resume sequence, initiated from a remote wakeup, completes. Resumes initiated by the host do not clear the wakeup enables.	R/W	1b
7	**Device Ready (READY)** The READY bit is used to indicate when the device is ready for normal operation. The READY bit remains deasserted for the following reasons: • Waiting for the Gigabit Ethernet PHY reset sequence to complete and the PHY to become operational. This could take over 125 ms depending on how the device is configured. • Waiting for content to be loaded from the EEPROM or OTP. This would only be visible to the application for the case of a USB Reset where the Ethernet MAC address is reloaded. See Table 15-3, "Device Ready Bit Behavior" for further details.	RO	0b
6:5	**Suspend Mode (SUSPEND_MODE)** Indicates which suspend power state to use after the Host suspends the device. If the device is unconfigured, it transitions to the NORMAL Unconfigured state and this register will reset to the value 10b. SUSPEND_MODE encoding: 00 = SUSPEND0 01 = SUSPEND1 10 = SUSPEND2 11 = SUSPEND3 **Note:** It is not valid to select any suspend variant besides SUSPEND2 when in the NORMAL Unconfigured state. **Note:** SUSPEND0 and SUSPEND1 are functionally identical in this device. They are maintained as separate selectable states for nomenclature compatibility with legacy devices.	R/W	10b

BITS	DESCRIPTION	TYPE	DEFAULT
4	**PHY Reset (PHY_RST)** Writing a '1' to this bit resets the Ethernet PHY. The internal logic automatically holds the PHY reset for a minimum of 4 ms. When the PHY is released from reset, this bit is automatically cleared. All writes to this bit are ignored while this bit is high. The Device Ready (READY) bit shall clear upon setting this bit. When the PHY is operational Device Ready (READY) bit shall assert. **Note:** This reset may be extended to 128 ms depending on the state of Disable Wait Analog Voltage Reference Stable (DIS_WAIT_ANA_REF). **Note:** This bit should be set after resuming from SUSPEND2.	SC	0b
3	**Wake-On-LAN Enable (WOL_EN)** Enables WOL as a wakeup event which includes the following. See Section 13.4.1, "Detecting Wakeup Events" for details on which wake events are affected by this bit. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b
2	**PHY Interrupt Enable (PHY_WAKE_EN)** Ethernet PHY Interrupt as a wakeup event. See Section 13.4.1, "Detecting Wakeup Events" for further details. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b

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<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>1:0</td><td>
WAKE-UP Status (WUPS)
This field, along with EEE WAKE-UP Status (EEE_WUPS), indicates the cause of the current wake-up event. WUPS bits are cleared by writing a ‘1’ to the appropriate bit. The encoding of these bits is as follows:
<table>
<tr><th>EEE_WUPS</th><th>WUPS[1:0]</th><th>EVENT</th></tr>
<tr><td>0</td><td>00</td><td>No wake-up event detected</td></tr>
<tr><td>X</td><td>X1</td><td>• Ethernet PHY Wake Event</td></tr>
<tr><td>X</td><td>1X</td><td>• Wake-On-LAN
• TCP SYN
• “Good Frame”
• Broadcast Frame
• Multicast Frame
• Perfect DA Match</td></tr>
<tr><td>1</td><td>XX</td><td>EEE Receive Wake (EEE_RX_WAKE)) (SUSPEND0 & SUSPEND3) / EEE Transmit Wake (EEE_TX_WAKE) (SUSPEND3)</td></tr>
</table>
More than one bit may be set indicating that multiple events occurred.

The WUPS field will not be set unless the corresponding event is enabled prior to entering the reduced power state.

These bits will set regardless of the values in Wake-On-LAN Enable (WOL_EN) and PHY Interrupt Enable (PHY_WAKE_EN).

If Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set, WUPS[1] will clear upon completion of a resume. See the RES_CLR_WKP_STS bit for further details.

Note: It is not valid to simultaneously clear the WUPS bits and change the contents of the Suspend Mode (SUSPEND_MODE) field.
</td><td>R/WC</td><td>00b</td></tr>
</table>

Note 15-10 The default value of this bit is determined by the Crystal Suspend Disable (XTAL_SUSP_DIS) bit of Configuration Flags 1 contained within the EEPROM, if present. If no EEPROM is present the default depends on the OTP programmed value. It the OTP is not programmed than 1b is the default. A USB Reset or Lite Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 1b if neither is available.

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TABLE 15-3: DEVICE READY BIT BEHAVIOR

Event	Internal PHY	External PHY
Transition into NORMAL-Unconfigured	Ready bit remains cleared since Ethernet PHY is reset to minimize power consumption.	Ready bit is set after EEPROM/ OTP loading is completed. EEPROM emulation does not introduce a comparable delay. This should only be visible to the application after a USB Reset in which and EEPROM/OTP load is required to retrieve the MAC address.
Transition from NORMAL-Unconfigured -> NORMAL-Configured	Ready bit asserts after Ethernet PHY reset is deasserted and PHY becomes operational.	Ready bit is set. There is no state change in READY bit since it is set in the NORMAL-Unconfigured state.
Transition from SUSPEND2 -> NORMAL-Configured	Ethernet PHY is held in reset while SUSPEND2 to save power. After PHY reset is deasserted after moving to the Normal-Configured the READY bit asserts.	The External Ethernet PHY is not reset from moving to SUSPEND2. Ready bit does not clear when entering SUSPEND2.
PHY Reset (PHY_RST)	Ready bit remains cleared until PHY reset deasserts.	Ready bit remains cleared until PHY reset deasserts.

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15.1.5 GENERAL PURPOSE IO CONFIGURATION 0 REGISTER (GPIO_CFG0)

Address: 018h Size: 32 bits

This register configures the external **GPIO[3:0]** pins.

In order for a GPIO to function as a wake event or interrupt source, it must be configured as an input. GPIO pins used to generate wake events must also be enabled by General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE).

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:12	**GPIO Enable (GPIOEN)** When clear, the pin functions as a GPIO. GPIOEN0 – bit 12 GPIOEN1 – bit 13 GPIOEN2 – bit 14 GPIOEN3 – bit 15 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-11
11:8	**GPIO Buffer Type (GPIOBUF)** When set, the output buffer for the corresponding GPIO signal is configured as a push/pull driver. When cleared, the corresponding GPIO signal is configured as an open-drain driver. Bits are assigned as follows: GPIOBUF0 – bit 8 GPIOBUF1 – bit 9 GPIOBUF2 – bit 10 GPIOBUF3 – bit 11 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-12
7:4	**GPIO Direction (GPIODIR)** When set, enables the corresponding GPIO as an output. When cleared the GPIO is enabled as an input. Bits are assigned as follows: GPIODIR0 – bit 4 GPIODIR1 – bit 5 GPIODIR2 – bit 6 GPIODIR3 – bit 7 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-13
3:0	**GPIO Data (GPIOD)** When enabled as an output, the value written is reflected on GPIOn. When read, GPIOn reflects the current state of the corresponding GPIO pin. Bits are assigned as follows: GPIOD0 – bit 0 GPIOD1 – bit 1 GPIOD2 – bit 2 GPIOD3 – bit 3 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-14

Note 15-11 The default value of this field is determined by the value of the GPIO 0-11 Enable contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0xF is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0xF if neither is present.

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Note 15-12 The default value of this field is determined by the value of the GPIO 0-11 Buffer contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0x0 is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0x0 if neither is present.

Note 15-13 The default value of this field is determined by the value of the GPIO 0-11 Direction contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0x0 is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0x0 if neither is present.

Note 15-14 The default value of this field is determined by the value of the GPIO 0-11 Data contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0x0 is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0x0 if neither is present. In the event that the GPIO is configured as an input the default state is unknown.

15.1.6 GENERAL PURPOSE IO CONFIGURATION 1 REGISTER (GPIO_CFG1)

Address: 01Ch Size: 32 bits

This register configures the external **GPIO[4:11]** pins.

In order for a GPIO to function as a wake event or interrupt source, it must be configured as an input. GPIOs used as wake events must also be enabled by General Purpose IO Wake Enable and Polarity Register (GPIO_WAKE).

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**GPIO Enable (GPIOEN)** When clear, the pin functions as a GPIO. GPIOEN4 - bit 24 GPIOEN5 - bit 25 GPIOEN6 - bit 26 GPIOEN7 - bit 27 GPIOEN8 - bit 28 GPIOEN9 - bit 29 GPIOEN10 - bit 30 GPIOEN11 - bit 31 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-15
23:16	**GPIO Buffer Type (GPIOBUF)** When set, the output buffer for the corresponding GPIO signal is configured as a push/pull driver. When cleared, the corresponding GPIO signal is configured as an open-drain driver. GPIOBUF4 - bit 16 GPIOBUF5 - bit 17 GPIOBUF6 - bit 18 GPIOBUF7 - bit 19 GPIOBUF8 - bit 20 GPIOBUF9 - bit 21 GPIOBUF10 - bit 22 GPIOBUF11 - bit 23 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-12

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BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**GPIO Direction (GPIODIR)** When set, enables the corresponding GPIO as output. When cleared, the GPIO is enabled as an input. GPIODIR4 - bit 8 GPIODIR5 - bit 9 GPIODIR6 - bit 10 GPIODIR7 - bit 11 GPIODIR8 - bit 12 GPIODIR9 - bit 13 GPIODIR10 - bit 14 GPIODIR11 - bit 15 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-13
7:0	**GPIO Data (GPIOD)** When enabled as an output, the value written is reflected on GPIOn. When read, GPIOn reflects the current state of the corresponding GPIO pin. GPIOD4 - bit 0 GPIOD5 - bit 1 GPIOD6 - bit 2 GPIOD7 - bit 3 GPIOD8 - bit 4 GPIOD9 - bit 5 GPIOD10 - bit 6 GPIOD11 - bit 7 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-14

Note 15-15 The default value of this field is determined by the value of the GPIO 0-11 Enable contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0xFF is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0xFF if neither is present.

15.1.7 GENERAL PURPOSE IO WAKE ENABLE AND POLARITY REGISTER (GPIO_WAKE)

Address: 020h Size: 32 bits

This register enables the GPIOs to function as wake events for the device when asserted. It also allows the polarity used for a wake event/interrupt to be configured.

Note: GPIOs must not cause a wake event to the device when not configured as a GPIO.

BITS	DESCRIPTION	TYPE	DEFAULT
31:28	**RESERVED**	RO	-
27:16	**GPIO Polarity 0-11 (GPIOPOL[11:0])** 0 = Wakeup/interrupt is triggered when GPIO is driven low 1 = Wakeup/interrupt is triggered when GPIO is driven high GPIOPOL0 - bit 16 GPIOPOL1 - bit 17 GPIOPOL2 - bit 18 GPIOPOL3 - bit 19 GPIOPOL4 - bit 20 GPIOPOL5 - bit 21 GPIOPOL6 - bit 22 GPIOPOL7 - bit 23 GPIOPOL8 - bit 24 GPIOPOL9 - bit 25 GPIOPOL10 - bit 26 GPIOPOL11 - bit 27 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-16
15:12	**RESERVED**	RO	-
11:0	**GPIO Wake 0-11 (GPIOWK[11:0])** 0 = The GPIO can not wake up the device. 1 = The GPIO can trigger a wake up event. GPIOWK0 - bit 0 GPIOWK1 - bit 1 GPIOWK2 - bit 2 GPIOWK3 - bit 3 GPIOWK4 - bit 4 GPIOWK5 - bit 5 GPIOWK6 - bit 6 GPIOWK7 - bit 7 GPIOWK8 - bit 8 GPIOWK9 - bit 9 GPIOWK10 - bit 10 GPIOWK11 - bit 11 **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-16

Note 15-16 The default value of this field is loaded from the associated bytes of the EEPROM. The high order, unused bits, of the EEPROM are ignored. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed than 0h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0h if neither is available.

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15.1.8 DATA PORT SELECT REGISTER (DP_SEL)

Offset: 024h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Data Port Ready (DPRDY)** The Data Port Ready bit indicates when the data port RAM access has completed. In the case of a read operation, this bit indicates when the read data has been stored in the DP_DATA register 1 = Data Port is ready. 0 = Data Port is busy processing a transaction.	RO	1b
30:4	**RESERVED**	RO	-
3:0	**Select (SEL)** Selects which RAM to access. 0000 = URX Buffer RAM (Do not access at run time) 0001 = RFE VLAN and DA Hash Table (VHF RAM) 0010 = LSO Header RAM (Do not access at run time) 0011 = FCT RX RAM (Do not access at run time) 0100 = FCT TX RAM (Do not access at run time) 0101 = Descriptor RAM (Do not access at run time) 0110 = RESERVED 0111 = UTX Buffer RAM (Do not access at run time) 1000 = RESERVED 1001 = RESERVED 1010 = RESERVED 1011 = RESERVED 1100 = RESERVED 1101 = RESERVED 1110 = RESERVED 1111 = RESERVED	R/W	0000b

15.1.9 DATA PORT COMMAND REGISTER (DP_CMD)

Offset: 028h Size: 32 bits

This register commences the data port access. Writing a one to this register will enable a write access, while writing a zero will do a read access.

The address and data registers need to be configured appropriately for the desired read or write operation before accessing this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Data Port Write**. Selects operation. Writing to this bit initiates the dataport access. 1 = Write operation 0 = Read operation	R/W	0b

15.1.10 DATA PORT ADDRESS REGISTER (DP_ADDR)

Offset: 02Ch Size: 32 bits

Indicates the address to be used for the data port access.

BITS	DESCRIPTION	TYPE	DEFAULT
31:14	**RESERVED**	RO	-
13:0	**Data Port Address[13:0]**	R/W	0000h

15.1.11 DATA PORT DATA REGISTER (DP_DATA)

Offset: 030h Size: 32 bits

The Data Port Data register holds the write data for a write access and the resultant read data for a read access.

Before reading this register for the result of a read operation, the Data Port Ready bit should be checked. The Data Port Ready bit must indicate the data port is ready. Otherwise the read operation is still in progress.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Data Port Data (DATA_PORT_DATA)**	R/W	0000_0000h

15.1.12 EEPROM COMMAND REGISTER (E2P_CMD)

Offset: 040h Size: 32 bits

This register is used to control the read and write operations on the Serial EEPROM.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**EPC Busy (EPC_BSY)** When a “1” is written into this bit, the operation specified in the EPC Command field is performed at the specified EEPROM address. This bit will remain set until the operation is at which time it will clear. In the case of a read, this means that the Host can read valid data from the EEPROM Data Register (E2P_DATA). The E2P_CMD and E2P_DATA registers should not be modified until this bit is cleared. In the case where a write is attempted and an EEPROM is not present, the EPC Busy remains busy until the EPC Time-out occurs. At that time, the busy bit is cleared.	SC	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
30:28	**EPC Command (EPC_CMD)** This field is used to issue commands to the EEPROM Controller. The EPC will execute commands when the EPC Busy bit is set. A new command must not be issued until the previous command completes. This field is encoded as follows: 000 = READ 001 = EWDS 010 = EWEN 011 = WRITE 100 = WRAL 101 = ERASE 110 = ERAL 111 = RELOAD **READ (Read Location):** This command will cause a read of the EEPROM location pointed to by EPC Address (EPC_ADDR). The result of the read is available in the E2P_DATA register. **EWDS (Erase/Write Disable):** After issued, the EEPROM will ignore erase and write commands. To re-enable erase/write operations, issue the EWEN command. **EWEN (Erase/Write Enable):** Enables the EEPROM for erase and write operations. The EEPROM will allow erase and write operations until the Erase/Write Disable command is sent, or until power is cycled. **Note:** The EEPROM device will power-up in the erase/write-disabled state. Any erase or write operations will fail until an Erase/Write Enable command is issued. **WRITE (Write Location):** If erase/write operations are enabled in the EEPROM, this command will cause the contents of the E2P_DATA register to be written to the EEPROM location selected by the EPC Address (EPC_ADDR) field. **WRAL (Write All):** If erase/write operations are enabled in the EEPROM, this command will cause the contents of the E2P_DATA register to be written to every EEPROM memory location. **ERASE (Erase Location):** If erase/write operations are enabled in the EEPROM, this command will erase the location selected by the EPC Address (EPC_ADDR) field. **ERAL (Erase All):** If erase/write operations are enabled in the EEPROM, this command will initiate a bulk erase of the entire EEPROM. **RELOAD (Data Reload):** Instructs the EEPROM Controller to reload the data from the EEPROM. If a value of A5h is not found in the first address of the EEPROM, the EEPROM is assumed to be un-programmed and the Reload operation will fail. The EPC Data Loaded (EPC_DL) bit indicates a successful load of the data. **Note:** A failed reload operation will result in no change to descriptor information or register contents. These items will not be set to default values as a result of the reload failure.	R/W	000b
27:11	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
10	**EPC Time-out (EPC_TO)** If an EEPROM operation is performed, and there is no response from the EEPROM within 30mS, the EEPROM Controller will time-out and return to its idle state. This bit is set when a time-out occurs, indicating that the last operation was unsuccessful. **Note:** If the EEDI pin is pulled-high (default if left unconnected), EPC commands will not time out if the EEPROM device is missing. In this case, the EPC Busy bit will be cleared as soon as the command sequence is complete. It should also be noted that the ERASE, ERAL, WRITE and WRAL commands are the only EPC commands that will time-out if an EEPROM device is not present and the EEDI signal is pulled low.	R/WC	0b
9	**EPC Data Loaded (EPC_DL)** When set, this bit indicates that a valid EEPROM was found, and that the MAC Address and default register programming has completed normally. This bit is set after a successful load of the data after power-up, or after a RELOAD command has completed.	R/WC	0b
8:0	**EPC Address (EPC_ADDR)** The 9-bit value in this field is used by the EEPROM Controller to address a specific memory location in the Serial EEPROM. This is a BYTE aligned address.	R/W	00h

15.1.13 EEPROM DATA REGISTER (E2P_DATA)

Offset: 044h Size: 32 bits

This register is used in conjunction with the E2P_CMD register to perform read and write operations to the Serial EEPROM.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**EEPROM Data (EPC_DATA)** Value read from or written to the EEPROM.	R/W	-

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15.1.14 BOS DESCRIPTOR ATTRIBUTES REGISTER (BOS_ATTR)

Offset: 050h Size: 32 bits

This register sets the length values for BOS Block contents that have been loaded into Descriptor RAM via the Data Port registers. The Descriptor RAM images may be used, in conjunction with this register, to facilitate customized operation when no EEPROM is present and OTP is not configured.

Note:

- If the block does not exist in Descriptor RAM, its size value must be written as 00h.
- This register only affects system operation when an EEPROM is not present, OTP is not configured and the EEPROM Emulation Enable (EEM) bit indicates Descriptor RAM and the Attributes Registers are to be used for descriptor processing.
- Writing to this register when an EEPROM is present or OTP is configured is prohibited and shall result in untoward operation and unexpected results.
- This register is protected by Reset Protection (RST_PROTECT).

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**BOS Block Size (BOS_BLOCK_SIZE)** Note 15-17	R/W	Note 15-18

Note 15-17 If this field is not 0, the block must include Binary Object Store (BOS) Descriptor; and may include USB 2.0 Extension Descriptor, and Container ID Descriptor.

Note 15-18 The default value of this field is determined by the value of the Binary Object Store (BOS) Block Length (Bytes) contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 00h if neither is available.

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15.1.15 HS DESCRIPTOR ATTRIBUTES REGISTER (HS_ATTR)

Address: 058h Size: 32 bits

This register sets the length values for HS descriptors that have been loaded into Descriptor RAM via the Data Port registers. The HS Polling interval is also defined by a field within this register. The Descriptor RAM images may be used, in conjunction with this register, to facilitate customized operation when no EEPROM is present or OTP is not configured.

Note:

- If a descriptor does not exist in Descriptor RAM, its size value must be written as 00h.
- This register only affects system operation when an EEPROM is not present, OTP is not configured, and the EEPROM Emulation Enable (EEM) bit indicates Descriptor RAM and the Attributes Registers are to be used for descriptor processing.
- Writing to this register when an EEPROM is present or OTP is configured is prohibited and will result in untoward operation and unexpected results.
- This register is protected by Reset Protection (RST_PROTECT).

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:16	**HS Polling Interval (HS_POLL_INT)**	R/W	Note 15-19
15:8	**HS Device Descriptor Size (HS_DEV_DESC_SIZE)** Note 15-20	R/W	Note 15-21
7:0	**HS Configuration Descriptor Size (HS_CFG_DESC_SIZE)** Note 15-20	R/W	Note 15-22

Note 15-19 The default value of this field is determined by the value of the High-Speed Polling Interval for Interrupt Endpoint contained within the EEPROM, if present. If no EEPROM is present then the vale programmed in OTP is used. If OTP is not configured then 04h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 04h if neither is present.

Note 15-20 The only legal values are 0 and 12h. Writing any other values will result in untoward behavior and unexpected results.

Note 15-21 The default value of this field is determined by the value of the High-Speed Device Descriptor (bytes) contained within the EEPROM, if present. If no EEPROM is present then the vale programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

Note 15-22 The default value of this field is determined by the value of the High-Speed Configuration and Interface Descriptor Length (bytes) contained within the EEPROM, if present. If no EEPROM is present then the vale programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

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15.1.16 FS DESCRIPTOR ATTRIBUTES REGISTER (FS_ATTR)

Address: 05Ch Size: 32 bits

This register sets the length values for FS descriptors that have been loaded into Descriptor RAM via the Data Port registers. The FS Polling interval is also defined by a field within this register. The Descriptor RAM images may be used, in conjunction with this register, to facilitate customized operation when no EEPROM is present or OTP is not configured.

Note:

- If a descriptor does not exist in Descriptor RAM, its size value must be written as 00h.
- This register only affects system operation when an EEPROM is not present, OTP is not configured, and the EEPROM Emulation Enable (EEM) bit indicates Descriptor RAM and the Attributes Registers are to be used for descriptor processing.
- Writing to this register when an EEPROM is present or OTP is configured is prohibited and will result in untoward operation and unexpected results.
- This register is protected by Reset Protection (RST_PROTECT)

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:16	**FS Polling Interval (FS_POLL_INT)**	R/W	Note 15-23
15:8	**FS Device Descriptor Size (FS_DEV_DESC_SIZE)** Note 15-24	R/W	Note 15-25
7:0	**FS Configuration Descriptor Size (FS_CFG_DESC_SIZE)** Note 15-24	R/W	Note 15-26

Note 15-23 The default value of this field is determined by the value of the Full-Speed Polling Interval for Interrupt Endpoint contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 01h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 01h if neither is present.

Note 15-24 The only legal values are 0 and 12h. Writing any other values will result in untoward behavior and unexpected results.

Note 15-25 The default value of this field is determined by the value of the Full-Speed Device Descriptor Length (bytes) contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

Note 15-26 The default value of this field is determined by the value of the Full-Speed Configuration and Interface Descriptor Length (bytes) contained within the EEPROM, if present. If no EEPROM is present then the vale programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

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15.1.17 STRING ATTRIBUTES REGISTER 0 (STRNG_ATTR0)

Offset: 060h Size: 32 bits

This register sets the length values for the named string descriptors that have been loaded into Descriptor RAM via the Data Port registers. The Descriptor RAM images may be used, in conjunction with this register, to facilitate customized operation when no EEPROM is present or OTP is not configured.

Note:

- If a descriptor does not exist in Descriptor RAM, its size value must be written as 00h.
- This register only affects system operation when an EEPROM is not present, OTP is not configured, and the EEPROM Emulation Enable (EEM) bit indicates Descriptor RAM and the Attributes Registers are to be used for descriptor processing.
- Writing to this register when an EEPROM is present or OTP is configured is prohibited and will result in untoward operation and unexpected results.
- This register is protected by Reset Protection (RST_PROTECT).

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**Configuration String Descriptor Size (CFGSTR_DESC_SIZE)**	R/W	Note 15-27
23:16	**Serial Number String Descriptor Size (SERSTR_DESC_SIZE)**	R/W	Note 15-28
15:8	**Product Name String Descriptor Size (PRODSTR_DESC_SIZE)**	R/W	Note 15-29
7:0	**Manufacturing String Descriptor Size (MANUF_DESC_SIZE)**	R/W	Note 15-30

Note 15-27 The default value of this field is determined by the value of the Configuration String Descriptor Length (bytes) contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

Note 15-28 The default value of this field is determined by the value of the Serial Number String Descriptor Length (bytes) contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

Note 15-29 The default value of this field is determined by the value of the Product Name String Descriptor Length (bytes) contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

Note 15-30 The default value of this field is determined by the value of the Manufacturer ID String Descriptor Length (bytes) contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

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15.1.18 STRING ATTRIBUTES REGISTER 1 (STRNG_ATTR1)

Offset: 064h Size: 32 bits

This register sets the length values for the named string descriptors that have been loaded into Descriptor RAM via the Data Port registers. The Descriptor RAM images may be used, in conjunction with this register, to facilitate customized operation when no EEPROM is present or OTP is not configured.

Note:

- If a descriptor does not exist in Descriptor RAM, its size value must be written as 00h.
- This register only affects system operation when an EEPROM is not present, OTP is not configured, and the EEPROM Emulation Enable (EEM) bit indicates Descriptor RAM and the Attributes Registers are to be used for descriptor processing.
- Writing to this register when an EEPROM is present or OTP is configured is prohibited and will result in untoward operation and unexpected results.
- This register is protected by Reset Protection (RST_PROTECT).

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**Interface String Descriptor Size (INTSTR_DESC_SIZE)**	R/W	Note 15-31

Note 15-31 The default value of this field is determined by the value of the Interface String Descriptor Length (bytes) contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

15.1.19 FLAG ATTRIBUTES REGISTER (FLAG_ATTR)

Offset: 068h Size: 32 bits

This register sets the value of the GPIO PME Flags 0 and GPIO PME Flags 1 when no EEPROM is present and customized operation, using Descriptor RAM images, is to occur.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:8	**GPIO PME Flags 1 (PME_FLAGS1)** Refer to Table 10-4, “GPIO PME Flags 1,” on page 107 for bit definitions. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-33
7:0	**GPIO PME Flags 0 (PME_FLAGS0)** Refer to Table 10-3, “GPIO PME Flags 0,” on page 106 for bit definitions. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-32

Note 15-32 The default value of this field is determined by the value of the GPIO PME Flags 0 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

Note 15-33 The default value of this field is determined by the value of the GPIO PME Flags 1 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

15.1.20 SOFTWARE GENERAL PURPOSE REGISTER X (SW_GPX)

Offset: 06Ch - 077h Size: 32 bits

The device implements three general purpose registers for use by host software.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Software General Purpose Register (SW_GPx)** **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	0h

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15.1.21 USB CONFIGURATION REGISTER 0 (USB_CFG0)

Offset: 080h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31	**RESERVED**	RO	-
30	**LPM Capability (LPM_CAP)** This bit enables the support of the Link Power Management (LPM) protocol. 0: LPM capability is not enabled. 1: LPM capability is enabled. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-36
29	**Suspend Enable (SUSP_EN)** When cleared this bit prevents the **SUSPEND_N** pin from asserting a suspend. Under normal operation when Suspend conditions are valid, the USB PHY enters suspend mode when this bit is set. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-34
28:16	**RESERVED**	RO	-
15:13	**Device Speed to Connect (DEV_SPEED)** 000: High-Speed 001: Full-Speed **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	000b
12:11	**RESERVED**	RO	-
10	**USB Bulk-In Transmitter (UTX) RESET** When set, the UTX is reset.	SC	0b
9	**USB Bulk-Out Receiver (URX) RESET** When set, the URX is reset.	SC	0b
8:7	**RESERVED**	RO	-
6	**Bulk-In Empty Response (BIR)** This bit controls the response to Bulk-In tokens when the RX FIFO is empty. 0 = Respond to the IN token with a ZLP 1 = Respond to the IN token with a NAK	R/W	0b
5	**Burst Cap Enable (BCE)** This register enables use of the Burst Cap Register (BURST_CAP). 0 = Burst Cap register is not used to limit the TX burst size. 1 = Burst Cap register is used to limit the TX burst size.	R/W	0b
4	**Port Swap (PORT_SWAP)** Swaps the mapping of **USB_DP** and **USB_DM**. 0 = **USB_DP** maps to USB D+ and **USB_DM** maps to USB D-. 1 = **USB_DP** maps to USB D- and **USB_DM** maps to USB D+.	RO	Note 15-35
3	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
2	**Remote Wakeup Support (RMT_WKP)** 0 = Device does not support remote wakeup. 1 = Device supports remote wakeup. This bit must be set for both DEVICE_REMOTE_WAKEUP and FUNCTION_REMOTE_WAKEUP to be supported. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-36
1	**Power Method (PWR_SEL)** This bit controls the device's USB power mode. 0 = The device is bus powered. 1 = The device is self powered. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-37
0	**Stall Bulk-Out Pipe Disable (SBP)** This bit controls the operation of the Bulk-Out pipe when the FIFO Controller detects the loss of sync condition. Please refer to Section 6.2.4, "TX Error Detection" for details. 0 = Stall the Bulk-Out pipe when loss of sync detected. 1 = Do not stall the Bulk-Out pipe when loss of sync detected.	R/W	0b

Note 15-34 The default value of this field is determined by Suspend Enable (SUSP_EN) bit of the Configuration Flags 0 field contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 1b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 1b if neither is available.

Note 15-35 The default value of this field is determined by Port Swap (CFG0_PORT_SWAP) bit of the Configuration Flags 0 field contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

Note 15-36 The default value of this field is determined by the respective bit of the Configuration Flags 0 field contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 1b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 1b if neither is available.

Note 15-37 The default value of this field is determined by the value of the Power Method (CFG0_PWR_SEL) bit of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present, 1b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or to be set to 1b if no EEPROM is present.

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15.1.22 USB CONFIGURATION REGISTER 1 (USB_CFG1)

Offset: 084h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:13	**HS Timeout Calibration (HS_TOUT_CAL)** The number of PHY clocks are indicated in this field. The controller multiplies this number by a bit-time factor, then adds the product to the high-speed inter-packet timeout duration in the core. This result accounts for additional delays introduced by the PHY. This is required because the delay introduced by generating the line-state condition varies among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The number of bit times added per PHY clock are: High-speed operation: ▪ One 30-MHz PHY clock = 16 bit times. ▪ One 60-MHz PHY clock = 8 bit times. **Note:** Only 60 MHz operation is supported in this device.	R/W	Note 15-40
12:7	**RESERVED**	RO	-
6:4	**FS Timeout Calibration (FS_TOUT_CAL)** The number of PHY clocks are indicated in this field. The controller multiplies this number by a bit-time factor, then adds the product to the full-speed inter-packet timeout duration in the core. This result accounts for additional delays introduced by the PHY. This is required because the delay introduced by generating the line-state condition varies among PHYs. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The number of bit times added per PHY clock are: Full-speed operation: • One 30-MHz PHY clock = 0.4 bit times. • One 60-MHz PHY clock = 0.2 bit times. • One 48-MHz PHY clock = 0.25 bit times **Note:** Only 60 MHz operation is supported in this device.	R/W	Note 15-41
3:2	**RESERVED**	RO	-
1:0	**Scale Down Mode** Scale down mode to reduce simulation time. When Scale-Down mode is enabled: Core uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled: Core uses actual timing values, as required for hardware operation. Scale-down status for HS/FS/LS Modes • 00: Disabled. Actual timing values are used. • 01: Enabled for all timing values except Device mode suspend and resume, including speed enumeration. • 10: Enabled for only Device mode suspend and resume. • 11: Enabled bit 0 and bit 1 scale-down values. **Note:** This field is for simulation only and should be set to 00b for normal operation.	RW	00b

Note 15-38 The default value of this field is determined by the respective bit in of Configuration Flags 0 within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0b if neither is present.

Note 15-39 The default value of this field is determined by the respective bit in of Configuration Flags 0 within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 1b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 1b if neither is present.

Note 15-40 The default value of this field is determined by the value of HS Timeout Calibration (HS_TOutCal) in Configuration Flags 2 within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

Note 15-41 The default value of this field is determined by the value of FS Timeout Calibration (FS_TOutCal) in Configuration Flags 2 within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00h is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00h if neither is present.

15.1.23 USB CONFIGURATION REGISTER 2 (USB_CFG2)

Offset: 088h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**HS Detach Time (HS_DETACH)** Indicates amount of time, in ms, the device shall detach from the USB bus after Soft Reset is requested when operating in high-speed or full-speed mode. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-42

Note 15-42 The default value of this field is determined by the value of HS Detach Time (HS_DETACH) of Configuration Flags 3 within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0x0A is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0x0A if neither is present.

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15.1.24 BURST CAP REGISTER (BURST_CAP)

Address: 090h Size: 32 bits

This register is used to limit the size of the data burst transmitted by the USB Bulk-In Transmitter (UTX). When the amount specified in the BURST_CAP register is transmitted, the UTX will send a ZLP.

Note: This register must be enabled through the USB Configuration Register 0 (USB_CFG0).

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**BURST_CAP** The maximum amount of contiguous data that may be transmitted by the UTX before a ZLP or short packet is sent. This field has units of 512 bytes for HS mode and 64 bytes for FS mode. **Note:** The amount of contiguous data specified must be >= the Maximum Frame Size (MAX_SIZE) specified in the MAC_RX register. Failure to obey this rule may result in untoward operation and may yield unpredictable results. **Note:** The device will disable the BURST_CAP function if the setting is less than or equal to 2048 bytes.	R/W	00h

15.1.25 BULK-IN DELAY REGISTER (BULK_IN_DLY)

Address: 094h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**Bulk In Delay** Before sending a short packet, or ZLP, the USB Bulk-In Transmitter (UTX) waits the delay specified by this register. This register has units of 16.667 ns and a default interval of 34.133 us.	R/W	0800h

15.1.26 INTERRUPT ENDPOINT CONTROL REGISTER (INT_EP_CTL)

Address: 098h Size: 32 bits

This register determines which events cause status to be reported by the interrupt endpoint. Please refer to Section 5.5, "Interrupt Endpoint," on page 31 for further details.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Interrupt Endpoint Always On (INTEP_ON)** When this bit is set, an interrupt packet will always be sent at the interrupt endpoint interval. 0 = Only allow the transmission of an interrupt packet when an interrupt source is enabled and occurs. 1 = Always transmit an interrupt packet at the interrupt interval.	R/W	0b
30:29	**RESERVED**	RO	-
28	**OTP Write Done Enable (OTP_WR_DONE_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
27	**RESERVED**	RO	-
26	**Energy Efficient Ethernet Start TX Low Power Enable (EEE_START_TX_LPI_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
25	**Energy Efficient Ethernet Stop TX Low Power Enable (EEE_STOP_TX_LPI_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
24	**Energy Efficient Ethernet RX Low Power Enable (EEE_RX_LPI_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
23	**MAC Reset Time Out (MACRTO_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
22	**RX Data FIFO Overflow Enable (RDFO_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
21	**Transmit Error Enable (TXE_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
20	**USB Status Interrupt Enable (USB_STS_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
19	**TX Disabled Interrupt Enable (TX_DIS_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
18	**RX Disabled Interrupt Enable (RX_DIS_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
17	**PHY Interrupt Enable (PHY_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
16	**Data Port Interrupt Enable (DP_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
15	**MAC Error Interrupt Enable (MAC_ERR_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
14	**TX Data FIFO Under-run Interrupt Enable (TDFU_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
13	**TX Data FIFO Overrun Interrupt Enable (TDFO_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
12	**USB Bulk-In Transmitter (UTX) Frame Pending Enable (UTX_FP_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b
11:0	**GPIOx Interrupt Enable (GPIOx_EN)** 0 = This event can not cause an interrupt packet to be issued. 1 = This event can cause an interrupt packet to be issued.	R/W	0b

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15.1.27 PIPE CONTROL REGISTER (PIPE_CTL)

Address: 09Ch Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**TX Swing (TxSwing)** Refer to table 5-3 of the PIPE3 specification. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-43
5:3	**TX Margin (TxMargin)** Refer to table 5-3 of the PIPE3 specification. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-44
2:1	**TX Deemphasis (TxDeemphasis)** Refer to table 5-3 of the PIPE3 specification. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-45
0	**Elasticity Buffer Mode (ElasticityBufferMode)** Refer to table 5-3 of the PIPE3 specification. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-46

Note 15-43 The default value of this field is determined by the value of the TX Swing (TxSwing) bit of Configuration Flags 1 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Lite Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

Note 15-44 The default value of this field is determined by the value of the TX Margin (TxMargin) bit of Configuration Flags 1 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Lite Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

Note 15-45 The default value of this field is determined by the value of the TX Deemphasis (TxDeemphasis) bit of Configuration Flags 1 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Lite Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

Note 15-46 The default value of this field is determined by the value of the Elasticity Buffer Mode (ElasticityBufferMode) bit of Configuration Flags 1 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Lite Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

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15.1.28 USB STATUS REGISTER (USB_STATUS)

Address: 0A8h Size: 32 bits

Bits 15:0 of this CSR are used to generate the USB_STS_INT bit of the Interrupt EP. They indicate a change in the state of the respective bit. When applicable, the current state of the bit is listed in the mirror bit location in bits 31:16.

BITS	DESCRIPTION	TYPE	DEFAULT
31:21	**RESERVED**	RO	-
20	**Remote Wakeup (REMOTE_WK)** Indicates the current state of Device Remote Wakeup.	RO/ NALR	0b
19	**Function Remote Wakeup (FUNC_REMOTE_WK)** Indicates the current state of Function Remote Wakeup Capable.	RO/ NALR	0b
18:5	**RESERVED**	RO	-
4	**Remote Wakeup Status Change (REMOTE_WK_STS)** Indicates that the host set or cleared Device Remote Wakeup.	R/WC	0b
3	**Function Remote Wakeup Status Change (FUNC_REMOTE_WK_STS)** Indicates that the host set or cleared Function Remote Wake Capable	R/WC	0b
2:0	**RESERVED**	RO	-

15.1.29 RECEIVE FILTERING ENGINE CONTROL REGISTER (RFE_CTL)

Offset: 0B0h Size: 32 bits

This register configures the Receive Filtering Engine (RFE).

If neither Enable IGMP Checksum Validation, Enable ICMP Checksum Validation or Enable TCP/UDP Checksum Validation bits are set, then the RFE inserts 0000h for the L3 raw checksum field.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15	**Always Pass Wakeup Frame (PASS_WKP)** When set, the RFE shall never discard a received wakeup frame which awakened the device while in SUSPEND3 and Store Wakeup Frame (STORE_WAKE) is set.	R/W	0b
14	**Enable IGMP Checksum Validation** When set, the RFE will check the IGMP checksum. Additionally, the RFE calculates the L3 raw checksum and inserts it into RX Status Word 1. **Note:** If the frame is not IGMP raw checksum is still calculated.	R/W	0b
13	**Enable ICMP Checksum Validation** When set, the RFE will check the ICMP checksum. Additionally, the RFE calculates the L3 raw checksum and inserts it into RX Status Word 1. **Note:** If the frame is not ICMP raw checksum is still calculated.	R/W	0b
12	**Enable TCP/UDP Checksum Validation** When set, the RFE will check the TCP or UDP checksum. Additionally, the RFE calculates the L3 raw checksum and inserts it into RX Status Word 1. **Note:** If the frame is not TCP or UDP the raw checksum is still calculated.	R/W	0b
11	**Enable IP Checksum Validation** When set, the RFE will check the IP checksum. This bit has no effect if the frame is not IPv4 or IPv6.	R/W	0b
10	**Accept Broadcast Frames (AB)** When set, all broadcast frames are accepted. Otherwise broadcast frames are dropped.	R/W	0b
9	**Accept Multicast Frames (AM)** When set, all multicast frames are accepted. Otherwise multicast frames must pass the perfect filtering or hash filtering. **Note:** This bit does not apply to broadcast frames.	R/W	0b
8	**Accept Unicast Frames (AU)** When set, all unicast frames are accepted.	R/W	0b
7	**Enable VLAN Tag Stripping** When set, this bit enables stripping of a received frame's VLAN ID.	R/W	0b
6	**Untagged Frame Filtering (UF)** When set, all untagged receive frames are discarded.	R/W	0b
5	**Enable VLAN Filtering (VF)** When set, this bit enables filtering of a received frame's VLAN ID.	R/W	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
4	**Enable Source Address Perfect Filtering (SPF)** When set, this bit enables perfect filtering of a received frame's Ethernet source address. **Note:** If destination address filtering is enabled (perfect or hash), the frame must pass both source address filtering and destination address filtering to not be discarded.	R/W	0b
3	**Enable Multicast Address Hash Filtering (MHF)** When set, multicast destination addresses will be hashed. **Note:** The broadcast address is never hashed.	R/W	0b
2	**Enable Destination Address Hash Filtering (DHF)** When set, unicast destination addresses will be hashed.	R/W	0b
1	**Enable Destination Address Perfect Filtering (DPF)** When set, this bit enables perfect filtering of a received frame's Ethernet destination address.	R/W	0b
0	**Reset Receive Filtering Engine** When set, this bit resets the RFE.	SC	0b

15.1.30 VLAN TYPE REGISTER (VLAN_TYPE)

Offset: 0B4h Size: 32 bits

This register extends the Ethernet type used to indicate the presence of a VLAN tag in the RFE in addition to 8100h. In the FCT this is the value used for the Ethernet type when VLAN tag insertion is enabled.

The intention of this register is to allow for a proprietary VLAN type to be supported. If only the standard VLAN type of 8100h is desired to be supported, then this register should retain its default value of 8100h.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**VLAN Ethernet Type**	R/W	8100h

15.1.31 FIFO CONTROLLER RX FIFO CONTROL REGISTER (FCT_RX_CTL)

Offset: 0C0h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31	**FCT RX Enable** When set, the FIFO is capable of accepting traffic from the RFE. If this bit is deasserted, all received frames from the RFE are aborted and not written into the FIFO. After this bit is asserted, the FIFO will accept the next full frame it receives. After the FIFO is enabled, the FIFO begins accepting data after it receives the first complete frame. If the FIFO is disabled while receiving a frame, the FIFO will allow the current frame to be received before disabling the FIFO. After the FIFO is successfully disabled the FCT RX Disabled bit is asserted. **Note:** This bit does not cause frame dropped counter to increment.	R/W	0b
30	**FCT RX RESET** When set, the FCT RX is reset. It also clears any remnant data from the FIFO stored in the UTX interface pipeline. The FIFO must be disabled before a reset is issued.	SC	f
29:26	**RESERVED**	RO	-
25	**Store Bad Frames** When set, the RX FCT will store errored frames that were detected by the Ethernet MAC. The following conditions cause the MAC to consider a frame bad: RX error, FCS error, runt frame, alignment error, jabber error, undersize frame error, and oversize frame error.	R/W	0b
24	**FCT RX Overflow**	R/WC	0b
23	**RX Frame Dropped** See RX Dropped Frames for a description	R/WC	0b
22:21	**RESERVED**	RO	-
20	**FCT RX Disabled** This bit indicates the FIFO has been successfully disabled via clearing the FCT RX Enable bit. It is set when the hardware disabling process, invoked by a transition of the FCT RX Enable bit from 1 to 0 (enabled to disabled), completes.	R/WC	0b
19:16	**RESERVED**	RO	-
15:0	**RX Data FIFO Used Space (RXUSED)** Reads the amount of space in bytes, used by the FIFO. For each frame, this field is incremented by the length of the frame rounded up to the nearest DWORD (if the payload does not end on a DWORD boundary). Additionally any Command Words or checksums associated with the frame are also added in.	RO	0000h

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15.1.32 FIFO CONTROLLER TX FIFO CONTROL REGISTER (FCT_TX_CTL)

Offsets: 0C4h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31	**FCT TX Enable** When set, the FIFO is capable of transmitting frames to the MAC. If the FIFO is disabled while transmitting a frame, the frame transmission is allowed to complete. Upon completion of the last frame FCT TX Disabled bit is asserted. An exception to the above can happen in half duplex mode in which the FIFO may discard the frame in transmit. This case happens when the frame in transmit is retried by the MAC after the FIFO has been disabled. The FIFO does not allow any further retries.	R/W	0b
30	**FCT TX Reset** When set, this bit resets the FCT TX. It also clears any remnant data from the FIFO stored in the URX interface pipeline. The FIFO must be disabled before a reset is issued.	SC	0b
29:21	**RESERVED**	RO	-
20	**FCT TX Disabled** This bit indicates the FIFO has been successfully disabled via clearing the FCT TX Enable bit. It is set when the hardware disabling process, invoked by a transition of the FCT TX Enable bit from 1 to 0 (enabled to disabled), completes.	R/WC	0b
19:16	**RESERVED**	RO	-
15:0	**TX Data FIFO Used Space (TXUSED)** Reads the amount of space in bytes, used by the FIFO. For each frame, this field is incremented by the length of the frame rounded up to the nearest DWORD (if the payload does not end on a DWORD boundary). Additionally any Command Words or checksums associated with the frame are also added in.	RO	0000h

15.1.33 FCT RX FIFO END REGISTER (FCT_RX_FIFO_END)

Offset: 0C8h Size: 32 bits

This register specifies the end address of the RX FIFO in DWORD units. The contents of this register times 128 plus 127 is the end address of the FIFO.

Note:	This register's contents may not be modified at run time. The RX data path must be halted before changing the FIFO size. After modifying the FIFO's size, the FIFO must be flushed.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6:0	**FCT_RX_FIFO_END**	R/W	17h

Note:	Maximum RX FIFO size is 12 KB which is the.default value.

15.1.34 FCT TX FIFO END REGISTER (FCT_TX_FIFO_END)

Offset: 0CCh Size: 32 bits

This register specifies the end address of the TX FIFO in DWORD units. The contents of this register times 128 plus 127 is the end address of the FIFO.

Note:	This register's contents may not be modified at run time. The TX data path must be halted before changing the FIFO size. After modifying the FIFO's size, the FIFO must be flushed.

BITS	DESCRIPTION	TYPE	DEFAULT
31:6	**RESERVED**	RO	-
5:0	**FCT_TX_FIFO_END**	R/W	17h

Note:	Maximum TX FIFO size is 12 KB which is the default.

15.1.35 FCT FLOW CONTROL THRESHOLD REGISTER (FCT_FLOW)

Offset: 0D0h Size: 32 bits

This register specifies the thresholds for controlling pause frame generation. The units of the thresholds are 512 bytes and correspond to high and low watermarks in the RX FIFO.

Note:	The values in this register must be programmed before the TX Flow Control Enable (TX_FCEN) bit is set. Please refer to Section 15.1.41, "Flow Control Register (FLOW)," on page 187 for further details.

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14:8	**Flow Control Off Threshold** The threshold to turn flow control off. If RX Data FIFO Used Space (RXUSED) / 512 is less than or equal to this value, then flow control is turned off.	R/W	0000000b
7	**RESERVED**	RO	-
6:0	**Flow Control On Threshold** The threshold to turn flow control on. If RX Data FIFO Used Space (RXUSED) / 512 is greater than or equal to this value, then flow control is turned on.	R/W	0000000b

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15.1.36 RX DATAPATH STORAGE (RX_DP_STOR)

Offset: 0D4h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Total RX Data Path Used Space (TOT_RXUSED)** Reads the amount of space in bytes, used by both the UTX FIFO and FCT RX FIFO.	RO	0000h
15:0	**UTX FIFO Used Space (UTX_RXUSED)** Reads the amount of space in bytes, used by the UTX FIFO.	RO	0000h

15.1.37 TX DATAPATH STORAGE (TX_DP_STOR)

Offset: 0D8h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Total TX Data Path Used Space (TOT_TXUSED)** Reads the amount of space in bytes, used by both the URX FIFO and FCT TX FIFO.	RO	0000h
15:0	**URX FIFO Used Space (URX_TXUSED)** Reads the amount of space in bytes, used by the URX FIFO.	RO	0000h

15.1.38 MAC CONTROL REGISTER (MAC_CR)

Offset: 100h Size: 32 bits

This register establishes the RX and TX operating modes.

BITS	DESCRIPTION	TYPE	DEFAULT
31:19	**RESERVED**	RO	-
18	**Energy Efficient Ethernet TX Clock Stop Enable (EEE_TX_CLK_STOP_EN)** When set, the MAC will halt the GMII GTX_CLK to the PHY during TX LPI. This bit is unused in 100Mbs mode. This bit should only be set if the Clock stop capable bit in PHY MMD register 3.1 indicates that the PHY is capable of allowing a stopped TX clock. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-47
17	**Energy Efficient Ethernet Enable (EEEEN)** When set, enables Energy Efficient Ethernet operation in the MAC. When cleared, Energy Efficient Ethernet operation is disabled. Note 15-48 The MAC will generate LPI requests even if Transmitter Enable (TXEN) is cleared and will decode the LPI indication even if Receiver Enable (RXEN) is cleared. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-47
16	**Energy Efficient Ethernet TX LPI Automatic Removal Enable (EEE_TX_LPI_AUTO_REMOVAL_EN)** When set, enables the automatic deassertion of LPI in anticipation of a periodic transmission event. The time to wait is specified in the EEE TX LPI Automatic Removal Delay Register (EEE_TX_LPI_AUTO_REMOVAL_DELAY). The interval is timed from the point where the MAC initiates LPI signaling. Host software should only change this field when Energy Efficient Ethernet Enable (EEEEN) is cleared. **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-47
15:14	**RESERVED**	RO	-
13	**Automatic Duplex Polarity (ADP)** This bit indicate the polarity of the FDUPLEX PHY LED. 0: DUPLEX asserted low indicates the PHY is in full duplex mode. 1: DUPLEX asserted high indicates the PHY is in full duplex mode. **Note:** This bit should not be modified while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set). **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	1b
12	**Automatic Duplex Detection (ADD)** When set, the MAC ignores the setting of the Duplex Mode (DPX) bit and automatically determines the duplex operational mode. The MAC uses a PHY LED/signal to accomplish mode detection and reports the last determined status via the Duplex Mode (DPX) bit. When reset, the setting of the Duplex Mode (DPX) bit determines Duplex operation. **Note:** This bit should not be modified while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set). **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-49

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BITS	DESCRIPTION	TYPE	DEFAULT
11	**Automatic Speed Detection (ASD)** When set, the MAC ignores the setting of the MAC Configuration (CFG) field and automatically determines the speed of operation. The MAC samples the RX_CLK input to accomplish speed detection and reports the last determined speed via the MAC Configuration (CFG) field. When reset, the setting of the MAC Configuration (CFG) field determines operational speed. **Note:** This bit should not be modified while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set). **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-50
10	**Internal Loopback Operation Mode (INT_LOOP)** Loops back data between the TX data path and RX data path interfaces. This is only for full duplex mode. In internal loopback mode, the TX frame is received by the Internal GMII interface, and sent back to the MAC without being sent to the PHY. 0: Normal mode 1: Internal loopback enabled **Note:** This bit should not be modified while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set).	R/W	0b
9:8	**RESERVED**	RO	-
7:6	**Back Off Limit (BOLMT)** The BOLMT bits allow the user to set its back-off limit in a relaxed or aggressive mode. According to IEEE 802.3, the MAC has to wait for a random number [r] of slot-times after it detects a collision, where: *(eq.1)0 < r < $_2$K* The exponent K is dependent on how many times the current frame to be transmitted has been retried, as follows: *(eq.2)K = min (n, 10) where n is the current number of retries.* If a frame has been retried three times, then K = 3 and r= 8 slot-times maximum. If it has been retried 12 times, then K = 10, and r = 1024 slot-times maximum. An LFSR (linear feedback shift register) counter emulates a random number generator, from which r is obtained. Once a collision is detected, the number of the current retry of the current frame is used to obtain K (eq.2). This value of K translates into the number of bits to use from the LFSR counter. If the value of K is 3, the MAC takes the value in the first three bits of the LFSR counter and uses it to count down to zero on every slot-time. This effectively causes the MAC to wait eight slot-times. To give the user more flexibility, the BOLMT value forces the number of bits to be used from the LFSR counter to a predetermined value as in the table below. Thus, if the value of K = 10, the MAC will look at the BOLMT if it is 00, then use the lower ten bits of the LFSR counter for the wait countdown. If the BOLMT is 10, then it will only use the value in the first four bits for the wait countdown, etc. Slot-time = 512 bit times. (See IEEE 802.3 Spec., Sections 4.2.3.2.5 and 4.4.2.1). **Note:** This bit should not be modified while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set).	R/W	00b
5:4	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
3	**Duplex Mode (DPX)** This bit determines the duplex operational mode of the MAC when the Automatic Duplex Detection (ADD) bit is reset. When the Automatic Duplex Detection (ADD) bit is set, this bit is read-only and reports the last determined duplex operational mode. When set, the MAC is operating in Full-Duplex mode, in which it can transmit and receive simultaneously. 0: MAC is in half duplex mode 1: MAC is in full duplex mode **Note:** This bit should not be modified while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set). **Note:** Half duplex mode is disabled if the detected or manually set speed is 1000Mbs, regardless of the setting of this bit. **Note:** This field is protected by Reset Protection (RST_PROTECT).	Note 15-51	Note 15-47
2:1	**MAC Configuration (CFG)** This field determines the operational speed of the MAC when the Automatic Speed Detection (ASD) bit is reset. When the Automatic Speed Detection (ASD) bit is set, this field is read-only and reports the last determined operational speed. 0: MII Mode - 10 Mbps 1: MII Mode - 100 Mbps 2,3: RGMII/GMII Mode - 1000 Mbps **Note:** This bit should not be modified while the MAC's receiver or transmitter is enabled (Receiver Enable (RXEN) or Transmitter Enable (TXEN) bit set). **Note:** This field is protected by Reset Protection (RST_PROTECT).	Note 15-52	Note 15-47
0	**MAC Reset (MRST)** 0: MAC is enabled 1: MAC is reset	SC	0b

Note 15-47 The default value of this field is determined by the value of the respective field in Configuration Flags 2 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0h is the default. A USB Reset or Soft Lite Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0h if neither is available.

Note 15-48 If this bit is manually changed, then the EEE configuration in the Ethernet PHY must be updated and auto-negotiation rerun.

Note 15-49 The default value of this field is determined by the value of the Automatic Duplex Detection (CFG0_ADD) bit of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 1b is the default. A USB Reset or Soft Lite Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 1b if neither is available.

Note 15-50 The default value of this field is determined by the value of the Automatic Speed Detection (CFG0_ASD) bit of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 0b is the default. A USB Reset or Soft Lite Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0b if neither is available.

Note 15-51 When Automatic Duplex Detection (ADD) is reset, this bit is R/W and determines duplex operation. When Automatic Duplex Detection (ADD) is set, this field is RO and reports the last duplex operational mode determined by the MAC.

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Note 15-52 When Automatic Speed Detection (ASD) is reset, this field is R/W and determines operational speed. When Automatic Speed Detection (ASD) is set, this field is RO and reports the last operational speed determined by the MAC.

15.1.39 MAC RECEIVE REGISTER (MAC_RX)

Offset: 104h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:30	**RESERVED**	RO	-
29:16	**Maximum Frame Size (MAX_SIZE)** Defines the maximum size for a received frame. Frames exceeding this size are aborted. **Note:** A frame longer than 11,264 bytes will cause the watchdog timer to truncate and abort the frame. **Note:** This field should not be modified while the MAC's receiver is enabled (Receiver Enable (RXEN) bit set in MAC Receive Register (MAC_RX)).	R/W	1518
15:6	**RESERVED**	RO	-
5	**Watchdog Truncation Length (WTL)** 0: The MAC truncates the Rx FRAME at MAC_RX.MAX_SIZE+1. The RxCmdA of the truncated received frame passed to the FCT has LONG bit set and length MAC_RX.MAX_SIZE+1 and FCS likely set. 1: The MAC truncates the Rx FRAME at 11265. The RxCmdA of the truncated received frame passed to the FCT has LONG bit set and length 11265 and FCS more than likely set and RWT bit set also. **Note:** This bit should not be modified while the MAC's receiver is enabled (Receiver Enable (RXEN) bit set in MAC Receive Register (MAC_RX)).	R/W	1b
4	**FCS Stripping** When set, the MAC will strip the FC (last 4 bytes) off of all received frames. **Note:** This bit should not be modified while the MAC's receiver is enabled (Receiver Enable (RXEN) bit set in MAC Receive Register (MAC_RX)).	R/W	0b
3	**RESERVED**	RO	-
2	**VLAN Frame Size Enforcement (FSE)** 0: Abort all frames larger than the maximum frame size. 1: Abort all non-VLAN frames larger than maximum frame size. Abort all frames with a single VLAN tag that are larger the maximum frame size + 4. Abort all frames with two VLAN tags that are larger than the maximum frame size + 8. **Note:** This bit should not be modified while the MAC's receiver is enabled (Receiver Enable (RXEN) bit set in MAC Receive Register (MAC_RX)).	R/W	0b
1	**Receiver Disabled (RXD)** This bit indicates the MAC's receiver has been successfully disabled via clearing the Receiver Enable (RXEN) bit. It is set when the hardware disabling process, invoked by a transition of the Receiver Enable (RXEN) bit from 1 to 0 (enabled to disabled), completes.	R/WC	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
0	**Receiver Enable (RXEN)** When set, the MAC's receiver is enabled and will receive frames from the PHY. When reset, the MAC's receiver is disabled and will not receive any frames from the PHY. If this bit is deasserted while a frame is being received, the received frames allowed to complete. Upon completion, the MAC's receiver is disabled and the Receiver Disabled (RXD) bit is asserted.	R/W	0b

15.1.40 MAC TRANSMIT REGISTER (MAC_TX)

Offset: 108h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2	**Bad FCS (BFCS)** When set, the MAC's transmitter will append a bad FCS on all transmitted frames. This feature is useful for diagnostic purposes. This function may only be used in conjunction with Insert FCS and Pad of TX Command A.	R/W	0b
1	**Transmitter Disabled (TXD)** This bit indicates the MAC's transmitter has been successfully disabled via clearing the Transmitter Enable (TXEN) bit. It is set when the hardware disabling process, invoked by a transition of the Transmitter Enable (TXEN) bit from 1 to 0 (enabled to disabled), completes.	R/WC	0b
0	**Transmitter Enable (TXEN)** When set, the MAC's transmitter is enabled and it will transmit frames from the buffer onto the cable. When reset, the MAC's transmitter is disabled and will not transmit any frames. If this bit is cleared while a frame is being transmitted, the frame is allowed to complete. Upon completion, the MAC's transmitter is disabled and the Transmitter Disabled (TXD) bit is asserted.	R/W	0b

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15.1.41 FLOW CONTROL REGISTER (FLOW)

Offset: 10Ch Size: 32 bits

This register is used to control the handling of the RX and TX flow control frames by the MAC.

RX flow control frames are received by the MAC. When RX flow control is enabled, the MAC will pause transmissions from the transmit data path for the amount of time specified in the flow control frame.

TX flow control frames may be generated manually or automatically using RX FIFO thresholds. By setting the FORCE_FC bit, a flow control frame will be manually transmitted with the value specified by Pause Time (FCPT). After the frame is transmitted, the FORCE_FC bit clears.

Whenever TX_FCEN is set, transmit flow control frames are generated automatically, based on the thresholds set in the FCT Flow Control Threshold Register (FCT_FLOW). Whenever the high watermark is crossed (RX Data FIFO Used Space (RXUSED) / 512 greater than or equal to Flow Control On Threshold), the MAC transmits a flow control frame with the pause value specified by the Pause Time (FCPT) field. When the low watermark is subsequently crossed (RX Data FIFO Used Space (RXUSED) / 512 less than or equal to Flow Control Off Threshold), the MAC transmits a flow control frame with a pause value of zero.

Flow Control is only applicable when the MAC is set in full duplex mode.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Force Transmission of TX Flow Control Frame (FORCE_FC)** This bit forces the transmission of a TX flow control frames. Writing a “1” initiates the frame transmission. The frame will be generated with the Pause Time value. After the frame is transmitted, the MAC will clear this bit.	SC	0b
30	**TX Flow Control Enable (TX_FCEN)** When set, enables the transmit MAC flow control function based on high and low watermarks in the RX FIFO, as discussed in this section. **Note:** The threshold values in the FCT Flow Control Threshold Register (FCT_FLOW) must be programmed before this bit is set.	R/W	0b
29	**RX Flow Control Enable (RX_FCEN)** When set, enables the receive MAC flow control function. The MAC decodes all incoming frames for control frames; if it receives a valid control frame (PAUSE command), it disables the transmitter for a specified time (Decoded pause time x slot time). When not set, the MAC flow control function is disabled; the MAC does not decode frames for control frames.	R/W	0b
28	**Forward Pause Frames (FPF)** Enables passing received pause frames to RX data path interface. 0 = Sink received pause frames. 1 = Pass received pause frames to the RX data path interface. **Note:** Flow Control is applicable when the MAC is set in full duplex mode.	R/W	0b
27:16	**RESERVED**	RO	-
15:0	**Pause Time (FCPT)** This field indicates the value to be used in the PAUSE TIME field in the control frame.	R/W	0000h

15.1.42 RANDOM NUMBER SEED VALUE REGISTER (RAND_SEED)

Offset: 110h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**Random Number Seed (RAND_SEED)** The MAC random number generator seed value. The content of this register is the seed value for the LFSR (linear feedback shift register) counter used to emulate the random number generator in the MAC TX back-off timer logic.	R/W	9876h

15.1.43 ERROR STATUS REGISTER (ERR_STS)

Offset: 114h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:9	**RESERVED**	RO	-
9	**RX Error (RXERR)** Indicates that a receive error (PHY RX error signal asserted) has been detected during frame reception.	R/WAC	0b
8	**FCS Error (FERR)** An FCS errored frame has been received.	R/WAC	0b
7	**Large Frame Error (LFERR)** A frame larger than the maximum allow frame size has been received.	R/WAC	0b
6	**Runt/Short Frame Error (RFERR)** A runt frame or a short frame has been received.	R/WAC	0b
5	**Receive Watchdog Timer Expired (RWTERR)** When set, this bit indicates the received frame was longer than 11,264 bytes and was truncated by the MAC.	R/WAC	0b
4	**Excessive Collision Error (ECERR)** A received frame was aborted due to sixteen collisions occurring.	R/WAC	0b
3	**Alignment Error (ALERR)** An alignment error has been detected on a received frame.	R/WAC	0b
2	**Under Run Error (URERR)** The MAC has been under run by the transmit data-path.	R/WAC	0b
1:0	**RESERVED**	RO	-

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15.1.44 MAC RECEIVE ADDRESS HIGH REGISTER (RX_ADDRH)

Address: 118h Size: 32 bits

This register contains the upper 16 bits of the physical address of the MAC, where RX_ADDRH[15:8] is the 6th octet of the received frame.

This register used to specify the address used for Perfect DA, Magic Packet and Wakeup frames, the unicast destination address for received pause frames, and the source address for transmitted pause frames. This register is not used for packet filtering.

Note: This register is protected by Reset Protection (RST_PROTECT).

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15-0	**Physical Address [47:32]** This field contains the upper 16 bits [47:32] of the physical address of the device.	R/W	FFFFh Note 15-53

Note 15-53 The default value of this field is determined by the value of the MAC Address field contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then FFFF_FFFFh is the default. A USB Reset will cause this field to be restored to the value last loaded from EEPROM, or OTP, otherwise the current value in this register will be maintained.

15.1.45 MAC RECEIVE ADDRESS LOW REGISTER (RX_ADDRL)

Address: 11Ch Size: 32 bits

This register contains the lower 32 bits of the physical address of the MAC, where RX_ADDRL[7:0] is the first octet of the Ethernet frame.

This register used to specify the address used for Perfect DA, Magic Packet, and Wakeup frames, the unicast destination address for received pause frames, and the source address for transmitted pause frames. This register is not used for packet filtering.

This register is protected by Reset Protection (RST_PROTECT).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Physical Address [31:0]** This field contains the lower 32 bits [31:0] of the physical address of the device.	R/W	FFFF_FFFFh Note 15-54

Note 15-54 The default value of this field is determined by the value of the MAC Address filed contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then FFFF_FFFFh is the default. A USB Reset will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to FFFF_FFFFh if neither is present.

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Table 15-4 illustrates the byte ordering of the RX_ADDRL and RX_ADDRH registers with respect to the reception of the Ethernet physical address.

TABLE 15-4: RX_ADDRL, RX_ADDRH BYTE ORDERING

RX_ADDRL, RX_ADDRH	ORDER OF RECEPTION ON ETHERNET
RX_ADDRL[7:0]	1st
RX_ADDRL[15:8]	2nd
RX_ADDRL[23:16]	3rd
RX_ADDRL[31:24]	4th
RX_ADDRH[7:0]	5th
RX_ADDRH[15:8]	6th

15.1.46 MII ACCESS REGISTER (MII_ACCESS)

Address: 120h Size: 32 bits

This register is used to control the management cycles to the PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:11	**PHY Address** For every access to this register, this field must be set to 00001b.	R/W	00001b
10:6	**MII Register Index (MIIRINDA)** These bits select the desired MII register in the PHY.	R/W	00000b
5:2	**RESERVED**	RO	-
1	**MII Write (MIIWnR)** Setting this bit tells the PHY that this will be a write operation using the MII data register. If this bit is not set, this will be a read operation, packing the data in the MII data register.	R/W	0b
0	**MII Busy (MIIBZY)** This bit must be polled to determine when the MII register access is complete. This bit must read a logical 0 before writing to this register or to the MII data register. The LAN driver software must set (1) this bit in order for the Host to read or write any of the MII PHY registers. During a MII register access, this bit will be set, signifying a read or write access is in progress. The MII data register must be kept valid until the MAC clears this bit during a PHY write operation. The MII data register is invalid until the MAC has cleared this bit during a PHY read operation.	SC	0b

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15.1.47 MII DATA REGISTER (MII_DATA)

Address: 124h Size: 32 bits

This register contains either the data to be written to the PHY register specified in the MII Access Register, or the read data from the PHY register whose index is specified in the MII Access Register. Refer to Section 15.1.46, "MII Access Register (MII_ACCESS)," on page 190 for further details.

Note: The MIIBZY bit in the MII_ACCESS register must be cleared when writing to this register.

BITS	DESCRIPTION		
31:16	**RESERVED**	RO	-
15:0	**MII Data** This contains the 16-bit value read from the PHY read operation or the 16-bit data value to be written to the PHY before an MII write operation.	R/W	0000h

15.1.48 EEE TX LPI REQUEST DELAY COUNT REGISTER (EEE_TX_LPI_REQUEST_DELAY_CNT)

Offset: 130h Size: 32 bits

Contains the count corresponding to the amount of time, in us, the MAC must wait after the TX FIFO is empty before invoking the LPI protocol.

Whenever the TX FIFO is empty, the device checks the Energy Efficient Ethernet Enable (EEEEN) bit of the MAC Control Register (MAC_CR) to determine whether or not the Energy Efficient Ethernet mode of operation is in effect. If the bit is clear, no action is taken, otherwise, the device waits the amount of time indicated in this register. After the wait period has expired, the LPI protocol is initiated and the Energy Efficient Ethernet Start TX Low Power Interrupt (EEE_START_TX_LPI_INT) bit of the Interrupt Status Register (INT_STS) will be set.

Note:

- Due to a 1us pre-scaler, the actually time can be up to 1us longer than specified.
- A value of zero is valid and will cause no delay to occur.

If the TX FIFO becomes non-empty, the timer is restarted.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**EEE TX LPI Request Delay Count (EEE_TX_LPI_REQUEST_DELAY_CNT)** Count representing time to wait before invoking LPI protocol. Units are in us. **Note:** Host software should only change this field when Energy Efficient Ethernet Enable (EEEEN) is cleared.	R/W	00000000h

APPLICATION NOTE: A value of zero may adversely affect the ability of the TX data path to support Gigabit operation. A reasonable value when the part is operating at Gigabit speeds is 50 us. This value may be increased pending the results of performance testing with EEE enabled. The motivation for 802.3az is the scenario where the EEE link is idle most of the time with the occasional full bandwidth transmission bursts. Aggressively optimizing power consumption during pockets of inactivity is not the objective for this mode of operation.

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15.1.49 EEE TIME WAIT TX SYSTEM REGISTER (EEE_TW_TX_SYS)

Offset: 134h Size: 32 bits

Contains the count corresponding to the amount of time, in us, the MAC must wait after LPI is exited before it can transmit packets. Time is specified in separate fields for 100Mbs and 1000Mbs operation. This wait time is in addition to the IPG time.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**EEE TIME Wait TX System Count 1000 (EEE_TW_TX_SYS_CNT_1000)** Count representing time to wait before commencing transmission after LPI is exited when operating at 1000Mbs. Units are in 0.5 us. Host software should only change this field when Energy Efficient Ethernet Enable (EEEEN) is cleared. **Note:** In order to meet the IEEE 802.3 specified requirement, the minimum value of this field should be 000021h.	R/W	000021h
15:0	**EEE TIME Wait TX System Count 100 (EEE_TW_TX_SYS_CNT_100)** Count representing time to wait before commencing transmission after LPI is exited when operating at 100Mbs. Units are in us. Host software should only change this field when Energy Efficient Ethernet Enable (EEEEN) is cleared. **Note:** In order to meet the IEEE 802.3 specified requirement, the minimum value of this field should be 00001Eh.	R/W	00001Eh

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15.1.50 EEE TX LPI AUTOMATIC REMOVAL DELAY REGISTER (EEE_TX_LPI_AUTO_REMOVAL_DELAY)

Offset: 138h Size: 32 bits

Contains the count corresponding to the amount of time, in us, the MAC will wait after the TX LPI protocol is initiated until it automatically deasserts LPI in anticipation of a periodic transmission. TX LPI automatic removal functionality is enabled via the Energy Efficient Ethernet TX LPI Automatic Removal Enable (EEE_TX_LPI_AUTO_REMOVAL_EN) bit of the MAC Control Register (MAC_CR).

When this time period expires, the Energy Efficient Ethernet Stop TX Low Power Interrupt (EEE_STOP_TX_LPI_INT) bit of the Interrupt Status Register (INT_STS) and the Energy Efficient Ethernet TX Wake (EEE_TX_WAKE) bit of the Wakeup Control and Status Register 1 (WUCSR1) will be set.

Upon automatic TX LPI deassertion, the MAC will return to waiting for the TX FIFO to be empty, for the time specified in EEE TX LPI Request Delay Count (EEE_TX_LPI_REQUEST_DELAY_CNT) before requesting LPI once again.

Note: Due to a 1 us pre-scaler, the actually time can be up to 1us longer than specified.

The MAC will generate LPI requests only when the Energy Efficient Ethernet Enable (EEEEN) bit of the MAC Control Register (MAC_CR) is set, the current speed is 100 Mbps or 1000 Mbps, the current duplex is full and the auto-negotiation result indicates that both the local and partner device support EEE at the current operating speed.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	RESERVED	RO	-
23:0	**EEE TX LPI Automatic Removal Delay Count (EEE_TX_LPI_AUTO_REMOVAL_DELAY_CNT)** Count representing time to wait after the TX LPI protocol is initiated until it is automatically deasserted in anticipation of a periodic transmission. Units are in us. **Note:** Host software should only change this field when Energy Efficient Ethernet Enable (EEEEN) is cleared.	R/W	000000h

15.1.51 WAKEUP CONTROL AND STATUS REGISTER 1 (WUCSR1)

Offset: 140h Size: 32 bits

This register contains data pertaining to the MAC's remote wakeup status and capabilities.

All enables within this register must be clear during normal operation. Failure to do so will result in improper MAC receive operation.

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14	**RFE Wake Enable (RFE_WAKE_EN)** When set, remote wakeup mode is enabled and device is capable of generating a wakeup from a non-errored receive frame that passes the RFE's filters. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b
13	**Energy Efficient Ethernet TX Wake (EEE_TX_WAKE)** The MAC sets this bit upon the transmitter exiting the Low Power Idle state due to the expiration of the time specified in EEE TX LPI Request Delay Count Register (EEE_TX_LPI_REQUEST_DELAY_CNT). This bit will not set if Energy Efficient Ethernet TX Wake Enable (EEE_TX_WAKE_EN) is cleared. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low.	R/WC	0b
12	**Energy Efficient Ethernet TX Wake Enable (EEE_TX_WAKE_EN)** When set, remote wakeup is enabled upon the transmitter exiting the Low Power Idle state. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b
11	**Energy Efficient Ethernet RX Wake (EEE_RX_WAKE)** The MAC sets this bit upon the receiver exiting Low Power Idle state due to the reception of wake signaling. This bit will not set if Energy Efficient Ethernet RX Wake Enable (EEE_RX_WAKE_EN) is cleared. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low.	R/WC	0b
10	**Energy Efficient Ethernet RX Wake Enable (EEE_RX_WAKE_EN)** When set, remote wakeup is enabled upon reception of wake signaling. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b
9	**RFE Wakeup Frame Received (RFE_WAKE_FR)** This bit is set upon reception of a non-errored frame that passes the RFE filters. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/WC	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
8	**Store Wakeup Frame (STORE_WAKE)** When set, the frame associated with a wake event is stored in the FCT RX FIFO. All subsequents frames received after the wake event which are not corrupted and pass any applicable frame filters in the MAC and RFE are stored in the FIFO. When cleared, only frames received after the wake event are stored in the RX FIFO. The frames must not be corrupted and pass any applicable frame filters in the MAC and RFE. **Note:** It is possible that the wakeup source was not a frame. In that case all subsequent received frames are stored in the FIFO. **Note:** This bit only has meaning when SUSPEND3 is used. For other suspend modes this bit shall have no affect.	R/W	0b
7	**Perfect DA Frame Received (PFDA_FR)** The MAC sets this bit upon receiving a valid frame with a destination address that matches the physical address. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/WC	0b
6	**Remote Wakeup Frame Received (WUFR)** The MAC sets this bit upon receiving a valid remote Wakeup Frame. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/WC	0b
5	**Magic Packet Received (MPR)** The MAC sets this bit upon receiving a valid Magic Packet. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/WC	0b
4	**Broadcast Frame Received (BCAST_FR)** The MAC Sets this bit upon receiving a valid broadcast frame. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/WC	0b
3	**Perfect DA Wakeup Enable (PFDA_EN)** When set, remote wakeup mode is enabled and the MAC is capable of waking up on receipt of a frame with a destination address that matches the physical address of the device. The physical address is stored in the MAC Receive Address High Register (RX_ADDRH) and MAC Receiver Address Low Register (RX_ADDRL). This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b
2	**Wakeup Frame Enable (WUEN)** When set, remote wakeup mode is enabled and the MAC is capable of detecting Wakeup Frames as programmed in the Wakeup Frame Filter. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b
1	**Magic Packet Enable (MPEN)** When set, Magic Packet wakeup mode is enabled. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
0	**Broadcast Wakeup Enable (BCAST_EN)** When set, remote wakeup mode is enabled and the MAC is capable of waking up from a broadcast frame. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b

15.1.52 WAKEUP SOURCE REGISTER (WK_SRC)

Offset: 144h Size: 32 bits

This register indicates the source of the wakeup event that resulted in the device issuing wakeup signaling. Any wake events that occurred while the device was being placed into the SUSPENDx state are ignored. Additionally, any wake events that occur after the device has commenced the process of waking up are likewise ignored.

It is possible for a received wakeup packet to match several of the conditions listed in this CSR. In that case all matching bits for that packet shall be set.

The status fields in this CSR are not cleared until explicitly done so by SW.

BITS	DESCRIPTION	TYPE	DEFAULT
31:20	**GPIO [11:0] (GPIOx_INT_WK)** These bits assert from a GPIO wake event that results in the device issuing wakeup signaling.	R/WAC	000h
19:17	**RESERVED**	RO	-
16	**IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD_WK)** The MAC sets this bit upon receiving a valid IPv6 TCP SYN packet that results in the device issuing wakeup signaling.	R/WAC	0b
15	**IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD_WK)** The MAC sets this bit upon receiving a valid IPv4 TCP SYN packet that results in the device issuing wakeup signaling.	R/WAC	0b
14	**Energy Efficient Ethernet TX Wake (EEE_TX_WK)** The MAC sets this bit upon the transmitter exiting the Low Power Idle state due to the expiration of the time specified in EEE TX LPI Request Delay Count Register (EEE_TX_LPI_REQUEST_DELAY_CNT). This bit will not set if Energy Efficient Ethernet TX Wake Enable (EEE_TX_WAKE_EN) is cleared. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low.	R/WAC	0b
13	**Energy Efficient Ethernet RX Wake (EEE_RX_WK)** The MAC sets this bit upon the receiver exiting Low Power Idle state due to the reception of wake signaling. This bit will not set if Energy Efficient Ethernet RX Wake Enable (EEE_RX_WAKE_EN) is cleared. This bit is held low if the Energy Efficient Ethernet Enable (EEEEN) bit in the MAC Control Register (MAC_CR) is low.	R/WAC	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
12	**RFE Wakeup Frame Received (RFE_FR_WK)** This bit is set bit upon reception of a non-errored frame that passes the RFE's filters and results in the device issuing wakeup signaling.	R/WAC	0b
11	**Perfect DA Frame Received (PFDA_FR_WK)** The MAC sets this bit upon receiving a valid frame with a destination address that matches the physical address that results in the device issuing wakeup signaling.	R/WAC	0b
10	**Magic Packet Received (MP_FR_WK)** The MAC sets this bit upon receiving a valid Magic Packet that results in the device issuing wakeup signaling.	R/WAC	0b
9	**Broadcast Frame Received (BCAST_FR_WK)** The MAC Sets this bit upon receiving a valid broadcast frame that results in the device issuing wakeup signaling.	R/WAC	0b
8	**Remote Wakeup Frame Received (WU_FR_WK)** The MAC sets this bit upon receiving a valid remote Wakeup Frame that results in the device issuing wakeup signaling.	R/WAC	0b
7:5	**RESERVED**	RO	-
4:0	**Remote Wakeup Frame Match (WUFF_MATCH)** This field indicates which wakeup frame filter caused the wake up event. The contents of this field are only valid when Remote Wakeup Frame Received (WU_FR_WK) is set.	R/WAC	0b

15.1.53 WAKEUP FILTER *X* CONFIGURATION REGISTER (WUF_CFG*X*)

Offset: 150h - 1CCh Size: 32 bits

These CSRs enable the respective wakeup filter to be enabled. A total of 32 programmable filters are available in this device where each filter can match a pattern up to 128 bytes in length.

Note: WUF_CFG0 supports Reset Protection (RST_PROTECT).

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Filter Enable** 0b: Filter disabled 1b: Filter enabled	R/W	0b Note 15-55
30:26	**RESERVED**	RO	-
25:24	**Filter Address Type** Defines the destination address type of the pattern (as specified for filter *x* in the Wakeup Filter x Byte Mask Registers (WUF_MASKx) block). 00b: Pattern applies only to unicast frames. 10b: Pattern applies only to multicast frames. X1b: Pattern applies to all frames.	R/W	00b Note 15-55
23:16	**Filter Pattern Offset** Specifies the offset of the first byte in the frame on which CRC checking begins for Wakeup Frame recognition. Offset 0 is the first byte of the incoming frame's destination address.	R/W	00h Note 15-55
15:0	**Filter CRC-16** Specifies the expected 16-bit CRC value for the filter that should be obtained by using the pattern offset and the byte mask programmed for the filter. This value is compared against the CRC calculated on the incoming frame, and a match indicates the reception of a Wakeup Frame.	R/W	0000h Note 15-55

Note 15-55 The default value for Wakeup Filter 0 is loaded from EEPROM, see Table 10-2, “EEPROM Format,” on page 103. If no EEPROM is present, or if this information is not configured, then the default depends on the OTP programmed value. It the OTP is not programmed then 0h is the default. A USB Reset or Lite Reset (LRST) shall cause this field to be restored to the image value last loaded from EEPROM, OTP, or to be set to 0h if neither is available.

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15.1.54 WAKEUP FILTER *X* BYTE MASK REGISTERS (WUF_MASK*X*)

Offset: 200h - 3FCh Size: 128 bits

Each of the 32 wakeup filters has a 128-bit byte mask. The 128-bit mask is accessed via 4 consecutive byte mask (DWORD) registers. The DWORD offset required to access a particular portion of the mask is indicated in the following table. The start offset of the least significant DWORD register for each 128-bit filter block is the first element in the range indicated in the preceding table and in the register map, Table 15-2, “System Control and Status Registers Map,” on page 139.

If bit j of the byte mask is set, the CRC machine processes byte *pattern offset + j* of the incoming frame. Otherwise, byte *pattern offset + j* is ignored.

Note: WUF_MASK0 supports Reset Protection (RST_PROTECT).

DWORD OFFSET	BITS	DESCRIPTION	TYPE	DEFAULT
00h	31:0	**Filter *x* Byte Mask [31:0]**	R/W	0h Note 15-55
01h	31:0	**Filter *x* Byte Mask [63:32]**	R/W	0h Note 15-55
02h	31:0	**Filter *x* Byte Mask [95:64]**	R/W	0h Note 15-55
03h	31:0	**Filter *x* Byte Mask [127:96]**	R/W	0h Note 15-55

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15.1.55 MAC ADDRESS PERFECT FILTER REGISTERS (ADDR_FILT*X*)

Offset: 400h - 504h Size: 32 bits

These registers specify the MAC addresses used for perfect filtering.

It is permissible to change the value of an entry at run time. However, the address valid bit must be cleared before doing so. Otherwise an invalid value will temporarily be in the MAC address filter.

Note: The MAC address storage scheme matches that for the RX_ADDRH and RX_ADDRL registers, see Table 15-4, "RX_ADDRL, RX_ADDRH Byte Ordering".

DWORD OFFSET	BITS	DESCRIPTION	TYPE	DEFAULT
0h	31	**Address Valid** When set, this bit indicates that the entry has valid data and is used in the perfect filtering.	R/W	0h
0h	30	**Address Type** When set, this bit indicates the address represents the MAC source address. Otherwise this entry applies to the MAC destination address.	R/W	0h
0h	29:16	**RESERVED**	RO	-
0h	15-0	**Physical Address [47:32]** This field contains the upper 16 bits [47:32] of the physical address of the device.	R/W	0h
1h	31:0	**Physical Address [31:0]** This field contains the lower 32 bits [31:0] of the physical address of the device.	R/W	0h

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15.1.56 WAKEUP CONTROL AND STATUS REGISTER 2 (WUCSR2)

Offset: 600h Size: 32 bits

This register contains data pertaining to Windows 7 Power Management wake and off-load features.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Checksum Disable (CSUM_DISABLE)** When clear, the IP header checksum, TCP checksum, and FCS are calculated and all must agree with the frame contents, in order for the frame (ARP, TCP_SYN, or NS) to be considered for detection analysis. When set, only the FCS is calculated and checked for ARP, TCP_SYN, and NS frames. The IP header checksum, ICMP payload checksum, and TCP checksum are not calculated, hence any mismatches are ignored.	R/W	0b
30:11	**RESERVED**	RO	-
10	**Forward ARP Frames (FARP_FR)** Enables passing received ARP frames that target this device and were processed by the ARP offload logic to the RX datapath interface. 0 = Sink received ARP frames. 1 = Pass received ARP frames to the RX datapath interface.	R/W	0b
9	**Forward NS Frames (FNS_FR)** Enables passing received NS frames that target this device and were processed by the NS offload logic to the RX datapath interface. 0 = Sink received NS frames. 1 = Pass received NS frames to the RX datapath interface.	R/W	0b
8	**NA SA Select (NA_SA_SEL)** Used to select source for IPv6 SA in NA message. When set, NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST) value is used as the source. When cleared, the Target Address in NS packet is used.	R/W	0b
7	**NS Packet Received (NS_RCD)** The MAC sets this bit upon receiving a valid NS packet.	R/WC	0b
6	**ARP Packet Received (ARP_RCD)** The MAC sets this bit upon receiving a valid ARP packet.	R/WC	0b
5	**IPv6 TCP SYN Packet Received (IPV6_TCPSYN_RCD)** The MAC sets this bit upon receiving a valid IPv6 TCP SYN packet. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/WC	0b
4	**IPv4 TCP SYN Packet Received (IPV4_TCPSYN_RCD)** The MAC sets this bit upon receiving a valid IPv4 TCP SYN packet. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Status (RES_CLR_WKP_STS) is set.	R/WC	0b
3	**NS Offload Enable (NS_OFFLOAD_EN)** When set, enables the response to Neighbor Solicitation packets.	R/W	0b
2	**ARP Offload Enable (ARP_OFFLOAD_EN)** When set, enables the response to ARP packets.	R/W	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
1	**IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN)** When set, enables the wakeup on receiving an IPv6 TCP SYN packet. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set. **Note this is only a documentation change.**	R/W	0b
0	**IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN)** When set, enables the wakeup on receiving an IPv4 TCP SYN packet. This bit is automatically cleared at the completion of a resume sequence if Resume Clears Remote Wakeup Enables (RES_CLR_WKP_EN) is set.	R/W	0b

15.1.57 NS*X* IPV6 DESTINATION ADDRESS REGISTER (NS*X*_IPV6_ADDR_DEST)

Offset: 610h - 61Ch, 650h - 65Ch Size: 32 bits

Used in IPv6 NS header matching, each IPv6 destination address is 128-bits. The 128-bit address is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for each 128-bit address block is the first element in the range indicated in the preceding table and in the register map, Table 15-2, “System Control and Status Registers Map,” on page 139.

These registers are used when NS Offload Enable (NS_OFFLOAD_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). Received packets whose Ethernet destination address is the device’s MAC address, a multi-cast address, or the broadcast address are processed as follows:

The headers of all IPv6 packets are checked to determine whether (for 0<=x<=1) NSx IPv6 Destination Address Register (NSx_IPV6_ADDR_DEST) matches the destination address specified in the IPv6 header. In the event that the IPv6 header destination address is a solicited node multicast address (i.e. it has a prefix that matches FF02::1:FF00:0/104), only the upper three bytes (NSx_IPv6_ADDR_DEST_3 [127:104]) are compared against the last 24 bits of the IPv6 header destination address.

Please refer to Section 8.5, "Neighbor Solicitation (NS) Offload," on page 82 for further information.

DWORD OFFSET	BITS	DESCRIPTION	TYPE	DEFAULT
00h	31:0	**NS*x*_IPv6_ADDR_DEST_0 [31:0]**	R/W	0000_0000h
01h	31:0	**NS*x*_IPv6_ADDR_DEST_1 [63:32]**	R/W	0000_0000h
02h	31:0	**NS*x*_IPv6_ADDR_DEST_2 [95:64]**	R/W	0000_0000h
03h	31:0	**NS*x*_IPv6_ADDR_DEST_3 [127:96]**	R/W	0000_0000h

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 15-5, "IPv6 Address Transmission Byte Ordering".

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TABLE 15-5: IPV6 ADDRESS TRANSMISSION BYTE ORDERING

NSx_IPV6_ADDR_DEST_x	IPv6 Address	Order of Reception on Ethernet
NSx_IPv6_ADDR_DEST_3[31:24]	[127:120]	1st
NSx_IPv6_ADDR_DEST_3[23:16]	[119:112]	2nd
NSx_IPv6_ADDR_DEST_3[15:8]	[111:104]	3rd
NSx_IPv6_ADDR_DEST_3[7:0]	[103:96]	4th
NSx_IPv6_ADDR_DEST_2[31:24]	[95:88]	5th
NSx_IPv6_ADDR_DEST_2[23:16]	[87:80]	6th
NSx_IPv6_ADDR_DEST_2[15:8]	[79:72]	7th
NSx_IPv6_ADDR_DEST_2[7:0]	[71:64]	8th
NSx_IPv6_ADDR_DEST_1[31:24]	[63:56]	9th
NSx_IPv6_ADDR_DEST_1[23:16]	[55:48]	10th
NSx_IPv6_ADDR_DEST_1[15:8]	[47:40]	11th
NSx_IPv6_ADDR_DEST_1[7:0]	[39:32]	12th
NSx_IPv6_ADDR_DEST_0[31:24]	[31:24]	13th
NSx_IPv6_ADDR_DEST_0[23:16]	[23:16]	14th
NSx_IPv6_ADDR_DEST_0[15:8]	[15:8]	15th
NSx_IPv6_ADDR_DEST_0[7:0]	[7:0]	16th

Note: This example applies to all other IPv6 address CSRs.

15.1.58 NS*X* IPV6 SOURCE ADDRESS REGISTER (NS*X*_IPV6_ADDR_SRC)

Offset:	620h - 62Ch, 660h - 66Ch	Size:	32 bits

Used in IPv6 NS header matching, each IPv6 source address is 128-bits. The 128-bit address is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for each 128-bit address block is the first element in the range indicated in the preceding table and in the register map, Table 15-2, “System Control and Status Registers Map,” on page 139.

These registers are used when NS Offload Enable (NS_OFFLOAD_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2). Received packets whose destination address is the device’s MAC address, a multi-cast address, or the broadcast address are processed as follows:

The headers of all IPv6 packets are checked to determine whether (for 0<=x<=1) NSx IPv6 Source Address Register (NSx_IPV6_ADDR_SRC) matches the source address specified in the IPv6 header.

Please refer to Section 8.5, "Neighbor Solicitation (NS) Offload," on page 82 for further information.

Note: A value of all 0’s in all 4 DWORD registers equates to a wild-card, causes checking to be ignored, and yields a match.

DWORD OFFSET	BITS	DESCRIPTION	TYPE	DEFAULT
00h	31:0	**NS*x*_IPv6_ADDR_SRC_0 [31:0]**	R/W	0000_0000h
01h	31:0	**NS*x*_IPv6_ADDR_SRC_1 [63:32]**	R/W	0000_0000h
02h	31:0	**NS*x*_IPv6_ADDR_SRC_2 [95:64]**	R/W	0000_0000h
03h	31:0	**NS*x*_IPv6_ADDR_SRC_3 [127:96]**	R/W	0000_0000h

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 15-5, "IPv6 Address Transmission Byte Ordering".

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15.1.59 NS*X* ICMPV6 ADDRESS 0 REGISTER (NS*X*_ICMPV6_ADDR0)

Offset:	630h - 63Ch, 670h - 67Ch	Size:	32 bits

Used in ICMPv6 NS target address matching. Each address is 128-bits and is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for each 128-bit address block is the first element in the range indicated in the preceding table and in the register map, Table 15-2, “System Control and Status Registers Map,” on page 139.

NS offload is enabled in the Wakeup Control and Status Register 2 (WUCSR2).

The target address specified in the NS request is compared to the values contained in the NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0) (these registers) and the corresponding NSx ICMPv6 Address 1 Register (NSx_ICMPV6_ADDR1), for all x where a match previously occurred in the IPv6 header. Please refer to Section 8.5, "Neighbor Solicitation (NS) Offload," on page 82 for further information.

Note: A value of all 0’s in all 4 DWORD registers disables the comparison with this field. No match is yielded.

DWORD OFFSET	BITS	DESCRIPTION	TYPE	DEFAULT
00h	31:0	**NS*x*_ICMPV6_ADDR0_0 [31:0]**	R/W	0000_0000h
01h	31:0	**NS*x*_ICMPV6_ADDR0_1 [63:32]**	R/W	0000_0000h
02h	31:0	**NS*x*_ICMPV6_ADDR0_2 [95:64]**	R/W	0000_0000h
03h	31:0	**NS*x*_ICMPV6_ADDR0_3 [127:96]**	R/W	0000_0000h

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 15-5, "IPv6 Address Transmission Byte Ordering".

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15.1.60 NS*X* ICMPV6 ADDRESS 1 REGISTER (NS*X*_ICMPV6_ADDR1)

Offset: 640h - 64Ch, 680h - 68Ch Size: 32 bits

See NSx ICMPv6 Address 0 Register (NSx_ICMPV6_ADDR0) for a description of the usage of this register.

Please refer to Section 8.5, "Neighbor Solicitation (NS) Offload," on page 82 for further information.

Note: A value of all 0's in all 4 DWORD registers disables the comparison with this field. No match is yielded.

DWORD OFFSET	BITS	DESCRIPTION	TYPE	DEFAULT
00h	31:0	**NS*x*_ICMPV6_ADDR1_0 [31:0]**	R/W	0000_0000h
01h	31:0	**NS*x*_ICMPV6_ADDR1_1 [63:32]**	R/W	0000_0000h
02h	31:0	**NS*x*_ICMPV6_ADDR1_2 [95:64]**	R/W	0000_0000h
03h	31:0	**NS*x*_ICMPV6_ADDR1_3 [127:96]**	R/W	0000_0000h

The ordering for transmission of an IPv6 address over Ethernet is illustrated in Table 15-5, "IPv6 Address Transmission Byte Ordering".

15.1.61 SYN IPV4 SOURCE ADDRESS REGISTER (SYN_IPV4_ADDR_SRC)

Offset: 690h Size: 32 bits

This register is utilized when IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2) and the device is in the SUSPEND0 or SUSPEND3 state. It holds the source address to be compared to that of received IPv4 headers prefixing TCP packets whose SYN bit is asserted.

IPv4 frames whose destination address is the device's MAC address, a multi-cast address, or the broadcast address are processed as follows:

A check is made for a TCP protocol match within the IPv4 header. Valid TCP packets whose SYN bit is asserted, having an IPv4 header whose source address and destination address match those specified in the SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC) and the SYN IPv4 Destination Address Register (SYN_IPV4_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv4 TCP Ports Register (SYN-_IPV4_TCP_PORTS), will cause a wakeup.

Please refer to Section 8.3.3.1, "IPv4 TCP SYN Detection," on page 80 for further information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**SYN IPv4 Source Address [31:0]** Used in IPv4 header matching for TCP SYN packets. **Note:** A value of all 0's equates to a wild-card, causes checking to be ignored, and yields a match.	R/W	0000_0000h

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The ordering for transmission of anIPv4 address over Ethernet is illustrated in Table 15-6, "IPv4 Address Transmission Byte Ordering".

TABLE 15-6: IPV4 ADDRESS TRANSMISSION BYTE ORDERING

SYN_IPV4_ADDR_SRC	IPv4 Address	Order of Reception on Ethernet
SYN_IPV4_ADDR_SRC[31:24]	[31:24]	1st
SYN_IPV4_ADDR_SRC[23:16]	[23:16]	2nd
SYN_IPV4_ADDR_SRC[15:8]	[15:8]	3rd
SYN_IPV4_ADDR_SRC[7:0]	[7:0]	4th

This example applies to all other IPv4 address CSRs.

15.1.62 SYN IPV4 DESTINATION ADDRESS REGISTER (SYN_IPV4_ADDR_DEST)

Offset: 694h Size: 32 bits

This register is utilized when IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2) and the device is in the SUSPEND0 or SUPSEND3 state. It holds the destination address to be compared to that of received IPv4 headers prefixing TCP packets whose SYN bit is asserted.

IPv4 frames whose destination address is the device's MAC address, a multi-cast address, or the broadcast address are processed as follows:

A check is made for a TCP protocol match within the IPv4 header. Valid TCP packets whose SYN bit is asserted, having an IPv4 header whose source address and destination address match those specified in the SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC) and the SYN IPv4 Destination Address Register (SYN_IPV4_ADDR_DEST), and whose source port and destination port match those specified by SYN IPv4 TCP Ports Register (SYN-_IPV4_TCP_PORTS), will cause a wakeup.

Please refer to Section 8.3.3.1, "IPv4 TCP SYN Detection," on page 80 for further information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**SYN IPv4 Destination Address [31:0]** Used in IPv4 heading matching for TCP SYN packets. **Note:** A value of all 0's equates to a wild-card, causes checking to be ignored, and yields a match.	R/W	0000_0000h

The ordering for transmission of anIPv4 address over Ethernet is illustrated in Table 15-6, "IPv4 Address Transmission Byte Ordering".

15.1.63 SYN IPV4 TCP PORTS REGISTER (SYN_IPV4_TCP_PORTS)

Offset: 698h Size: 32 bits

This register is utilized when IPv4 TCP SYN Wake Enable (IPV4_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2) and the device is in the SUSPEND0 or SUPSEND3 state. It holds the source and destination ports to be compared to that of received TCP packets whose SYN bit is asserted that are prefixed by a IPv4 header.

IPv4 frames whose destination address is the device's MAC address, a multi-cast address, or the broadcast address are processed as follows:

A check is made for a TCP protocol match within the IPv4 header. Valid TCP packets whose SYN bit is asserted, having an IPv4 header whose source address and destination address match those specified in the SYN IPv4 Source Address Register (SYN_IPV4_ADDR_SRC) and the SYN IPv4 Destination Address Register (SYN_IPV4_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv4 TCP Ports Register (SYN-_IPV4_TCP_PORTS), will cause a wakeup.

Please refer to Section 8.3.3.1, "IPv4 TCP SYN Detection," on page 80 for further information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Destination Port (IPV4_DEST_PORT)** Used in IPv4 TCP port matching for TCP SYN packets. **Note:** A value of all 0's equates to a wild-card, causes checking to be ignored, and yields a match.	R/W	0000h
15:0	**Source Port (IPV4_SRC_PORT)** Used in IPv4 TCP port matching for TCP SYN packets. **Note:** A value of all 0's equates to a wild-card, causes checking to be ignored, and yields a match.	R/W	0000h

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15.1.64 SYN IPV6 SOURCE ADDRESS REGISTER (SYN_IPV6_ADDR_SRC)

Offset: 69Ch - 6A8h Size: 32 bits

This register is used in IPv6 header matching for TCP SYN packets and is 128-bits. The address is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for the 128-bit address block is the first element in the range indicated in the preceding table and in the register map, Table 15-2, “System Control and Status Registers Map,” on page 139.

This register is utilized when IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2) and the device is in the SUSPEND0 state. It holds the source address to be compared to that of the IPv6 header (or an extension header) prefixing a TCP packet whose SYN bit is asserted. The IPv6 frame must have previously passed a check to ensure that its destination address is the device’s MAC address, a multi-cast address, or the broadcast address.

Valid TCP packets whose SYN bit is asserted, having an IPv6 header whose source address and destination address match those specified by the SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC) and the SYN IPv6 Destination Address Register (SYN_IPV6_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS), will cause a wakeup.

Please refer to Section 8.3.4, "IPv6 TCP SYN Detection," on page 81 for further information.

Note:	A value of all 0’s in all 4 DWORD registers equates to a wild-card, causes checking to be ignored, and yields a match.

DWORD OFFSET	BITS	DESCRIPTION	TYPE	DEFAULT
00h	31:0	**SYN_IPV6_ADDR_SRC_0 [31:0]**	R/W	0000_0000h
01h	31:0	**SYN_IPV6_ADDR_SRC_1 [63:32]**	R/W	0000_0000h
02h	31:0	**SYN_IPV6_ADDR_SRC_2 [95:64]**	R/W	0000_0000h
03h	31:0	**SYN_IPV6_ADDR_SRC_3 [127:96]**	R/W	0000_0000h

The ordering for transmission of the IPv6 address over Ethernet is illustrated in Table 15-5, "IPv6 Address Transmission Byte Ordering".

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15.1.65 SYN IPV6 DESTINATION ADDRESS REGISTER (SYN_IPV6_ADDR_DEST)

Offset: 6ACh - 6B8h Size: 32 bits

This register is used in IPv6 header matching for TCP SYN packets and is 128-bits. The address is accessed via 4 consecutive (DWORD) registers. The DWORD offset required to access a particular portion of the address is indicated in the following table. The start offset of the least significant DWORD register for the 128-bit address block is the first element in the range indicated in the preceding table and in the register map, Table 15-2, “System Control and Status Registers Map,” on page 139.

This register is utilized when IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2) and the device is in the SUSPEND0 or SUSPEND3 state. It holds the destination address to be compared to that of the IPv6 header (or an extension header) prefixing a TCP packet whose SYN bit is asserted. The IPv6 frame must have previously passed a check to ensure that its destination address is the device’s MAC address, a multi-cast address, or the broadcast address.

Valid TCP packets whose SYN bit is asserted, having an IPv6 header whose source address and destination address match those specified by the SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC) and the SYN IPv6 Destination Address Register (SYN_IPV6_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS), will cause a wakeup.

Please refer to Section 8.3.4, "IPv6 TCP SYN Detection," on page 81 for further information.

Note: A value of all 0’s in all 4 DWORD registers equates to a wild-card, causes checking to be ignored, and yields a match.

DWORD OFFSET	BITS	DESCRIPTION	TYPE	DEFAULT
00h	31:0	**SYN_IPV6_ADDR_DEST_0 [31:0]**	R/W	0000_0000h
01h	31:0	**SYN_IPV6_ADDR_DEST_1 [63:32]**	R/W	0000_0000h
02h	31:0	**SYN_IPV6_ADDR_DEST_2 [95:64]**	R/W	0000_0000h
03h	31:0	**SYN_IPV6_ADDR_DEST_3 [127:96]**	R/W	0000_0000h

The ordering for transmission of the IPv6 address over Ethernet is illustrated in Table 15-5, "IPv6 Address Transmission Byte Ordering".

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15.1.66 SYN IPV6 TCP PORTS REGISTER (SYN_IPV6_TCP_PORTS)

Offset: 6BCh Size: 32 bits

This register is utilized when IPv6 TCP SYN Wake Enable (IPV6_TCPSYN_WAKE_EN) is set in the Wakeup Control and Status Register 2 (WUCSR2) and the device is in the SUSPEND0 state. It holds the source and destination ports to be compared to that of received TCP packets whose SYN bit is asserted that are prefixed by a IPv6 header or extension header.

IPv6 frames whose destination address is the device's MAC address, a multi-cast address, or the broadcast address are processed as follows:

A check is made for a TCP protocol match within the IPv6 header. Valid TCP packets whose SYN bit is asserted, having an IPv6 header whose source address and destination address match those specified in the SYN IPv6 Source Address Register (SYN_IPV6_ADDR_SRC) and the SYN IPv6 Destination Address Register (SYN_IPV6_ADDR_DEST), and whose source port and destination port match those specified by the SYN IPv6 TCP Ports Register (SYN_IPV6_TCP_PORTS), will cause a wakeup.

Please refer to Section 8.3.4, "IPv6 TCP SYN Detection," on page 81 for further information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Destination Port (IPV6_DEST_PORT)** Used in IPv6 TCP port matching for TCP SYN packets. **Note:** A value of all 0's equates to a wild-card, causes checking to be ignored, and yields a match.	R/W	0000h
15:0	**Source Port (IPV6_SRC_PORT)** Used in IPv6 TCP port matching for TCP SYN packets. **Note:** A value of all 0's equates to a wild-card, causes checking to be ignored, and yields a match.	R/W	0000h

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15.1.67 ARP SENDER PROTOCOL ADDRESS REGISTER (ARP_SPA)

Offset: 6C0h Size: 32 bits

This register is utilized when ARP offload is enabled in the Wakeup Control and Status Register 2 (WUCSR2). The frame type for all received Ethernet frames is examined and those of type 0806h (ARP frames) are checked to ensure that the MAC destination address matches the device's MAC address or is the broadcast address. If the packet passes these tests, the contents of this register is compared to the SPA field of the ARP message and the contents of the ARP Target Protocol Address Register (ARP_TPA) is compared to the TPA field of the ARP message. If the contents of both registers match the contents of the message and no errors occurred on the frame, then the MAC TX is signaled to transmit an ARP response frame to the sender.

Please refer to Section 8.6, "ARP Offload," on page 84 for further information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**ARP_SPA [31:0]** Used in ARP matching. **Note:** A value of all 0's = wild-card, causes checking to be ignored, and yields a match.	R/W	0000h

Note: Note: The ordering for transmission of anIPv4 address over Ethernet is illustrated in Table 15-6, "IPv4 Address Transmission Byte Ordering".

15.1.68 ARP TARGET PROTOCOL ADDRESS REGISTER (ARP_TPA)

Offset: 6C4h Size: 32 bits

This register is utilized when ARP offload is enabled in the Wakeup Control and Status Register 2 (WUCSR2). The frame type for all received Ethernet frames is examined and those of type 0806h (ARP frames) are checked to ensure that the MAC destination address matches the device's MAC address or is the broadcast address. If the packet passes these tests, the contents of the ARP Sender Protocol Address Register (ARP_SPA) is compared to the SPA field of the ARP message and the contents of the this register is compared to the TPA field of the ARP message. If the contents of both registers match the contents of the message and no errors occurred on the frame, then the MAC TX is signaled to transmit an ARP response frame to the sender.

Please refer to Section 8.6, "ARP Offload," on page 84 for further information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**ARP_TPA [31:0]** Used in ARP matching. **Note:** A value of all 0's = wild-card, causes checking to be ignored, and yields a match.	R/W	0000h

Note: Note: The ordering for transmission of anIPv4 address over Ethernet is illustrated in Table 15-6, "IPv4 Address Transmission Byte Ordering".

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15.1.69 PHY DEVICE IDENTIFIER (PHY_DEV_ID)

Offset: 700h Size: 32 bits

This register defines the integrated Ethernet PHY's OUI, Model Number, and Device Revision Number.

BITS	DESCRIPTION	TYPE	DEFAULT
31:28	**Revision Number**	RO	0h
27:22	**Model Number**	RO	13h
21:0	**OUI** Organizationally-Unique Identifier. Assigned to the 3rd through 24th bit of the OUI.	RO	00_01F0h

15.2 USB PHY Control and Status Registers

Note:	**RESERVED address space in the USB PHY Control and Status Registers Map must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.**

TABLE 15-7: USB PHY CONTROL AND STATUS REGISTERS MAP

OFFSET (1200h+offset)	REGISTER NAME
000h	Common Block Test Register (COM_TEST)
004h – 0C0h	Reserved
0C4h	USB 2.0 AFE Test Register (USB2_TEST)
0C8h	USB 2.0 AFE Upstream Control Register (USB2_AFE_CTRL)
0CCh – 13Ch	Reserved
140h	HSIC Enable Register (HSIC_EN)

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15.2.1 COMMON BLOCK TEST REGISTER (COM_TEST)

Offset: 000h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Clock Disable (CLOCK_DISABLE)** When set, the clocks to the common block register will be gated off.	R/W	0b
30:25	**RESERVED**	RO	-
24	**Common Block Test Register Select (COM_BLK_SEL)** Common Block Test register select. 0: Passes functional signals to the Common block 1: Passes test signals to the Common block	R/W	0b
23	**Common XTAL Gain Select (COM_TST_XTAL_GAIN)** 0: XTAL drive amplitude limited to 0.9V 1: XTAL drive amplitude increased to 1V	R/W	0b
22:20	**RESERVED**	RO	-
19	**Input Reference Frequency Select for all PLLs (COM_REF_FREQ)** 0: 25 MHz - POR 1: 24 MHz **Note:** Gigabit Ethernet PHY requires 25 MHz. 24 MHz is not a valid operational setting.	R/W	0b
18	**1.2V POR (COM_V12CR_RDY)** POR output from the core 1.2V supply. Active high when core supply is above 0.85V. Signal is gated off by internal 3V POR signal (active high threshold of 2.7V).	RO	0b
17	**Enable Link Power Management Mode (COM_PLL_LPM_MODE)** Enables fast startup of the USB2 PLL.	R/W	Note 15-56
16	**Enable USB 2.0 PLL (COM_PLL_EN)**	R/W	1b
15	**Common Suspend (COM_SUSPENDB)** Powers down the common circuitry (Biasing and PLL). When asserted, this signal overrides all local UTMI suspend signals and will power down all AFE blocks connected to it. This signal is active low.	R/W	0b
14	**XTAL Suspend (COM_XTAL_SUSPENDB)** When asserted, this signal will power down the XTAL block. The XTAL clock can be kept running when **SUSPEND_N** is asserted for LPM. This signal is active low.	R/W	0b
13	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
12	**PLL Clock Usable (COM_CLK_USABLE)** 0: Clocks not usable 1: Clocks are usable	RO	0b
11:10	**RESERVED**	RO	-
9	**AFE_RDY_TIM_DIS** When set disables the AFE ready timer.	R/W	0b
8:1	**RESERVED**	RO	-
0	**Clock gate bypass mode select (PHY_CLK_GATE_BYPASS)** 0: Functional mode. 1: Forcibly puts all clock gating logic in the chip in bypass mode.	R/W	0b

Note 15-56 The default value of this field is determined by the Enable Link Power Management Mode (COM_PLL_LPM_MODE) bit in of Configuration Flags 0 within the EEPROM, if present. The field chosen depends on whether the device is in HS or FS mode. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0b if neither is present.

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15.2.2 USB 2.0 AFE TEST REGISTER (USB2_TEST)

Offset: 0C4h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:23	**RESERVED**	RO	-
22	**FS/LS Driver Output Enable (USB2_FS_OEB)** Active low. 0: Driver enabled 1: Driver tri-stated	R/W	0b
21	**FS/LS Positive Output Data (USB2_FS_VPO)** Drives data to the DP output.	R/W	0b
20	**FS/LS Negative Output Data (USB2_FS_VMO)** Drives data to the DM output	R/W	0b
19	**FS/LS Differential Receiver Output (USB2_FS_DATA)**	RO	0b
18:16	**RESERVED**	RO	-
15:14	**HS Transmit Valid Mask (USB2_HS_TXVALID)** Indicates which bits of the AFE_HS_TXVALID[1:0] bus is valid. 00: No bits valid 01: LSB valid 10: Invalid combination 11: Both bits valid	R/W	00b
13:12	**HS Transmit Data (USB2_HS_TXDATA)** Driver data is transmitted LSB first.	R/W	00b
11	**HS Current Source Enable (USB2_HS_CS_EN)** 0: Driver powered-down 1: Driver powered-up This signal will be asserted active whenever the port is in Hi-Speed mode.	R/W	0b
10:8	**HS Output Current (PHY_BOOST)** 000b: Nominal 17.78mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-57
7	**Rpu DP Termination Control (USB2_RPU_DP_EN)** Enable the 1.5 Kohm termination on DP when active.	R/W	0b

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BITS	DESCRIPTION	TYPE	DEFAULT
6	**Rpu DP Termination Control (USB2_RPU_DM_EN)** Enable the 1.5 Kohm termination on DP when active.	R/W	0b
5	**Rpd DP Termination Control (USB2_RPD_DP_EN)** Enable the 15 Kohm termination on DP when active.	R/W	0b
4	**Rpd DM Termination Control (USB2_RPD_DM_EN)** Enable the 15 Kohm termination on DM when active.	R/W	0b
3:2	**RESERVED**	RO	-
1	**HS Driver Active (USB2_HS_TXACTIVE)** Places the HS driver in low power mode when disabled (during IDLE). 0: Driver in low-power mode 1: Driver in active transmit mode (17.78 mA source active)	R/W	0b
0	**RESERVED**	RO	-

Note 15-57 The default value of this field is determined by the value of the PHY Boost (CFG0_PHY_BOOST) field in Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then default depends on the OTP programmed value. It the OTP is not programmed then 000b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or to be set to 000b if no EEPROM is present.

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15.2.3 USB 2.0 AFE UPSTREAM CONTROL REGISTER (USB2_AFE_CTRL)

Offset: 0C8h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:30	**RESERVED**	RO	-
29	**HS Termination Control (USB2_HS_TERM_EN)** Enable the 45 Kohm termination on DP and DM when active.	R/W	0b
28	**AFE High Speed Squelch (USB2_HS_SQUELCH_B)** Indicates when the HS oversampled data is valid. Active low. 0: Data valid 1: Data is invalid	RO	0b
27	**AFE High Speed Disconnect (USB2_HS_DISC)** Indicates when the line is disconnected in HS mode. This signal should only be strobed during HS EOP on the 32nd bit time. 0: Normal condition 1: Disconnect condition	RO	0b
26:24	**Squelch Tune (USB2_SQU_TUNE)** 000: Nominal 100mV Trip Point 001: Decrease by 12.5mV 010: Decrease by 25mV 011: Decrease by 37.5mV 100: Decrease by 50mV 101: Decrease by 62.5mV 110: Increase by 25mV 111: Increase by 12.5mV **Note:** This field is protected by Reset Protection (RST_PROTECT).	R/W	Note 15-58
23:0	**RESERVED**	RO	-

Note 15-58 The default value of this field is determined by the value of the Squelch Threshold (CFG0_SQU_THR) field of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 3'b000 is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 000b if neither is present.

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15.2.4 HSIC ENABLE REGISTER (HSIC_EN)

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Offset: 140h Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:25	**RESERVED**	RO	-
24	**HSIC Interface Enable (HSIC_ENABLE)** 0: Port is in USB mode 1: Port is in HSIC mode.	R/W	Note 15-59
23:19	**RESERVED**	RO	-
18	**HSIC 50ohm Driver Data and Strobe Enable (HSIC_DS_EN50)** Selects the driver output impedance. 0: 40ohm driver 1: 50ohm driver.	R/W	Note 15-60
17	**HSIC Slew Tune Test Bit Data and Strobe (HSIC_DS_SLEW_TUNE)** Reduces transmit slew rate on Data/Strobe by 30%. 0: TX Slew boost disabled (Default) 1: TX Slew boosted by 30%	R/W	Note 15-61
16	**HSIC Pin Swap (HSIC_PIN_SWAP)** When set the HSIC Data and Strobe pins swap.	R/W	Note 15-62
15:0	**RESERVED**	RO	-

Note 15-59 The default value of is 1b when the HSIC_SEL pin is tied to VDD. Otherwise the default value is 0b.

Note 15-60 The default value of this field is determined by the value of the HSIC 50ohm Driver Data and Strobe Enable (HSIC_DS_EN50) field of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0b if neither is present.

Note 15-61 The default value of this field is determined by the value of the HSIC Slew Tune Test Bit Data and Strobe (HSIC_DS_SLEW_TUNE) field of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0b if neither is present.

Note 15-62 The default value of this field is determined by the value of the HSIC Pin Swap (HSIC_PIN_SWAP) field of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0b if neither is present.

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15.3 Ethernet PHY Control and Status Registers

The Ethernet PHY registers are not memory mapped. These registers are accessed indirectly through the Ethernet MAC via the MII Access Register (MII_ACCESS) and MII Data Register (MII_DATA). The Ethernet PHY provides access to the following main categories of registers:

- Ethernet PHY Main Page Registers
- Ethernet PHY Extended Page 1 Registers
- Ethernet PHY Extended Page 2 Registers

Note: Access to the PHY register pages is controlled via the Ethernet PHY Extended Page Access Register. When extended page 1 or 2 register access is enabled, reads and writes to registers 16 through 30 affect the extended registers for the corresponding page instead of the main page registers in the IEEE-specified register space. Registers 0 through 15 are not affected by the state of the extended page register access. Writing 0000h to the Ethernet PHY Extended Page Access Register restores main page register access.

Note: All unlisted register index values are not supported and should not be addressed.

TABLE 15-8: ETHERNET PHY MAIN PAGE REGISTERS

INDEX (IN DECIMAL)	REGISTER NAME
0	Ethernet PHY Mode Control Register
1	Ethernet PHY Mode Status Register
2	Ethernet PHY Device Identifier 1 Register
3	Ethernet PHY Device Identifier 2 Register
4	Ethernet PHY Device Auto-Negotiation Advertisement Register
5	Ethernet PHY Auto-Negotiation Link Partner Ability Register
6	Ethernet PHY Auto-Negotiation Expansion Register
7	Ethernet PHY Auto-Negotiation Next Page TX Register
8	Ethernet PHY Auto-Negotiation Link Partner Next Page RX Register
9	Ethernet PHY 1000BASE-T Control Register
10	Ethernet PHY 1000BASE-T Status Register
11-12	RESERVED
13	Ethernet PHY MMD Access Control Register
14	Ethernet PHY MMD Access Address/Data Register
15	Ethernet PHY 1000BASE-T Status Extension 1 Register
16	Ethernet PHY 100BASE-TX Status Extension Register
17	Ethernet PHY 1000BASE-T Status Extension 2 Register
18	Ethernet PHY Bypass Control Register
19	100BASE-TX/1000BASE-T Receive Error Counter Register

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TABLE 15-8: ETHERNET PHY MAIN PAGE REGISTERS (CONTINUED)

INDEX (IN DECIMAL)	REGISTER NAME
20	100BASE-TX/1000BASE-T False Carrier Error Counter Register
21	10BASE-T/100BASE-TX/1000BASE-T Link Disconnect Counter Register
22	Ethernet PHY Extended 10BASE-T Control and Status Register
23	Ethernet PHY Extended PHY Control 1 Register
24	Ethernet PHY Extended PHY Control 2 Register
25	Ethernet PHY Interrupt Mask Register
26	Ethernet PHY Interrupt Status Register
27	RESERVED
28	Ethernet PHY Auxiliary Control and Status Register
29	Ethernet PHY LED Mode Select Register
30	Ethernet PHY LED Behavior Register
31	Ethernet PHY Extended Page Access Register

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15.3.1 ETHERNET PHY MAIN PAGE REGISTERS

This section details the Ethernet PHY main page register descriptions.

Note:	Ethernet PHY main page registers 0 through 15 may be accessed on the following pages: Page 0, 1, 2. The pages that a particular register is accessible on are also listed in the individual register description. Access to the PHY register pages is controlled via the Ethernet PHY Extended Page Access Register.

15.3.1.1 Ethernet PHY Mode Control Register

Index (In Decimal): 0 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15	**PHY Soft Reset (RESET)** 1 = PHY software reset. Bit is self-clearing.	R/W SC	0b
14	**Digital Loopback** 0 = normal operation 1 = Digital loopback mode	R/W	0b
13	**Speed Select[0]** Together with Speed Select[1], sets speed per the following table: [Speed Select1][Speed Select0] 00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	0b
12	**Auto-Negotiation Enable** 0 = disable auto-negotiate process 1 = enable auto-negotiate process (overrides the Speed Select[0], Speed Select[1], and Duplex Mode bits of this register)	R/W	1b
11	**Power Down** 0 = normal operation 1 = General power down mode **Note:** The Auto-Negotiation Enable must be cleared before setting the Power Down bit.	R/W	0b
10	**RESERVED**	RO	-
9	**Restart Auto-Negotiate** 0 = normal operation 1 = restart auto-negotiate process **Note:** Bit is self-clearing.	R/W SC	0b
8	**Duplex Mode** 0 = half duplex 1 = full duplex **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	0b
7	**RESERVED**	RO	-
6	**Speed Select[1]** See description for Speed Select[0] for details.	RO	1b
5:0	**RESERVED**	RO	-

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15.3.1.2 Ethernet PHY Mode Status Register

Index (In Decimal): 1 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15	**100BASE-T4** 0 = no T4 ability 1 = T4 able	RO	0b
14	**100BASE-TX Full Duplex** 0 = no TX full duplex ability 1 = TX with full duplex	RO	1b
13	**100BASE-TX Half Duplex** 0 = no TX half duplex ability 1 = TX with half duplex	RO	1b
12	**10BASE-T Full Duplex** 0 = no 10Mbps with full duplex ability 1 = 10Mbps with full duplex	RO	1b
11	**10BASE-T Half Duplex** 0 = no 10Mbps with half duplex ability 1 = 10Mbps with half duplex	RO	1b
10	**100BASE-T2 Full Duplex** 0 = PHY not able to perform full duplex 100BASE-T2 1 = PHY able to perform full duplex 100BASE-T2	RO	0b
9	**100BASE-T2 Half Duplex** 0 = PHY not able to perform half duplex 100BASE-T2 1 = PHY able to perform half duplex 100BASE-T2	RO	0b
8	**Extended Status** 0 = no extended status information in register 15 1 = extended status information in register 15	RO	1b
7:6	**RESERVED**	RO	-
5	**Auto-Negotiate Complete** 0 = auto-negotiate process not completed 1 = auto-negotiate process completed	RO	0b
4	**Remote Fault** 0 = no remote fault 1 = remote fault condition detected	RO	0b
3	**Auto-Negotiate Ability** 0 = unable to perform auto-negotiation function 1 = able to perform auto-negotiation function	RO	1b
2	**Link Status** 0 = link is down 1 = link is up	RO/LL	0b
1	**Jabber Detect** 0 = no 10BASE-T jabber condition detected 1 = 10BASE-T jabber condition detected	RO	0b
0	**Extended Capabilities** 0 = does not support extended capabilities registers 1 = supports extended capabilities registers	RO	1b

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15.3.1.3 Ethernet PHY Device Identifier 1 Register

Index (In Decimal): 2 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**PHY ID Number** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0007h

15.3.1.4 Ethernet PHY Device Identifier 2 Register

Index (In Decimal): 3 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15:10	**PHY ID Number** Assigned to the 19th through 24th bits of the OUI.	RO	110000b
9:4	**Model Number** Six-bit manufacturer's model number.	R/W	010011b
3:0	**Revision Number** Four-bit manufacturer's revision number.	R/W	Note 15-63

Note 15-63 The default value of this field will vary depending on the silicon revision number.

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15.3.1.5 Ethernet PHY Device Auto-Negotiation Advertisement Register

Index (In Decimal): 4 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Next Page** 0 = no next page ability 1 = next page capable **Note:**	R/W	0b
14	**RESERVED**	RO	-
13	**Remote Fault** 0 = no remote fault 1 = remote fault detected	R/W	0b
12	**RESERVED**	RO	-
11	**Asymmetric Pause** 0 = Asymmetrical pause direction is not advertised 1 = Asymmetrical pause direction is advertised	R/W	0b
10	**Pause Operation** 0 = Pause operation is not advertised 1 = Pause operation is advertised	R/W	0b
9	**RESERVED**	RO	-
8	**100BASE-TX Full Duplex** 0 = no TX full duplex ability 1 = TX with full duplex	R/W	1b
7	**100BASE-TX** 0 = no TX ability 1 = TX able	R/W	1b
6	**10BASE-T Full Duplex** 0 = no 10Mbps with full duplex ability 1 = 10Mbps with full duplex	R/W	1b
5	**10BASE-T** 0 = no 10Mbps ability 1 = 10Mbps able	R/W	1b
4:0	**Selector Field** 00001 = IEEE 802.3	R/W	00001b

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15.3.1.6 Ethernet PHY Auto-Negotiation Link Partner Ability Register

Index (In Decimal): 5 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Link Partner Next Page** 0 = no next page ability 1 = next page capable	RO	0b
14	**Link Partner Acknowledge** 0 = link code word not yet received 1 = link code word received from partner	RO	0b
13	**Link Partner Remote Fault** 0 = no remote fault 1 = remote fault detected	RO	0b
12	**RESERVED**	RO	-
11	**Link Partner Asymmetric Pause** 0 = Asymmetrical pause direction is not advertised 1 = Asymmetrical pause direction is advertised	R/W	0b
10	**Link Partner Pause Operation** 0 = Symmetrical pause operation is not advertised 1 = Symmetrical pause operation is advertised	RO	0b
9	**Link Partner 100BASE-T4** 0 = no T4 ability 1 = T4 able **Note:** This PHY does not support T4 ability.	RO	0b
8	**Link Partner 100BASE-TX Full Duplex** 0 = no TX full duplex ability 1 = TX with full duplex	RO	0b
7	**Link Partner 100BASE-TX Half Duplex** 0 = no TX half duplex ability 1 = TX half duplex able	RO	0b
6	**Link Partner 10BASE-T Full Duplex** 0 = no 10Mbps with full duplex ability 1 = 10Mbps with full duplex	RO	0b
5	**Link Partner 10BASE-T Half Duplex** 0 = no 10Mbps half duplex ability 1 = 10Mbps half duplex able	RO	0b
4:0	**Link Partner Selector Field** 00001 = IEEE 802.3	RO	00000b

15.3.1.7 Ethernet PHY Auto-Negotiation Expansion Register

Index (In Decimal): 6 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15:5	**RESERVED**	RO	-
4	**Parallel Detection Fault** 0 = no fault detected by parallel detection logic 1 = fault detected by parallel detection logic	RO/LH	0b
3	**Link Partner Next Page Able** 0 = link partner does not have next page ability 1 = link partner has next page ability	RO	0b
2	**Next Page Able** 0 = local device does not have next page ability 1 = local device has next page ability	RO	1b
1	**Page Received** 0 = new page not yet received 1 = new page received	RO/LH	0b
0	**Link Partner Auto-Negotiation Able** 0 = link partner does not have auto-negotiation ability 1 = link partner has auto-negotiation ability	RO	0b

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15.3.1.8 Ethernet PHY Auto-Negotiation Next Page TX Register

Index (In Decimal): 7 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Software Next Page** 0 = Last page 1 = More pages to follow	R/W	0b
14	**RESERVED**	RO	-
13	**Software Message Page** 0 = unformatted page 1 = message page	R/W	1b
12	**Acknowledge** 0 = device cannot comply with message 1 = device will comply with message	R/W	0b
11	**Toggle** 0 = previous transmitted LCW = 1 1 = previous transmitted LCW = 0	RO	0b
10:0	**Message Code** Message/Unformatted Code Field	RW	000 0000 0001b

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15.3.1.9 Ethernet PHY Auto-Negotiation Link Partner Next Page RX Register

Index (In Decimal): 8 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Link Partner Software Next Page** 0 = Last page 1 = More pages to follow	RO	0b
14	**Link Partner Acknowledge** 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0b
13	**Link Partner Software Message Page** 0 = unformatted page 1 = message page	RO	0b
12	**Acknowledge from Link Partner** 0 = device cannot comply with message 1 = device will comply with message	RO	0b
11	**Link Partner Toggle** 0 = previous transmitted LCW = 1 1 = previous transmitted LCW = 0	RO	0b
10:0	**Link Partner Message Code** Message/Unformatted Code Field	RO	000 0000 0000b

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15.3.1.10 Ethernet PHY 1000BASE-T Control Register

Index (In Decimal): 9 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15:13	**Test Mode** IEEE 802.3 clause 40.6.1.1.2 transmitter test mode. 000 = Normal mode 001 = Test Mode 1 - Transmit waveform test 010 = Test Mode 2 - Transmit jitter test in Master mode 011 = Test Mode 3 - Transmit jitter test in Slave mode 100 = Test Mode 4 - Transmitter distortion test 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000b
12	**Master/Slave Manual Configuration Enable** 0 = disable MASTER-SLAVE manual configuration value 1 = enable MASTER-SLAVE manual configuration value	R/W	0b
11	**Master/Slave Manual Configuration Value** Active only when the Master/Slave Manual Configuration Enable bit of this register is 1. 0 = Configure PHY as slave 1 = Configure PHY as master	R/W	0b
10	**Port Type** 0 = single-port device 1 = multi-port device	R/W	0b
9	**1000BASE-T Full Duplex** 0 = advertise PHY is not 1000BASE-T full duplex capable 1 = advertise PHY is 1000BASE-T full duplex capable	R/W	1b
8	**1000BASE-T Half Duplex** 0 = advertise PHY is not 1000BASE-T half duplex capable 1 = advertise PHY is 1000BASE-T half duplex capable	R/W	1b
7:0	**RESERVED**	RO	-

15.3.1.11 Ethernet PHY 1000BASE-T Status Register

Index (In Decimal): 10 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Master/Slave Configuration Fault** 0 = No MASTER-SLAVE configuration fault detected 1 = MASTER-SLAVE configuration fault detected	RO/LH	0b
14	**Master/Slave Configuration Resolution** 0 = Local PHY configuration resolved to SLAVE 1 = Local PHY configuration resolved to MASTER	RO	0b
13	**Local 1000BASE-T Receiver Status** 0 = Local Receiver not OK 1 = Local Receiver OK	RO	0b
12	**Remote (Link Partner) Receiver Status** 0 = Remote Receiver not OK 1 = Remote Receiver OK	RO	0b
11	**Link Partner Advertised 1000BASE-T Full Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T full duplex 1 = Link Partner is capable of 1000BASE-T full duplex	RO	0b
10	**Link Partner Advertised 1000BASE-T Half Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T half duplex 1 = Link Partner is capable of 1000BASE-T half duplex	RO	0b
9:8	**RESERVED**	RO	-
7:0	**1000BASE-T Idle Error Count** Cumulative count of the errors detected when the receiver is receiving idles.	RO/SC	00h

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15.3.1.12 Ethernet PHY MMD Access Control Register

Index (In Decimal): 13 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15:14	**MMD Access Function** 00 = Address 01 = Data, no post-increment 10 = Data, post-increment on reads and writes 11 = Data, post-increment on writes only	R/W	00b
13:5	**RESERVED**	RO	-
4:0	**MMD Access Device Address**	R/W	00000b

Note: Auto-address incrementing in a write is not supported.

Note: Refer to Section 15.4, "MDIO Manageable Device (MMD) Control and Status Registers," on page 255 for details on the available MMD registers.

15.3.1.13 Ethernet PHY MMD Access Address/Data Register

Index (In Decimal): 14 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**MMD Address/Data** If MMD Access Device Address is 00b, this field is the MMD address. Otherwise, this field is the MMD data.	R/W	0000h

Note: Refer to Section 15.4, "MDIO Manageable Device (MMD) Control and Status Registers," on page 255 for details on the available MMD registers.

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15.3.1.14 Ethernet PHY 1000BASE-T Status Extension 1 Register

Index (In Decimal): 15 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15	**1000BASE-X Full Duplex** 0 = PHY not able to perform full duplex 1000BASE-X 1 = PHY able to perform full duplex 1000BASE-X	RO	0b
14	**1000BASE-X Half Duplex** 0 = PHY not able to perform half duplex 1000BASE-X 1 = PHY able to perform half duplex 1000BASE-X	RO	0b
13	**1000BASE-T Full Duplex** 0 = PHY not able to perform full duplex 1000BASE-T 1 = PHY able to perform full duplex 1000BASE-T	RO	1b
12	**1000BASE-T Half Duplex** 0 = PHY not able to perform half duplex 1000BASE-T 1 = PHY able to perform half duplex 1000BASE-T	RO	1b
11:0	**RESERVED**	RO	-

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15.3.1.15 Ethernet PHY 100BASE-TX Status Extension Register

Index (In Decimal): 16 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15	**100BASE-TX Descrambler Locked**	RO	0b
14	**100BASE-TX Descrambler Lock Error Detected**	RO/SC	0b
13	**100BASE-TX Link-Disconnect State**	RO/SC	0b
12	**100BASE-TX Current Link Status**	RO	0b
11	**100BASE-TX Receive Error Detected**	RO/SC	0b
10	**100BASE-TX Transmit Error Detected**	RO/SC	0b
9	**100BASE-TX Start-of-stream Delimiter Error Detected**	RO/SC	0b
8	**100BASE-TX End-of-stream Delimiter Error Detected**	RO/SC	0b
7:0	**RESERVED**	RO	-

15.3.1.16 Ethernet PHY 1000BASE-T Status Extension 2 Register

Index (In Decimal): 17 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15	**1000BASE-T Descrambler Locked**	RO	0b
14	**1000BASE-T Descrambler Lock Error Detected**	RO/SC	0b
13	**1000BASE-T Link-Disconnect State**	RO/SC	0b
12	**1000BASE-T Current Link Status**	RO	0b
11	**1000BASE-T Receive Error Detected**	RO/SC	0b
10	**1000BASE-T Transmit Error Detected**	RO/SC	0b
9	**1000BASE-T Start-of-stream Delimiter Error Detected**	RO/SC	0b
8	**1000BASE-T End-of-stream Delimiter Error Detected**	RO/SC	0b
7	**1000BASE-T Carrier Extension Error Detected**	RO/SC	0b
6	**Non-compliant 1000BASE-T BCM5400 Detected**	RO	0b
5	**MDI Crossover Error Detected**	RO	0b
4:0	**RESERVED**	RO	-

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15.3.1.17 Ethernet PHY Bypass Control Register

Index (In Decimal): 18 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Disabled Transmitter Output to Media**	R/W	0b
14	**Bypass 4B/5B Encoder/Decoder**	R/W	0b
13	**Bypass Scrambler**	R/W	0b
12	**Bypass Descrambler**	R/W	0b
11	**Bypass PCS Receive**	R/W	0b
10	**Bypass PCS Transmit**	R/W	0b
9	**Bypass Link Fail Inhibit Timer**	R/W	0b
8	**RESERVED**	RO	-
7	**Disable Auto-MDI/MDI-X in Forced 10/100 Mode**	R/W	1b
6	**Non-compliant BCM5400 Detect Disable**	R/W	0b
5	**Disable Auto-MDI/MDI-X Correction**	R/W	0b
4	**Disable Polarity Inversion Correction**	R/W	0b
3	**Ignore Advertised Ability** 0 = Ignore advertised ability in parallel detect enable 1 = Do not ignore advertised ability	R/W	1b
2	**Pulse Shape Filter Disable** Disables $(0.75 + 0.25z^{-1})$ pulse shaping filter in 1000BASE-T transmitter	R/W	0b
1	**Automatic 1000BASE-T Next-page Exchange Disable** Disables automatic 1000BASE-T next-page exchanges	R/W	0b
0	**RESERVED**	RO	-

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15.3.1.18 100BASE-TX/1000BASE-T Receive Error Counter Register

Index (In Decimal): 19 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**RESERVED**	RO	-
7:0	**100BASE-TX/1000BASE-T Receive Error Counter** This single counter counts both 100BASE-TX and 1000BASE-T events when the respective link is up. The counter saturates at 255 and clears upon being read.	RO/SC	00h

15.3.1.19 100BASE-TX/1000BASE-T False Carrier Error Counter Register

Index (In Decimal): 20 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**RESERVED**	RO	-
7:0	**100BASE-TX/1000BASE-T False Carrier Error Counter** This single counter counts both 100BASE-TX and 1000BASE-T events when the respective link is up. The counter saturates at 255 and clears upon being read.	RO/SC	00h

15.3.1.20 10BASE-T/100BASE-TX/1000BASE-T Link Disconnect Counter Register

Index (In Decimal): 21 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**RESERVED**	RO	-
7:0	**10BASE-T/100BASE-TX/1000BASE-T Link Disconnect Counter** This counter counts all copper PHY link drops. The counter saturates at 255 and clears upon being read.	RO/SC	00h

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15.3.1.21 Ethernet PHY Extended 10BASE-T Control and Status Register

Index (In Decimal): 22 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Disable 10BASE-T Link-integrity State Machine**	R/W	0b
14	**Disable 10BASE-T Jabber Detect**	R/W	0b
13	**Disable 10BASE-T Echo Mode**	R/W	1b
12	**Disable 10BASE-T Signal Quality Error Test**	R/W	1b
11:10	**10BASE-T Squelch Threshold Control** 00 = Nominal squelch threshold (300 mV) 01 = Reduced squelch threshold (197 mV) 10 = Raised squelch threshold (450 mV) 11 = RESERVED	R/W	00b
9	**Sticky Reset Enable**	R/W	1b
8	**EOF Error Detected**	RO/SC	0b
7	**10BASE-T Disconnected**	RO/SC	0b
6	**10BASE-T Link Status**	RO	0b
5:3	**RESERVED**	RO	-
2:1	**Carrier-Sense Control** 00 = CRS equals receiving or (transmitting & ~FDX) 01 = CRS equals (receiving or transmitting) & ~FDX 10 = CRS equals receiving 11 = CRS equals receiving & ~FDX Where FDX=1 in full-duplex mode.	R/W	00b
0	**RESERVED**	RO	-

15.3.1.22 Ethernet PHY Extended PHY Control 1 Register

Index (In Decimal): 23 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15:4	**RESERVED**	RO	-
3	**Far-End Loopback Enable**	R/W	0b
2:0	**RESERVED**	RO	-

15.3.1.23 Ethernet PHY Extended PHY Control 2 Register

Index (In Decimal): 24 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15:13	**100BASE-TX Edge Rate Control** 011 = +3 edge rate (slowest) 010 = +2 edge rate 001 = +1 Default edge rate 000 = Default edge rate 111 = -1 edge rate 110 = -2 edge rate 101 = -3 edge rate 100 = -4 edge rate (fastest)	R/W	000b
12:6	**RESERVED**	RO	-
5:4	**Jumbo Packet FIFO Configuration** 00 = Normal IEEE 1518-byte packet length 01 = 9000-byte jumbo packet length 10 = 12000-byte jumbo packet length 11 = RESERVED	R/W	00b
3:1	**RESERVED**	RO	-
0	**Cable Loopback Mode Enable**	R/W	0b

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15.3.1.24 Ethernet PHY Interrupt Mask Register

Index (In Decimal): 25 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Interrupt Enable**	R/W	0b
14	**Speed State-Change Interrupt Mask**	R/W	0b
13	**Link State-Change Interrupt Mask**	R/W	0b
12	**Full Duplex State-Change Interrupt Mask**	R/W	0b
11	**Auto-Negotiation Error Interrupt Mask**	R/W	0b
10	**Auto-Negotiation Complete Interrupt Mask**	R/W	0b
9	**In-line Powered Device (PoE) Detected Interrupt Mask**	R/W	0b
8	**Symbol Error Interrupt Mask**	R/W	0b
7	**Fast Link Failure Interrupt Mask**	R/W	0b
6	**RESERVED**	RO	-
5	**Extended Interrupt Mask**	R/W	0b
4	**Wake on LAN (WoL) Interrupt Mask**	R/W	0b
3	**False-carrier Interrupt Mask**	R/W	0b
2	**Link Speed Downshift Detected Interrupt Mask**	R/W	0b
1	**Master/Slave Resolution Error Interrupt Mask**	R/W	0b
0	**RX_ER Interrupt Mask**	R/W	0b

Note: No status bit is set in the Ethernet PHY Interrupt Status Register if the corresponding interrupt mask bit in the Ethernet PHY Interrupt Mask Register is clear. When an interrupt mask is clear, the actual corresponding interrupt condition may still be set internally (i.e., it is “pending”), but will not be reflected in the corresponding Ethernet PHY Interrupt Status Register bit. In the latter case, any pending internal interrupt condition will be reflected in the corresponding Ethernet PHY Interrupt Status Register bit when the corresponding bit is set in the Ethernet PHY Interrupt Mask Register. The actual interrupt condition will be cleared when the Ethernet PHY Interrupt Status Register is read, but only if the corresponding interrupt mask bit is set at the time of the Ethernet PHY Interrupt Status Register read. Therefore, the following sequence for enabling interrupts is recommended:

1. Write the Ethernet PHY Interrupt Mask Register to enable the desired interrupts by setting the individual bits, but DO NOT set the Interrupt Enable bit. This prevents any pending interrupts from being reflected on the Interrupt Status bit of the Ethernet PHY Interrupt Status Register and therefore the interrupt pin will not assert.
2. Read the Ethernet PHY Interrupt Status Register to clear any pending interrupts for enabled interrupt sources. If necessary, service those actions as required.
3. Write the Ethernet PHY Interrupt Mask Register to enable the desired interrupts (set individual bits) AND the Interrupt Enable bit concurrently. Now all desired NEW interrupts can be received with no risk of previously generated interrupts being reflected.

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15.3.1.25 Ethernet PHY Interrupt Status Register

Index (In Decimal): 26 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Interrupt Status**	R/W	0b
14	**Speed State-Change Interrupt Status**	R/W	0b
13	**Link State-Change Interrupt Status**	R/W	0b
12	**Full Duplex State-Change Interrupt Status**	R/W	0b
11	**Auto-Negotiation Error Interrupt Status**	R/W	0b
10	**Auto-Negotiation Complete Interrupt Status**	R/W	0b
9	**In-line Powered Device (PoE) Detected Interrupt Status**	R/W	0b
8	**Symbol Error Interrupt Status**	R/W	0b
7	**Fast Link Failure Interrupt Status**	R/W	0b
6	**RESERVED**	RO	-
5	**Extended Interrupt Status**	R/W	0b
4	**Wake on LAN (WoL) Interrupt Status**	R/W	0b
3	**False-carrier Interrupt Status**	R/W	0b
2	**Link Speed Downshift Interrupt Status**	R/W	0b
1	**Master/Slave Resolution Error Interrupt Status**	R/W	0b
0	**RX_ER Interrupt Status**	R/W	0b

Note: No status bit is set in the Ethernet PHY Interrupt Status Register if the corresponding interrupt mask bit in the Ethernet PHY Interrupt Mask Register is clear. When an interrupt mask is clear, the actual corresponding interrupt condition may still be set internally (i.e., it is “pending”), but will not be reflected in the corresponding Ethernet PHY Interrupt Status Register bit. In the latter case, any pending internal interrupt condition will be reflected in the corresponding Ethernet PHY Interrupt Status Register bit when the corresponding bit is set in the Ethernet PHY Interrupt Mask Register. The actual interrupt condition will be cleared when the Ethernet PHY Interrupt Status Register is read, but only if the corresponding interrupt mask bit is set at the time of the Ethernet PHY Interrupt Status Register read. Therefore, the following sequence for enabling interrupts is recommended:

1. Write the Ethernet PHY Interrupt Mask Register to enable the desired interrupts by setting the individual bits, but DO NOT set the Interrupt Enable bit. This prevents any pending interrupts from being reflected on the Interrupt Status bit of the Ethernet PHY Interrupt Status Register and therefore the interrupt pin will not assert.
2. Read the Ethernet PHY Interrupt Status Register to clear any pending interrupts for enabled interrupt sources. If necessary, service those actions as required.
3. Write the Ethernet PHY Interrupt Mask Register to enable the desired interrupts (set individual bits) AND the Interrupt Enable bit concurrently. Now all desired NEW interrupts can be received with no risk of previously generated interrupts being reflected.

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15.3.1.26 Ethernet PHY Auxiliary Control and Status Register

Index (In Decimal): 28 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Interrupt Auto-negotiation Complete**	RO	0b
14	**Auto-negotiation Disabled**	RO	0b
13	**MDI/MDI-X Crossover Indication**	RO	0b
12	**CD Pair Swap Indication**	RO	0b
11:8	**Pairs A (11), B (10), C (9), and D (8) Polarity Inversion Indication**	RO	0000b
7	**Link Status Timeout Control [1]** Together with Link Status Timeout Control [0], sets link status timeout per the following table: 00 = 1 second 01 = 2 seconds 10 = 3 seconds 11 = 4 seconds	R/W	Note 15-64
6	**Enhanced PHY Enable**	R/W	Note 15-65
5	**Duplex Status** 0 = Half duplex 1 = Full duplex	RO	0b
4:3	**Link Speed Status** 00 = 10BASE-T 01 = 100BASE-TX 10 = 1000BASE-T 11 = RESERVED	RO	-
2	**Link Status Timeout Control [0]** See description for Link Status Timeout Control [1] for details.	R/W	Note 15-64
1:0	**RESERVED**	RO	-

Note 15-64 The default value of this field is determined by the value of the Link Time Out Control (LINK_TIME_OUT_CTRL) field of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0b if neither is present.

Note 15-65 The default value of this field is determined by the value of the Enhanced PHY Enable (ACT_PHY_EN) field of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 0b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 0b if neither is present.

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15.3.1.27 Ethernet PHY LED Mode Select Register

Index (In Decimal): 29 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15:12	**LED3 Configuration** This field configures the **LED3** pin function. Refer to Table 15-9 for definitions.	R/W	1000b
11:8	**LED2 Configuration** This field configures the **LED2** pin function. Refer to Table 15-9 for definitions.	R/W	0000b
7:4	**LED1 Configuration** This field configures the **LED1** pin function. Refer to Table 15-9 for definitions.	R/W	0010b
3:0	**LED0 Configuration** This field configures the **LED0** pin function. Refer to Table 15-9 for definitions.	R/W	0001b

Table 15-9 details the various LED configuration functions. For additional information, refer to Section 9.3, "LED Interface," on page 92.

TABLE 15-9: LEDX PIN FUNCTION CONFIGURATION

LED Configuration	Description
0000	Link/Activity (default for **LED2**)
0001	Link1000/Activity (default for **LED0**)
0010	Link100/Activity (default for **LED1**)
0011	Link10/Activity
0100	Link100/1000/Activity
0101	Link10/1000/Activity
0110	Link10/100/Activity
0111	RESERVED
1000	Duplex/Collision (default for **LED3**)
1001	Collision
1010	Activity
1011	RESERVED
1100	Auto-negotiation Fault
1101	RESERVED
1110	Force LED Off (suppresses LED blink after reset/coma)
1111	Force LED On (suppresses LED blink after reset/coma)
Others	RESERVED

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15.3.1.28 Ethernet PHY LED Behavior Register

Index (In Decimal): 30 Size: 16 bits
Page: 0

BITS	DESCRIPTION	TYPE	DEFAULT
15	**RESERVED**	RO	-
14	**LED Activity Output Select**	R/W	0b
13	**RESERVED**	RO	-
12	**LED Pulsing Enable**	R/W	0b
11:10	**LED Blink / Pulse-Stretch Rate** 00 = 2.5 Hz Blink Rate / 400 ms pulse-stretch 01 = 5 Hz Blink Rate / 200 ms pulse-stretch 10 = 10 Hz Blink Rate / 100 ms pulse-stretch 11 = 20 Hz Blink Rate / 50 ms pulse-stretch	R/W	01b
9	**RESERVED**	RO	-
8:5	**LED Pulse Stretch Enables** Configures **LED3** (bit 8), **LED2** (bit 7), **LED1** (bit 6), **LED0** (bit 5) to either pulse-stretch when 1, or blink when 0.	R/W	0000b
4	**RESERVED**	RO	-
3:0	**LED Combination Disables** Configures **LED3** (bit 3), **LED2** (bit 2), **LED1** (bit 1), **LED0** (bit 0) to either combine link/activity and duplex/collision when 0, or disable combination, providing link-only and duplex-only when 1.	R/W	0000b

15.3.1.29 Ethernet PHY Extended Page Access Register

Index (In Decimal): 31 Size: 16 bits
Pages: 0,1,2

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Ethernet PHY Register Page Select** This field selects the Ethernet PHY register page to access: 0000h = Ethernet PHY Main Page Registers (0-30) 0001h = Ethernet PHY Extended Page 1 Registers (16-30) 0002h = Ethernet PHY Extended Page 2 Registers (16-30) **Note:** All other configurations are reserved.	R/W	0000h

15.3.2 ETHERNET PHY EXTENDED PAGE 1 REGISTERS

This section details the Ethernet PHY extended page 1 register descriptions. To access the extended page 1 registers (16E1 through 30E1), enable extended register page 1 access by writing 0001h to the Ethernet PHY Extended Page Access Register. When extended page 1 register access is enabled, reads and writes to registers 16 through 30 affect the extended registers for the corresponding page instead of the main page registers in the IEEE-specified register space. Registers 0 through 15 are not affected by the state of the extended page register access.

Note: Writing 0000h to the Ethernet PHY Extended Page Access Register restores main page register access.

TABLE 15-10: ETHERNET PHY EXTENDED PAGE 1 REGISTERS

INDEX (IN DECIMAL)	REGISTER NAME
0-15	Refer to Ethernet PHY Main Page Registers
16E1-17E1	RESERVED
18E1	Ethernet PHY Page 1 Receive Good Counter Register
19E1	Ethernet PHY Page 1 LED and Crossover Control Register
20E1	Ethernet PHY Page 1 Extended PHY Control 3 Register
21E1-22E1	RESERVED
23E1	Ethernet PHY Page 1 Extended PHY Control 4 Register
24E1-28E1	RESERVED
29E1	Ethernet PHY Page 1 Ethernet Packet Generator (EPG) Control 1 Register
30E1	Ethernet PHY Page 1 Ethernet Packet Generator (EPG) Control 2 Register
31E1	Ethernet PHY Extended Page Access Register (same as main page)

Note: In Table 15-10, extended page 1 registers are indicated with an “E1” after the index number.

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15.3.2.1 Ethernet PHY Page 1 Receive Good Counter Register

Index (In Decimal): 18 Size: 16 bits
Page: 1

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Packet Counter Active** This bit indicates at least 1 packet has been received with a good CRC since the last read. This bit clears upon read.	RO/SC	0b
14	**RESERVED**	RO	-
13:0	**Packet Counter** This field indicates the number of packets received with a good CRC since the last read. This bit clears upon read.	RO/SC	0000h

15.3.2.2 Ethernet PHY Page 1 LED and Crossover Control Register

Index (In Decimal): 19 Size: 16 bits
Page: 1

BITS	DESCRIPTION	TYPE	DEFAULT
15:5	**RESERVED**	RO	-
4	**Fast Link Failure Enable** 0 = Disabled 1 = Enabled	R/W	0b
3:2	**MDI/MDI-X Force Enable** 00 = Normal HP Auto-MDIX operation 01 = Reserved 10 = Copper media forced to MDI 11 = Copper media forced to MDI-X	R/W	00b
1:0	**RESERVED** **Note:** To ensure proper operation, the value read from this field must be written back during a write.	R/W	-

15.3.2.3 Ethernet PHY Page 1 Extended PHY Control 3 Register

Index (In Decimal): 20 Size: 16 bits
Page: 1

BITS	DESCRIPTION	TYPE	DEFAULT
15	**RESERVED**	RO	-
14:13	**Enhanced PHY Sleep Timer** Sets time between wake events 00 = 1 second 01 = 2 seconds 10 = 3 seconds 11 = 4 seconds	R/W	Note 15-66
12:11	**Enhanced PHY Wake Timer** Sets the duration of wake attempts (sending link pulses) 00 = 160 ms 01 = 400 ms 10 = 800 ms 11 = 2 seconds	R/W	Note 15-67
10:6	**RESERVED**	RO	-
5	**Enable 10BASE-T No Preamble** When 1, 10BASE-T will assert the internal receive data valid signal when data is presented to the receiver even without a preamble preceding it.	R/W	0b
4	**Enable Cable Impairment Auto-Downshift** When 1, enables cable impairment auto-downshift in cases where problems with pairs C and D prevents the link from coming up in 1000BASE-T	R/W	0b
3:2	**Link Speed Auto-Downshift Control** 00 = Downshift after 2 failed 1000BASE-T auto-negotiation attempts 01 = Downshift after 3 failed 1000BASE-T auto-negotiation attempts 10 = Downshift after 4 failed 1000BASE-T auto-negotiation attempts 11 = Downshift after 5 failed 1000BASE-T auto-negotiation attempts	R/W	01b
1	**Apply Downshift** 1 indicates a downshift is required or has occurred.	RO	0b
0	**Link Quality** 1 indicates good link quality. (always 1 when 10BASE-T link is up)	RO	0b

Note 15-66 The default value of this field is determined by the value of the Enhanced PHY Sleep Timer (PHY_SLEEP_TIMER) field of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 01b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 01b if neither is present.

Note 15-67 The default value of this field is determined by the value of the Enhanced PHY Wake Timer (PHY_WAKE_TIMER) field of Configuration Flags 0 contained within the EEPROM, if present. If no EEPROM is present then the value programmed in OTP is used. If OTP is not configured then 00b is the default. A USB Reset or Lite Reset (LRST) will cause this field to be restored to the image value last loaded from EEPROM, or OTP, or to be set to 00b if neither is present.

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15.3.2.4 Ethernet PHY Page 1 Extended PHY Control 4 Register

Index (In Decimal): 23 Size: 16 bits
Page: 1

BITS	DESCRIPTION	TYPE	DEFAULT
15:11	**PHY Address**	RO	00000b
10	**Enable Inline Powered Device Detection**	R/W	0b
9:8	**Inline Power Capable Device Detection Status**	RO	00b
7:0	**Receive Packet CRC Error Counter**	RO/SC	00h

15.3.2.5 Ethernet PHY Page 1 Ethernet Packet Generator (EPG) Control 1 Register

Index (In Decimal): 29 Size: 16 bits
Page: 1

BITS	DESCRIPTION	TYPE	DEFAULT
15	**EPG Enable**	R/W	0b
14	**EPG Run/Stop** 0 = Stop EPG (the EPG will stop after completing an integral multiple of 10,000 packets) 1 = Run EPG	R/W	0b
13	**Transmission Duration** 0 = Send 30,000,000/3,000,000/300,000 packets in 1000BASE-T/100BASE-TX/10BASE-T 1 = Continuously send	R/W	0b
12:11	**Packet Length** 00 = 125 bytes 01 = 64 bytes 10 = 1518 bytes 11 = 10,000 byte jumbo packet	R/W	00b
10	**Inter-packet Gap** 0 = 96 bit times 1 = 8192 bit times	R/W	0b
9:6	**Lowest Nibble of 6-byte Destination Address** **Note:** All upper nibbles are Fh.	R/W	0001b
5:2	**Lowest Nibble of 6-byte Source Address** **Note:** All upper nibbles are Fh.	R/W	0000b
1	**Payload Type** 0 = Fixed payload pattern 1 = Randomly generated payload pattern	R/W	0b
0	**Bad FCS Generation** 0 = Generate packets with good CRC 1 = Generate packets with bad CRC	R/W	0b

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15.3.2.6 Ethernet PHY Page 1 Ethernet Packet Generator (EPG) Control 2 Register

Index (In Decimal): 30 Size: 16 bits
Page: 1

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**EPG Packet Payload Data Pattern** 16-bit repeated data pattern	R/W	0000h

15.3.3 ETHERNET PHY EXTENDED PAGE 2 REGISTERS

This section details the Ethernet PHY extended page 2 register descriptions. To access the extended page 2 registers (16E2 through 30E2), enable extended register page 2 access by writing 0002h to the Ethernet PHY Extended Page Access Register. When extended page 2 register access is enabled, reads and writes to registers 16 through 30 affect the extended registers for the corresponding page instead of the main page registers in the IEEE-specified register space. Registers 0 through 15 are not affected by the state of the extended page register access.

Note: Writing 0000h to the Ethernet PHY Extended Page Access Register restores main page register access.

TABLE 15-11: ETHERNET PHY EXTENDED PAGE 2 REGISTERS

INDEX (IN DECIMAL)	REGISTER NAME
0-15	Refer to Ethernet PHY Main Page Registers
16E2	Ethernet PHY Page 2 Copper Physical Medium Dependent (PMD) TX Control Register
17E2	Ethernet PHY Page 2 EEE Control Register
18E2-27E2	RESERVED
28E2	Ethernet PHY Page 2 Extended Interrupt Mask Register
29E2	Ethernet PHY Page 2 Extended Interrupt Status Register
30E2	RESERVED
31E2	Ethernet PHY Extended Page Access Register (same as main page)

Note: In Table 15-11, extended page 2 registers are indicated with an “E2” after the index number.

15.3.3.1 Ethernet PHY Page 2 Copper Physical Medium Dependent (PMD) TX Control Register

Index (In Decimal): 16 Size: 16 bits
Page: 2

BITS	DESCRIPTION	TYPE	DEFAULT
15:12	**1000BASE-T Transmit Signal Amplitude Trim**	R/W	0000b
11:8	**100BASE-TX Transmit Signal Amplitude Trim**	R/W	0010b
7:4	**10BASE-T Transmit Signal Amplitude Trim**	R/W	1101b
3:0	**10BASE-Te Transmit Signal Amplitude Trim**	R/W	1110b

Note: This register provides control over the amplitude settings for the transmit side of the copper PMD interface. These bits provide the ability to make small adjustments in the signal amplitude to compensate for minor variations in the magnetic from different vendors. Extreme caution must be exercised when changing these settings from the default values as they have a direct impact on the signal quality. Changing these settings will also affect the linearity and harmonic distortion of the transmitted signals.

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15.3.3.2 Ethernet PHY Page 2 EEE Control Register

Index (In Decimal): 17 Size: 16 bits
Page: 2

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Enable Energy Efficient (802.3az) 10BASE-Te Operating Mode**	R/W	0b
14	**RESERVED**	RO	-
13:10	**Invert LED Polarity** Invert the polarity of the **LED[3:0]** signals. 0 = (default) drives an active low signal on the corresponding **LEDx** pin. 1 = drives an active high signal on the corresponding **LEDx** pin.	R/W	0000b
9	**RESERVED**	RO	-
8	**Current Link Status** 0 = PHY link is currently down 1 = PHY link is currently up	RO	0b
7	**1000BASE-T EEE Enable Status** 0 = Auto-negotiation did not resolve to link in 1000BASE-T with EEE 1 = Auto-negotiation resolved to link in 1000BASE-T with EEE	RO	0b
6	**100BASE-TX EEE Enable Status** 0 = Auto-negotiation did not resolve to link in 100BASE-TX with EEE 1 = Auto-negotiation resolved to link in 100BASE-TX with EEE	RO	0b
5	**Enable 1000BASE-T Force Mode** When 1, enables 1000BASE-T force mode to allow the PHY to link up in 1000BASE-T mode without forcing master/slave when the Speed Select[1] and Speed Select[0] bits of the Ethernet PHY Mode Control Register are set to 10b.	R/W	0b
4	**Force Transmit LPI** 0 = Transmit idles being received from the MAC 1 = Enable transmission of LPI on the MDI instead of normal idles when receiving normal idles from the MAC	R/W	0b
3	**Inhibit 100BASE-TX Transmit EEE LPI** When 1, disables transmission of EEE LPI on transmit path MDI in 100BASE-TX mode when receiving LPI from the MAC	R/W	0b
2	**Inhibit 100BASE-TX Receive EEE LPI** When 1, disables transmission of EEE LPI on receive path MAC interface in 100BASE-TX mode when receiving LPI from the MDI	R/W	0b
1	**Inhibit 1000BASE-T Transmit EEE LPI** When 1, disables transmission of EEE LPI on transmit path MDI in 1000BASE-T mode when receiving LPI from the MAC	R/W	0b
0	**Inhibit 1000BASE-T Receive EEE LPI** When 1, disables transmission of EEE LPI on receive path MAC interface in 1000BASE-T mode when receiving LPI from the MDI	R/W	0b

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15.3.3.3 Ethernet PHY Page 2 Extended Interrupt Mask Register

Index (In Decimal): 28 Size: 16 bits
Page: 2

BITS	DESCRIPTION	TYPE	DEFAULT
15:4	**RESERVED**	RO	-
3	**EEE Link Fail Interrupt Mask**	R/W	0b
2	**EEE RX TQ Timer Interrupt Mask**	R/W	0b
1	**EEE Wait Quiet/RX TS Timer Interrupt Mask**	R/W	0b
0	**EEE Wake Error Interrupt Mask**	R/W	0b

15.3.3.4 Ethernet PHY Page 2 Extended Interrupt Status Register

Index (In Decimal): 29 Size: 16 bits
Page: 2

BITS	DESCRIPTION	TYPE	DEFAULT
15:4	**RESERVED**	RO	-
3	**EEE Link Fail Interrupt Status**	R/W SC	0b
2	**EEE RX TQ Timer Interrupt Status**	R/W SC	0b
1	**EEE Wait Quiet/RX TS Timer Interrupt Status**	R/W SC	0b
0	**EEE Wake Error Interrupt Status**	R/W SC	0b

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15.4 MDIO Manageable Device (MMD) Control and Status Registers

The device MMD registers adhere to the *IEEE 802.3-2008 45.2 MDIO Interface Registers* specification. The MMD registers are not memory mapped. These registers are accessed indirectly via the Ethernet PHY MMD Access Control Register and Ethernet PHY MMD Access Address/Data Register. Table 15-12 lists the available MMD control and status registers.

TABLE 15-12: MMD CONTROL AND STATUS REGISTERS MAP

MMD Device Address	Index	Register Name
3	1	PCS Status 1 (PCS_STATUS_1)
	20	EEE Capability (EEE_CAPABILITY)
	22	EEE Wake Error Counter (EEE_Wake_ERROR_COUNTER)
7	60	EEE Advertisement (EEE_ADVERTISEMENT)
	61	EEE Link Partner Advertisement (EEE_LP_ADVERTISEMENT)

15.4.1 PCS STATUS 1 (PCS_STATUS_1)

Device.Register Address: 3.1 (decimal) 3.1 (hexadecimal) Size: 16 bits

This register provides status of the EEE operation from the PCS for the currently active link.

BITS	DESCRIPTION	TYPE	DEFAULT
15:12	**RESERVED**	RO	-
11	**TX LPI Received** 0: TX PCS has received LPI 1: TX LPI not received	RO/LH	0b
10	**RX LPI Received** 0: RX PCS has received LPI 1: RX LPI not received	RO/LH	0b
9	**TX LPI Indication** 0: TX PCS is currently receiving LPI 1: TX PCS not currently receiving	RO	0b
8	**RX LPI Indication** 0: RX PCS is currently receiving LPI 1: RX PCS not currently receiving	RO	0b
7:3	**RESERVED**	RO	-
2	**PCS Receive Link Status** 0: PCS receive link up 1: PCS receive link down	RO	0b
1:0	**RESERVED**	RO	-

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15.4.2 EEE CAPABILITY (EEE_CAPABILITY)

Device.Register Address: 3.20 (decimal) / 3.14 (hexadecimal) Size: 16 bits

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type.

BITS	DESCRIPTION	TYPE	DEFAULT
15:3	**RESERVED**	RO	-
2	**1000BASE-T EEE** 0: EEE is not supported for 1000BASE-T 1: EEE is supported for 1000BASE-T	RO	0b
1	**100BASE-TX EEE** 0: EEE is not supported for 100BASE-TX 1: EEE is supported for 100BASE-TX	RO	0b
0	**RESERVED**	RO	-

15.4.3 EEE WAKE ERROR COUNTER (EEE_WAKE_ERROR_COUNTER)

Device.Register Address: 3.22 (decimal) / 3.16 (hexadecimal) Size: 16 bits

This register is used by the PHY to count wake time faults where the PHY fails to complete its normal wake sequence within the time required. This 16-bit counter is reset to all zeros when the EE wake error counter is read or when the PHY undergoes hardware or software reset.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Wake Error Counter**	RO	0000h

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15.4.4 EEE ADVERTISEMENT (EEE_ADVERTISEMENT)

Device.Register Address: 7.60 (Decimal) Size: 16 bits
7.3C (Hexadecimal)

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code.

BITS	DESCRIPTION	TYPE	DEFAULT
15:3	**RESERVED**	RO	-
2	**1000BASE-T EEE Advertisement** 0: Do not advertise that 1000BASE-T EEE capability 1: Advertise that 1000BASE-T EEE capability	R/W	0b
1	**100BASE-TX EEE Advertisement** 0: Do not advertise that 100BASE-TX EEE capability 1: Advertise that 100BASE-TX EEE capability	R/W	0b
0	**RESERVED**	RO	-

15.4.5 EEE LINK PARTNER ADVERTISEMENT (EEE_LP_ADVERTISEMENT)

Device.Register Address: 7.61 (Decimal) Size: 16 bits
7.3D (Hexadecimal)

When the auto-negotiation process has completed, this register reflects the contents of the link partners EEE advertisement register.

BITS	DESCRIPTION	TYPE	DEFAULT
15:3	**RESERVED**	RO	-
2	**1000BASE-T EEE Link Partner Advertisement** 0: Link partner is not advertising 1000BASE-T EEE capability 1: Link partner is advertising 1000BASE-T EEE capability	R/W	0b
1	**100BASE-TX EEE Link Partner Advertisement** 0: Link partner is not advertising 100BASE-TX EEE capability 1: Link partner is advertising 100BASE-TX EEE capability	R/W	0b
0	**RESERVED**	RO	-

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16.0 OPERATIONAL CHARACTERISTICS

16.1 Absolute Maximum Ratings*

Supply Voltage (**VDDVARIO**, **VDD_SW_IN**, **VDD33_REG_IN**) (Note 16-1) . . . . . -0.5 V to +4.6 V

+3.3 V Analog Supply Voltage (**VDD33A**) (Note 16-1) . . . . . -0.5 V to +4.6 V

+2.5 V Analog Supply Voltage (**VDD25A**) (Note 16-1) . . . . . -0.5 V to +3.2 V

+1.2 V Analog Supply Voltage (**VDD12A**) (Note 16-1) . . . . . -0.5 V to +1.5 V

Digital Supply Voltage (**VDD12CORE**, **VDD12HSIC**) (Note 16-1) . . . . . -0.5 V to +1.5 V

Positive voltage on input signal pins, with respect to ground . . . . . +4.6 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.5 V

Storage Temperature . . . . . -65°C to +150°C

Lead Temperature Range. . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . +/-2 kV

Note 16-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 16.2, "Operating Conditions**", Section 16.5, "DC Specifications", or any other applicable section of this specification is not implied.

16.2 Operating Conditions**

Supply Voltage (**VDD33_REG_IN**) (Note 16-1) . . . . . +2.97 V to +3.63 V

Supply Voltage (**VDD_SW_IN**) (Note 16-1) . . . . . +2.97 V to +3.63 V

Supply Voltage (**VDDVARIO**) (Note 16-1) . . . . . +1.62 V to +3.63 V

+3.3 V Analog Supply Voltage (**VDD33A**) (Note 16-1) . . . . . +2.97 V to +3.63 V

+2.5 V Analog Supply Voltage (**VDD25A**) (Note 16-1) . . . . . +2.38 V to +2.63 V

+1.2 V Analog Supply Voltage (**VDD12A**) (Note 16-1) . . . . . +1.1 V to +1.26 V

Digital Supply Voltage (**VDD12CORE**, **VDD12HSIC**) (Note 16-1) . . . . . +1.1 V to +1.26 V

Positive voltage on input signal pins, with respect to ground . . . . . +3.3 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.3 V

Ambient Operating Temperature in Still Air (T_A) . . . . . Note 16-2

Note 16-2 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

Proper operation of the device is guaranteed only within the ranges specified in this section. After the device has completed power-up, **VDDVARIO and **VDD_SW_IN** must maintain their voltage level with ±10%. Varying the voltage greater than ±10% after the device has completed power-up can cause errors in device operation.

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16.3 Package Thermal Specifications

TABLE 16-1: PACKAGE THERMAL PARAMETERS

Parameter	Symbol	°C/W	Velocity (meters/s)
Thermal Resistance Junction to Ambient	Θ_{JA}	26	0
Thermal Resistance Junction to Top of Case	Θ_{JC}	2.3	0
Thermal Resistance Junction to Board	Θ_{JB}	14	0
Thermal Resistance Junction to Bottom of Case	Ψ_{JT}	0.2	0

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51.

16.4 Current Consumption and Power Dissipation

This section details the power consumption of the device as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

16.4.1 SUSPEND0

TABLE 16-2: SUSPEND0 CURRENT & POWER

Parameter	Typical	Unit
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	60	mA
Power Dissipation	199	mW

16.4.2 SUSPEND1

TABLE 16-3: SUSPEND1 CURRENT & POWER

Parameter	Typical	Unit
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	60	mA
Power Dissipation	199	mW

16.4.3 SUSPEND2

TABLE 16-4: SUSPEND2 CURRENT & POWER

Parameter	Typical	Unit
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	2.4	mA
Power Dissipation	8	mW

16.4.4 SUSPEND3

TABLE 16-5: SUSPEND3 CURRENT & POWER

Parameter	Typical	Unit
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	183	mA
Power Dissipation	603	mW

16.4.5 OPERATIONAL

16.4.5.1 Hi-Speed (USB)

TABLE 16-6: HI-SPEED (USB) CURRENT & POWER

Parameter	Typical	Unit
1000BASE-T Full Duplex (USB Hi-Speed)		
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	211	mA
Power Dissipation	695	mW
100BASE-TX Full Duplex (USB Hi-Speed)		
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	126	mA
Power Dissipation	414	mW
10BASE-T Full Duplex (USB Hi-Speed)		
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	72	mA
Power Dissipation	237	mW

16.4.5.2 Hi-Speed HSIC

TABLE 16-7: HI-SPEED (HSIC) CURRENT & POWER

Parameter	Typical	Unit
1000BASE-T Full Duplex (HSIC Hi-Speed)		
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	207	mA
Power Dissipation	682	mW
100BASE-TX Full Duplex (HSIC Hi-Speed)		
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	122	mA
Power Dissipation	402	mW
10BASE-T Full Duplex (HSIC Hi-Speed)		
3.3 V Supply Current (**VDDVARIO**, **VDD33A**, **VDD33_REG_IN**, **VDD_SW_IN** = 3.3 V)	68	mA
Power Dissipation	224	mW

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16.4.5.3 Absolute Max Power Dissipation

TABLE 16-8: ABSOLUTE MAX POWER DISSIPATION

Parameter	Typical	Unit
Absolute Max Power Dissipation	781	mW

16.5 DC Specifications

TABLE 16-9: I/O BUFFER CHARACTERISTICS

Parameter	Symbol	Min	1.8V Typ	2.5V Typ	3.3V Typ	Max	Units	Notes
VIS Type Input Buffer								
Low Input Level	V_{ILI}	-0.3				0.39*VDDVARIO	V	
High Input Level	V_{IHI}	0.63*VDDVARIO				3.6	V	
Negative-Going Threshold	V_{ILT}	0.67	0.80	1.09	1.42	1.61	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	0.81	0.94	1.22	1.54	1.74	V	Schmitt trigger
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	100	141	123	127	245	mV	
Input Leakage (V_{IN} = VSS or VDDVARIO)	I_{IH}	-10				10	µA	Note 16-3
Input Capacitance	C_{IN}					2	pF	
O8 Type Input Buffer								
Low Output Level	V_{OL}					0.4	V	I_{OL} = -8 mA
High Output Level	V_{OH}	VDDVARIO-0.4					V	I_{OH} = 8 mA
OD8 Type Input Buffer								
Low Output Level	V_{OL}					0.4	V	I_{OL} = -8 mA
O12 Type Input Buffer								
Low Output Level	V_{OL}					0.4	V	I_{OL} = -12 mA
High Output Level	V_{OH}	VDDVARIO-0.4					V	I_{OH} = 12 mA
OD12 Type Input Buffer								
Low Output Level	V_{OL}					0.4	V	I_{OL} = -12 mA

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TABLE 16-9: I/O BUFFER CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Min	1.8V Typ	2.5V Typ	3.3V Typ	Max	Units	Notes
HSIC Type Input Buffer								
Low Input Level	V_{IL}	-0.3				0.35***VDD12A**	V	
High Input Level	V_{IH}	0.65***VDD12A**				**VDD12A**+0.3	V	
Low Output Level	V_{OL}					0.25***VDD12A**	V	
High Output Level	V_{OH}	0.75***VDD12A**					V	
I/O Pad Drive Strength (HSIC_DS_EN50=low)	O_D	38		40		42	Ohm	Note 16-4
I/O Pad Drive Strength (HSIC_DS_EN50=high)	O_D	47.5		50		52.5	Ohm	Note 16-4
ICLK Type Input Buffer (XI Input)								Note 16-5
Low Input Level	V_{ILI}	-0.3				0.50	V	
High Input Level	V_{IHI}	0.85				**VDD33**	V	

Note 16-3 This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add ±50 uA per-pin (typical).

Note 16-4 Refer to the HSIC 50ohm Driver Data and Strobe Enable (HSIC_DS_EN50) field of the HSIC Enable Register (HSIC_EN) for permissible values.

Note 16-5 **XI** can optionally be driven from a 25 MHz singled-ended clock oscillator.

16.6 AC Specifications

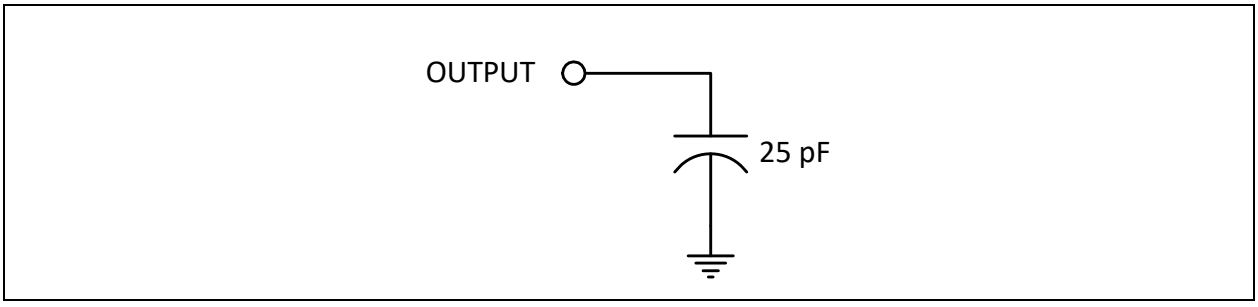
This section details the various AC timing specifications of the device.

Note: The Ethernet TX/RX pin timing adheres to the IEEE 802.3 specification. Refer to the IEEE 802.3 specification for detailed Ethernet timing information.

16.6.1 EQUIVALENT TEST LOAD

Output timing specifications assume a 25 pF equivalent test load, unless otherwise noted, as illustrated in Figure 16-1.

FIGURE 16-1: OUTPUT EQUIVALENT TEST LOAD



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16.6.2 RESET_N TIMING

Figure 16-2 illustrates the **RESET_N** timing requirements. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified

FIGURE 16-2: RESET_N TIMING

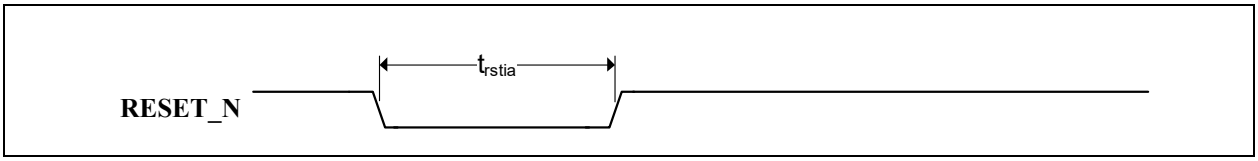

TABLE 16-10: RESET_N TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	**RESET_N** input assertion time	1			µs

16.6.3 JTAG TIMING

This section specifies the JTAG timing of the device.

FIGURE 16-3: JTAG TIMING

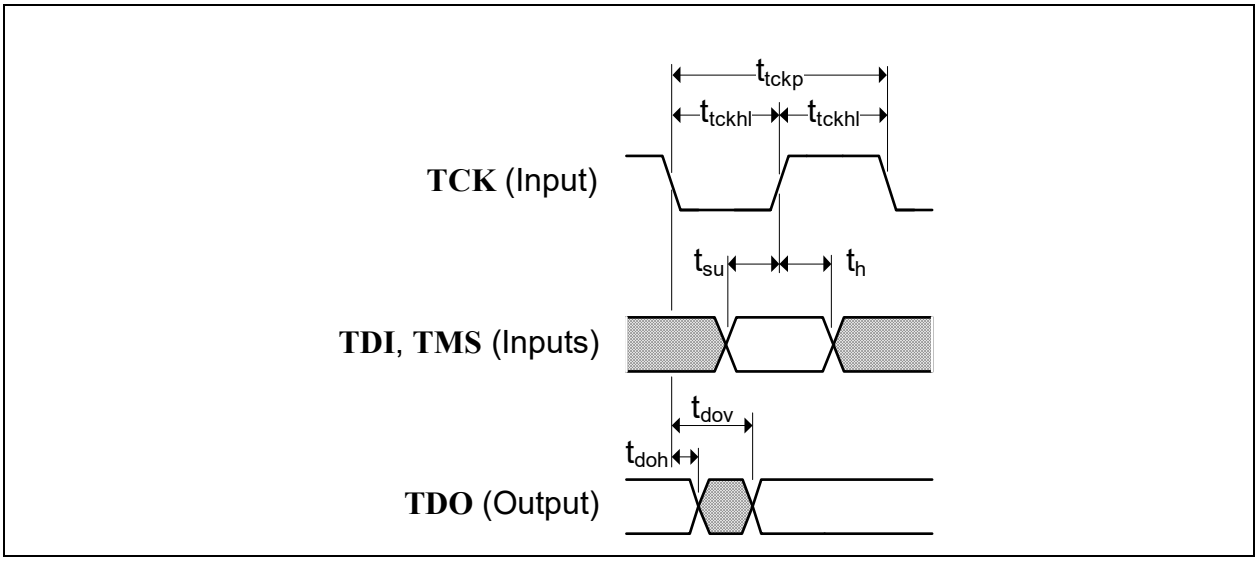

TABLE 16-11: JTAG TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{tckp}	**TCK** clock period	40			ns
t_{tckhl}	**TCK** clock high/low time	t_{tckp}*0.4		t_{tckp}*0.6	ns
t_{su}	**TDI**, **TMS** setup to TCK rising edge	10			ns
t_h	**TDI**, **TMS** hold from TCK rising edge	10			ns
t_{dov}	**TDO** output valid from TCK falling edge			16	ns
$t_{doinvld}$	**TDO** output invalid from TCK falling edge	0			ns

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16.6.4 EEPROM TIMING

This section specifies the EEPROM timing requirements for the device.

FIGURE 16-4: EEPROM TIMING

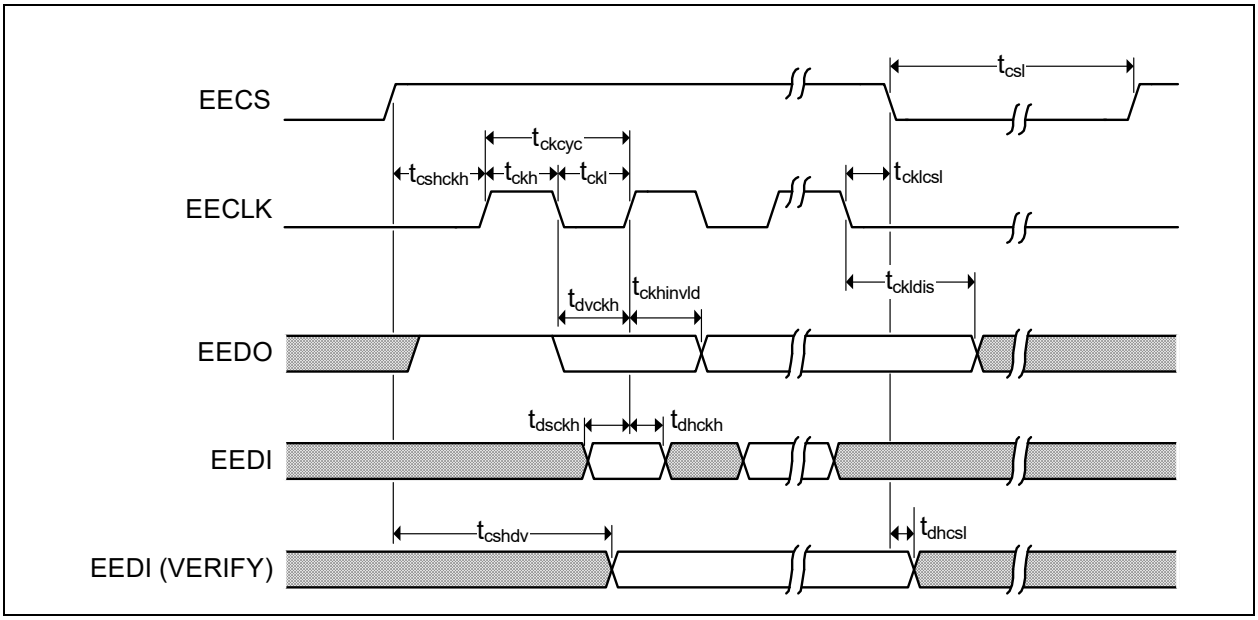

TABLE 16-12: EEPROM TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{ckcyc}	**EECLK** Cycle time	1110		1130	ns
t_{ckh}	**EECLK** High time	550		570	ns
t_{ckl}	**EECLK** Low time	550		570	ns
t_{cshckh}	**EECS** high before rising edge of **EECLK**	1070			ns
t_{cklcsl}	**EECLK** falling edge to **EECS** low	30			ns
t_{dvckh}	**EEDO** valid before rising edge of **EECLK**	550			ns
$t_{ckhinvld}$	**EEDO** invalid after rising edge **EECLK**	550			ns
t_{dsckh}	**EEDI** setup to rising edge of **EECLK**	90			ns
t_{dhckh}	**EEDI** hold after rising edge of **EECLK**	0			ns
t_{ckldis}	**EECLK** low to data disable (OUTPUT)	580			ns
t_{cshdv}	**EEDIO** valid after **EECS** high (VERIFY)			600	ns
t_{dhcsl}	**EEDIO** hold after **EECS** low (VERIFY)	0			ns
t_{csl}	**EECS** low	1070			ns

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16.7 Clock Circuit

The device can accept either a 25MHz crystal (preferred) or a 25 MHz single-ended clock oscillator (+/- 50ppm) input. If the single-ended clock oscillator method is implemented, **XO** should be left unconnected and **XI** should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XI/XO**). See Table 16-13 for the recommended crystal specifications.

TABLE 16-13: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut			AT, typ			
Crystal Oscillation Mode			Fundamental Mode			
Crystal Calibration Mode			Parallel Resonant Mode			
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	+/-50	PPM	Note 16-6
Frequency Stability Over Temp	F_{temp}	-	-	+/-50	PPM	Note 16-6
Frequency Deviation Over Time	F_{age}	-	+/-3 to 5	-	PPM	Note 16-7
Total Allowable PPM Budget		-	-	+/-50	PPM	Note 16-8
Shunt Capacitance	C_O	-	-	6	pF	
Load Capacitance	C_L	-	-	18	pF	
Motional Inductance	LM			10	mH	
Drive Level	P_W	-	-	250	uW	
Equivalent Series Resistance	R_1	-	-	50	Ohm	
Operating Temperature Range		Note 16-9	-	Note 16-10	°C	
XI Pin Capacitance		-	3 typ	-	pF	Note 16-11
XO Pin Capacitance		-	3 typ	-	pF	Note 16-11

Note 16-6 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependent. Since any particular application must meet the IEEE +/-50 PPM Total PPM Budget, the combination of these two values must be approximately +/-45 PPM (allowing for aging).

Note 16-7 Frequency Deviation Over Time is also referred to as Aging.

Note 16-8 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as +/- 50 PPM.

Note 16-9 0°C for commercial version, -40°C for industrial version.

Note 16-10 +70°C for commercial version, +85°C for industrial version.

Note 16-11 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The **XI/XO** pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

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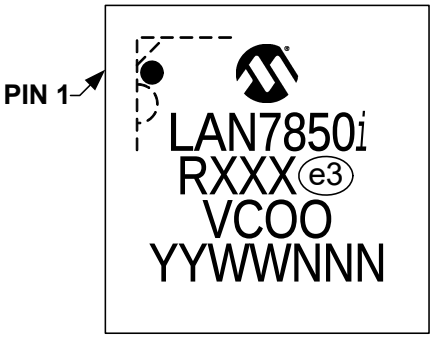
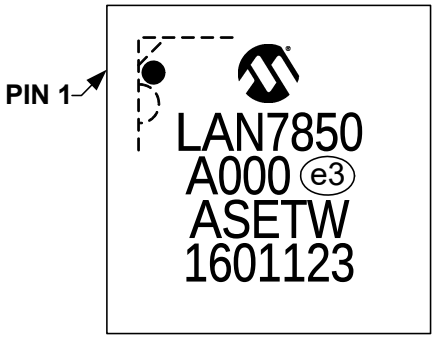
17.0 PACKAGE INFORMATION

17.1 Package Marking Information

56-Lead SQFN (8x8x0.9 mm)



Example



Legend:		
	LAN7850	Product part number
	i	Temperature range designator (Blank = commercial, *i* = industrial)
	R	Major product revision
	XXX	Internal engineering code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	V	Plant of assembly
	COO	Country of origin
	YYWWNNN	Traceability code

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17.2 Package Details

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

FIGURE 17-1: 56-SQFN PACKAGE (DRAWING)

56-Lead Plastic Quad Flat, No Lead Package [QFN] – Package Code: 4F
8x8x0.9mm Body, 5.9x5.9mm Exposed Pad, 0.4mm Contact Length

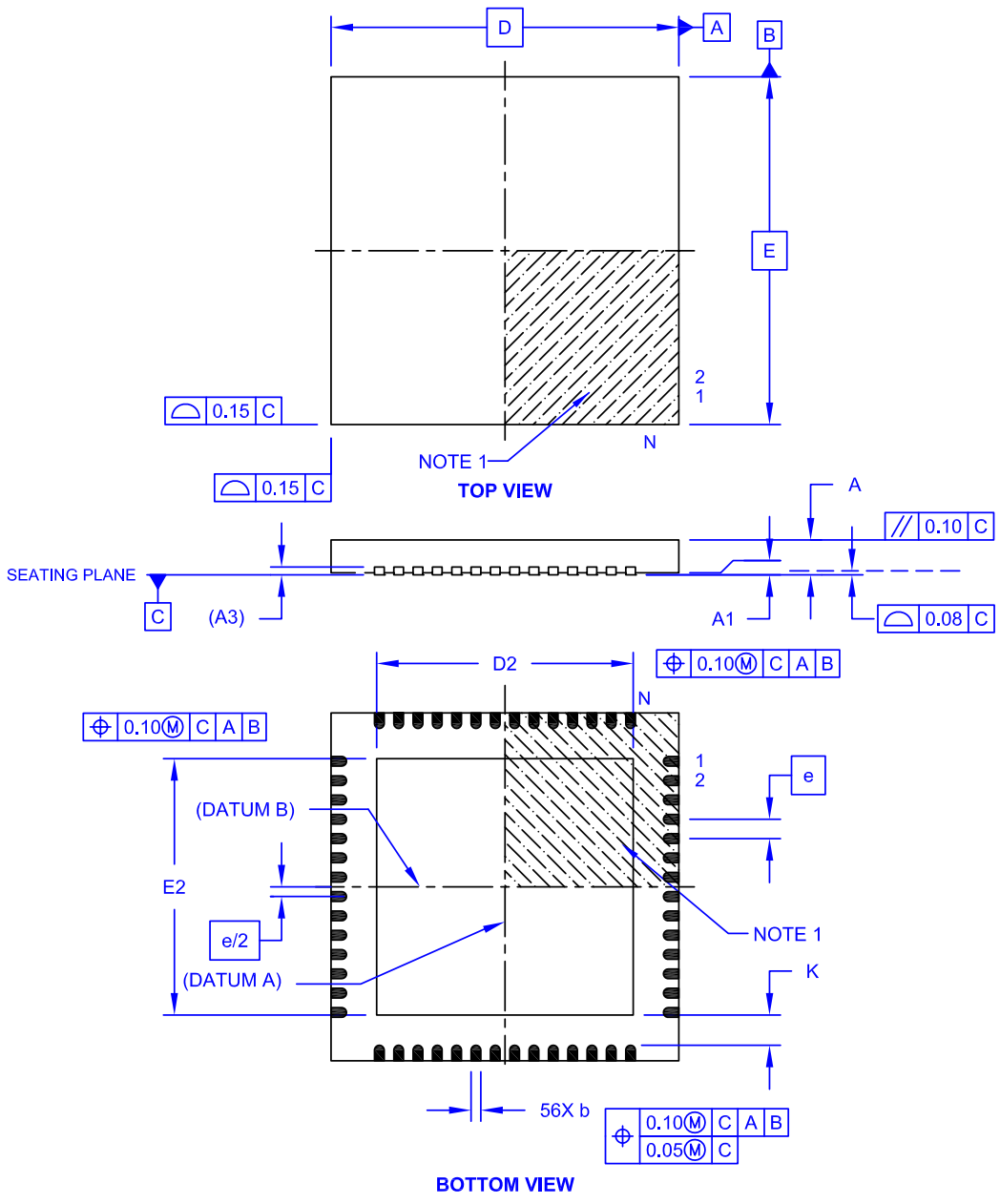

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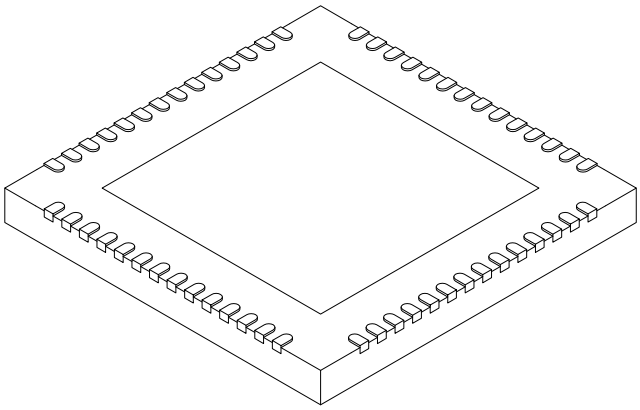
FIGURE 17-2: 56-SQFN PACKAGE (DIMENSIONS)

56-Lead Plastic Quad Flat, No Lead Package [QFN] – Package Code: 4F
8x8x0.9mm Body, 5.9x5.9mm Exposed Pad, 0.4mm Contact Length



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		56	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	5.80	5.90	6.00
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	5.80	5.90	6.00
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.55	0.65	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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18.0 DATA SHEET REVISION HISTORY

TABLE 18-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001993F (12-02-21)	Table 3-2, "Pin Descriptions"	TEST pin description modified.
DS00001993E (12-05-18)	Cover, Section 9.0, "Gigabit Ethernet PHY (GPHY)," on page 90, Section 9.1, "Category 5 Twisted Pair Media Interface," on page 90, Section 15.3.2, "Ethernet PHY Extended Page 1 Registers," on page 246,	Removed references to cable diagnostic functions.
DS00001993D (07-06-17)	Table 3-1, "Pin Assignments"	Removed +2.5V from Switcher Input Voltage description.
	Figure 4-1, "Power Connection Diagram"	- Changed +2.5-3.3V to +3.3V - Modified note under figure
DS00001993C (10-17-16)	Product Identification System	Updated ordering codes.
DS00001993B (03-31-16)	All	Initial Release

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PRODUCT IDENTIFICATION SYSTEM

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PART NO.	[X](1)	-	[X]	/	XXX
Device	Tape and Reel Option		Temperature Range		Package

Device:	LAN7850	
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel(Note 1)
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)	
Package:	8JX = 56-pin SQFN	

Examples:

a) LAN7850/8JX
Tray, Commercial temp., 56-pin SQFN

b) LAN7850T-I/8JX
Tape & reel, Industrial temp., 56-pin SQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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