LAN9381/2/3/4

7-Port AVB/TSN Gigabit Ethernet Switch with Integrated CPU and 100BASE-T1 PHYs

Highlights

- Up to 5x 100BASE-T1 ports
- 1x 100BASE-TX port (LAN9382/LAN9384 only)
- Up to 3x RGMII/RMII/MII, 1x (1G/2.5G) SGMII port
- 300MHz ARM Cortex M7 CPU subsystem
- Integrated 2MB flash code memory
- Hardware security engine
- Cascade mode for higher port count with LAN937x or LAN938x families
- Enhanced EMC performance
- Full AVB Audio Video Bridging
- Time Sensitive Networking Support
- OPEN Alliance TC10 Sleep/Wakeup
- LinkMD®+ enhanced cable diagnostics
- FlexPWR® technology power management
- Small-footprint 128-pin TQFP (14 x 14 mm) package
- AEC-Q100 automotive product qualification
- Grade 2 Automotive temperature (-40°C to +105°C)
- Functional safety ready

Target Applications

- Advanced Driver-Assistance Systems (ADAS)
- Infotainment
- Telematics & Smart Antennas
- In-Vehicle Backbone
- Gateways

Features

- Switch Management Capabilities
  - Full wire-speed, non-blocking Gigabit switch core
  - Compliant to OPEN TC11 switch requirements
  - <140ms “Ethernet Ready” time, with secure boot
  - 1K MAC table
  - IEEE 802.1Q VLAN support
  - AVB and TSN hardware support:
    - IEEE 802.1AS time synchronization
    - IEEE 1588v2 PTP and clock synchronization
    - IEEE 802.Qav traffic shaping
    - IEEE 802.1Qbv (TSN) time-aware scheduler
    - IEEE 802.1Qci (TSN) ingress filtering and policing
    - IEEE 802.1QCB (TSN) frame replication and elimination
  - 8 shapers per port, one for each queue
  - Smart low-latency cut-through forwarding mode
  - Deep Packet Inspection (DPI) using TCAM
    - TCAM classification of Layers 2,3,4 and beyond
- Up to 5x Integrated 100BASE-T1 Ethernet PHYs (4x for LAN9381/LAN9382, 5x for LAN9383/LAN9384)
  - Compliant with IEEE 802.3bw-2015
  - 100Mbps over single balanced twisted pair cable
  - Extended cable reach >15m
  - On-chip filtering & termination for balanced UTP cable
- 1x Integrated 100BASE-TX/10BASE-T Port (LAN9382/LAN9384 only)
  - Compliant with IEEE 802.3/802.3u
  - Auto-negotiation and Auto-MDI/MDI-X support
  - On-chip termination resistors and internal biasing
- Up to 3x Configurable External MAC Ports
  - Reduced Gigabit Media Independent Interface (RGMII)
  - Reduced Media Independent Interface (RMII) with 50MHz reference clock input/output option
  - Media Independent Interface (MII) in PHY/MAC mode
  - Serial Gigabit Media Independent Interface (SGMII)
- IEEE 1588v2 PTP and Clock Synchronization
  - Transparent Clock (TC) with auto correction update
  - Master and slave Ordinary Clock (OC) support
  - End-to-end (E2E) or peer-to-peer (P2P)
  - PTP multicast and unicast message support
  - PTP message transport over IPv4/v6 and IEEE 802.3
  - IEEE 1588v2 PTP packet filtering
  - Time Aware Precision GPIO
- CPU Subsystem
  - 300MHz ARM Cortex M7 CPU
  - 64KB immutable ROM
  - 768KB RAM with configurable ITCM and DTCM (32KB to 512KB)
  - 2MB flash
  - 2x SPI master/slave controllers
  - I^2C interface
  - Secure I^2C EEPROM configuration
  - Secure JTAG implementation
- Advanced Diagnostics
  - OPEN Alliance (TC1) advanced diagnostics compliant
  - LinkMD®+ cable diagnostic capabilities
    - Determines cable opens/shorts/length (TX & T1)
    - Signal Quality Indicator (SQI) with MSE, peak values, and peak/threshold interrupt (T1)
  - Self-test packet generator/detector
  - Loopback modes
  - Extended MIB performance counters
- EtherGREEN™ Energy Efficiency
  - Low-power 100BASE-T1 PHY technology
  - OPEN Alliance TC10 sleep/wakeup (partial networking)
  - Non-TC10 link partner energy detect wake-up support
- Low RF Emissions
  - Integrated transmission filtering
  - xMII data and 125MHz clock prog. slew rate control
  - OPEN Alliance (TC6) RGMII EPL compliant
  - Exceeds OPEN Alliance Transceiver EMC Test Spec.

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- Hardware Security Engine
  - SHA256/512 Digest Engine (for fast secure boot)
  - ECDSA cryptographic accelerator
  - Optional firmware code (AES-128/256) encryption/decryption in Flash
  - OTP immutable key storage
  - Truly immutable boot ROM implemented in physical hardware ROM
  - Re-flashing over Ethernet port for OTA (Over The Air) updates
  - Optional TA100 Trust Anchor support
  - Deep packet inspection support for every packet/port
  - IEEE 802.1AR (802.1x) port and MAC authentication
  - IEEE 802.1Qci per stream ingress filtering & policing
- Functional Safety Ready
  - Fault diagnostic safety features include:
    -System clock monitor with standby clock switchover
    -Memory check with fault injection
    -ECC RAM
    -Self test on boot with fault injection
    -Gap free over and under voltage detection with interrupt
    -SHA-256 secure boot
    -Performance monitoring counters
    -IEEE 802.1CB frame replication and elimination support
    -Cable diagnostics (opens/shorts/distance)
    -SQI (receive signal quality monitoring)
  - Collateral support includes Safety Manual and FMEDA calculator (on request)

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1.0 INTRODUCTION

1.1 General Description

The Microchip LAN9381/LAN9382/LAN9383/LAN9384 (LAN938x) is a scalable, compact and cost-effective, multi-Port AVB/TSN 100BASE-T1 Ethernet Switch family based on the IEEE 802.3bw-2015 specification. The LAN938x incorporates a layer-2+ managed high-performance Ethernet switch, up to five (four for the LAN9381/2, five for the LAN9383/4) 100BASE-T1 physical layer transceivers (PHYs), up to three MAC ports, and an ARM Cortex M7 CPU subsystem. With the addition of integrated 2MB code flash memory and a hardware security engine, the LAN938x family delivers a fully integrated, single-chip AVB/TSN bridge solution. An additional IEEE 802.3/802.3u complaint 100BASE-TX (LAN9382/4 only) port is provided for applications where an integrated automotive OBD port is required. The LAN938x is available in a Grade 2 Automotive (-40°C to +105°C) temperature range and is qualified to AEC-Q100 automotive use cases such as gateways, Automated Driver-Assistance Systems (ADAS), infotainment, telematics, and in-vehicle networking.

The LAN938x fully supports the IEEE family of Audio Video Bridging (AVB) standards, which provide high Quality of Service (QoS) for latency sensitive traffic streams over Ethernet. Hardware time-stamping and time-keeping features support IEEE 802.1AS (gPTP) and IEEE 1588v2 (PTP) time synchronization. All ports feature eight egress queues and an IEEE 802.1Qav credit based traffic shaper and time aware scheduler, as per the IEEE 802.1Qbv specification. Additional Time Sensitive Networking functionality includes an IEEE 802.1Qci ingress filtering and policing engine, and IEEE 802.1CB (TSN) frame replication and elimination support.

The LAN938x can operate either as a standalone bridge or as a system co-processor with an external host CPU. The external host can manage the switch via SPI, MDIO, or an Ethernet port, in a secure manner.

Additionally, a robust assortment of EtherGREEN^{TM} energy efficiency features are provided, including Open Alliance TC10 sleep/wakeup partial networking, non-TC10 link partner energy detect wake-up, and ultra-deep-sleep power down.

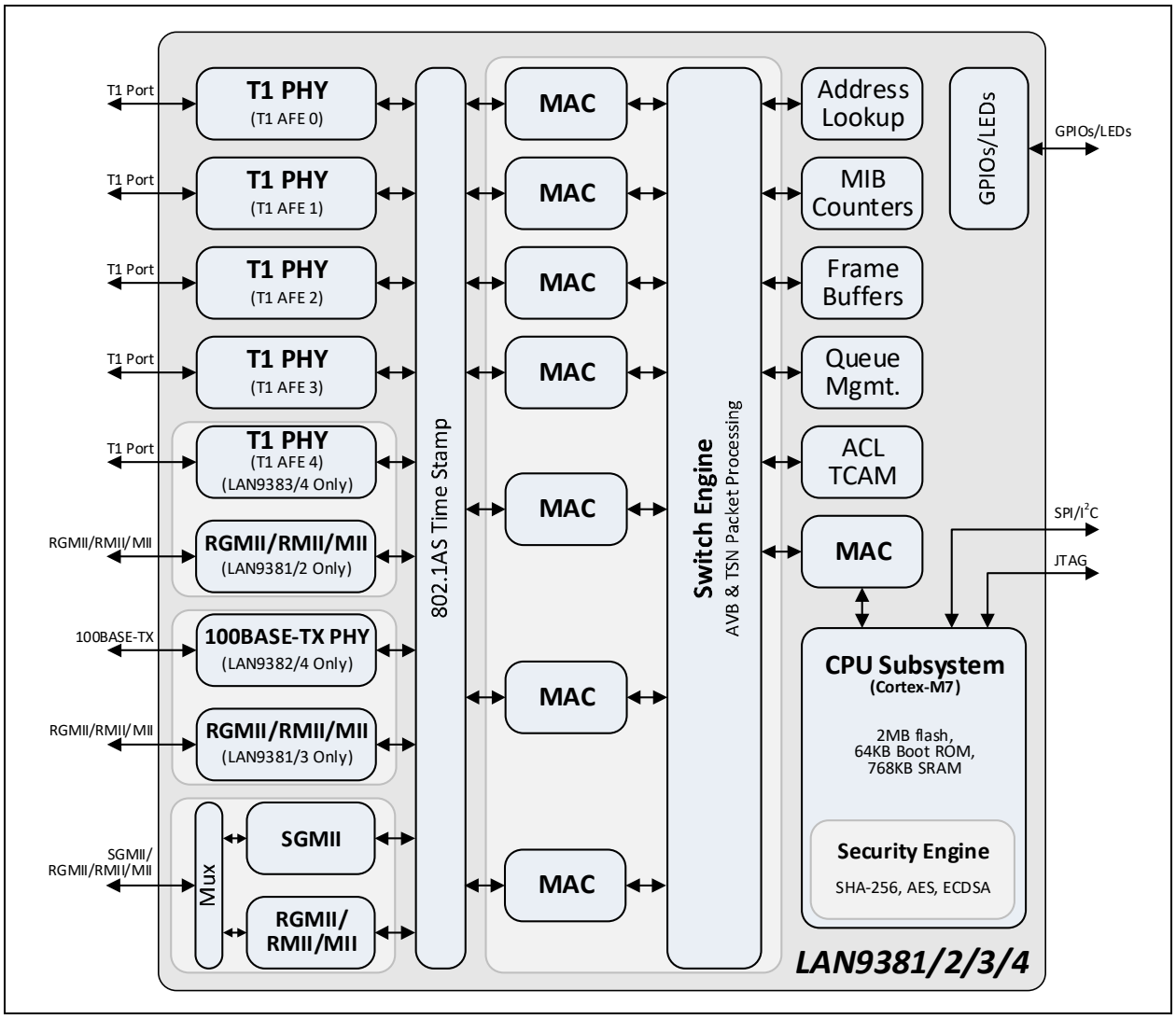
Table 1-1 provides a summary of the feature differences between members of the LAN938x device family:

TABLE 1-1: LAN938X FAMILY FEATURE MATRIX

Part Number	Package	# of Integrated 100BASE-T1 PHYs	100BASE-TX Ports	RGMII/RMII/MII Ports	SGMII/ RGMII/RMII/MII Ports	Full AVB Support	Time Sensitive Networking Support	OPEN Alliance TC10 Sleep/Wakeup Energy Efficiency	Cascade Mode Support	AEC-Q100 Qualification	Grade 2 Automotive Temp. (-40° to 105°C)
LAN9381	128-TQFP	4	0	2	1	X	X	X	X	X	X
LAN9382	128-TQFP	4	1	1	1	X	X	X	X	X	X
LAN9383	128-TQFP	5	0	1	1	X	X	X	X	X	X
LAN9384	128-TQFP	5	1	0	1	X	X	X	X	X	X

An internal block diagram of the LAN938x is shown in Figure 1-1.

FIGURE 1-1: INTERNAL BLOCK DIAGRAM



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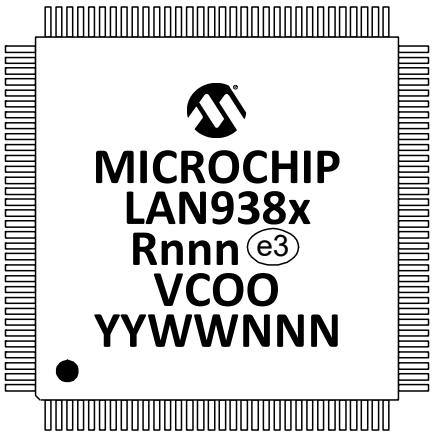
2.0 PACKAGE INFORMATION

2.1 Package Marking Information

128-TQFP-EP



Legend:	x	Part number (1, 2, 3, or 4)
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	V	Plant assembly
	COO	Country of origin
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

2.2 Package Drawings

FIGURE 2-1: PACKAGE (DRAWING)

128-Lead Thin Quad Flatpack (6XX) - 14x14x1.0 mm Body [TQFP]
With 10x10 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

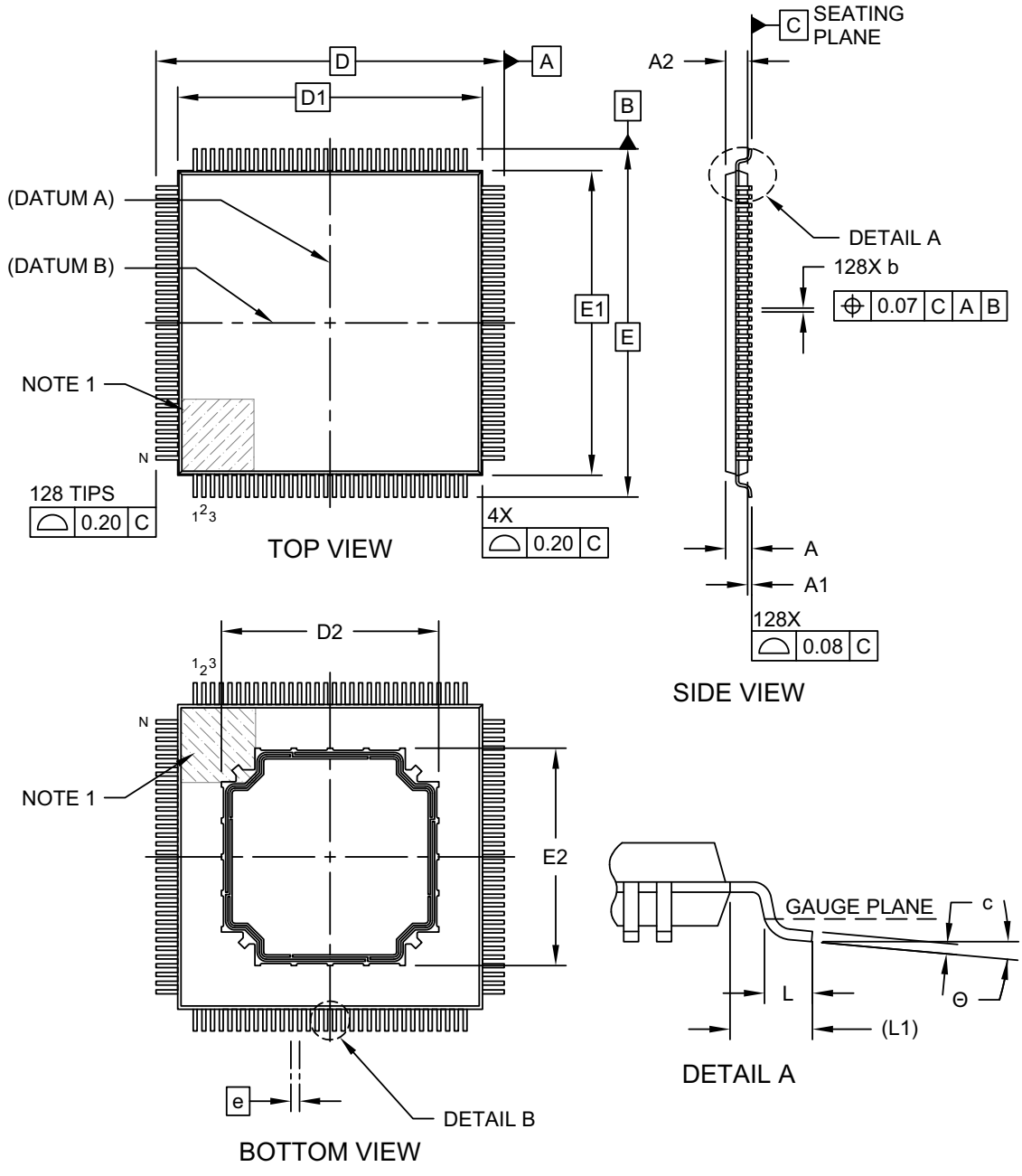


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FIGURE 2-2: PACKAGE (DIMENSIONS)

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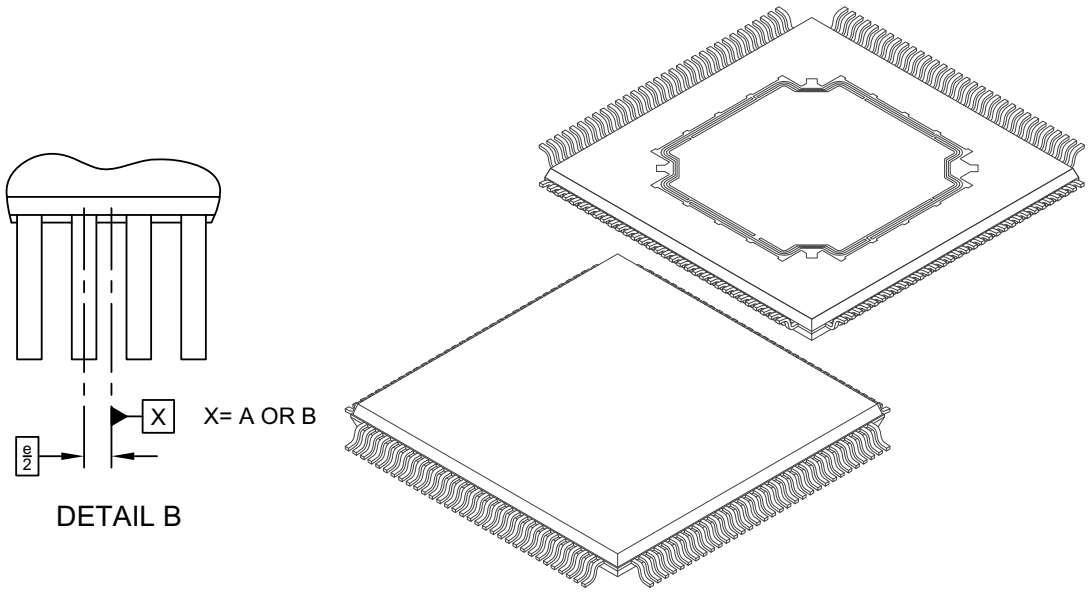

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		128	
Pitch	e		0.40 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		16.00 BSC	
Molded Package Length	D1		14.00 BSC	
Exposed Pad Length	D2	9.85	10.00	10.15
Overall Width	E		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Exposed Pad Width	E2	9.85	10.00	10.15
Terminal Width	b	0.13	0.18	0.23
Terminal Length	L	0.45	0.60	0.75
Terminal Thickness	c	0.09	-	0.20
Footprint	(L1)		1.00 REF	
Footprint Angle	Θ	0°	-	7°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-418B Sheet 2 of 2

FIGURE 2-3: PACKAGE (LAND PATTERN)

128-Lead Thin Quad Flatpack (6XX) - 14x14x1.0 mm Body [TQFP]
With 10x10 mm Exposed Pad

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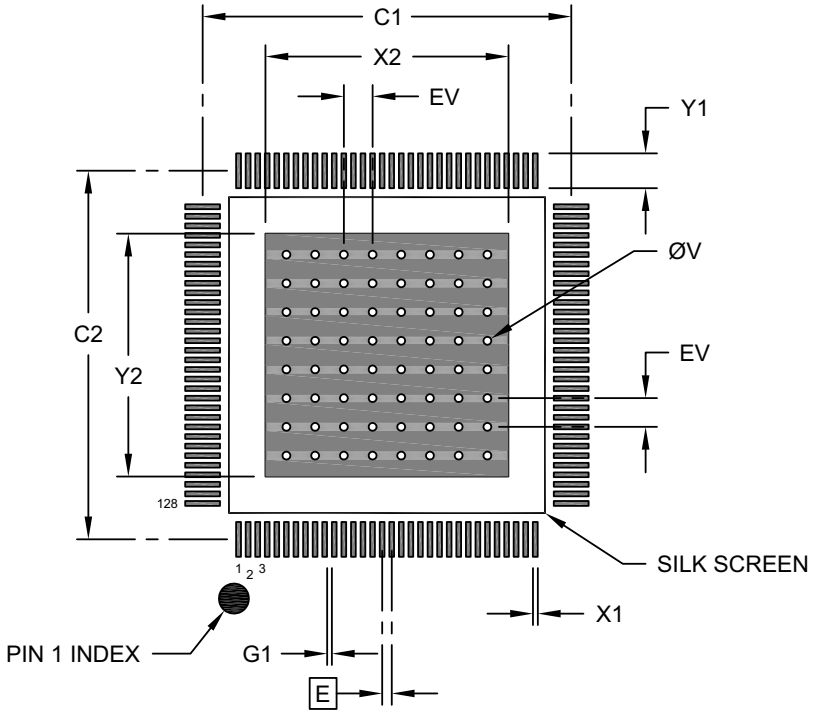

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			10.50
Center Pad Length	Y2			10.50
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X128)	X1			0.20
Contact Pad Length (X128)	Y1			1.54
Contact Pad to Contact Pad (X124)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2418B

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APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS0003296B (01-28-20)	Features/Cover	Modified third bullet under Highlights: Changed “1 x SGMII port” to “1x (1G/2.5G) SGMII port” Modified Hardware Security Engine as follows: Changed first bullet, “SHA256 Digest” to “SHA256/512” Digest Changed third bullet, “encryption/decryption” to “(AES-128/256) encryption/decryption”
DS0003296A (11-15-19)	Initial Document Release.	

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PART NO.	[X](1)	-	X	/	XXX	XXX
Device	Tape & Reel Option		Temp. Range		Package	Automotive Code

Device:	LAN9381 = 7-Port Switch (4 T1, 1 SGMII, 2 RGMII) LAN9382 = 7-Port Switch (4 T1, 1 SGMII, 1 RGMII, 1 TX) LAN9383 = 7-Port Switch (5 T1, 1 SGMII, 1 RGMII) LAN9384 = 7-Port Switch (5 T1, 1 SGMII, 1 TX)	
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel (Note 1)
Temperature Range:	-V	= -40°C to +105°C (Grade 2 Automotive)
Package:	6XX	= 128-pin TQFP-EP
Automotive Code:	Vxx	= 3 character code with “V” prefix, specifying automotive product

Examples:

a) LAN9381-V/6XXVAO
Standard packaging,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

b) LAN9381T-V/6XXVAO
Tape & reel,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

c) LAN9382-V/6XXVAO
Standard packaging,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

d) LAN9382T-V/6XXVAO
Tape & reel,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

e) LAN9383-V/6XXVAO
Standard packaging,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

f) LAN9383T-V/6XXVAO
Tape & reel,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

g) LAN9384-V/6XXVAO
Standard packaging,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

h) LAN9384T-V/6XXVAO
Tape & reel,
Grade 2 Automotive temperature,
128-pin TQFP-EP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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