PM8363

QuadPHY® 1GR

4 CHANNEL PHYSICAL LAYER TRANSCEIVER WITH GIGABIT ETHERNET PCS AND RGMII INTERFACE

Data Sheet

Released

Issue No. 4: December 2005

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U.S. Patent No. -6,552,619

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Revision History

Issue No.	Issue Date	Details of Change
4	December 2005	• Updated ordering information including RoHS-compliant device details.
3	May 2004	• MDIO timing updated • HSTL drive levels updated • VDDA current updated • Power Requirements updated • Device latency updated • 933Mbit/s data rate support added
2	April 2003	Initial release to customers.
1	April 2003	Initial internal release.

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1 Definitions

The following table defines terms and abbreviations used in this document.

Table 1 Definitions

Term	Definition
ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
BIST	Built-in Self Test
CABGA	Chip Array Ball Grid Array
CMOS	Complementary Metal-oxide Silicon
COL	Collision Detect.
CRS	Carrier Sense
DDR	Dual Data Rate or Double Data Rate
HSTL	High Speed Transceiver Logic
FIFO	First In, First Out
IEEE	Institute of Electrical and Electronics Engineers
IPG	Interpacket Gap
JTAG	Joint Test Action Group
MDC/MDIO	Management Data Clock/Management Data Input/Output
PCS	Physical Coding Sublayer
RGMII	Reduced Gigabit Medium-Independent Interface
RTBI	Reduced Ten Bit Interface

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2 Features

General

- Four 933Mbit/s to 1.25 Gbit/s IEEE 802.3-2000 Gigabit Ethernet and Fibre Channel Physical Interfaces (RTBI serdes mode only) (FC-PI) System Compliant Transceivers.
- Integrated clock synthesis, clock recovery, serializer/deserializer, built-in self-test, 8B/10B codec and IEEE 802.3-2000 Gigabit Ethernet Physical Coding Sublayer (PCS) logic.
- Rate matching via IDLE character insertion and deletion capable of compensating up to ±200 ppm of clock difference between reference clock and incoming serial data stream.
- Pin programmable or software configurable operation using 2 pin IEEE 802.3 MDC/MDIO serial management interface.
- Ultra-low power operation using 0.18µ technology.

Serial Interface

- High-speed outputs feature programmable output current to optimize drive distance and power - directly drives 50 Ω (100 Ω differential) systems.
- Direct AC coupled interface to copper serial backplanes, optics and coaxial cable.

Parallel Interface

- DDR parallel interface with synchronous receive clock (clock forwarding).
- Local or Recovered Receive Clock Modes.
- Supports RGMII/RTBI (Reduced Ten-bit Interface) v2.0 standards.
- Receive channel output clocks eliminate the need for PLLs in interface ASICs.
- Supports 1.5V JEDEC HSTL class I and 1.8V Expanded HSTL class I for unterminated DDR interface.
- Supports 2.5V /1.8V LVCMOS for rest of digital interface.

Test Features

- IEEE 1149.1 JTAG Boundary Scan support.
- Built-in self-test (BIST) via internal packet generator/checker.
- Per-channel control of serial and parallel loopback.
- 8B/10B error counters.

Physical

- Thermally enhanced 196-pin, 15mm x 15mm CABGA Package.

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3 References

1. IEEE 802.3-2000 Gigabit Ethernet, 2000 Edition.

2. Methodologies for Jitter and Signal Quality Specification (MJSQ) Rev. 4.0.

3. Fibre Channel Physical Interfaces (FC-PI) Rev. 13.

4. IEEE 1149.1-2001 Standard Test Access Port and Boundary Scan Architecture, 23 July 2001.

5. Reduced Gigabit Media Independent Interface (RGMII), December 10, 2000, Revision 2.0.

6. HSTL 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits, EIA/HESD8-6, August 1995.

7. Electronic Industries Association. *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)*: EIA/JESD51. December 1995.

8. Electronic Industries Alliance 1999. *Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board: JESD51-8*. October 1999.

9. Telcordia Technologies. *Network Equipment-Building System (NEBS) Requirements: Physical Protection: Telcordia Technologies Generic Requirements GR-63-CORE*. Issue 1. October 1995.

10. SEMI (Semiconductor Equipment and Materials International). *SEMI G30-88 Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages*. 1988.

11. PMC-Sierra, Inc. *JTAG Test Features Description Applications Note*. PMC-2021518. Issue 1, November 2002.

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4 Application Examples

The QuadPHY® 1GR has numerous applications in networking, storage and computing systems requiring high-speed serial I/O technology. Typical applications include backplane interconnect, Gigabit Ethernet line cards and Fiber Channel line cards.

- High-speed serial backplanes.
- IEEE 802.3-2000 Gigabit Ethernet dense line cards.
- ANSI X3T11 Fibre Channel dense line cards.
- Intra-system and inter-system interconnect.
- Chassis Extender.

4.1 Gigabit Ethernet Switch/Router Application

Figure 1 shows the QuadPHY 1GR in a Gigabit Ethernet Switch/Router Application. This application demonstrates the many uses of the QuadPHY 1GR. On the line cards, the QuadPHY 1GR functions as the Gigabit Ethernet Transceiver as well as the interface to the backplane. On the switch card, the QuadPHY 1GR provides a dense, high-speed interconnect to the line cards over a copper backplane.

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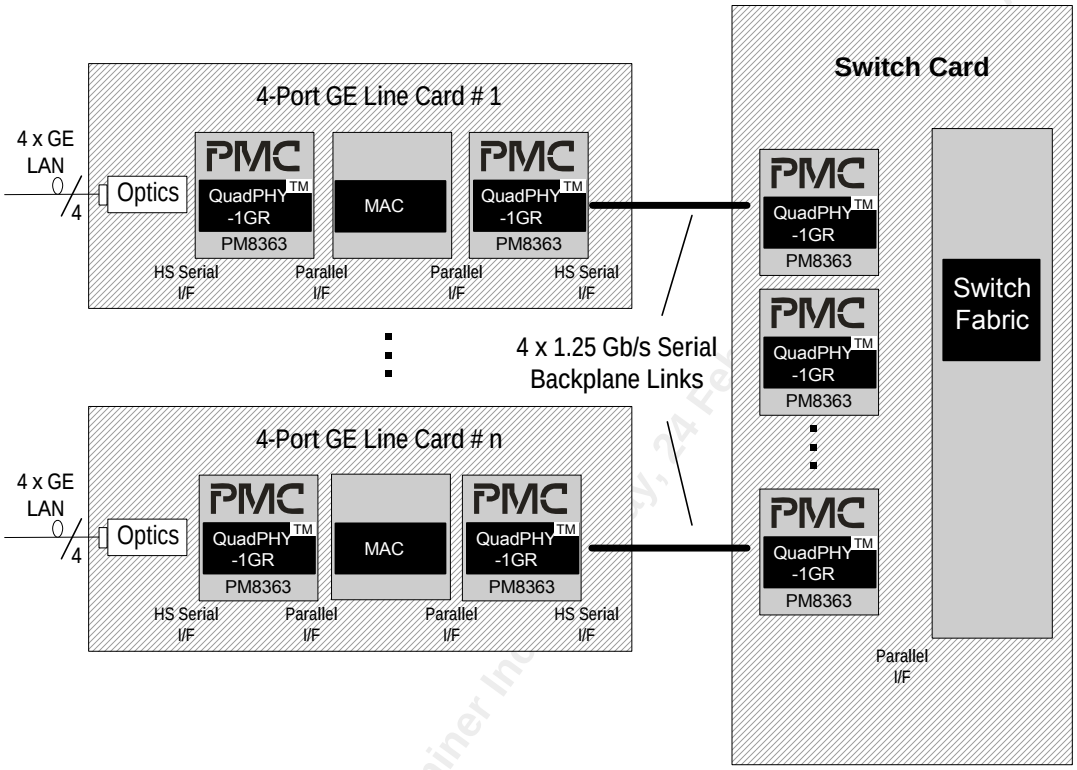
Figure 1 QuadPHY® 1GR in Switch/Router Applications



4.2 IEEE 802.3-2000 Gigabit Ethernet Transceiver

As a Gigabit Ethernet Transceiver, the QuadPHY 1GR integrates the PCS layer down to the PMA layer for fiber mediums, and from the PCS layer down to the PMD layer for copper mediums. The gray shaded cells in Figure 2 shows the supported functions of the device. The QuadPHY 1GR may be configured to enable or disable certain layers.

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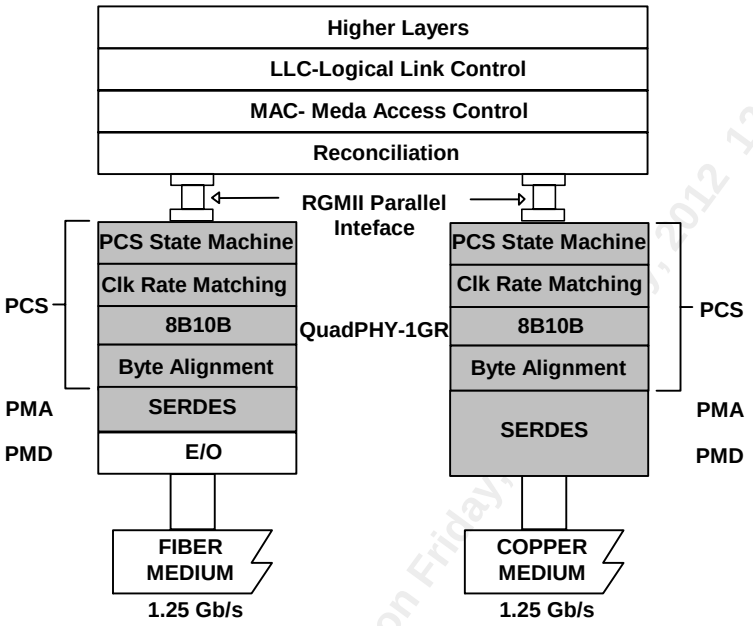
Figure 2 IEEE 802.3-2000 Gigabit Ethernet Supported Functions



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5 Block Diagram

The block diagram of the QuadPHY 1GR is shown in Figure 3 and the Loopback Diagram is shown in Figure 4.

Figure 3 QuadPHY 1GR Block Diagram

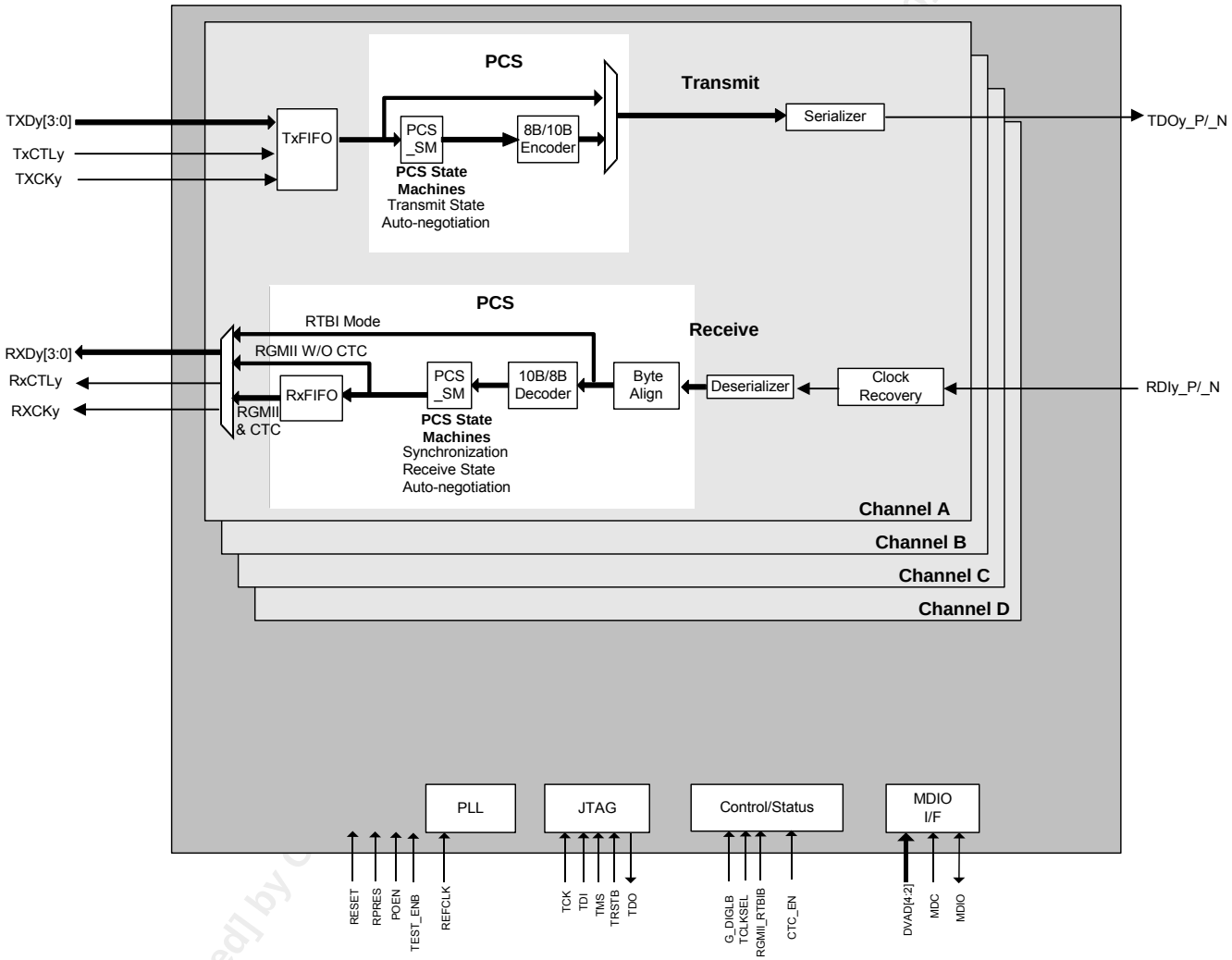

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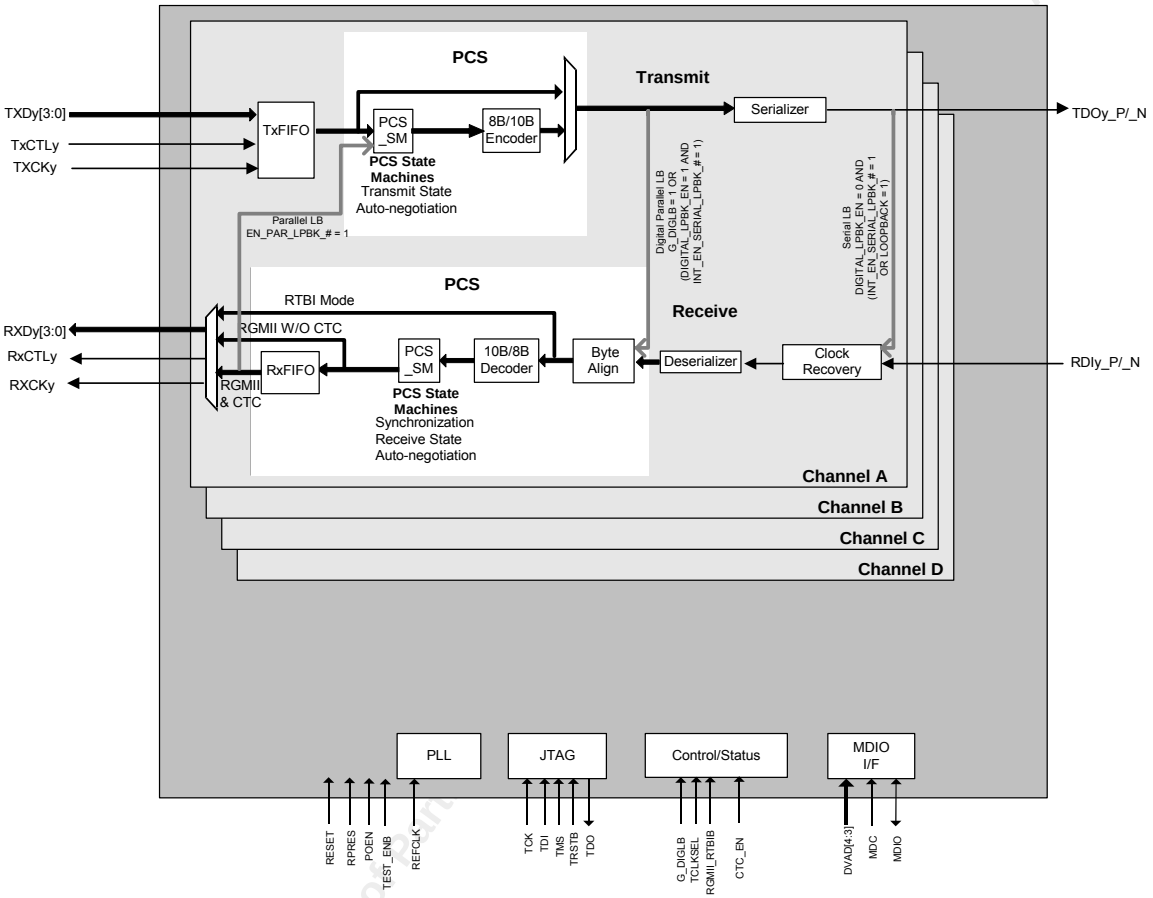
Figure 4 QuadPHY 1GR Loopback Diagram



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6 Description

6.1 Overview

The PM8363 QuadPHY 1GR is a low power, four-channel transceiver suitable for applications such as high-speed serial backplanes and dense Gigabit Ethernet line cards.

RTBI Mode

In the transmit direction, the PM8363 takes 10-bit data, serializes the data and transmits it differentially at 933Mbit/s to 1.25 Gbit/s. The PM8363 integrates an RTBI-compliant parallel interface, serializer, clock synthesis unit and differential transmitters.

In the receive direction, the PM8363 receives serial differential data, recovers the data and converts it back to 10-bit data. The PM8363 integrates differential receivers, clock recovery unit and an RTBI-compliant parallel interface. The received data can be output using the recovered clock only in RTBI mode.

The QuadPHY 1GR supports a Dual Data Rate (DDR) Parallel Interface with independent receive and transmit ports. The interface is RTBI compliant (as specified in the Reduced Gigabit Media Independent Interface Specification v2.0).

RGMII Mode

In the transmit direction, the PM8363 implements an RGMII interface which accepts RGMII formatted data, inputs it to the PCS Tx State Machine, performs 8B/10B encoding, serializes the data and transmits it differentially at 933Mbit/s to 1.25Gbit/s. The PM8363 integrates an RGMII compatible parallel interface, 8B/10B encoder, IEEE 802.3-2000 Gigabit Ethernet PCS logic, serializer, clock synthesis unit and differential transmitters.

In the receive direction, the PM8363 receives serial differential data, deserializes it, performs byte alignment, decodes the data, inputs it to the PCS Rx State Machine and outputs the data in RGMII format on the parallel interface. The PM8363 integrates differential receivers, clock recovery unit, IEEE 802.3-2000 Gigabit Ethernet PCS logic, 8B/10B decoder, receive FIFOs and an RGMII/RTBI compatible parallel interface. The received data can be output using the recovered clock or local clock in RGMII mode.

In addition to these fundamental SERDES functions, the PM8363 provides rate compensation. A system requires rate compensation if the transmitting device and receiving device are operating from different clock sources (i.e. are asynchronous). For example, if four asynchronous 1.25 Gbit/s links from four line cards are transmitting over a backplane to one receiving device, the receiving device must provide rate compensation to achieve a common local clock. The receive logic compensates for these clock differences by inserting or deleting special 8B/10B IDLE characters. Rate compensation can be enabled or disabled in RGMII mode, but cannot be enabled in RTBI mode.

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The QuadPHY 1GR supports a Dual Data Rate (DDR) Parallel Interface with independent receive and transmit ports. The interface is RGMII compatible (as specified in the Reduced Gigabit Media Independent Interface Specification v2.0). The receive output RGMII interface can be synchronized to either the received data's recovered clock or the QuadPHY 1GR's local reference clock.

General

The PM8363 has four transmit and four receive channels (A to D). Figure 3 shows a detailed block diagram for the functionality of channel A. The block diagrams of channels B, C and D are identical to channel A.

The QuadPHY 1GR supports IEEE 802.3-2000 Gigabit Ethernet and Fibre Channel Physical Interfaces (FC-PI) Rev. 13. The high-speed outputs feature programmable output drive that enables directly driving 50 Ω (100 Ω differential) systems. This allows direct interface to optical modules, coax, or serial backplanes.

The selection of interface modes, as well as operating features such as the internal 8B/10B encoding/decoder, full duplex PCS, frequency compensation, and parallel loopback, can be done via the 2-pin serial MDC/MDIO management interface, or through external pins for systems that do not support MDC/MDIO. The QuadPHY 1GR supports parallel loopback mode for testing. Support for built-in self test (BIST) via an internal packet generator/checker is also provided on a per transceiver basis.

The part is produced in 0.18 µM. The HSTL Class I I/O is capable of operating at 1.5V or 1.8V. The CMOS I/O compatible with 2.5V or 1.8V LVCMOS I/Os. IEEE 1149.1 JTAG is fully supported and the 196-pin CABGA package has a small 15x15 mm footprint.

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7 Pin Diagram

The QuadPHY 1GR is packaged in a 196-ball Chip Array Ball Grid Array (CABGA) package. Dimensions are 15 mm by 15 mm. Figure 5 shows the QuadPHY 1GR.pin diagram.

Figure 5 QuadPHY 1GR Pin Diagram

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	RXDB[0]	NC	NC	NC	RXCKA	RXDA[0]	TXCKA	TXDA[0]	NC	TEST[4]	VDDA	TDOD_N	TDOD_P	VSS	A
B	RXDB[1]	VSS	VDDQ	NC	VSS	VDDQ	TXDA[1]	VSS	VDDQ	TEST[5]	VDDA	NC	NC	VSS	B
C	RXCKB	RXDB[2]	NC	RXCTLA	RXDA[3]	RXDA[1]	TXDA[2]	TXDA[3]	NC	NC	VDDA	TDOC_N	TDOC_P	VSS	C
D	RXDB[3]	RXCTLB	NC	VSS	VDDQ	RXDA[2]	VSS	VDDQ	TXCTLA	NC	VDDA	TDOB_N	TDOB_P	VSS	D
E	TXCKB	TXDB[0]	TXDB[1]	TXDB[2]	G_DIGLB	RGMII_RTBIB	NC	TCLKSEL	POEN	RESET	VDDA	VDDA	VSS	VSS	E
F	MDC	MDIO	TXDB[3]	TXCTLB	NC	VSS	VSS	VSS	VSS	VDDI	VDDA	TDOA_N	TDOA_P	VSS	F
G	VDDS	VREF	TCK	TDI	TRSTB	VSS	VSS	VSS	VSS	VDDI	VDDI	NC	NC	VSSA	G
H	REFCLK	VSS	TMS	TDO	CTC_EN	VSS	VSS	VSS	VSS	VDDI	VDDI	NC	NC	VSSA	H
J	VSS	VDDS	TXDC[3]	TXCTLC	PRES	VSS	VSS	VSS	VSS	VDDI	VDDA	RDID_N	RDID_P	VSS	J
K	TXCKC	TXDC[0]	TXDC[1]	TXDC[2]	DVAD0	DVAD1	DVAD2	DVAD3	DVAD4	NC	VDDA	VDDA	VSS	VSS	K
L	RXDC[3]	RXCTLC	NC	VSS	VDDQ	RXDD[2]	VSS	VDDQ	TXCTLD	TEST[3]	VDDA	RDIC_N	RDIC_P	VSS	L
M	RXCKC	RXDC[2]	NC	RXCTLD	RXDD[3]	RXDD[1]	TXDD[2]	TXDD[3]	NC	TEST[2]	VDDA	RDIB_N	RDIB_P	VSS	M
N	RXDC[1]	VSS	VDDQ	NC	VSS	VDDQ	TXDD[1]	VSS	VDDQ	TEST[1]	VDDA	NC	NC	VSS	N
P	RXDC[0]	NC	NC	NC	RXCKD	RXDD[0]	TXCKD	TXDD[0]	NC	TEST[0]	TEST_ENB	RDIA_N	RDIA_P	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

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8 Pin Description

The following tables describe all pins of the QuadPHY 1GR.

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Table 2 Receive Path Pins

Pin Name	Type	Pin No.	Function
RDIA_P RDIA_N RDIB_P RDIB_N RDIC_P RDIC_N RDID_P RDID_N	Input High-speed Differential	P13 P12 M13 M12 L13 L12 J13 J12	Differential, high-speed serial **Receive Data Input pins**. This data must be 8B/10B line coded and operate in the range from 933Mbit/s and 1.25 Gbit/s. The differential inputs are internally terminated with 100 Ω differential terminations. These Receive channels are ignored when Serial Loopback is enabled using the INT_EN_SERIAL_LPBK [D:A] bits in Loopback Control Register These inputs are enabled by default. If a channel is enabled, active data must be provided to it. Do not use pull-up/pull-down resistors on the high-speed differential inputs. These inputs may be left unconnected when this channel is not used.
RXCKA	Output HSTL	A5	The **Receive Reference Clock Channel A** is a continuous receive reference clock that operates between 93.3Mhz and 125Mhz. Depending on the mode of operation, the receive clock may be recovered from the high speed received data or derived from the local reference clock. The rising edge of RXCKA is used to sample the least significant nibble of data on the RXDA[3:0] and the RXCTLA pins. The falling edge of RXCKA is used to sample the most significant nibble of data on the RXDA[3:0] and the RXCTLA pins. The received data can be output using recovered clock or local clock in RGMII mode, and recovered clock only in RTBI mode.
RXDA[3] RXDA[2] RXDA[1] RXDA[0]	Output HSTL	C5 D6 C6 A6	The **Receive Data Channel A** is generated from the RDIA_P, RDIA_N inputs. When RGMII mode is selected, RGMII Data bits 3:0 are updated using the rising edge of RXCKA and RGMII Data bits 7:4 are updated on the falling edge of RXCKA. When RTBI mode is selected, RTBI Data bits 3:0 are updated using the rising edge of RXCKA and RTBI Data bits 8:5 are updated on the falling edge of RXCKA. Please refer to Figure 17 and Figure 18 for details on functional timing between clock and data. RXDA[0] represents the first bit of the word received on the differential pairs RDIA_P, RDIA_N.

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Pin Name	Type	Pin No.	Function
RXCTLA	Output HSTL	C4	The **Receive Control Channel A** pin outputs either a control in RGMII mode or a data bit in RTBI mode. When RGMII mode is selected, RXCTLA outputs RXDV on the rising edge of RXCKA and a derivative (XOR) of RXDV and RXERR on the falling edge of RXCKA. When RTBI mode is selected, RXCTLA outputs data bit 4 on the rising edge of RXCKA and data bit 9 on the falling edge of RXCKA. Please refer to Figure 17 and Figure 18 for details on functional timing between clock and data.
RXCKB	Output HSTL	C1	The **Receive Reference Clock Channel B** is a continuous receive reference clock that operates between 93.3Mhz and 125Mhz. Depending on the mode of operation, the receive clock may be recovered from the high speed received data or derived from the local reference clock. The rising edge of RXCKB is used to sample the least significant nibble of data on the RXDB[3:0] and the RXCTLB pins. The falling edge of RXCKB is used to sample the most significant nibble of data on the RXDB[3:0] and the RXCTLB pins. The received data can be output using recovered clock or local clock in RGMII mode, and recovered clock only in RTBI mode.
RXDB[3] RXDB[2] RXDB[1] RXDB[0]	Output HSTL	D1 C2 B1 A1	The **Receive Data Channel B** is generated from the RDIB_P, RDIB_N inputs. When RGMII mode is selected, RGMII Data bits 3:0 are updated using the rising edge of RXCKB and RGMII Data bits 7:4 are updated on the falling edge of RXCKB. When RTBI mode is selected, RTBI Data bits 3:0 are updated using the rising edge of RXCKB and RTBI Data bits 8:5 are updated on the falling edge of RXCKB. Please refer to Figure 17 and Figure 18 for details on functional timing between clock and data. RXDB[0] represents the first bit of the word received on the differential pairs RDIB_P, RDIB_N.
RXCTLB	Output HSTL	D2	The **Receive Control Channel B** pin outputs either a control in RGMII mode or a data bit in RTBI mode. When RGMII mode is selected, RXCTLB outputs RXDV on the rising edge of RXCKB and a derivative (XOR) of RXDV and RXERR on the falling edge of RXCKB. When RTBI mode is selected, RXCTLB outputs data bit 4 on the rising edge of RXCKB and data bit 9 on the falling edge of RXCKB. Please refer to Figure 17 and Figure 18 for details on functional timing between clock and data.

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Pin Name	Type	Pin No.	Function
RXCKC	Output HSTL	M1	The **Receive Reference Clock Channel C** is a continuous receive reference clock that operates between 93.3Mhz and 125Mhz. Depending on the mode of operation, the receive clock may be recovered from the high speed received data or derived from the local reference clock. The rising edge of RXCKC is used to sample the least significant nibble of data on the RXDC[3:0] and the RXCTLC pins. The falling edge of RXCKC is used to sample the most significant nibble of data on the RXDC[3:0] and the RXCTLC pins. The received data can be output using recovered clock or local clock in RGMII mode, and recovered clock only in RTBI mode.
RXDC[3] RXDC[2] RXDC[1] RXDC[0]	Output HSTL	L1 M2 N1 P1	The **Receive Data Channel C** is generated from the RDIC_P, RDIC_N inputs. When RGMII mode is selected, RGMII Data bits 3:0 are updated using the rising edge of RXCKC and RGMII Data bits 7:4 are updated on the falling edge of RXCKC. When RTBI mode is selected, RTBI Data bits 3:0 are updated using the rising edge of RXCKC and RTBI Data bits 8:5 are updated on the falling edge of RXCKC. Please refer to Figure 17 and Figure 18 for details on functional timing between clock and data. RXDC[0] represents the first bit of the word received on the differential pairs RDIC_P, RDIC_N.
RXCTLC	Output HSTL	L2	The **Receive Control Channel C** pin outputs either a control in RGMII mode or a data bit in RTBI mode. When RGMII mode is selected, RXCTLC outputs RXDV on the rising edge of RXCKC and a derivative (XOR) of RXDV and RXERR on the falling edge of RXCKC. When RTBI mode is selected, RXCTLC outputs data bit 4 on the rising edge of RXCKC and data bit 9 on the falling edge of RXCKC. Please refer to Figure 17 and Figure 18 for details on functional timing between clock and data.
RXCKD	Output HSTL	P5	The **Receive Reference Clock Channel D** is a continuous receive reference clock that operates between 93.3Mhz and 125Mhz. Depending on the mode of operation, the receive clock may be recovered from the high speed received data or derived from the local reference clock. The rising edge of RXCKD is used to sample the least significant nibble of data on the RXDD[3:0] and the RXCTLD pins. The falling edge of RXCKD is used to sample the most significant nibble of data on the RXDD[3:0] and the RXCTLD pins. The received data can be output using recovered clock or local clock in RGMII mode, and recovered clock only in RTBI mode.

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Pin Name	Type	Pin No.	Function
RXDD[3] RXDD[2] RXDD[1] RXDD[0]	Output HSTL	M5 L6 M6 P6	The **Receive Data Channel D** is generated from the RDID_P, RDID_N inputs. When RGMII mode is selected, RGMII Data bits 3:0 are updated using the rising edge of RXCKD and RGMII Data bits 7:4 are updated on the falling edge of RXCKD. When RTBI mode is selected, RTBI Data bits 3:0 are updated using the rising edge of RXCKD and RTBI Data bits 8:5 are updated on the falling edge of RXCKD. Please refer to Figure 17 and Figure 18 for details on functional timing between clock and data. RXDD[0] represents the first bit of the word received on the differential pairs RDID_P, RDID_N.
RXCTLD	Output HSTL	M4	The **Receive Control Channel D** pin outputs either a control in RGMII mode or a data bit in RTBI mode. When RGMII mode is selected, RXCTLD outputs RXDV on the rising edge of RXCKD and a derivative (XOR) of RXDV and RXERR on the falling edge of RXCKD. When RTBI mode is selected, RXCTLD outputs data bit 4 on the rising edge of RXCKD and data bit 9 on the falling edge of RXCKD. Please refer to Figure 17 and Figure 18 for details on functional timing between clock and data.

Table 3 Transmit Path Pins

Pin Name	Type	Pin No.	Function
TDOA_P TDOA_N TDOB_P TDOB_N TDOC_P TDOC_N TDOD_P TDOD_N	Output High-speed Differential	F13 F12 D13 D12 C13 C12 A13 A12	Differential, high-speed serial **Transmit Data Output** pins. This data is operating from between 933Mbit/s and 1.25 Gbit/s and is 8B/10B encoded. The differential outputs are internally terminated with 100-ohm differential terminations. These outputs are inactive when serial loopback is enables. These outputs are enabled by default. Do not use pull-up or pull-down resistors on the high-speed differential outputs. The outputs may be left unconnected if this channel is not used

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Pin Name	Type	Pin No.	Function
TXCKA	Input HSTL	A7	The **Transmit Reference Clock Channel A** can operate between 93.3Mhz and 125Mhz. The rising edge of TXCKA is used to clock in the least significant nibble of data on the TXDA[3:0] and the TXCTLA pins. The falling edge of TXCKA is used to clock in the most significant nibble of data on the TXDA[3:0] and the TXCTLA pins. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel A-D RGMII/RTBI Tx data. If this pin is not used, it should be tied to ground.
TXDA[3] TXDA[2] TXDA[1] TXDA[0]	Input HSTL	C8 C7 B7 A8	The **Transmit Data Channel A** is the source of data on TDOA_P, TDOA_N outputs. When RGMII mode is selected, RGMII Data bits 3:0 are loaded into the QuadPHY 1GR on the rising edge of TXCKA and RGMII Data bits 7:4 are loaded on the falling edge of TXCKA. When RTBI mode is selected, RTBI Data bits 3:0 are loaded into the QuadPHY 1GR on the rising edge of TXCKA and RTBI Data bits 8:5 are loaded on the falling edge of TXCKA. Please refer to Figure 6 for details on functional timing between clock and data. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel A RGMII/RTBI data Tx. TXDA[0] represents the first bit of the word transmitted on the differential pairs TDOA_P, TDPA_N. If these pins are not used, they should be tied to ground.
TXCTLA	Input HSTL	D9	The **Transmit Control Channel A** pin accepts either a control in RGMII mode or a data bit in RTBI mode. When RGMII mode is selected, TXCTLA input TXEN on the rising edge of TXCKA and a logical derivative (XOR) of TXEN and TXERR on the falling edge of TXCKA. When RTBI mode is selected, TXCTLA inputs data bit 4 on the rising edge of TXCKA and data bit 9 on the falling edge of TXCKA. Please refer to Figure 6 for details on functional timing between clock and data. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel A RGMII/RTBI TXCTLA. If this pin is not used, it should be tied to ground.

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Pin Name	Type	Pin No.	Function
TXCKB	Input HSTL	E1	The **Transmit Reference Clock Channel B** can operate between 93.3Mhz and 125Mhz. The rising edge of TXCKB is used to clock in the least significant nibble of data on the TXDB[3:0] and the TXCTLB pins. The falling edge of TXCKB is used to clock in the most significant nibble of data on the TXDB[3:0] and the TXCTLB pins. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel B RGMII/RTBI Tx data. TXCKB should be tied to ground. If this pin is not used, it should be tied to ground.
TXDB[3] TXDB[2] TXDB[1] TXDB[0]	Input HSTL	F3 E4 E3 E2	The **Transmit Data Channel B** is the source of data on TDOB_P, TDOB_N outputs. When RGMII mode is selected, RGMII Data bits 3:0 are loaded into the QuadPHY 1GR on the rising edge of TXCKB and RGMII Data bits 7:4 are loaded on the falling edge of TXCKB. When RTBI mode is selected, RTBI Data bits 3:0 are loaded into the QuadPHY 1GR on the rising edge of TXCKB and RTBI Data bits 8:5 are loaded on the falling edge of TXCKB. Please refer to Figure 6 for details on functional timing between clock and data. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel B RGMII/RTBI data Tx. TXDB[0] represents the first bit of the word transmitted on the differential pairs TDOB_P, TDPB_N. If these pins are not used, they should be tied to ground.
TXCTLB	Input HSTL	F4	The **Transmit Control Channel B** pin accepts either a control in RGMII mode or a data bit in RTBI mode. When RGMII mode is selected, TXCTLB input TXEN on the rising edge of TXCKB and a logical derivative (XOR) of TXEN and TXERR on the falling edge of TXCKB. When RTBI mode is selected, TXCTLB inputs data bit 4 on the rising edge of TXCKB and data bit 9 on the falling edge of TXCKB. Please refer to Figure 6 for details on functional timing between clock and data. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel B RGMII/RTBI TXCTLB. If this pin is not used, it should be tied to ground.

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Pin Name	Type	Pin No.	Function
TXCKC	Input HSTL	K1	The **Transmit Reference Clock Channel C** can operate between 93.3Mhz and 125Mhz. The rising edge of TXCKC is used to clock in the least significant nibble of data on the TXDC[3:0] and the TXCTLC pins. The falling edge of TXCKC is used to clock in the most significant nibble of data on the TXDC[3:0] and the TXCTLC pins. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel C RGMII/RTBI Tx data. TXCKB should be tied to ground. If this pin is not used, it should be tied to ground.
TXDC[3] TXDC[2] TXDC[1] TXDC[0]	Input HSTL	J3 K4 K3 K2	The **Transmit Data Channel C** is the source of data on TDOC_P, TDOC_N outputs. When RGMII mode is selected, RGMII Data bits 3:0 are loaded into the QuadPHY 1GR on the rising edge of TXCKC and RGMII Data bits 7:4 are loaded on the falling edge of TXCKC. When RTBI mode is selected, RTBI Data bits 3:0 are loaded into the QuadPHY 1GR on the rising edge of TXCKC and RTBI Data bits 8:5 are loaded on the falling edge of TXCKC. Please refer to Figure 6 for details on functional timing between clock and data. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel C RGMII/RTBI data Tx. TXDC[0] represents the first bit of the word transmitted on the differential pairs TDOC_P, TDPC_N. If these pins are not used, they should be tied to ground.
TXCTLC	Input HSTL	J4	The **Transmit Control Channel C** pin accepts either a control in RGMII mode or a data bit in RTBI mode. When RGMII mode is selected, TXCTLC input TXEN on the rising edge of TXCKC and a logical derivative (XOR) of TXEN and TXERR on the falling edge of TXCKC. Please refer to Figure 6 for details on functional timing between clock and data. When RTBI mode is selected, TXCTLC inputs data bit 4 on the rising edge of TXCKC and data bit 9 on the falling edge of TXCKC. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel C RGMII/RTBI TXCTLC. If this pin is not used, it should be tied to ground.

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Pin Name	Type	Pin No.	Function
TXCKD	Input HSTL	P7	The **Transmit Reference Clock Channel D** can operate between 93.3Mhz and 125Mhz. The rising edge of TXCKD is used to clock in the least significant nibble of data on the TXDD[3:0] and the TXCTLD pins. The falling edge of TXCKD is used to clock in the most significant nibble of data on the TXDD[3:0] and the TXCTLD pins. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel D RGMII/RTBI Tx data. TXCKB should be tied to ground. If this pin is not used, it should be tied to ground.
TXDD[3] TXDD[2] TXDD[1] TXDD[0]	Input HSTL	M8 M7 N7 P8	The **Transmit Data Channel D** is the source of data on TDOD_P, TDOD_N outputs. When RGMII mode is selected, RGMII Data bits 3:0 are loaded into the QuadPHY 1GR on the rising edge of TXCKD and RGMII Data bits 7:4 are loaded on the falling edge of TXCKD. When RTBI mode is selected, RTBI Data bits 3:0 are loaded into the QuadPHY 1GR on the rising edge of TXCKD and RTBI Data bits 8:5 are loaded on the falling edge of TXCKD. Please refer to Figure 6 for details on functional timing between clock and data. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel D RGMII/RTBI data Tx. TXDD[0] represents the first bit of the word transmitted on the differential pairs TDOD_P, TDPD_N. If these pins are not used, they should be tied to ground.
TXCTLD	Input HSTL	L9	The **Transmit Control Channel D** pin accepts either a control in RGMII mode or a data bit in RTBI mode. When RGMII mode is selected, TXCTLD input TXEN on the rising edge of TXCKD and a logical derivative (XOR) of TXEN and TXERR on the falling edge of TXCKD. When RTBI mode is selected, TXCTLD inputs data bit 4 on the rising edge of TXCKD and data bit 9 on the falling edge of TXCKD. Please refer to Figure 6 for details on functional timing between clock and data. If TCLKSEL pin is set to logic 0, TXCKA clocks Channel D RGMII/RTBI TXCTLD. If this pin is not used, it should be tied to ground.

Table 4 MDC/MDIO Pins

Pin Name	Type	Pin No.	Function

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Pin Name	Type	Pin No.	Function
DVAD4 DVAD3 DVAD2	Input HSTL (1.8 V LVCMOS Compatible)	K9 K8 K7	SERDES **Device Address**. Pins DVAD[4:2] define the base device address of the QuadPHY 1GR.. The MDC/MDIO protocol addresses this device when the 3 MSBs of the PHYAD address match pins DVAD[4:2]. The two LSBs of the MDC/MDIO protocol PHYAD address point to the specific SERDES within the device. PHYAD[4:2] = DVAD[4:2] => selects device. PHYAD[1:0] = 00 - 11 => selects channel A-D respectively (00 is channel A)
MDIO	Input/Output LVCMOS	F2	**Management Data Input/Output**. This terminal is the management interface (MI) serial port. During MI write cycles, input data is placed on this terminal and sampled by MDC. During a MI read cycle the MDIO terminal outputs management interface register information. Input data is sampled on the rising edge of MDC. Input and output data on this terminal is referenced to the rising edge of MDC. Note that MDIO should be externally pulled up to VDDQ with a 10kΩ resistor for proper operation between accesses.
MDC	Input LVCMOS	F1	**Management Data Clock**. Used to control data transfer to/from the management interface registers. Management interface input data is sampled on the rising edges of MDC. When data is to be output on the MDIO terminal it is referenced to the rising edge of MDC. MDC can be aperiodic. The presence of a clock on REFCLK is required for proper operation of the MDC/MDIO interface.

Table 5 Configuration/Status Pins

Pin Name	Type	Pin No.	Function
RGMII_RTBIB	Input HSTL (1.8 V LVCMOS Compatible)	E6	**Decoder/Encoder Enable** (Active high). This static signal must be pulled high or low prior to deasserting RESET. Enables the internal 8B/10B encoder/ decoder, PCS and RGMII across all channels. When set to 0, the device processes 10B encoded data only with PCS disabled and output RTBI on parallel bus. This terminal is logically ORed with the INT_DEC_ENC_ENABLE control bit of register 0x11 to enable 8B/10B encode/decode and is also logically ORed with the PCS_ENABLE of register 0x11 to enable PCS logic.

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Pin Name	Type	Pin No.	Function
CTC_EN	Input HSTL (1.8 V LVCMOS Compatible)	H5	**Clock Tolerance Compensation Enable**. This static signal must be pulled high or low prior to deasserting RESET. This control pin is logically ORed with INT_CTC_EN bit of register 0x18. When high, the QuadPHY 1GR performs frequency compensation on incoming data and REFCLK is used for receive clock on the DDR interface for all channels. When low, frequency compensation is disabled and recovered clock is used for receive clock on the DDR interface for all channels. If RTBI mode (RGMII_RTBIB = 0) is enable, CTC_EN should be set to logic 0 in normal operation mode, such that frequency compensation disabled and recovered clock is used for the receive clock on the DDR interface. When using internal BIST logic (refer to 11.1 for details), CTC_EN can be enabled.
G_DIGLB	Input HSTL (1.8 V LVCMOS Compatible)	E5	**Enable Global Digital Loopback**. This static signal must be pulled high or low prior to deasserting RESET. When high, the QuadPHY 1GR internally connects all transmit input parallel ports to their corresponding receive parallel output ports just before the parallel to serial conversion. Data is still sent to the serial outputs. When low, this loopback mode is disabled. When G_DIGLB is low, per Channel transmit input parallel ports to receive output parallel ports can be enabled by setting DIGITAL_PLBK_EN in register 0x18 to logic 1 and the corresponding INT_EN_SERIAL_LPBK_y in register 0x16 to logic 1.
TCLKSEL	Input Pullup HSTL (1.8 V LVCMOS Compatible)	E8	**Transmit Clock Select (TCLKSEL) selects one clock for all four transmit channels or one clock for each transmit channels**. When this bit is set to logic low, all channels uses TXCKA to sample transmit data over the parallel transmit RGMII/RTBI interface. When set to logic high, each channel uses it corresponding transmit clock to sample transmit data over the parallel transmit RGMII/RTBI interface.
REFCLK	Input LVCMOS	H1	**Reference Clock**. Requires an accurate, low jitter, 100 ppm for frequencies between 93.3 and 125 MHz reference clock. The clock synthesis PLL uses REFCLK to generate a phase locked 10X internal clock. The PLL expects an uninterrupted reference clock. If the reference clock is disrupted for any duration of time, a hardware reset maybe necessary to allow the PLL to fully recover. REFCLK is referenced to VDDS voltage levels (see the D.C Characteristics Section for details about Vol and Voh logic thresholds). The presence of a clock on REFCLK is required for proper operation of the MDC/MDIO interface.
RESET	Input HSTL (1.8 V LVCMOS Compatible)	E10	The active-high **Reset** (RESET) signal provides an asynchronous QuadPHY 1GR reset to all flip-flops. The minimum reset assertion time is 500 ns.

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Table 6 JTAG Pins

Pin Name	Type	Pin No.	Function
TCK	Input LVCMOS	G3	The **Test Clock** (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TDI	Input LVCMOS Pullup	G4	The **Test Data Input** (TDI) signal carries test data into the QuadPHY 1GR via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TMS	Input Pullup LVCMOS	H3	The **Test Mode Select** (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TRSTB	Input Pullup LVCMOS	G5	The active-low **Test Reset** (TRSTB) signal provides an asynchronous QuadPHY 1GR test access port reset via the IEEE P1149.1 test access port. TRSTB must be pulled low during normal device operation. This places the JTAG logic into the reset state.
TDO	Output Tristate LVCMOS	H4	The **Test Data Output** (TDO) signal carries test data out of the QuadPHY 1GR via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is inactive except when scanning of data is in progress.

Table 7 Miscellaneous Pins

Pin Name	Type	Pin No.	Function
POEN	Input HSTL (1.8 V LVCMOS Compatible)	E9	**Parallel Output Enable** (active high). Tristates all the parallel output drivers RXDy[3:0], RXCTLy and RXCx when low.
TEST_OUT[5:0]	Output HSTL	B10 A10 L10 M10 N10 P10	Reserved for PMC Test Purposes. Must be left unconnected.
TEST_ENB	Input Pullup HSTL (1.8 V LVCMOS Compatible)	P11	Reserved for PMC Test Purposes. Must be left unconnected.

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Pin Name	Type	Pin No.	Function
n/c		K10 F5 A9 C9 C10 D10 M9 P9 P3 L3 M3 N4 P4 P2 A3 D3 C3 B4 A4 A2 B13 B12 G13 G12 H13 H12 N13 N12 E7	These pins should be left unconnected.
DVAD0, DVAD1 (TEST_ABI)	Analog	K6 K5	These pins are used for analog test and should be left unconnected.
VREF	Voltage Reference	G2	Input reference voltage (VREF) should be connected to the HSTL input reference voltage power supply (1/2 of VDDQ). Peak to peak ac noise on VREF may not exceed 2% VREF DC.
PRES	Analog Bias	J5	Terminal for a **Precision Resistor** of 10k 1% reference resistor is connected between this terminal and ground. This sets the internal reference current sources.

Table 8 Digital Power and Digital Ground Pins

Pin Name	Type	Pin No.	Function
VDD	Power Digital Core	G11 H11 F10 G10 H10 J10	Digital core power. This is, V_{DD} = 1.8 V $\pm$ 5%, for the digital core logic.

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Pin Name	Type	Pin No.	Function
VDDQ	Power Digital I/O	B9 N9 D8 L8 B6 N6 D5 L5 B3 N3	Digital I/O power for HSTL. Nominal 1.5 V ± 5% or 1.8 V ± 5%for HSTL I/O.
VDDS	Power Digital I/O	G1 J2	Digital I/O power. Nominal 1.8 V ± 5% or 2.5 V ± 5% for CMOS I/O.
GND	Ground Digital	A14 B14 C14 D14 E14 F14 J14 K14 L14 M14 N14 P14 E13 K13 B8 N8 D7 L7 B5 N5 D4 L4 B2 N2 H2 J1	Digital ground.
T_GND	Ground Digital Thermal	F9 G9 H9 J9 F8 G8 H8 J8 F7 G7 H7 J7 F6 G6 H6 J6	Thermal ground. Used as a ground pin and to conduct heat away from the part and into the PCB. This ground should be attached to the same ground plane as GND.

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Table 9 Analog Power and Ground Pins

Pin Name	Type	Pin No.	Function
VDDA	Power Analog	E12 K12 A11 B11 C11 D11 E11 F11 J11 K11 L11 M11 N11	Analog Power. This is, V_{DDA} = 1.8 V ± 5% and must be separated from digital power.
GNDA	Ground Analog	G14 H14	Analog ground. Connect to same ground plane as GND pins.

Notes:

1. Digital and analog ground pins are not connected together internally. Failure to connect any of these pins can cause malfunction or damage to the QuadPHY 1GR.
2. Digital and analog power pins are not connected together internally. Failure to connect any of these pins could also result in malfunction or damage to the QuadPHY 1GR

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9 Functional Description

9.1 Modes of Operation

The QuadPHY 1GR has three modes of operation:

1. RGMII Mode with recovered or reference clock
2. RTBI Mode
3. Parallel Loopback Mode

The RGMII mode enables 8B/10B encoding and decoding, PCS and output/input 8 bit data on RGMII parallel interface. RGMII mode is enabled when RGMII_RTBIB is set to logic 1. When in RGMII mode, the receive data can be output timed to the recovered clock or to the local reference clock. Frequency compensation, controlled by CTC_EN, is required when data is output timed to the local reference clock.

When RGMII mode is enabled, Clock Compensation mode can be enabled to use the channel Receive FIFOs to synchronize the received data to the local clock domain (REFCLK). When RGMII mode is enabled and Clock Compensation Mode is disabled, the channel Receive FIFOs are bypassed and the recovered clocks are used at RGMII output Rx interface. This mode provides lower latency since the internal Receive FIFOs are bypassed. Clock Compensation mode can be enabled by setting CTC_EN to logic 1.

The RTBI mode disables 8B/10B encoding and decoding, disables PCS and outputs/inputs 10 bit data on RTBI parallel interface. When RTBI mode is selected, Clock Tolerance Compensation Mode should be disabled and recovered clocks are used at RTBI output Rx interface. RTBI mode is selected when RGMII_RTBIB is set to logic 0. In RTBI mode, comma detection could be enabled by setting ENABLE_COMMA_DETECT to 1 (default) in register 0x11. This mode provides the lowest latency since the internal Receive FIFOs and PCS logic are bypassed.

The Global Digital Loopback Mode loops parallel transmit input RGMII/RTBI data back to parallel receive output RGMII/RTBI data just before the parallel to serial conversion. The parallel transmit input RGMII data still goes out on the serial transmit line. The data on serial receive line is ignored. The Parallel Loopback Mode can be enabled on all four channels by setting G_DIGLB pin to logic 1 or INT_EN_SERIAL_LPBK bits in register 0x16 and DIGITAL_LPBK_EN in register 0x18 to logic 1.

9.2 Serial Channel Overview

The QuadPHY 1GR uses high-speed serial channel technology to communicate data between chips. Each channel consists of a differential transmit pair and a differential receive pair. The device supports PECL voltage swings and the receiver inputs are designed to be capacitively coupled external to the device.

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The QuadPHY 1GR requires that received data to be 8B/10B encoded to ensure sufficient transition density. The QuadPHY 1GR's internal 8B/10B encoder/decoder can be disabled (RTBI Mode) if an external 8B/10B encoder/decoder is used. The 8B/10B coding method offers several advantages including high-transition density, low DC offset and availability of special control characters (see Section 9.2.1).

9.2.1 8B Code Group Bit Mappings

Table 10 identifies the valid control code groups that encode/decode properly. In RGMII mode, QuadPHY 1GR only recognizes following K bit values.

Table 10 Valid K Bit Values

K-Bit	Valid 9-bit Value (hex)	Code	Definition
K28.0	0x11C	/R/[1]	Suggested Skip/Replace Idle Character
K28.1	0x13C		Alternate Skip/Replace Idle Character
K28.2	0x15C		Alternate Skip/Replace Idle Character
K28.3	0x17C	/A/	Suggested Alignment Idle Character
K28.4	0x19C		Alternate Skip/Replace Idle Character
K28.5	0x1BC	/K/	Synchronization Idle Character
K28.6	0x1DC		Alternate Skip/Replace Idle Character
K28.7	0x1FC		Special Diagnostics Character
K23.7	0x1F7	/R/	Carrier-Extend for 1000BaseX PCS Apps
K27.7	0x1FB	/S/	Start-of-Packet
K29.7	0x1FD	/T/	End-of-Packet
K30.7	0x1FE	/V/	Error Propagation

Note:

1. Refer to Table 48-4 Defined ordered_sets and special code groups in the IEEE P802.3-2000.

For backplane applications, the usage of these characters is not limited by the QuadPHY 1GR in RTBI mode. For Gigabit Ethernet applications, these characters must be used in a manner consistent with the 802.3 specification.

9.2.2 Clock Synthesizer

The Clock Synthesizer uses a PLL to synthesize a clock from the REFCLK input. The frequency of the PLL clock is 10 times the frequency of REFCLK, and a single synthesized clock is used to transmit serial data on all 4 transmit channels.

The PLL clock frequency can be varied over a range of 933MHz to 1.25 GHz by changing the frequency of REFCLK. The PLL has a fixed multiplication ratio of 10, so the frequency of REFCLK must be 1/10 the required PLL clock frequency as illustrated in Table 11.

The PLL in the Clock Synthesizer requires a 10 k Ω ± 1% precision resistor on the PRES terminal.

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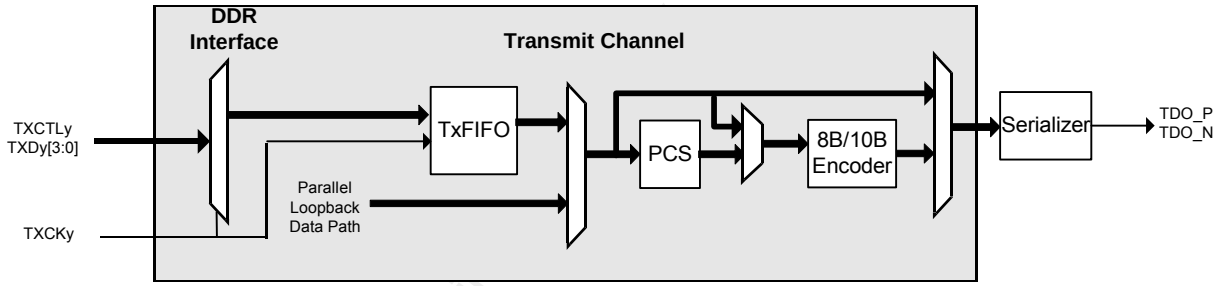
Table 11 Example REFCLK and PLL Clock Combinations

REFCLK Frequency	Multiplier	PLL Clock Frequency	Transmit Data Rate
93.3 Mhz	10x	933 MHz	933 Mbit/s
106.25 MHz	10X	1.0625 GHz	1.0625 Gbit/s
125 MHz	10X	1.25 GHz	1.25 Gbit/s

9.2.3 Transmit Path

The QuadPHY 1GR contains four transmit channels. Each channel consists of a DDR Parallel Interface, Transmit FIFO, Transmit PCS, 8B/10B Encoder, and Serializer. The 8B/10B encoder and PCS logic are bypassed when operating in RTBI mode. The data must be frequency synchronous with REFCLK. The configuration of these functional blocks is shown in Figure 6.

Figure 6 Transmit Channel Functional Blocks



RGMII/RTBI DDR Parallel Transmit Input Interface

Each transmit parallel interface consists of 5 data/control pins: TXCTLy and TXDy[3:0]. There are two modes of operations for the DDR interface: RGMII Mode, and RTBI Mode. There are two clocking modes for the DDR interface: Shared TCK Mode and Individual TCK Mode. The TXCKy transmit clock must be frequency synchronous with REFCLK. The TxFIFO accounts for phase difference between TXCKy and REFCLK.

When in RGMII Mode, bits 3:0 of the transmit data GMII byte TXDBy[7:0] are sampled from TXDy[3:0] pins using the rising edge of the transmit clock. The bits 7:4 of the transmit data GMII byte TXDBy[7:0] are sampled from TXDy[3:0] pins on the falling edge of the transmit clock. GMII TXENy is sampled from TXCTLy using the rising edge of the transmit clock. The derivative (XOR) of TXENy and TXERRy is sampled from TXCTLy using the falling edge of the transmit clock.

The input DDR interface supports center aligned timing. Figure 7 shows the functional timing of the RGMII transmit input interface. The mapping of TXENy, TXERRy and TXDBy[7:0] to GMII signals are listed in Table 13.

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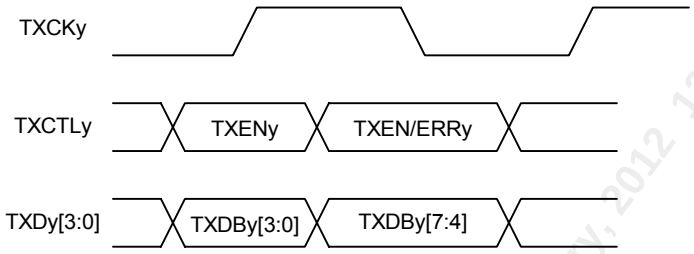
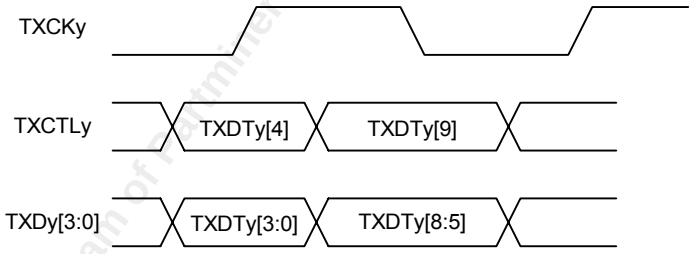
Figure 7 Center Aligned RGMII Transmit (Input) Functional Timing



When in the RTBI Mode, bits 3:0 of the transmit 10-bit data TXDTy[9:0] are sampled from TXDy[3:0] and TXDTy[4] from TXCTLy using the rising edge of the transmit clock. The bits 8:5 of the transmit 10-bit data TXDTy[9:0] are sampled from TXDy[3:0] and TXDTy[9] from TXCTLy on the falling edge of the transmit clock.

Figure 8 shows the functional timing of the RGMII transmit input interface. The mapping of TXDTy[9:0] to 10-bit code are listed in Table 13.

Figure 8 Center Aligned RTBI Transmit (Input) Functional Timing



If TCLKSEL = 0, the transmit clock for RGMII/RTBI input transmit interface of all the four channels uses one single clock TXCKA. If TCLKSEL = 1, the transmit clock for RGMII/RTBI input transmit interface uses the transmit clock (TXCKy) for that channel.

Table 12 summarizes the mapping of RGMII/RTBI parallel transmit input ports to the 4 high-speed serial transmit output channels.

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Table 12 Parallel Transmit Interface Summary for RGMII/RTBI

Serial Tx Ch	Parallel Transmit Input Ports	Tx Ref Clock	Tx Ref Clock	Data Loaded			
		TCLK SEL=1	TCLK SEL=0	Rising Edge RGMII	Falling Edge RGMII	Rising Edge RTBI	Falling Edge RTBI
A	TXCTLA, TXDA[3:0]	TXCKA	TXCKA	TXENA TXDBA[3:0]	TXEN/ERRA TXDBA[7:4]	TXDTA[4] TXDTA[3:0]	TXDTA[9] TXDTA[8:5]
B	TXCTLB, TXDB[3:0]	TXCKA	TXCKB	TXENB TXDBB[3:0]	TXEN/ERRB TXDBB[7:4]	TXDTB[4] TXDTB[3:0]	TXDTB[9] TXDTB[8:5]
C	TXCTLC, TXDC[3:0]	TXCKA	TXCKC	TXENC TXDBC[3:0]	TXEN/ERRC TXDBC[7:4]	TXDTC[4] TXDTC[3:0]	TXDTC[9] TXDTC[8:5]
D	TXCTLD, TXDD[3:0]	TXCKA	TXCKD	TXEND TXDBD[3:0]	TXEN/ERRD TXDBD[7:4]	TXDTD[4] TXDTD[3:0]	TXDTD[9] TXDTD[8:5]

Table 13 Mapping of 10-bit or Byte transmit data

TXDTy[9:0] from RTBI	10B Transmit Data	TXDB[7:0], TXENy, TXERRy from RGMII	GMII DATA
TXDy[9]	j	TX_ERRy	TX_ER
TXDy[8]	h	TX_ENy	TX_EN
TXDy[7]	g	TXDBy[7]	TXD7
TXDy[6]	f	TXDBy[6]	TXD6
TXDy[5]	i	TXDBy[5]	TXD5
TXDy[4]	e	TXDBy[4]	TXD4
TXDy[3]	d	TXDBy[3]	TXD3
TXDy[2]	c	TXDBy[2]	TXD2
TXDy[1]	b	TXDBy[1]	TXD1
TXDy[0]	a	TXDBy[0]	TXD0

Transmit FIFO

The Transmit FIFO is a 6-word by 10-bit FIFO that transfers data from the TXCKy domain to the internal clock domain that is synchronous to REFCLK. The TXCKy and the REFCLK must be synchronous. Once an arbitrary phase relationship is established, the phase deviation must not vary by more than ±500ps. Should the phase change more than ±500ps, momentary corruption of data may occur.

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Transmit PCS

The QuadPHY 1GR supports the 1000Base-X PCS for full-duplex applications. Note that carrier sense (CRS) and collision detect (COL) are not supported per *IEEE 802.3-2000* standard. The PCS functionality is enabled by setting the PCS_ENABLE bit in PMC Control 2 Register to logic 1 and the INT_DEC_ENC_ENABLE bit in PMC Control 2 Register or the RGMII_RTBIB pin to logic 1.

The PCS transmit logic contains an 8B/10B encoder and a single transmit state machine whose operation is consistent with the operation of the two transmit state machines that run in unison within clause 36 of IEEE *802.3-2000*. All transmit blocks are compatible with the *IEEE 802.3-2000* (Clauses 36 and 37). The PCS transmit logic supports a minimum of 5 byte IPG between data.

8B/10B Encoder

When enabled, the encoder internally accepts an 8-bit word plus k bit from the PCS Tx State Machine and encodes these bits into a 10-bit code. The encoder generates a running disparity for its own use in generating sub-blocks of 6- and 4-bit codes that limit the run length and maintain DC balance of the serialized bits. The Encoder logic is enabled either by connecting the RGMII_RTBIB pin to logic 1 or programming PMC Control 2 Register, bit 7 (INT_DEC_ENC_ENABLE) with logic value 1. Rules for encoding are specified in IEEE *802.3-2000*.

Serializer

The serializer accepts 10-bit transmission characters and converts them from a parallel format to a serial bit stream at bit rates between 933 Mbit/s and 1.25 Gbit/s. The serializer accepts a 10-bit parallel word with the least significant bit being transmitted first.

9.2.4 Receive Path

The QuadPHY 1GR contains four receive channels. Each channel consists of a Clock and Data Recovery Unit (CDRU), Byte Alignment logic, 8/B/10B Decoder, Receive PCS, Receive FIFO, and a DDR Parallel Output Interface. The configuration of these functional blocks are shown in Figure 9.

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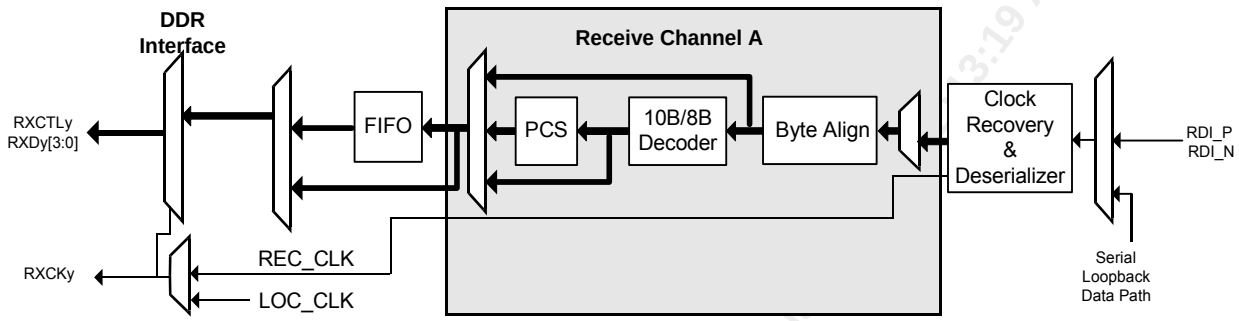
Figure 9 Receive Channel Functional Blocks



Each channel's CDRU, comma detection and byte alignment logic run independently. The comma detection logic is programmable to detect +comma, -comma, or both. The decoded words with K bits are optionally retimed by the Receive FIFO with IDLE character insertion/deletion for frequency compensation.

The receiver input data must be AC coupled with a transfer rate between 933Mbit/s ± 200 ppm and 1.25 Gbit/s ± 200 ppm. The QuadPHY 1GR supports on-chip 100Ω differential termination. The data is expected to be a 10-bit encoded data stream as specified in *IEEE 802.3-2000*. The clock recovery circuit recovers a clock (REC_CLK) from the incoming data. The recovered clock is used to sample the data. Both the recovered clock and data are provided to the deserializer independently for each channel.

Serial input ports may be internally looped-back to the serial output ports for testing purposes. While in a serial loopback mode, the serial output pins are held at a differential one. Serial loopback may be enabled using one of the following mechanisms:

- Assert INT_EN_SERIAL_LPBK_y control bit in the Loopback Control Register
- Assert Loopback bit in the channel's GMII Control register

Clock and Data Recovery

A 933 Mbit/s to 1.25 Gbit/s receive clock is extracted from the 10-bit coded serial data stream independently on each channel. The data rate of the received serial bit stream should be between 933 Mbit/s and 1.25 Gbit/s to guarantee proper lock. The receive clock locks to the input within 5 mS after a valid input data stream is applied. The received data is de-serialized and byte aligned. The recovered clock is synchronous to the REFCLK if no data is present on the RDI serial inputs. The de-serializer converts the received serial stream into 10-bit parallel data.

The bit synchronization time, the time required for the Clock and Data Recovery unit to recover the incoming bitstream error-free, is influenced by several factors including:

- Receive jitter.
- Relative phase difference between the incoming bitstream and the signal to which the CDRU was previously synchronized.

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- Transition density.
- DC Common Mode voltage offsets

The bit synchronization time is independent of the ppm offset, but the incoming bitstream must be within +/- 200 ppm of the local REFCLK.

The maximum bit synchronization time is required under conditions of minimum permissible receiver eye opening & worst-case relative phase difference alignment between the bitstream and the CDRU. Under these conditions, the maximum bit sync time is determined by the transition density of the incoming bit stream. Should a difference in DC Common Mode voltages exist, the minimum signal amplitude must be increased by an equivalent amount in order to maintain the shortest possible bit sync time.

An 8B/10B coded bitstreams that contain the idle ordered set of K28.5, D16.2 provides a nominal transition density of approximately 60%, and results in a maximum bit synchronization time of 500 bit times With other transition densities, the bit synchronization time can be calculated as:

> **T_BitSync** (in bit times) = 24000 / nominal transition density (expressed as a percentage)

This determination of bit sync time is only applicable when the CDRU inputs are switched from one transitioning bitstream to another. Should the inputs remain inactive for several 1000s of bit times, bit synchronization is delayed while the external AC coupling capacitors at the input of the SERDES charge to their steady state values. In this case, the maximum bit synchronization time is 2000 bit times.

Byte Alignment and Synchronization

The character alignment logic searches the coded incoming serial stream for a sequence defined in *IEEE 802.3-2000* as a comma. A comma is the sequence 0011111 or its complement and is unique in valid 10B coded data. This makes the comma useful for detecting proper alignment of incoming characters to byte boundaries. Upon detecting a comma, the alignment logic shifts the incoming data to align the received data properly in the 10-bit character field. An optional Byte-Sync State machine, shown in Figure 10, is implemented on a per channel basis to enable character alignment and preserve the alignment through occasional bit errors.

If a channel's Byte Synchronization State Machine is in the LOSS_OF_SYNC state, it can acquire synchronization by detecting four code-groups that contain commas without detecting code-group errors. An initial comma must be detected by the character alignment logic before the state machine can start the synchronization process. Once synchronization is acquired, the channel moves into the SYNC_ACQ_1 state. The state machine tests the received code-group to move between the SYNC_ACQ_1 and LOSS_OF_SYNC states. To prevent loss of synchronization during occasional bit errors, hysteresis can be added by setting the BA_HYST_EN bit in PMC Control 3 Register. The Byte Sync State Machine operates independently from the PCS Synchronization State Machine described in PCS Receive Section.

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Hysteresis is normally disabled upon reset. In this case, once the channel's synchronization state machine has entered the SYNC_ACQ_1 state, any realignment caused by the detection of a comma in a new location causes the channel to move to the LOSS_OF_SYNC state. If hysteresis is enabled, the synchronization process uses the hysteresis defined in the synchronization state machine. Even if a channel's hysteresis is disabled, the synchronization state machine continues to monitor alignment and supply a synchronization status indication. If a channel's synchronization state machine enters the LOSS_OF_SYNC state, the corresponding BYTE_ALIGN_STAT_[D:A] bit in Auto-Negotiation Status Register 2 latches the low valued status and holds it until a read of that register is performed.

The serial bit stream must be ordered 'abcdeifghj' with 'a' being the first bit received and 'j' the last bit received. The recovered receive clocks are neither stretched nor slivered during character alignment. During alignment up to, but not exceeding, four 10-bit code groups may be deleted or modified while aligning the code group to the edges of the receive clock.

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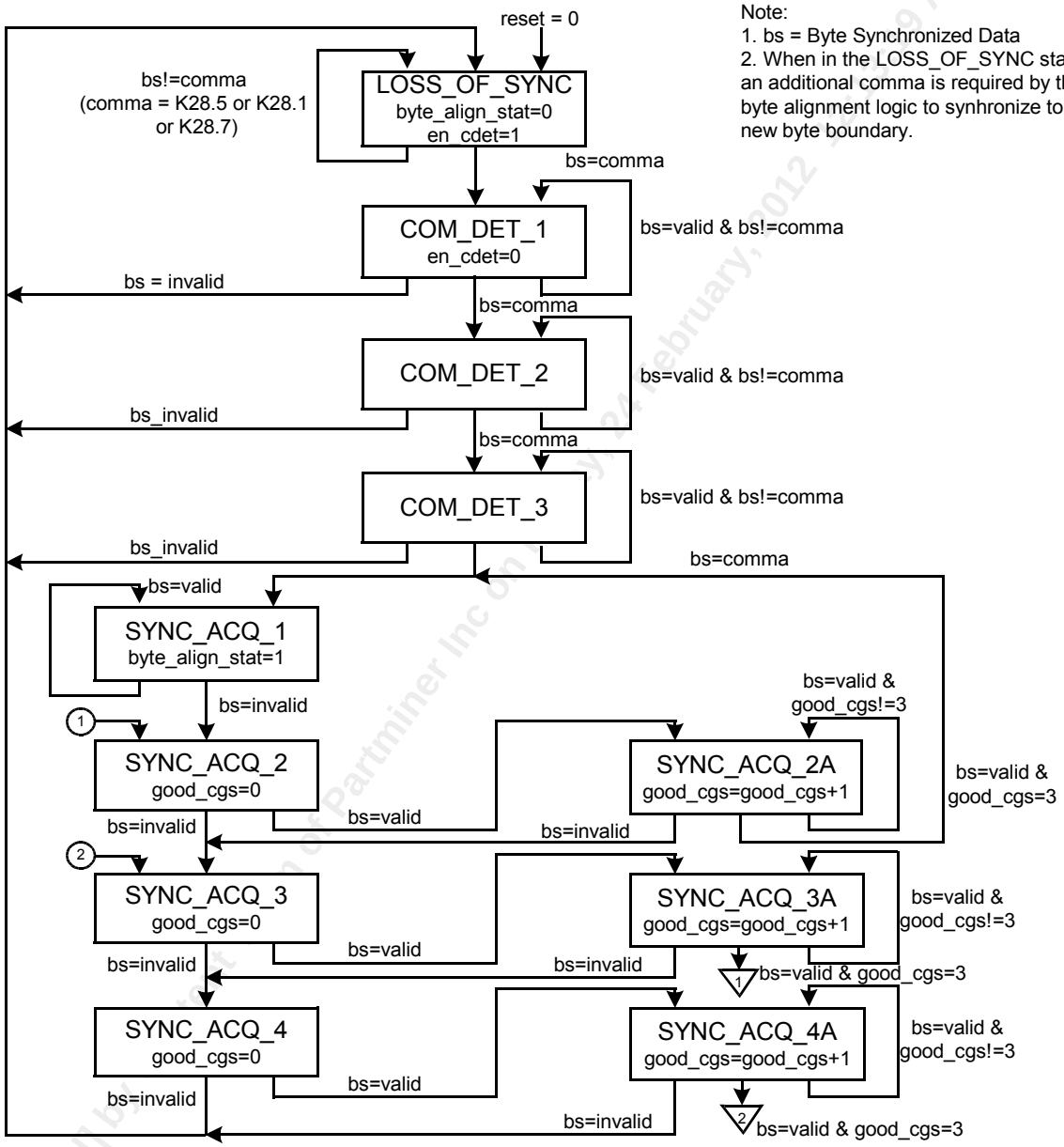
Figure 10 Byte Synchronization State Machine



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8B/10B Decoder

When enabled, each receive channel decodes incoming data into an 8-bit data byte and an associated control bit called the k-bit and passes this data to the PCS state machines. The PCS Rx state machine converts the 8-bit data + k-bit into the RGMII format before it is presented on the Rx RGMII interface. The decoder monitors for proper disparity and coding logging errors. A 10th bit for indicating a code violation or disparity error is also routed with the 9-bit parallel data

When the EN_CODE_ERR_CHK bit in Register 0x1B is a logic 1, the 8B/10B decoder in the corresponding channel counts coding errors received and flags the error count reaching the maximum set by PKT_CNT[14:0] in Register 0x1C. The error is indicated by the CODE_ERR_EXCEED bit in register 0x1B being read as logic 1. CODE_ERR_EXCEED holds the error until register 0x1B is read. The 8B/10B coding error counters in all channels are cleared whenever the CODE_ERR_STB bit in register 0x18 is set to logic 1. CODE_ERR_STB is self-clearing.

Receive PCS

The QuadPHY 1GR supports the 1000Base-X PCS for full-duplex applications. Note that carrier sense (CRS) and collision detect (COL) are not supported per *IEEE 802.3-2000* standard. The PCS functionality is enabled by setting the PCS_ENABLE bit and the INT_DEC_ENC_ENABLE bit in Register 0x11 or by setting RGMII_RTBIB pin to logic 1

The PCS receive logic contains an 8B/10B decoder, synchronization state machine, carrier detection logic, receive state machine, and auto-negotiation (AN) state machine. All receive blocks are compliant with the *IEEE 802.3-2000* (Clauses 36 and 37). The PCS Auto-negotiation State Machine, shown in Figure 15, supports both base page and next page exchange as well as having programmable link timers. The link timer value can be programmed via LINK_TIMER_MODE bits [1:0] of Register 0x11. The link timers can be set to approximately 12.6 ms or 16.8 ms to be compliant with the *IEEE 802.3-2000*, the default is 16.8 ms. These state machines are enabled when the PCS_ENABLE bit in Register 0x11 is set to a logic 1 or when the RGMII_RTBIB pin is logic 1.

The management interface provides AN registers as prescribed by *IEEE 802.3-2000*. Additionally, two status registers, Registers 0x19 (Auto Negotiation Status 1) and 0x1A (Auto Negotiation Status 2), have been added for polling the four separate ports with a single management register read. Register 0x19 contains a base page received and a next page received indication for each port. These bits clear on read. Normally during AN, a channel's base page received bit gets set once and then the next page received bit for that channel would get set for any subsequent pages received. If the base page received bit becomes set again during AN, it is an indication that AN has been restarted for that port. Register 0x1A contains an indication for each channel that AN has completed. Both of the status registers reflect same information found in Register 0x01 (Status), bit 5 and Register 0x06 (AN Expansion), bit 1. Reading Register 0x19 only clears that register; it does not clear the page received bits in Register 0x06. The opposite is also true; when reading Register 0x06, Register 0x19 is not cleared.

Additional information on PCS and GMII can be found in *IEEE* 802.3 sections 35 and 36.

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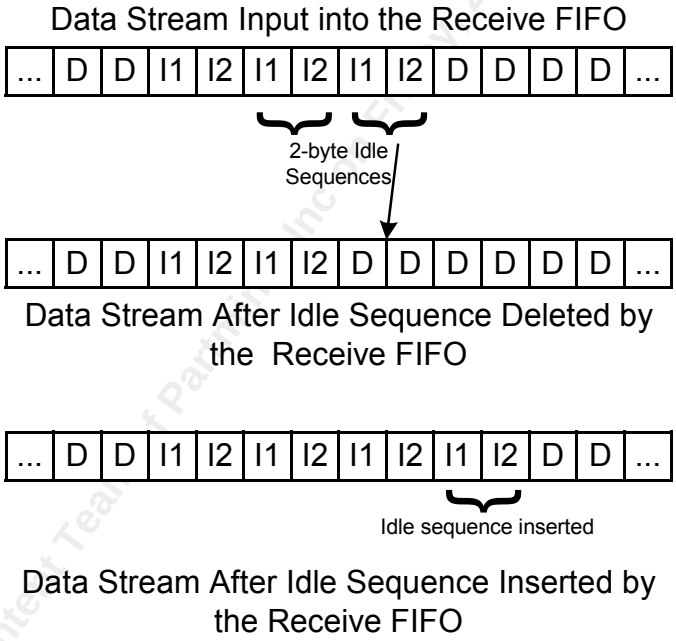
Receive FIFO

The Receive FIFO transfers data from the recovered clock domain to the internal clock domain synchronous to REFCLK. The Receive FIFO compensates for differences in the clock tolerances. The FIFO is enabled when CTC_EN is 1 in RGMII Mode.

The Receive FIFO achieves clock tolerance compensation by inserting or deleting 2 octet wide Gigabit Ethernet IDLE (K28.5, D16.2) sequences. Figure 11 illustrates the insertion (and deletion) of an IDLE sequence when the recovered clock is running slower (or faster) than the REFCLK. The Receive FIFO only deletes an IDLE sequence when more than one IDLE sequence is recognized. When the Receive FIFO inserts an IDLE sequence, the IDLE sequence inserted is the same as the previous IDLE sequence received.

Figure 11 Insertion/Deletion of Idle Sequences by the Receive FIFO



The depth of the Receive FIFO determines the amount of clock frequency difference the QuadPHY 1GR can tolerate. The QuadPHY 1GR has a sixteen (16) character deep FIFO on each receive channel. This enables the QuadPHY 1GR to tolerate up to ±200 ppm clock differences on 1600 byte packets with 4 byte IPG. However, larger packet sizes (16K bytes) can be accommodated in systems with tighter clock differences (±100 ppm) and appropriate IPG (4 bytes).

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The typical additional latency due to FIFO operation is six bytes. To accommodate 16K-byte packets with ±100 ppm reference clock difference between systems, the alignment logic requires that it is able to insert or remove two IDLE sequences between packets. Depending on the relative frequency between reference clock and the received data frequency, the additional latency due to the FIFO operation could be 2 bytes to 12 bytes.

Maximum Size Packets Supported

Internal logic within the QuadPHY 1GR establishes a relationship between the frequency at which serial data is received (f_{DATA}) and ten times the reference clock frequency (f_{REFCLK}) provided by the local clock. This relationship allows the device to recover incoming serial data and place it on the REFCLK domain for further processing. The difference in these two frequencies is usually stated in parts per million (ppm) and is calculated as follows:

$$c_{ppm} = 10^6 \cdot \left| (10 \cdot f_{REFCLK} - f_{DATA}) / (10 \cdot f_{REFCLK}) \right| \quad (1)$$

The maximum allowable frequency offset between the incoming data and the local REFCLK is 200ppm regardless of which operating mode is being used.

When Clock Tolerance Compensation is disabled (CTC_EN = 0 and INT_CTC_EN = 0), there is no maximum packet size. The Receive FIFO is bypassed in this mode and each channel operates on its own independent recovered clock domain.

When Clock Tolerance Compensation is enabled (CTC_EN = 1 or INT_CTC_EN = 1), a maximum packet size is established due to the finite size of the Receive FIFO. When Clock Tolerance Compensation is enabled, the recovered data is sent through the Receive FIFO where all channels are placed on a common clock domain defined by the REFCLK frequency. The maximum packet size (in bytes) supported in this mode can be calculated by the following formula:

$$S_{max} = (10^6 \cdot 5) / c_{ppm} \quad (2)$$

The Receive FIFO performs Clock Tolerance Compensation by inserting or deleting IDLE pairs. Each IDLE pair consists of 2 bytes sequence that are defined in the IDLE1/IDLE2 and IDLE1a/IDLE2a registers. The number of IDLE pairs required in each IPG is dependant upon S_{max} (the maximum packet size used in the system) and C_{ppm}. The number of required IDLE pairs (REQIDLPRS) can be calculated by using the following formula:

$$REQIDLPRS = int [S_{max} \cdot (2 \cdot C_{ppm} / 10^6)] \quad (3)$$

RGMII/RTBI DDR Parallel Receive Output Interface

Each receive parallel interface consists of 5 data/control pins: RXCTLy and RXDy[3:0]. There are two modes of operations for the DDR interface: RGMII Mode and RTBI Mode. There are two sources for the receive clock in RGMII Mode.

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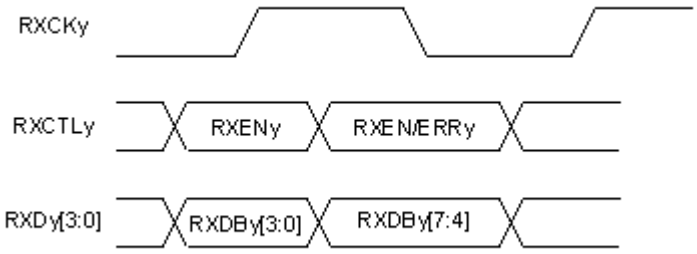
The RGMII Mode or the RTBI Mode can be selected by setting RGMII_RTBIB pin high/low. If the RTBI Mode is selected, receive FIFO is bypassed and recovered clock is used for receive clock of the RTBI output interface. If the RGMII Mode is selected, the source of receive clock for RGMII output interface depends on the value of CTC_EN pin. If CTC_EN is set high, the receive FIFO is enabled and the reference clock is used as the receive clock for the RGMII output interface. If CTC_EN is set low, the receive FIFO is bypassed and the recovered clock is used as the receive clock for the RGMII output interface.

When in the RGMII Mode, bits 3:0 of the receive GMII data byte RXDBy[7:0] are output to RXDy[3:0] pins using the rising edge of the receive clock. The bits 7:4 of the receive GMII data byte RXDBy[7:0] are output to RXDy[3:0] pins using the falling edge of the receive clock. RXENy is output to RXCTLy pin using the rising edge of the receive clock. The derivative (XOR) of RXENy and RXERRy is output to RXCTLy pin using the falling edge of the receive clock. Figure 12 shows the functional timing of the RGMII receive output interface. The mapping of RXENy, RXERRy and RXDBy[7:0] to GMII signals are listed in Table 15.

Figure 12 Center Aligned RGMII Receive (Output) Functional Timing



When in the RTBI Mode, bits 3:0 of the receive 10-bit data RXDTy[9:0] are output to RXDy[3:0] and RXDTy[4] is output to RXCTLy using the rising edge of the receive clock. The bits 8:5 of the receive 10-bit data RXDTy[9:0] are output to RXDy[3:0] and RXDTy[9] from RXCTLy on the falling edge of the receive clock. Figure 13 shows the functional timing of the RGMII receive output interface. The mapping of RXDTy[9:0] to 10-bit code are listed in Table 15.

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Figure 13 Center Aligned RTBI Receive (Output) Functional Timing

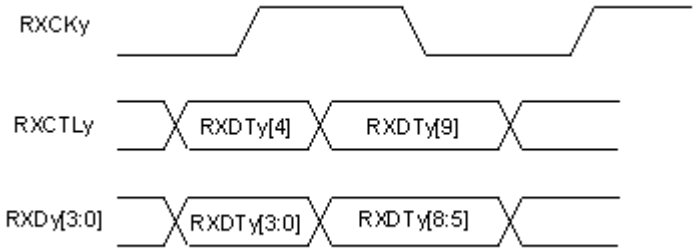

Table 14 summarizes the mapping of RGMII/RTBI parallel receive output ports to the 4 high-speed serial receive output channels.

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Table 14 Parallel Receive Interface Summary for RGMII/RTBI

Serial Tx Ch	Parallel Receive Output Ports	Rx Clock Source	Rx Clock Source	Data Loaded			
		CTC_EN= 1	CTC_EN= 0	Rising Edge RGMII	Falling Edge RGMII	Rising Edge RTBI	Falling Edge RTBI
A	RXCTLA, RXDA[3:0]	REFCLK	recovered clock	RXENA RXDBA[3:0]	RXEN/ERRA RXDBA[7:4]	RXDTA[4] RXDTA[3:0]	RXDTA[9] RXDTA[8:5]
B	RXCTLB, RXDB[3:0]	REFCLK	recovered clock	RXENB RXDBB[3:0]	RXEN/ERRB RXDBB[7:4]	RXDTB[4] RXDTB[3:0]	RXDTB[9] RXDTB[8:5]
C	RXCTLC, RXDC[3:0]	REFCLK	recovered clock	RXENC RXDBC[3:0]	RXEN/ERRC RXDBC[7:4]	RXDTC[4] RXDTC[3:0]	RXDTC[9] RXDTC[8:5]
D	RXCTLD, RXDD[3:0]	REFCLK	recovered clock	RXEND RXDBD[3:0]	RXEN/ERRD RXDBD[7:4]	RXDTD[4] RXDTD[3:0]	RXDTD[9] RXDTD[8:5]

Table 15 Mapping of 10-bit or Byte receive data

RXDTy[9:0] from RTBI	10B Receive Data	RXDB[7:0], RXENy, RXERRy from RGMII	GMII DATA
RXDy[9]	j	RX_ERRy	RX_ER
RXDy[8]	h	RX_ENy	RX_EN
RXDy[7]	g	RXDBy[7]	RXD7
RXDy[6]	f	RXDBy[6]	RXD6
RXDy[5]	i	RXDBy[5]	RXD5
RXDy[4]	e	RXDBy[4]	RXD4
RXDy[3]	d	RXDBy[3]	RXD3
RXDy[2]	c	RXDBy[2]	RXD2
RXDy[1]	b	RXDBy[1]	RXD1
RXDy[0]	a	RXDBy[0]	RXD0

9.3 JTAG Test Access Port

The QuadPHY 1GR supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The JTAG Test Access Port (TAP) consists of the five standard pins (TRSTB, TCK, TMS, TDI and TDO) to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal that resets the TAP controller. TCK is the test clock that samples data on input (TDI) and output (TDO). The TMS input directs the TAP controller through its states. The basic boundary scan architecture is shown below.

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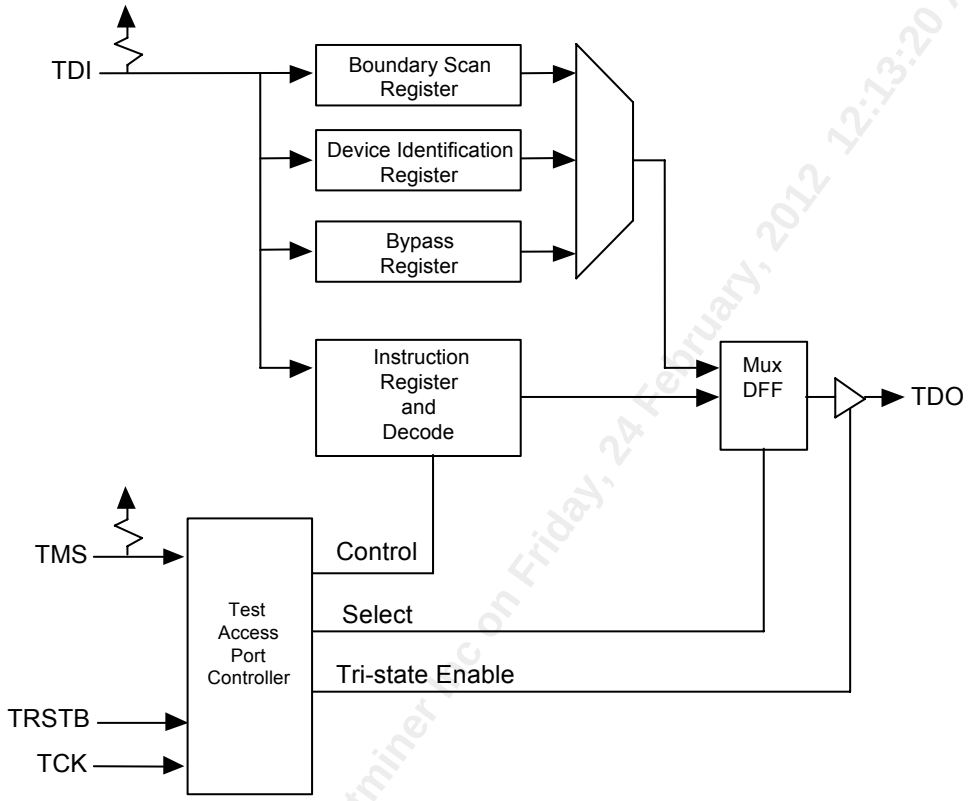
Figure 14 Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input (TDI) to primary output (TDO). The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output (TDO). In addition, patterns can be shifted in on primary input (TDI) and forced onto all digital outputs.

9.3.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input (TCK). All state transitions are controlled using primary input (TMS). The finite state machine is shown in Figure 15.

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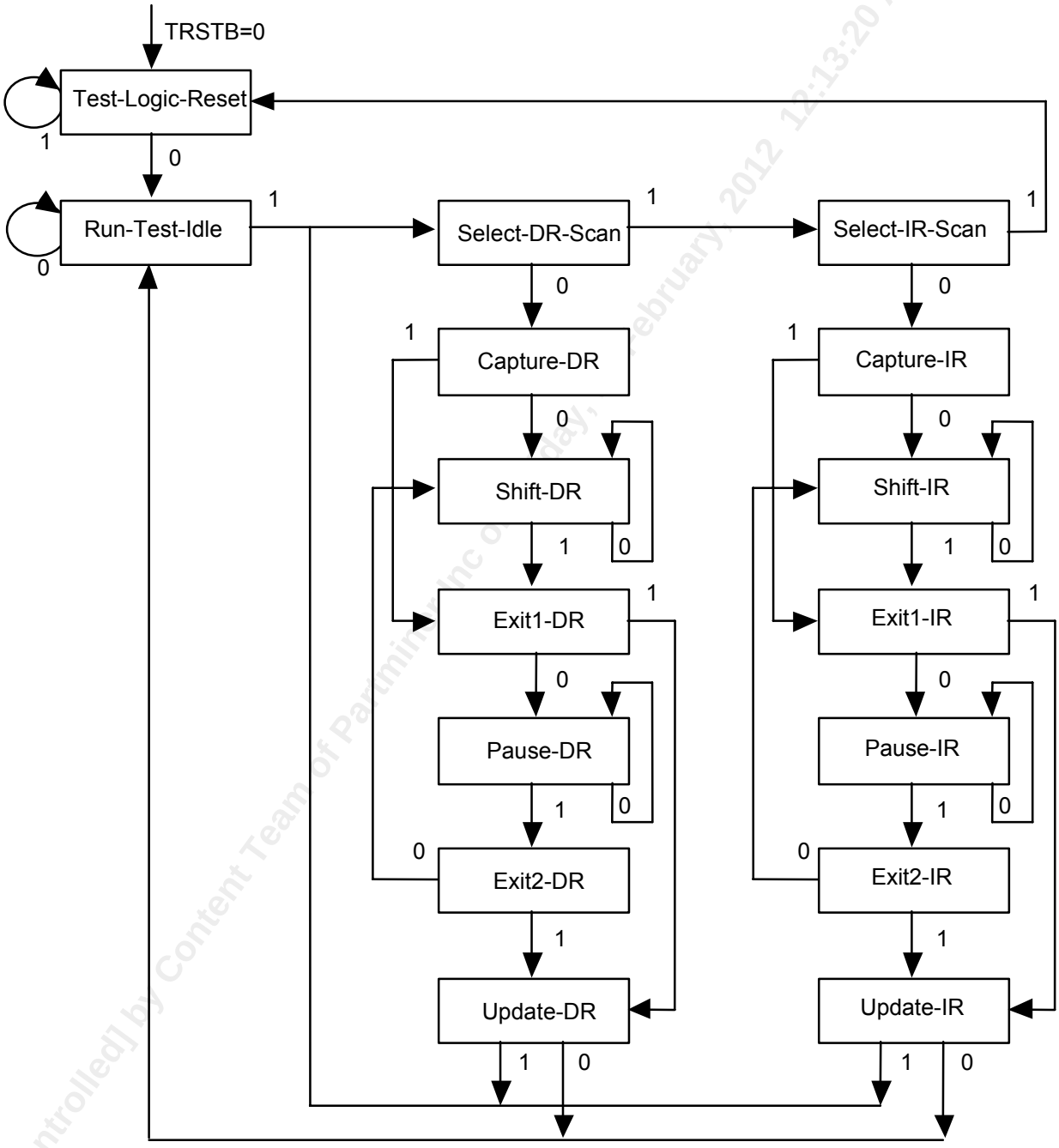
Figure 15 TAP Controller Finite State Machine



Notes:

1. TRSTB must be set to a logic 1 in order to transition out of the Test-Logic-Reset State.

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2. The value shown adjacent to each state transition in Figure 20 represents the signal present at TMS at the rising edge of TCK.
3. All transitions are dependent on the logic level of TMS.

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

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The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

9.3.2 Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects a serial test data register path between input (TDI) and output (TDO).

BYPASS

The bypass instruction shifts data from input (TDI) to output (TDO) with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input (TDI) and output (TDO). Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input (TDI) into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state. The QuadPHY 1GR identification code has not been assigned at this time.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output (TDO) using the Shift-DR state

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9.4 Management Interface

The QuadPHY 1GR implements a management interface that uses a protocol defined in *IEEE* 802.3. This 2-wire interface is used for configuration, control and status of up to four QuadPHY 1GR devices and consists of MDC (management data clock) and MDIO (management data I/O) terminals. This interface allows serial read/write of internal control and status registers. The register map is defined in Figure 18. Note that there are both global address registers, a single register used for all channels and addressed only by bits PHYAD[4:3] of the management frame, and per-port addressed registers, a register addressed using all bits of PHYAD of the management frame. Figure 16 illustrates the addressing of both the global and per-port registers.

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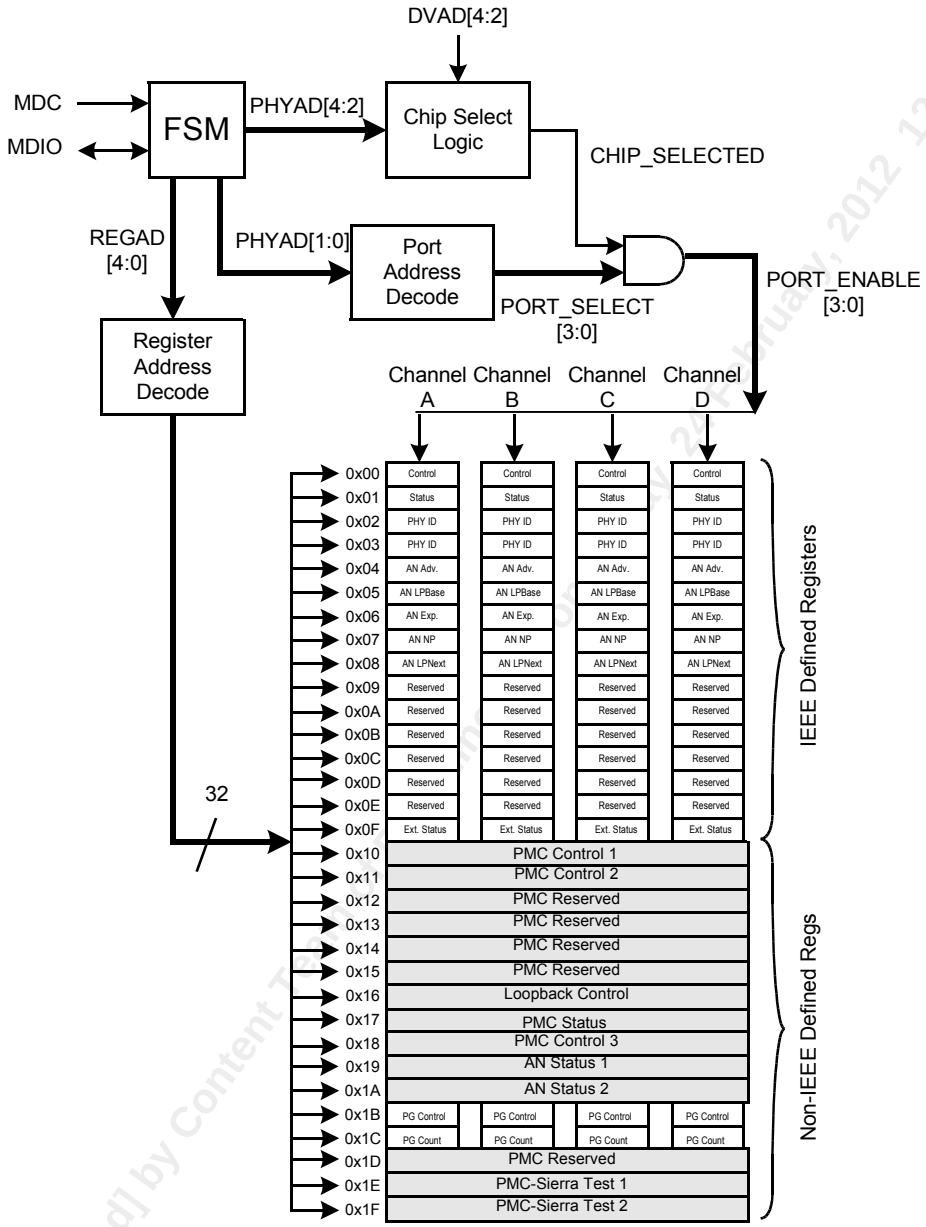
Figure 16 Register Access



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Frames transmitted on the management interface have the frame structure shown in. The order of bit transmission is from left to right.

Table 16 Management Interface Frame Format

	PRE	ST	OP	PHYAD	REGAD	TA	Data	Idle
READ	1 1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1 1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

PRE (Preamble) - At the beginning of each transaction, the management interface controller sends a sequence of 32 contiguous logic 1 bits on MDIO with 32 corresponding cycles on MDC to provide the QuadPHY 1GR with a pattern that it uses to establish synchronization. The QuadPHY 1GR observes a sequence of 32 contiguous 1 bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

ST (Start of Frame) - is indicated by a <01> pattern. This pattern assures transitions from the default logic 1 line state to 0 and back to 1.

OP (Operation Code) - The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.

PHYAD (PHY Address) - is 5 bits, allowing 32 unique device addresses (i.e., eight QuadPHY 1GRs consisting of four devices each.) The first PHY address bit transmitted and received is the MSB of the address.

The QuadPHY 1GR responds only when the PHYAD[4:2] bits match the DVAD[4:2] terminal values. A given port is addressable by the PHYAD[1:0] bits.

PHYAD[4:2] = DVAD[4:2] => selects device.

PHYAD[1:0] = 00 - 11 => selects channel A-D respectively (000 is channel A)

REGAD (Register Address) – is 5 bits, allowing 32 individual registers to be addressed within each QuadPHY 1GR. The first Register Address bit transmitted and received is the MSB of the address.

TA (Turnaround) – is a 2-bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction. For a read transaction, both the management interface controller and the QuadPHY 1GR remain in a high-impedance state for the first bit time of the turnaround. The QuadPHY 1GR drives a 0 bit during the second bit time of the turnaround of a read transaction. During a write transaction, the management interface controller drives a 1 bit for the first bit time of the turnaround and a 0 bit for the second bit time of the turnaround.

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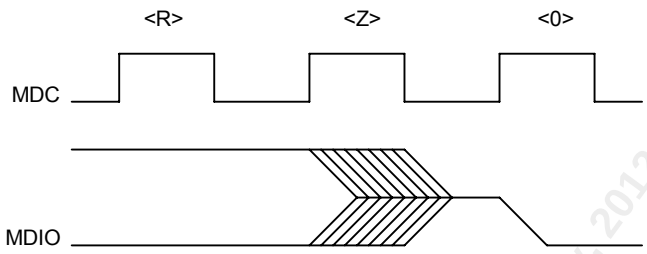
Figure 17 Behavior of MDIO During TA Field of a Read Transaction



DATA - 16-bit field. The first data bit transmitted and received is bit 15 (MSB) of the register being addressed.

IDLE – logic state on MDIO is high-impedance. MDIO must be pulled high when not driven.

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Figure 18 Register Memory Map

Address (Quad)	Register
0x00	GMII Control
0x01	GMII Status
0x02	GMII PHY Identifier
0x03	GMII PHY Identifier
0x04	GMII Auto-Negotiation Advertisement
0x05	GMII Auto-Negotiation Link Partner Base Page Ability
0x06	GMII Auto-Negotiation Expansion
0x07	GMII Auto-Negotiation Next Page Transmit
0x08	GMII Auto-Negotiation Link Partner Next Page Received
0x09	GMII Reserved
0x0A	GMII Reserved
0x0B	GMII Reserved
0x0C	GMII Reserved
0x0D	GMII Reserved
0x0E	GMII Reserved
0x0F	GMII Extended Status
0x10	PMC Control 1
0x11	PMC Control 2
0x12	PMC Reserved
0x13	PMC Reserved
0x14	PMC Reserved
0x15	PMC Reserved
0x16	Loopback Control
0x17	PMC Status
0x18	PMC Control 3
0x19	Auto-Negotiation Status 1
0x1A	Auto-Negotiation Status 2
0x1B	Packet Generator/Checker Control/Status
0x1C	Packet Generator Count Control
0x1D	PMC Reserved
0x1E	Reserved/PMC Test 1
0x1F	Reserved/PMC Test 2

Note:

1. Registers 0x00 – 0x0F are only valid when RGMII_RTBIB = 1.

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10 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the QuadPHY 1GR.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read
2. In configuration bits that can be written into can also be read back. This allows the processor controlling the QuadPHY 1GR to determine the programming state of the block
3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted
4. Writing into read-only normal mode register bit locations does not affect QuadPHY 1GR operation unless otherwise noted
5. Certain register bits are reserved. These bits are associated with either reserved addresses dictated by the IEEE 802.3 standard or PMC-Sierra Test functions. To ensure that the QuadPHY 1GR operates as intended, reserved register bits must be written with their default value as indicated by the register bit description

10.1 IEEE Defined Registers (only applicable in RGMII mode)

Register 0x00: GMII Control

Bit	Type	Function	Default
Bit 15	R/W[1]	RESET	0
Bit 14	R/W	LOOPBACK	0
Bit 13	R	SPEED_SELECTION_LSB	0
Bit 12	R/W	AN_ENABLE	1
Bit 11	R/W	POWER_DOWN	0
Bit 10	R/W	ISOLATE	0
Bit 9	R/W[1]	RESTART_AN	0
Bit 8	R	DUPLEX_MODE	1
Bit 7	R	COLLISION_TEST	0
Bit 6	R	SPEED_SELECTION_MSB	1
Bit 5	R	RESERVED	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

Notes:

1. This bit self clears when written with a Logic 1.

The GMII Control Register provides control over the basic functionality of the QuadPHY 1GR. For additional information refer to *IEEE* Standard 802.3, Section 22.2.4.1.

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SPEED_SELECTION_MSB

The SPEED_SELECTION_MSB bit is used in conjunction with the SPEED_SELECTION_LSB bit (bit 13) to select the speed of operation. Since the QuadPHY 1GR only supports 1000 Mbit/s operation, the SPEED_SELECTION_MSB is a read only bit that is always set to a logic 1.

COLLISION_TEST

The Collision Test functions are not supported by the QuadPHY 1GR. Therefore, the COLLISION_TEST bit is a read only bit that is always set to 0.

DUPLEX_MODE

The QuadPHY 1GR operates in full-duplex mode. Therefore, the DUPLEX_MODE bit is a read only bit that is always set to a logic 1.

RESTART_AN

If a PHY reports via the AN_ENABLE bit (bit 12), that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the QuadPHY 1GR returns a value of 0 for the RESTART_AN bit. If this is the case, the RESTART_AN bit should be written as 0 and any attempt to write a logic 1 is ignored.

Otherwise, the Auto-Negotiation process is started by setting the RESTART_AN to a logic 1. This bit is self-clearing, and the RESTART_AN bit returns a logic 1 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process is not affected by writing a logic 0 into bit RESTART_AN bit.

ISOLATE

The ISOLATE bit is initialized to a logic 0 for normal operation. If the ISOLATE bit is set to a logic 1 and the QuadPHY 1GR's PCS Logic is enabled, the associated transmit and receive channel data paths is disabled and is isolated from the GMII. If the QuadPHY 1GR's PCS Logic is disabled, the state of the ISOLATE bit has no effect on the channel's operation.

POWER_DOWN

The associated channel on the QuadPHY 1GR is placed in a low-power consumption state by setting the POWER_DOWN bit to a logic 1. Clearing the POWER_DOWN bit to a logic 0 allows for normal operation. The QuadPHY 1GR's PCS Logic must be enabled to allow the POWER_DOWN bit to operate as specified. If the PCS Logic is disabled, the state of the POWER_DOWN bit has no effect on the channel's operation. While in the power-down state, the QuadPHY 1GR responds to management transitions.

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AN_ENABLE

The Auto-Negotiation process is enabled by setting the AN_ENABLE bit to a logic 1. If the AN_ENABLE bit is enabled, the Speed Select and Duplex Mode bits have no effect on the link configuration other then providing status. If the AN_ENABLE bit is cleared to a logic 0 then the Speed Select and Duplex Mode bits determines the link configuration.

SPEED_SELECTION_LSB

The SPEED_SELECTION_LSB bit is used in conjunction with the SPEED_SELECTION_MSB bit (bit 6) to select the speed of operation. Since the QuadPHY 1GR supports only 1000 Mbit/s operation, the SPEED_SELECTION_LSB is a read-only bit that is always set to a logic 0.

LOOPBACK

The QuadPHY 1GR is placed into High-speed Serial Loopback Mode when the LOOPBACK bit is set to a logic 1. When the LOOPBACK bit is set, the QuadPHY 1GR accepts data from the GMII transmit data path and returns it to the GMII receive data path. Clearing the LOOPBACK bit to a logic 0 allows the QuadPHY 1GR to operate normally. The DIGITAL_LOOPBACK_EN Control Bit (Bit 7 of Register 0x18) must be set to a logic 0 to operate this Serial Loopback Mode.

RESET

Setting this bit to a logic 1 resets the associated channel in the QuadPHY 1GR. This action sets the status and control registers to their default states. As a consequence, this action can change the internal state of the QuadPHY 1GR and the state of the physical link associated with the QuadPHY 1GR. This bit is self-clearing and the QuadPHY 1GR returns a value of 1 in bit 15 until the reset process is complete. The QuadPHY 1GR is not required to accept a write transaction to the control register until the reset process is complete and writes to bits of the control register other than bit 15 could have no effect until the reset process is completed.

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Register 0x01: GMII Status

Bit	Type	Function	Default
Bit 15	R	100BASE-T4	0
Bit 14	R	100BASE-X_FULL_DUPLEX	0
Bit 13	R	100BASE-X_HALF_DUPLEX	0
Bit 12	R	10MBS_FULL_DUPLEX	0
Bit 11	R	10MBS_HALF_DUPLEX	0
Bit 10	R	100BASE-T2_FULL_DUPLEX	0
Bit 9	R	100BASE-T2_HALF_DUPLEX	0
Bit 8	R	EXTENDED_STATUS	1
Bit 7	R	RESERVED	0
Bit 6	R	MF_PREAMBLE_SUPPRESSION	1
Bit 5	R	AN_COMPLETE	0
Bit 4	R[1]	REMOTE_FAULT	0
Bit 3	R	AN_ABILITY	1
Bit 2	R[2]	LINK_STATUS	0
Bit 1	R	JABBER_DETECT	0
Bit 0	R	EXTENDED_CAPABILITY	1

Notes:

1. This bit latches high and is cleared when read.
2. This bit latches low and is set when read.

The GMII Status Register provides status over the basic functionality of the QuadPHY 1GR. All of the bits in the Status Register are read only, a write to this register has no effect. For additional information refer to *IEEE* Standard 802.3, Section 22.2.4.2.

EXTENDED_CAPABILITY

The EXTENDED_CAPABILITY bit is set to a logic 1 which indicates that the QuadPHY 1GR provides an extended set of capabilities that can be accessed through the extended register set.

JABBER_DETECT

The QuadPHY 1GR is specified to operate at 1000 Mbit/s. PHYs specified to operate at this speed do not incorporate the Jabber Detect function, as this function is defined to be preformed in the repeater unit at this speed. Therefore, the QuadPHY 1GR always returns a value of 0 for JABBER_DETECT.

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LINK_STATUS

When the LINK_STATUS bit is read as a logic 1, it indicates that the QuadPHY 1GR has determined that a valid link has been established. When read as a logic 0, it indicates that the link is not valid. The LINK_STATUS bit is implemented with a latching function, such that the occurrence of a link failure causes the LINK_STATUS bit to be cleared and remain cleared until the GMII Status Register is read.

AN_ABILITY

The QuadPHY 1GR has the ability to perform Auto-Negotiation. Therefore, the AN_ABILITY bit returns a logic 1 when read.

REMOTE_FAULT

When the REMOTE_FAULT bit is read as a logic 1, it indicates that a remote fault condition has been detected. The REMOTE_FAULT bit is implemented with a latching function, such that the occurrence of a remote fault causes the REMOTE_FAULT bit to be set and remain set until the GMII Register is read or when the QuadPHY 1GR is reset.

AN_COMPLETE

When the AN_COMPLETE bit is read as a logic 1, it indicates that the Auto-Negotiation process has been completed, and that the contents of the extended registers implemented by the Auto-Negotiation protocol are valid. The QuadPHY 1GR returns value of 0 in the AN_COMPLETE bit if Auto-Negotiation is disabled.

MF_PREAMBLE_SUPPRESSION

The QuadPHY 1GR is capable of accepting management frames regardless of whether they are or are not preceded by the preamble pattern described in the IEEE Standard 802.3, Section 22.2.4.4.2. Therefore, the MF_PREAMBLE_SUPPRESSION bit returns a logic 1 when read.

EXTENDED_STATUS

The QuadPHY 1GR provides extended base register status information in GMII register 0x0F. Therefore, this bit returns a logic 1 when read.

100BASE-T2_HALF_DUPLEX

The QuadPHY 1GR does not support half duplex link transmission and reception using the 100BASE-T2 signaling specification. Therefore, this bit returns a logic 0 when read.

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100BASE-T2_FULL_DUPLEX

The QuadPHY 1GR does not support full duplex link transmission and reception using the 100BASE-T2 signaling specification. Therefore, this bit returns a logic 0 when read.

10MBS_HALF_DUPLEX

The QuadPHY 1GR does not support half duplex link transmission and reception while operating at 10 Mbit/s. Therefore, this bit returns a logic 0 when read.

10MBS_FULL_DUPLEX

The QuadPHY 1GR does not support full duplex link transmission and reception while operating at 10 Mbit/s. Therefore, this bit returns a logic 0 when read.

100BASE-X_HALF_DUPLEX

The QuadPHY 1GR does not support half duplex link transmission and reception using the 100BASE-X signaling specification. Therefore, this bit returns a logic 0 when read.

100BASE-X_FULL_DUPLEX

The QuadPHY 1GR does not support full duplex link transmission and reception using the 100BASE-X signaling specification. Therefore, this bit returns a logic 0 when read.

100BASE-T4

The QuadPHY 1GR does not support link transmission and reception using the 100BASE-T4 signaling specification. Therefore, this bit returns a logic 0 when read.

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Register 0x02: GMII PHY Identifier 1

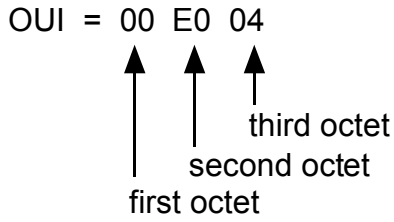
Bit	Type	Function	Default
Bit 15	R	PHY_ID_1[15]	0
Bit 14	R	PHY_ID_1[14]	0
Bit 13	R	PHY_ID_1[13]	0
Bit 12	R	PHY_ID_1[12]	0
Bit 11	R	PHY_ID_1[11]	0
Bit 10	R	PHY_ID_1[10]	0
Bit 9	R	PHY_ID_1[9]	0
Bit 8	R	PHY_ID_1[8]	0
Bit 7	R	PHY_ID_1[7]	0
Bit 6	R	PHY_ID_1[6]	0
Bit 5	R	PHY_ID_1[5]	0
Bit 4	R	PHY_ID_1[4]	1
Bit 3	R	PHY_ID_1[3]	1
Bit 2	R	PHY_ID_1[2]	1
Bit 1	R	PHY_ID_1[1]	0
Bit 0	R	PHY_ID_1[0]	0

The GMII PHY Identifier 1 register contains bit 3 through 18 of the Organizationally Unique Identifier (OUI) assigned to PMC-Sierra by the IEEE. This PHY Identifier is intended to provide sufficient information to support the ResourceTypeID object as required in *IEEE* Standard 802.3, Section 30.1.2.

PHY_ID_1[15:0]

The PHY_ID_1 bits contain bits 3 through 18 of the Organizationally Unique Identifier (OUI). The 3rd bit of the OUI is assigned to PHY_ID_1[15], the 4th bit of the OUI is assigned to PHY_ID_1[14], and so on. Bit PHY_ID_1[0] contains the 18th bit of the OUI. The default setting for PHY_ID_1[15:0] is 0x001Ch.

The Organizationally Unique Identifier (OUI) field is a 24-bit field that extends across the two GMII PHY Identifier Registers. Its value is 00E004H. The mapping of the OUI to the PHY Identifier registers is described below.



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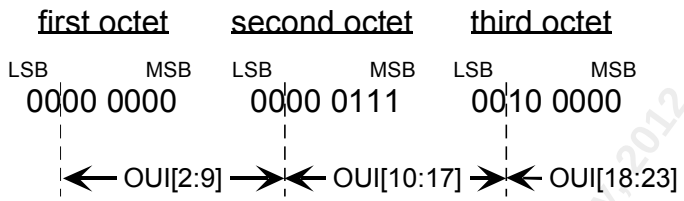
Each octet is represented as a conventional two digit hexadecimal numeral where the first (left-most) digit of the pair is the more significant. The mapping of the OUI to the GMII PHY Identifier registers of the QuadPHY 1GR is described below.



PHY Identifier 1 [15:0] = OUI[2:17] = 001C

PHY Identifier 2 [15:10] = OUI[18:23] = 20

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Register 0x03: GMII PHY Identifier 2

Bit	Type	Function	Default
Bit 15	R	PHY_ID_2[15]	1
Bit 14	R	PHY_ID_2[14]	0
Bit 13	R	PHY_ID_2[13]	0
Bit 12	R	PHY_ID_2[12]	0
Bit 11	R	PHY_ID_2[11]	0
Bit 10	R	PHY_ID_2[10]	0
Bit 9	R	PHY_ID_2[9]	0
Bit 8	R	PHY_ID_2[8]	0
Bit 7	R	PHY_ID_2[7]	1
Bit 6	R	PHY_ID_2[6]	0
Bit 5	R	PHY_ID_2[5]	1
Bit 4	R	PHY_ID_2[4]	0
Bit 3	R	PHY_ID_2[3]	0
Bit 2	R	PHY_ID_2[2]	0
Bit 1	R	PHY_ID_2[1]	0
Bit 0	R	PHY_ID_2[0]	0

The GMII PHY Identifier 2 register contains the 19th through 24th bits of the Organizationally Unique Identifier (OUI) assigned to PMC-Sierra by the IEEE, the 6 bit Manufacturing Model Number and the 4 bit Revision Number. The default value for the GMII PHY Identifier 2 register is 0x80A0.

PHY_ID_2[3:0]

PHY_ID_2[3:0] contain the 4 bit Revision Number of the QuadPHY 1GR. The default setting for these bits change with device revision. The revision number for Revision A of the QuadPHY 1GR is 0x00.

PHY_ID_2[9:4]

PHY_ID_2[9:4] contain the 6 bit Manufacturing Model Number. The default setting for these bits is ’001010’.

PHY_ID_2[15:10]

PHY_ID_2[15:10] contain the 19th through 24th bits of the Organizationally Unique Identifier (OUI). The default setting for these bits is 0x20.

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Register 0x04: GMII Auto-Negotiation Advertisement

Bit	Type	Function	Default
Bit 15	R/W	NEXT_PAGE	0
Bit 14	R	RESERVED	0
Bit 13	R/W	REMOTE_FAULT[1]	0
Bit 12	R/W	REMOTE_FAULT[0]	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R/W	PAUSE[1]	0
Bit 7	R/W	PAUSE[0]	0
Bit 6	R/W	HALF_DUPLEX	0
Bit 5	R/W	FULL_DUPLEX	1
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

The GMII Auto-Negotiation Advertisement register contains the advertised ability of the QuadPHY 1GR. Before Auto-Negotiation starts, this register is configured to advertise the abilities of the QuadPHY 1GR.

FULL_DUPLEX

The QuadPHY 1GR is capable of full-duplex operation. This bit is set to a logic 1 for normal operation

HALF_DUPLEX

The QuadPHY 1GR only supports full-duplex operation. This bit should be set to a logic 0 for normal operation.

PAUSE[1:0]

PAUSE Capabilities. The QuadPHY 1GR's PAUSE capability is encoded in bits 8:7, and the decodes are shown in the Pause Encoding Table below.

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[7]	[8]	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

REMOTE_FAULT[1:0]

The QuadPHY 1GR's remote fault condition is encoded in bits 13:12 of the base page. Values are shown in Remote Fault Encoding Table shown below. The default value is 0x00b. The QuadPHY 1GR indicates a fault by setting a non-zero Remote Fault encoding and re-negotiating.

[12]	[13]	Description
0	0	No error, link OK
0	1	Offline
1	0	Link Failure
1	1	Auto-Negotiation Error

NEXT_PAGE

The base page can set the NEXT_PAGE bit to a logic 1 to request next page transmission. Subsequent next pages can set the NEXT_PAGE bit to a logic 0 in order to communicate that there is no more next page information to be sent.

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Register 0x05: GMII Auto-Negotiation Link Partner Ability Base Page

Bit	Type	Function	Default
Bit 15	R	NEXT_PAGE	0
Bit 14	R	ACKNOWLEDGE	0
Bit 13	R	REMOTE_FAULT[1]	0
Bit 12	R	REMOTE_FAULT[0]	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R	PAUSE[1]	0
Bit 7	R	PAUSE[0]	0
Bit 6	R	HALF_DUPLEX	0
Bit 5	R	FULL_DUPLEX	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

The GMII Auto-Negotiation Link Partner Ability Base Page register contains the advertised ability of the link partner's base page. The values contained in the GMII Auto-Negotiation Link Partner Ability Base Page register are guaranteed to be valid either once the Auto-Negotiation has successfully completed, as indicated by the Auto-Negotiation Complete bit in the GMII Status register or when the Page Received bit in the GMII Auto-Negotiation Expansion Register is set to a logic 1.

All of the bits in the GMII Auto-Negotiation Link Partner Ability Base Page register are read only. A write to this register has no effect.

FULL_DUPLEX

If the FULL_DUPLEX bit is set to logic 1, it means that the QuadPHY 1GR's Link Partner is capable of operating in full-duplex mode. This bit is initialized to a logic 0.

HALF_DUPLEX

If the HALF_DUPLEX bit is set to logic 1, it means that the QuadPHY 1GR's Link Partner is capable of operating in half-duplex mode. This bit is initialized to a logic 0.

PAUSE[1:0]

PAUSE Capabilities. The Link Partner's PAUSE capability is encoded in bits 8:7, and the decodes are shown in the Pause Encoding Table below.

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[7]	[8]	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

REMOTE_FAULT[1:0]

The Link Partner's remote fault condition is encoded in bits 13:12 of the base page. Values are shown in Remote Fault Encoding Table shown below. The default value is 0x00b. The Link Partner indicates a fault by sending a non-zero Remote Fault encoding and during Auto-Negotiation.

[12]	[13]	Description
0	0	No error, link OK
0	1	Offline
1	0	Link_Failure
1	1	Auto-Negotiation_Error

ACKNOWLEDGE

The Acknowledge (Ack) bit is used by the Auto-Negotiation function to indicate that the local device has successfully received its link partner's base page.

Logic 0 = device has not received the message.

Logic 1 = device has received the message.

NEXT_PAGE

The base page and subsequent next pages can set the NEXT_PAGE bit to a logic 1 to indicate that there is additional next pages to be received. Subsequent next pages can set the NEXT_PAGE bit to a logic 0 in order to communicate that there the last page has been received.

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Register 0x06: GMII Auto-Negotiation Expansion

Bit	Type	Function	Default
Bit 15	R	RESERVED	0
Bit 14	R	RESERVED	0
Bit 13	R	RESERVED	0
Bit 12	R	RESERVED	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R	RESERVED	0
Bit 7	R	RESERVED	0
Bit 6	R	RESERVED	0
Bit 5	R	RESERVED	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	NEXT_PAGE_ABLE	1
Bit 1	R[1]	PAGE_RECEIVED	0
Bit 0	R	RESERVED	0

Notes:

1. This bit latches high and is cleared when read.

All of the bits in the GMII Auto-Negotiation Expansion register are read only. A write to this register has no effect.

PAGE_RECEIVED

The PAGE_RECEIVED bit is reset to a logic 0 on a read to the GMII Auto-Negotiation Expansion register. Subsequent to the setting of the Page Received bit, and in order to prevent overlay of the Auto-Negotiation Link Partner Ability Next Page register, the Auto-Negotiation Link Partner Ability Next Page register should be read before the Auto-Negotiation Next Page Transmit register is written.

NEXT_PAGE_ABLE

The Next Page Able bit is set to a logic 1 to indicate that the QuadPHY 1GR supports the Next Page function.

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Register 0x07: GMII Auto-Negotiation Next Page Transmit

Bit	Type	Function	Default
Bit 15	R/W	NEXT_PAGE	0
Bit 14	R	RESERVED	0
Bit 13	R/W	MESSAGE_PAGE	0
Bit 12	R/W	ACKNOWLEDGE_2	0
Bit 11	R	TOGGLE	0
Bit 10	R/W	MESSAGE_UNFORMATTED_CODE FIELD[10]	0
Bit 9	R/W	MESSAGE_UNFORMATTED_CODE FIELD[9]	0
Bit 8	R/W	MESSAGE_UNFORMATTED_CODE FIELD[8]	0
Bit 7	R/W	MESSAGE_UNFORMATTED_CODE FIELD[7]	0
Bit 6	R/W	MESSAGE_UNFORMATTED_CODE FIELD[6]	0
Bit 5	R/W	MESSAGE_UNFORMATTED_CODE FIELD[5]	0
Bit 4	R/W	MESSAGE_UNFORMATTED_CODE FIELD[4]	0
Bit 3	R/W	MESSAGE_UNFORMATTED_CODE FIELD[3]	0
Bit 2	R/W	MESSAGE_UNFORMATTED_CODE FIELD[2]	0
Bit 1	R/W	MESSAGE_UNFORMATTED_CODE FIELD[1]	0
Bit 0	R/W	MESSAGE_UNFORMATTED_CODE FIELD[0]	0

The GMII Auto-Negotiation Next Page Transmit register contains the advertised ability of the QuadPHY 1GR's next page.

MESSAGE_UNFORMATTED_CODE FIELD[10:0]

The MESSAGE_UNFORMATTED_CODE FIELD is an eleven bit wide field, encoding 2048 possible messages. Message Code Field definitions are found in the IEEE 802.3u/Annex 28C.

TOGGLE

The TOGGLE bit is used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange. The bit is always set to the opposite value of the Toggle bit in the previously exchanged Link Code Word. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word and therefore can assume a value of logic 1 or 0.

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ACKNOWLEDGE_2

The ACKNOWLEDGE_2 bit is used by next page function to indicate that a device has the ability to comply with the message. The ACKNOWLEDGE_2 bit is set as follows:

Logic 0 = device cannot comply with message.

Logic 1 = will comply with message.

MESSAGE_PAGE

The MESSAGE_PAGE bit is used by the Next Page function to differentiate a Message Page from an Unformatted Page. The MESSAGE_PAGE bit is set as follows:

Logic 0 = Unformatted Page.

Logic 1 = Message Page.

NEXT_PAGE

The NEXT_PAGE bit is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. The NEXT_PAGE bit is set as follows:

Logic 0 = Last Page.

Logic 1 = Additional Next Page(s) will follow.

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Register 0x08: GMII Auto-Negotiation Link Partner Next Page Ability

Bit	Type	Function	Default
Bit 15	R	NEXT_PAGE	0
Bit 14	R	ACKNOWLEDGE	0
Bit 13	R	MESSAGE_PAGE	0
Bit 12	R	ACKNOWLEDGE_2	0
Bit 11	R	TOGGLE	0
Bit 10	R	MESSAGE_UNFORMATTED_CODE FIELD[10]	0
Bit 9	R	MESSAGE_UNFORMATTED_CODE FIELD[9]	0
Bit 8	R	MESSAGE_UNFORMATTED_CODE FIELD[8]	0
Bit 7	R	MESSAGE_UNFORMATTED_CODE FIELD[7]	0
Bit 6	R	MESSAGE_UNFORMATTED_CODE FIELD[6]	0
Bit 5	R	MESSAGE_UNFORMATTED_CODE FIELD[5]	0
Bit 4	R	MESSAGE_UNFORMATTED_CODE FIELD[4]	0
Bit 3	R	MESSAGE_UNFORMATTED_CODE FIELD[3]	0
Bit 2	R	MESSAGE_UNFORMATTED_CODE FIELD[2]	0
Bit 1	R	MESSAGE_UNFORMATTED_CODE FIELD[1]	0
Bit 0	R	MESSAGE_UNFORMATTED_CODE FIELD[0]	0

The GMII Auto-Negotiation Link Partner Next Page Ability register contains the ability of the link partner's next page. The GMII Auto-Negotiation Link Partner Next Page Ability register is a read only register. Any writes to this register have no effect.

MESSAGE_UNFORMATTED_CODE FIELD[10:0]

The MESSAGE_UNFORMATTED_CODE FIELD is an eleven bit wide field, encoding 2048 possible messages. Message Code Field definitions are found in the IEEE 802.3u/Annex 28C.

TOGGLE

The TOGGLE bit is used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange. The bit is always set to the opposite value of the Toggle bit in the previously exchanged Link Code Word. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word and therefore can assume a value of logic 1 or 0.

ACKNOWLEDGE_2

The ACKNOWLEDGE_2 bit is used by next page function to indicate that a device has the ability to comply with the message. The ACKNOWLEDGE_2 bit is set as follows:

Logic 0 = device cannot comply with message.

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Logic 1 = will comply with message.

MESSAGE_PAGE

The MESSAGE_PAGE bit is used by the Next Page function to differentiate a Message Page from an Unformatted Page. The MESSAGE_PAGE bit is set as follows:

Logic 0 = Unformatted Page.

Logic 1 = Message Page.

ACKNOWLEDGE

The ACKNOWLEDGE bit is used by the next page function to indicate that a device has received the message. The ACKNOWLEDGE bit is set as follows:

Logic 0 = device has not received the message.

Logic 1 = device has received the message.

NEXT_PAGE

The NEXT_PAGE bit is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. The NEXT_PAGE bit is set as follows:

Logic 0 = Last Page.

Logic 1 = Additional Next Page(s) will follow.

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Registers 0x09 through 0x0E: Reserved

Bit	Type	Function	Default
Bit 15	R	RESERVED	0
Bit 14	R	RESERVED	0
Bit 13	R	RESERVED	0
Bit 12	R	RESERVED	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R	RESERVED	0
Bit 7	R	RESERVED	0
Bit 6	R	RESERVED	0
Bit 5	R	RESERVED	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

Registers 0x09 through 0x0E are reserved for feature use. These registers are read only. Any writes to these registers have no effect.

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Register 0x0F: GMII Extended Status

Bit	Type	Function	Default
Bit 15	R	1000BASE-X_FULL_DUPLEX	1
Bit 14	R	1000BASE-X_HALF_DUPLEX	0
Bit 13	R	1000BASE-T_FULL_DUPLEX	0
Bit 12	R	1000BASE-T_HALF_DUPLEX	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R	RESERVED	0
Bit 7	R	RESERVED	0
Bit 6	R	RESERVED	0
Bit 5	R	RESERVED	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

The Extended Status register is supported by the QuadPHY 1GR. All bits in the Extended Status register are read only. Any writes to this register have no effect.

1000BASE-T_HALF_DUPLEX

This bit is always read as logic 0, as the QuadPHY 1GR does not support 1000BASE-T Half Duplex Operation.

1000BASE-T_FULL_DUPLEX

This bit is always read as logic 0, as the QuadPHY 1GR does not support 1000BASE-T Full Duplex Operation.

1000BASE-X_HALF_DUPLEX

This bit is always read as logic 0, as the QuadPHY 1GR does not support 1000BASE-X Half Duplex Operation.

1000BASE-X_FULL_DUPLEX

This bit is always read as logic 1, as the QuadPHY 1GR has the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification.

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10.2 Non-IEEE Defined Registers

Register 0x10: PMC Control 1

Bit	Type	Function	Default
Bit 15	R/W	ENABLE_CHN_D	1
Bit 14	R/W	RESERVED	0
Bit 13	R/W	ENABLE_CHN_C	1
Bit 12	R/W	RESERVED	0
Bit 11	R/W	ENABLE_CHN_B	1
Bit 10	R/W	RESERVED	0
Bit 9	R/W	ENABLE_CHN_A	1
Bit 8	R/W	RESERVED	0
Bit 7	R/W	COMMA_DETECT_SEL[1]	1
Bit 6	R/W	COMMA_DETECT_SEL[0]	0
Bit 5	R/W	HIGH_AMPLITUDE	1
Bit 4	R	RESERVED	0
Bit 3	R/W	FILTER_COEFFICIENTS [3]	1
Bit 2	R/W	FILTER_COEFFICIENTS [2]	0
Bit 1	R/W	FILTER_COEFFICIENTS [1]	0
Bit 0	R/W	FILTER_COEFFICIENTS [0]	0

The PMC Control 1 register provides control over custom functionality in the QuadPHY 1GR. This register controls functionality across all four channels of the device.

FILTER_COEFFICIENTS[3:0]

These bits select the time constants of the digital filter of the clock recovery function. The requirement for advancing the phase of the recovered clock by 1/16 of a baud interval is that the difference between the number of late and early data edges exceeds 4x FILT[3:0]. While the clock phase tracking is not a linear control system, FILT[3:0] provide the capability to track frequency modulation (jitter) on the input waveforms ranging from approximately 1 MHz to 16 MHz without attenuation.

For proper operation, use the default setting. Values 0x1 through 0xF are valid. A value of 0x0 is not valid and should not be used.

HIGH_AMPLITUDE

This bit selects the drive capability for the TDO+ and TDO- terminals. When set to 1, the TDO+/TDO- terminals are configured for high amplitude drive. If the High Amplitude bit is set to 0, the terminals are configured for low amplitude drive

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COMMA_DETECT_SEL[1:0]

These bits enable positive, negative, or both positive and negative comma detection. When COMMA_DETECT_SEL[1] is set to 1, positive comma detection is enabled. Setting COMMA_DETECT_SEL[0] to 1 enables negative comma detection.

ENABLE_CHN_A through D

The ENABLE_CHN bit enables or disables the operation of the associated Channel on the QuadPHY 1GR. If these bits are set to a logic 1 the associated channel is enabled. If these bits are set to a logic 0, the assoicated channel is disabled. When a channel is disabled, the receive clock continues to toggle but at a slower frequency. All ENABLE_CHN bits are initialized to a logic 1.

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Register 0x11: PMC Control 2

Bit	Type	Function	Default
Bit 15	R/W	INT_TCLKSEL	0
Bit 14	R/W	RESERVED	0
Bit 13	R/W	RESERVED	1
Bit 12	R/W	RESERVED	0
Bit 11	R/W	RESERVED	0
Bit 10	R/W	RESERVED	0
Bit 9	R/W	IPOEN	1
Bit 8	R/W	ENABLE_COMMA_DETECT	1
Bit 7	R/W	INT_DEC_ENC_ENABLE	0
Bit 6	R/W	RESERVED	0
Bit 5	R/W	RESERVED	0
Bit 4	R/W	RESERVED	0
Bit 3	R/W	SOFT_RESET	0
Bit 2	R/W	PCS_ENABLE	0
Bit 1	R/W	LINK_TIMER_MODE1	0
Bit 0	R/W	LINK_TIMER_MODE0	0

The PMC Control 2 register provides control over custom functionality in the QuadPHY 1GR. This register controls functionality across all four channels of the device.

LINK_TIMER_MODE[1:0]

Link Timer Mode. These bits control the duration of the link timers within the Auto-Negotiation logic.

[1]	[0]	Duration
0	0	16.8ms
0	1	12.6ms
1	0	500ns (test mode)
1	1	250ns (test mode)

PCS_ENABLE

The PCS_ENABLE bit is logically OR'd with the RGMII_RTBIB input terminal. Enable PCS Data Processing (enable = 1). When this bit is set to 1, the chip processes PCS data and treats the parallel interface as RGMII (4 bits data plus TXCTL or RXCTL).

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SOFT_RESET

Soft Reset (Active High). This bit resets all the logic and state machines in the receive and transmit channels to their original state. The PLL, configuration and status register bits are not affected by the assertion of this bit. This bit is NOT self-clearing. Once set by an MDC/MDIO access, it can be cleared immediately with another MDC/MDIO access.

QuadINT_DEC_ENC_ENABLE

The INT_DEC_ENC_ENABLE bit is logically OR'd with the RGMII_RTBIB input terminal. It controls if the Internal Decoder/Encoder is enabled. If it is set to logic 1 the Internal Decoder/Encoder is enabled.

ENABLE_COMMA_DETECT

The ENABLE_COMMA_DETECT bit controls if the Comma Detect is enabled and if byte alignment is performed on incoming comma sequences. Based on the configuration of the Comma Detect Select Bits in the PMC Control 1 Register, the comma alignment can be programmed to align on positive, negative, or both positive and negative commas. If this bit is set to logic 1, the Comma Detect is enabled.

IPOEN

The IPOEN bit controls the Internal Parallel Output Enable. This bit is logically ANDed with the POEN input terminal. If it is set to logic 1 the Parallel Outputs are enabled.

INT_TCLKSEL

The INT_TCLKSEL bit is logically Ored with TCLKSEL input terminal. The INT_TCLKSEL bit controls the selection of the Transmit Clocks. If set to logic 1, four separate TXCK input pins are active, each providing the input timing reference for the corresponding channel. When set to logic 0, a single TXCK input (TXCKA) is used as the timing reference for all input channels. The other transmit clocks are ignored.

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Register 0x12 – 0x15: PMC Reserved

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Register 0x16: Loopback Control

Bit	Type	Function	Default
Bit 15	R/W	INT_EN_SERIAL_LPBK_D	0
Bit 14	R/W	RESERVED	0
Bit 13	R/W	INT_EN_SERIAL_LPBK_C	0
Bit 12	R/W	RESERVED	0
Bit 11	R/W	INT_EN_SERIAL_LPBK_B	0
Bit 10	R/W	RESERVED	0
Bit 9	R/W	INT_EN_SERIAL_LPBK_A	0
Bit 8	R/W	RESERVED	0
Bit 7	R/W	EN_PAR_LPBK_D	0
Bit 6	R/W	RESERVED	0
Bit 5	R/W	EN_PAR_LPBK_C	0
Bit 4	R/W	RESERVED	0
Bit 3	R/W	EN_PAR_LPBK_B	0
Bit 2	R/W	RESERVED	0
Bit 1	R/W	EN_PAR_LPBK_A	0
Bit 0	R/W	RESERVED	0

The PMC Loopback Control register provides control over the QuadPHY 1GR's serial and parallel loopback capabilities.

EN_PAR_LPBK_A:D

The EN_PAR_LPBK_A:D bits control the loop-back function for the parallel data on each channel. When these bits are set to a logic 1, the associated RXDy[3:0]/RXCTLy outputs are routed to the corresponding channel inputs. In normal operation, the TXDy[3:0]/TXCTLy inputs are routed to the channel inputs. The QuadPHY 1GR must be configured for a diagnostic operating mode in order to use parallel loopback. See Section 12.3 for more details.

INT_EN_SERIAL_LPBK_A :D

The INT_EN_SERIAL_LPBK_A :D bits enable the loop-back function for the corresponding serial channel. When set to a logic 1, the QuadPHY 1GR routes the internal output of the Serializer to the input of the clock recovery block. The TDO+/TDO- terminals for the selected channel are held in the 1 state as long as this bits are active.

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Register 0x17: Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R[1]	Reserved	0
Bit 10	R[1]	PLL_LOCK	0
Bit 9	R	RESERVED	0
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	1
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Note:

1. This bit latches low and is set when read

The PMC Status register provides status of the QuadPHY 1GR.

PLL_LOCK

The PLL_LOCK bit when 0 indicates that the PLL has lost lock. This failure indication is sustained until register 0x17 is read even if the PLL regains lock. When PLL_LOCK is a logic 1, this indicates that the PLL has achieved and maintained lock.

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Register 0x18: PMC Control 3

Bit	Type	Function	Default
Bit 15	R/W	RESERVED	0
Bit 14	R/W	RESERVED	0
Bit 13	R/W	RESERVED	0
Bit 12	R/W	INT_CTC_EN	0
Bit 11	R	RESERVED	0
Bit 10	R/W	RESERVED	1
Bit 9	R/W	BA_HYST_EN	0
Bit 8	R/W	RESERVED	1
Bit 7	R/W	DIGITAL_LPBK_EN	0
Bit 6	R/W[1]	CODE_ERR_STB	0
Bit 5	R/W	RESERVED	0
Bit 4	R/W	RESERVED	0
Bit 3	R/W	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

Note:

1. This bit self clears when written with a 1.

The PMC Control 3 register provides control over custom functionality in the QuadPHY 1GR. This register controls functionality across all four channels of the device.

CODE_ERR_STB

When 1, CODE_ERR_STB clears all 8B/10B code error counters within the 8B/10B decoder blocks. The CODE_ERR_STB is self-clearing. When 0, the 8B/10B code error counters continue to increment on received code errors until the maximum count, CODE_ERR_THR[14:0] is reached. CODE_ERR_THR is equivalent to PKT_CNT[14:0] in the Packet Generator Control register when EN_CODE_ERR_CHK is a 1.

DIGITAL_LPBK_EN

When 1, DIGITAL_LPBK_EN enables the INT_EN_SERIAL_LPBK_[D:A] bits in the Loopback Control register to enable the purely digital loopback path per channel. This path is from the output of the encoder in the transmit path to the input of the byte alignment logic in the receive path. When 0, DIGITAL_LPBK_EN enables the INT_EN_SERIAL_LPBK_[D:A] bits in the Loopback Control register to enable the high-speed serial loopback path. This bit and all the INT_EN_SERIAL_LPBK_[D:A] bits are logically ORed with the input terminal G_DIGLB.

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BA_HYST_EN

When 1, BA_HYST_EN enables the byte synchronization state machine within the byte alignment logic to control when the byte alignment logic can realign to a comma. When BA_HYST_EN is a logic 0, the byte alignment logic realigns immediately to a received comma pattern.

INT_CTC_EN

This bit is logically ORed with the CTC_EN input pin. The INT_INS_DEL_EN bit controls whether the QuadPHY 1GR inserts or deletes IDLEs in to its Receive FIFOs for clock compensation. When the INT_INS_DEL_EN bit is set to a logic 0, the QuadPHY 1GR does not insert and delete IDLEs from its Receive FIFO. If the INS_DEL_EN bit is set to a logic 1, the QuadPHY 1GR inserts and delete IDLEs from its Receive FIFO.

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Register 0x19: Auto-Negotiation Status 1

Bit	Type	Function	Default
Bit 15	R[1]	BASE_PAGE_RX_D	0
Bit 14	R[1]	RESERVED	0
Bit 13	R[1]	BASE_PAGE_RX_C	0
Bit 12	R[1]	RESERVED	0
Bit 11	R[1]	BASE_PAGE_RX_B	0
Bit 10	R[1]	RESERVED	0
Bit 9	R[1]	BASE_PAGE_RX_A	0
Bit 8	R[1]	RESERVED	0
Bit 7	R[1]	NEXT_PAGE_RX_D	0
Bit 6	R[1]	RESERVED	0
Bit 5	R[1]	NEXT_PAGE_RX_C	0
Bit 4	R[1]	RESERVED	0
Bit 3	R[1]	NEXT_PAGE_RX_B	0
Bit 2	R[1]	RESERVED	0
Bit 1	R[1]	NEXT_PAGE_RX_A	0
Bit 0	R[1]	RESERVED	0

Note:

1. This bit latches high and is cleared when read

The Auto-Negotiation Status 1 register provides Base Page and Next Page reception status for each channel of the QuadPHY 1GR.

NEXT_PAGE_RX_A through D

The NEXT_PAGE_RX bit indicates if a Next Page has been successfully received on the specified Channel. All NEXT_PAGE_RX bits are cleared on a read.

BASE_PAGE_RX_A through D

The BASE_PAGE_RX bits indicate if a Base Page has been successfully received on the specified Channel. All BASE_PAGE_RX bits are cleared on a read.

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Register 0x1A: Auto-Negotiation Status 2

Bit	Type	Function	Default
Bit 15	R	AN_CMPLETE_D	0
Bit 14	R	RESERVED	0
Bit 13	R	AN_CMPLETE_C	0
Bit 12	R	RESERVED	0
Bit 11	R	AN_CMPLETE_B	0
Bit 10	R	RESERVED	0
Bit 9	R	AN_CMPLETE_A	0
Bit 8	R	RESERVED	0
Bit 7	R[1]	BYTE_ALIGN_STAT_D	0
Bit 6	R[1]	RESERVED	0
Bit 5	R[1]	BYTE_ALIGN_STAT_C	0
Bit 4	R[1]	RESERVED	0
Bit 3	R[1]	BYTE_ALIGN_STAT_B	0
Bit 2	R[1]	RESERVED	0
Bit 1	R[1]	BYTE_ALIGN_STAT_A	0
Bit 0	R[1]	RESERVED	0

Note:

1. This bit latches low and is set when read

The Auto-Negotiation Status 2 register provides Auto-Negotiation Complete status for each channel of the QuadPHY 1GR.

BYTE_ALIGN_STAT_A through D

The BYTE_ALIGN_STAT provide byte alignment status. If the bit for the associated channel is read as a logic 0, it indicates that the byte synchronization state machine within the byte alignment logic for the specified channel has determined that byte alignment has been lost. This failure indication is sustained until register 0x1A is read even if byte alignment is regained. If the BYTE_ALIGN_STAT bit for the associated channel is read as a logic 1, it indicates that the byte synchronization state machine within the byte alignment logic for channel A has determined that byte alignment has been achieved.

AN_CMPLETE_A through D

The AN_CMPLETE bits indicate if the Auto-Negotiation has completed on the specified Channel of the QuadPHY 1GR.

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Register 0x1B: Packet Generator/Checker Control/Status

Bit	Type	Function	Default
Bit 15	R/W	EN_PKT_GEN	0
Bit 14	R/W	EN_PKT_COMP	0
Bit 13	R/W[1]	ERROR_CNT_RESET	0
Bit 12	R/W[1]	FORCE_ERROR	0
Bit 11	R/W	EN_CODE_ERR_CHK	0
Bit 10	R[2]	CODE_ERR_EXCEED	0
Bit 9	R[2]	RXFIFO_RESYNC	0
Bit 8	R[2]	TXFIFO_RESYNC	0
Bit 7	R	ERROR_CNT[7]	0
Bit 6	R	ERROR_CNT[6]	0
Bit 5	R	ERROR_CNT[5]	0
Bit 4	R	ERROR_CNT[4]	0
Bit 3	R	ERROR_CNT[3]	0
Bit 2	R	ERROR_CNT[2]	0
Bit 1	R	ERROR_CNT[1]	0
Bit 0	R	ERROR_CNT[0]	0

Notes:

1. This bit self clears when written with a 1.
2. This bit latches high and is cleared when read.

The Packet Generator/Checker Control/Status register provides control and status information for QuadPHY 1GR's Packet Generator and Checker capabilities. The QuadPHY 1GR provides a Packet Generator/Checker Control/Status register for each channel.

ERROR_CNT[7:0]

The ERROR_CNT bits identify the number of errors that have occurred on the associated channel. This counter resets to 0x00h upon set the ERROR_CNT RESET bit. The Error Counter does not rollover when it reaches its maximum count of 0xFFh. It holds the 0xFFh value until it is reset.

TXFIFO_RESYNC

When 1, the TXFIFO_RESYNC bit indicates that the transmit FIFO within the channel has resynchronized its read and write pointers to avoid pointer collision. This resync indication is sustained until register 0x1B is read.

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RXFIFO_RESYNC

When 1, the RXFIFO_RESYNC bit indicates that the Receive FIFO within the channel has resynchronized its read and write pointers to avoid pointer collision. This resync indication is sustained until register 0x1B is read.

CODE_ERR_EXCEED

When 1, the CODE_ERR_EXCEED bit indicates that the 8B/10B code error counter within the decoder logic has exceeded the error count threshold, CODE_ERR_THR[14:0]. CODE_ERR_THR is equivalent to PKT_CNT[14 :0] in register 0x1C when EN_CODE_ERR_CHK is a 1. When the error count exceeds the CODE_ERR_THR, CODE_ERR_EXCEED is sustained as a 1 until register 0x1B is read. The 8B/10B coding error counters in all channels is cleared whenever the CODE_ERR_STB bit in register 0x18 is set to logic 1.

The Code Error test feature can be used with the Packet Generator enabled and operating in Continuous Test Generation Mode.

EN_CODE_ERR_CHK

When 1, the 8B/10B code error counter within the decoder logic counts received code errors and indicates that the count has exceeded the CODE_ERR_THR count by setting CODE_ERR_EXCEED to a 1. When 0, the 8B/10B code error counter is disabled.

FORCE_ERROR

The FORCE_ERROR bit forces the packet generator to create a single byte error in the next data byte or in the next packet if IDLE is currently being generated. This bit is self clearing.

ERROR_CNT_RESET

The ERROR_CNT_RESET bit resets the Error Counter to 0x00h. This bit is self clearing.

EN_PKT_COMP

The EN_PKT_COMP bit enables the Packet Comparator for an associated channel.

EN_PKT_GEN

The EN_PKT_COMP bit enables the Packet Generator for an associated channel.

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Register 0x1C: Packet Generator Count Control

Bit	Type	Function	Default
Bit 15	R/W	CONT_TEST_GEN	0
Bit 14	R/W	PKT_CNT[14]	0
Bit 13	R/W	PKT_CNT[13]	0
Bit 12	R/W	PKT_CNT[12]	0
Bit 11	R/W	PKT_CNT[11]	0
Bit 10	R/W	PKT_CNT[10]	0
Bit 9	R/W	PKT_CNT[9]	0
Bit 8	R/W	PKT_CNT[8]	0
Bit 7	R/W	PKT_CNT[7]	0
Bit 6	R/W	PKT_CNT[6]	0
Bit 5	R/W	PKT_CNT[5]	0
Bit 4	R/W	PKT_CNT[4]	0
Bit 3	R/W	PKT_CNT[3]	0
Bit 2	R/W	PKT_CNT[2]	0
Bit 1	R/W	PKT_CNT[1]	0
Bit 0	R/W	PKT_CNT[0]	0

The Packet Generator Count Control register provides control over the Packet Generator capabilities. The QuadPHY 1GR provides a Packet Generator Count Control register for each channel.

PKT_CNT[14:0]

The PKT_CNT bits define the total number of frames that the Packet Generator sends for an associated channel.

In order to generate a fixed number of packets, the desired packet count must be first written into PKT_CNT[14:0], then the packet generator must be turned on by setting Bit 15 in register 0x1B to a logic 1 (EN_PKT_GEN). Once the packet generator finishes sending packets, it returns to sending idle pairs. Additional sets of packets can be generated by toggling the EN_PKT_GEN bit from a logic 0 to a logic 1.

PKT_CNT is also used to define the 8B/10B code error threshold, CODE_ERR_THR, when EN_CODE_ERR_CHK is set to a logic 1. The 8B/10B code error counter within the decoder logic counts received code errors and indicates that the count has exceeded the CODE_ERR_THR count by setting CODE_ERR_EXCEED to a logic 1. The valid range for the Code Error Threshold is 0x0000 to 0x7FFE. A value of 0x7FFF does not set the CODE_ERR_EXCEED to a logic 1.

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CONT_TEST_GEN

The CONT_TEST_GEN bit controls whether the Packet Generator for an associated channel sends continues frames or if it sends the PKT_CNT[14 :0] number of frames. If the CONT_TEST_GEN bit is set to a logic 1, it sends an unlimited number of frames. If it is set to a logic 0, the number of frames is limited by the value set in the PKT_CNT[14 :0] bits.

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11 Test Features Description

11.1 Packet Generator and Packet Comparator

The device has one packet generator and one packet comparator for each channel: a packet generator is located within the transmit logic of each channel; a packet comparator is located within the receive logic of each channel.

Turning on a particular packet generator causes the transmit logic to ignore data on that lanes' transmit parallel input ports. Normally, this data is serialized and sent to its respective serial output; however, with the packet generator enabled, the output of the packet generator is serialized instead, and then sent to its respective serial output.

When a packet comparator is enabled, data which is received goes to the packet comparator. The data coming out of its respective parallel outputs should be ignored

The packet generator and comparator can only be operated while the device is configured for this specific mode. RGMII_RTBIB pin should be set to logic 0 to disable PCS, 8B/10B should be enabled by setting INT_DEC_ENC_EN of register 0x11 to logic 1, Receive FIFO should be enabled by setting CTC_EN pin logic 1. The COMMA_DETECT_SEL register bits in register 0x10 have to set to "11" to detect both positive and negative commas. This device does not support other modes.

The packet generators and packet comparator are for test and diagnostics of the part. Normal operations on any of the four channels are not recommended. Since no logic is included to provide graceful transitions between normal operating and packet generation, transition artifacts are likely to occur at the parallel receiver outputs. When disabling the packet generator, a soft reset is recommended for proper device operation.

11.1.1 Practical Uses of the Packet Generator and Packet Comparators

The most straightforward use of the packet generators and packet comparators is to enable them while in internal serial loopback mode. When used in this mode, the packet generator of channel A communicates to the packet comparator of channel A, the packet generator of channel B communicates to the packet comparator of channel B, etc. By using internal serial loopback and these packet generators and packet comparators, the operation of individual channels can be confirmed within a device. This checks the majority of the analog and digital circuitry within this particular channel; however, it does not check analog or digital I/O.

The packet generator of a particular lane does not necessarily have to be used with the packet comparator of that same lane. For a particular serial link, the packet generator of one device can communicate to the packet comparator of another device. This mechanism is useful for verifying that a particular link is working. This also tests the analog outputs of the packet generating device and the analog inputs of the packet receiving device.

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11.1.2 Packet Generator Operation

The packet generator creates a repetitive pattern of packets and IPG. The pattern is created as 8B data. The packet generator is started by setting the EN_PKT_GEN bit (Register 0x1B, bit 15). It sends the number of packets (N) and then idles until it is disabled. The packet data is fixed and contains 256 characters starting with 00h and incrementing to FFh. N ranges from 1 to (2^{15}-1) or is continuous. Register 28 sets N. When the generator is enabled, idle pairs (for IPG) are sent before packets (256 idle pairs), between packets (10 idle pairs) and after the packets continuously until the generator is disabled.

Errors can be introduced into the data packet, for testing the packet comparator logic being stuck-at-0, by setting the FORCE_ERROR bit (Register 0x1B bit 12). This is a self-clearing bit that creates one error each time it is set. An error is created by replacing a character with the repeat of the preceding character instead of the next character in the sequence. For instance, if the FORCE_ERROR bit is sensed during a data packet when 07h is being generated, the character after 07h would normally be 08h, but 07h would be sent in its place. If the FORCE_ERROR bit is sensed during the IPG, SOP or EOP, 00h, 00h, 02h, etc. is sent at the start of the packet instead of the normal 00h, 01h, 02h, etc. Finally, if the error is sensed during FFh, the EOP is replaced with the data character FFh.

11.1.3 Packet Comparator Operation

The packet comparator looks for packets of 256 bytes starting with 00h and incrementing to FFh that are framed by SOP and EOP. Idles are not checked or counted. If SOP is encountered and the subsequent 257 characters are not 00h to FFh and EOP, the error count in Register 0x1B is incremented.

To start the packet checker, EN_PKT_COMP, Register 0x1B, bit 14, must be set to 1. The error count is cleared by setting ERROR_CT_RESET = 1 (Register 0x1B, bit 13). ERROR_CNT_RESET is self-clearing.

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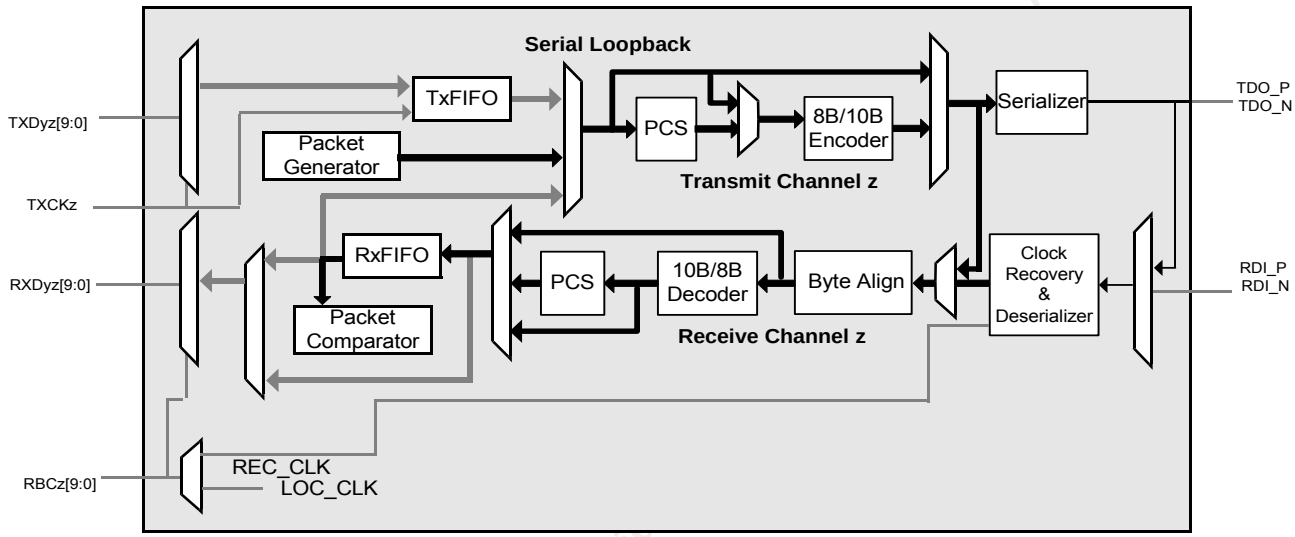
Figure 19 Serial Loopback Data Path with Packet Generator/Comparator Enabled



Links between two different QuadPHY 1GR devices can also be tested by enabling the appropriate packet generator in the source QuadPHY 1GR device and the packet comparator in the sink QuadPHY 1GR device. Serial Loopback in both devices must be disabled.

11.2 JTAG Test Access Port

The QuadPHY 1GR JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 17 Instruction Register

Length - 3 bits

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Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 18 Identification Register

Length	32 bits
Version number	0x0
Part Number	0x8363
Manufacturer's identification code	0x0CD
Device identification	0x083630CD

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12 Operation

12.1 SERDES or RTBI Configuration

The QuadPHY 1GR device can start in hardware for SERDES or RTBI mode by setting:

RGMII_RTBIB = 0;
CTC_EN = 0;
G_DIGLB = 0.

12.2 GE PCS or RGMII Configuration

The QuadPHY 1GR device can start in hardware for GE PCS or RGMII mode by setting:

RGMII_RTBIB = 1;
CTC_EN = 0 if no clock rate compensation; CTC_EN = 1 if clock rate compensation is required;
G_DIGLB = 0.

12.3 Parallel Loopback

To use parallel loopback while in RGMII mode, please set CTC_EN to logic 1. CTC_EN is controllable thorough the configuration pin or through register bit 12 in register 18h.

To use parallel loopback while in RTBI mode you must first configure the QuadPHY 1GR to operate in a diagnostic mode. This is necessary because the Rx FIFO operation must be enabled in order to use the parallel loopback feature. The incoming traffic has to be 8B/10B encoded. The following procedure shows the configuration changes that are required when operating in RTBI mode before parallel loopback can be used.

1. RGMII_RTBIB pin should pulled/driven LOW

2. Toggle the RESET PIN on the chip

3. Enable the encoder/decoder - write 2380h to address 0x11h

4. Enable clock tolerance compensation – write 1500h to address 0x18h (alternatively the CTC_EN pin can be driven HIGH before step 2)

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12.4 Power-up

The QuadPHY 1GR device can start in hardware only mode, without any microprocessor interface in all major operational modes. However, a microprocessor interface is required for testing and debugging within the QuadPHY 1GR, as well as activating various Loopback and packet generation/checking functions. Table 19 shows pins that are available on the QuadPHY 1GR for hardware only configuration.

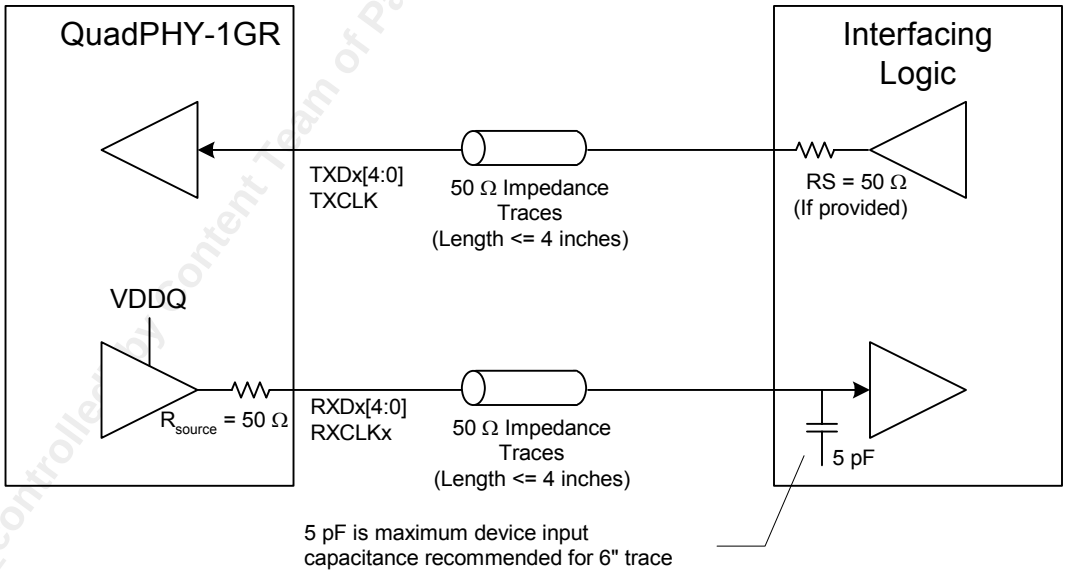
Power can be applied to the QuadPHY 1GR pins in any order. This includes the condition where VDD and VDDA are 1.8 Volts and VDDQ = 1.5 Volts or 1.8 Volts and VDDS = 1.8 Volts or 2.5 Volts. A hardware reset is required after power-up.

12.5 Parallel Interface

The parallel interface uses HSTL input and output buffers that can operate at either 1.5 volt or 1.8 volt levels. The output buffer has an integrated series termination resistor to produce a 38 Ω to 50 Ω output impedance. The input buffer is HSTL input, with no internal parallel terminations. Figure 20 shows the recommended configuration of the parallel interface.

The interface is designed to operate over un-terminated 50 Ω PCB traces. The maximum length of each trace should not exceed 4 inches. If trace lengths greater then 4 inches are necessary, PMC-Sierra strongly recommends performing transmission line modeling and analysis to evaluate the actual performance of the interface.

Figure 20 Parallel Receive and Transmit Interface



The voltage levels that are present at the parallel interface inputs of the "interfacing logic" are functions of silicon process variation, temperature, and voltage supply. In addition, they are affected by:

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- trace impedance
- length of the interconnecting trace
- capacitance of the input of the "interfacing logic"
- frequency of operation

It is important to note that these voltage levels do not necessarily correspond to the Voh and Vol levels that are specified in Section 16. PMC-Sierra recommends that transmission line modeling and analysis be used to determine the dynamic performance of the interface with a specific application

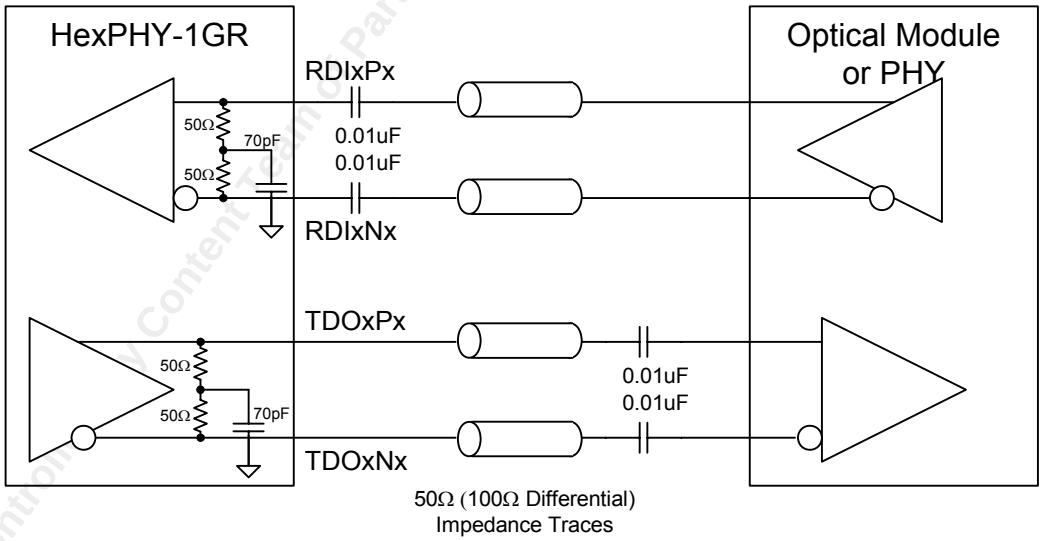
12.6 High-Speed Serial Interface

As shown in Figure 21, the high-speed serial interface is a set of differential drivers and receivers operating over 50 Ω transmission lines. The serial transmit outputs are internally terminated, complementary current-sourcing drivers. The serial receive inputs are differential receivers with internal 100Ω differential terminations.

For proper operation, all high-speed inputs must be capacitively coupled, as shown in Figure 21. The QuadPHY 1GR is internally biased to the proper DC operating point.

The equivalent line length difference between the P and N of the high speed inputs should be less than or equal to 5/16 of an inch (less than 50 ps of skew on FR4 material).

Figure 21 High-Speed Serial Interface



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12.7 Clock Requirements

REFCLK is a maximum 125 MHz ±100 ppm 40/60 or better oscillator. The maximum jitter allowed is 50 ps peak to peak, or approx 7 ps rms. REFCLK feeds 2.5/1.8 V CMOS input. The oscillator requires good power supply rejection to provide a low jitter clock input to the device. The driving crystal oscillator may be capacitively coupled to REFCLK and biased around the switching threshold of the REFCLK input.

12.8 Hardware/Software Configuration Options

The following table summarizes the relationships between the terminals and registers used to configure the *QuadPHY 1GR.*

Table 19 Hardware/Software Configuration Options

Function	Terminals	Bit Name (Register Bit)	Relationship with S/W-H/W
8B/10B Encode/Decode	RGMII_RTBIB	INT_DEC_ENC_ENABLE (Reg 0x11, Bit 7)	OR
PCS Logic Enable	RGMII_RTBIB	PCS_ENABLE (Reg 0x11, Bit 2)	OR
TCLK Selection	TCLKSEL	INT_TCLKSEL (Reg 0x11, Bit 15)	OR
Parallel Output Enable	POEN	IPOEN (Reg 0x11, Bit 9)	AND
Parallel Loopback	G_DIGLB	INT_EN_SERIAL_[D:A] (Reg 0x16) and DIGITAL_LPBK_EN (Reg 0x18, Bit 7)	OR
Clock Compensation Enable	CTC_EN	INT_CTC_EN (Reg 0x18, Bit 12)	OR

12.9 Analog Considerations

A precision resistor must be connected between the PRES terminal and ground to provide a reference for internal bias circuits. The value of PRES must be 10kΩ ± 1%.

12.10 JTAG Considerations

A pull-down resister connected to the QuadPHY 1GR's TRSTB pin is recommended to assure that the JTAG TAP Controller remains in a reset state during normal operation of the device.

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13 Functional Timing

This section outlines the functional timing for the MDC/MDIO serial port. The functional timing for the receive and transmit parallel ports is described in detail in Sections 10.2.3 and 10.2.4.

13.1 MDC/MDIO Interface

The MDC/MDIO interface is a 2-wire single master, multi-slave protocol. The master device sources the clock (MDC) to all slaves. The tri-state data (MDIO) wire is attached to all devices and is used for reading and writing. Figure 22 contains functional timing for an MDC/MDIO write cycle. A 32-bit preamble (PRE) can be skipped if the STA determines that all PHY devices can handle management frames without it.

Figure 22 MDC/MDIO Write Cycle

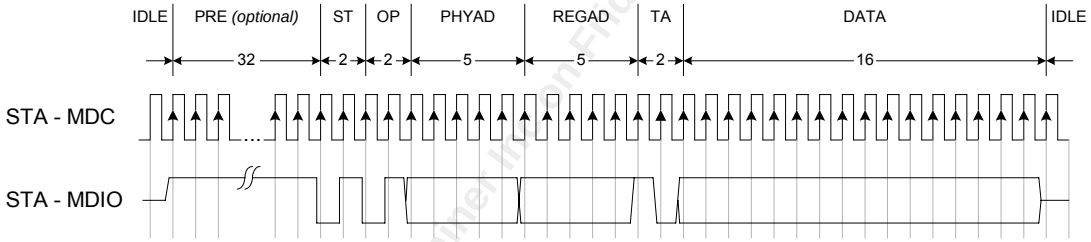
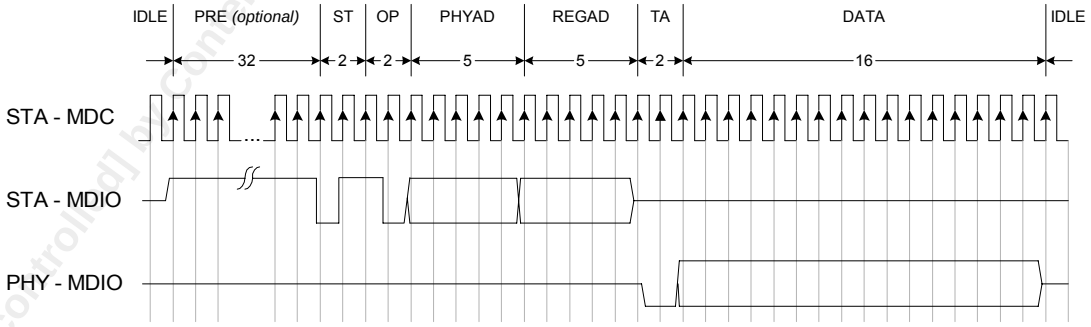


Figure 23 demonstrates an MDC/MDIO read cycle. Here too, the 32 bit preamble can be optionally skipped if the STA determines that all the PHY devices can handle management frames without it.

Figure 23 MDC/MDIO Read Cycle



It is required for a preamble to be applied to the MDC/MDIO interface whenever an error has occurred during an access. This allows the interface to recover from the error. In the case of a free running MDC clock, this can be accomplished by having a pause in the interface, since the MDIO pin is pulled-up when not in use.

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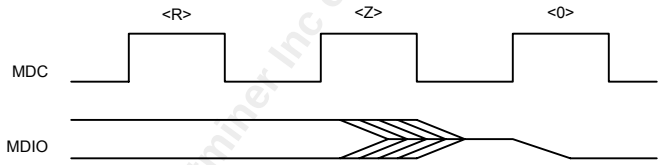
Notes:

1. IDLE – Idle. The period when data transfer on MDIO is inactive. The MDC clock may stall until the next transfer or continue to run.
2. PRE[31:0] – Preamble. An optional stream of 32 - 1's which assures the receive logic that a transfer is about to occur.
3. ST[1:0] – Start bits. This is always a 0b01.
4. OP[1:0] – Operation Code. A read is an 0b10 and a write is an 0b01.
5. PHYAD[[4:0] – PHY Address. This is the 5 bit address in which this device compares to its internal address.
6. REGAD[4:0] – Register Address. This is the specific register within the selected address.
7. TA[1:0] – Turn Around Cycle. This is a 2 bit time spacing interval which exists to avoid contention on the MDIO net during a read cycle.
8. DATA[15:0] – Data. This is either read data supplied by the slave or write data supplied by the master.

Figure 24 shows how the MDIO signal transitions during the turn around cycles of a read transaction. These turn around cycles are necessary to avoid contention on the MDIO net.

Figure 24 Behavior of MDIO During TA Field of a Read Transaction



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14 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 20 Maximum Ratings

Case Temperature Under Bias	-40 C to +125 C
Storage Temperature	-40 C to +125 C
2.5V Supply Voltage (VDDS)	-0.3 V to 3.6 V
1.8V Supply Voltage (VDDI, VDDQ)	-0.3 V to +2.5 V
Input pad tolerance	-2 V < Vpin < VDDQ +2 V for 10 ns, 100 mA max
Output pad overshoot limits	-2 V < Vpin < VDDQ +2 V for 10 ns, 100 mA max
Voltage on Digital Input or Bidirectional Pin w/VDDS	-0.3 V to VDDS + 0.3 V
Voltage on Digital Input or Bidirectional Pin w/VDDQ	-0.3 V to VDDQ + 0.3V
Voltage on any Digital Output Pin w/VDDQ	-0.3 V to VDDQ + 0.3 V
Voltage on any Differential Pin	-0.3 V to V_{DD} + 0.3 V
Static Discharge Voltage	±2000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead/Ball Temperature	+225 +0, -5 °C
Absolute Maximum Junction Temperature	+150 °C

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15 Power Information

15.1 Power Requirements

Table 21 Power Requirements

Conditions	Parameter	Typ[1,3]	Thermal[4]	Max[2]	Units
4 Ports Enabled, V_{DDQ} = 1.8V	I_{DD} (V_{DD}=1.8V)	351	—	631	mA
	I_{DDA} (V_{DDA}=1.8V)	60	—	115	mA
	I_{DDS} (V_{DDS}=1.8V)	15	—	18	mA
	I_{DDQ} (V_{DDQ}=1.8V)	140	—	175	mA
	P (V_{DDQ}=1.8V)	0.95		1.3	W
4 Ports Enabled, V_{DDQ} = 1.5V	I_{DD} (V_{DD}=1.8V)	351	—	631	mA
	I_{DDA} (V_{DDA}=1.8V)	60	—	115	mA
	I_{DDS} (V_{DDS}=1.8V)	15	—	18	mA
	I_{DDQ} (V_{DDQ}=1.5V)	140	—	175	mA
	P (V_{DDQ}=1.5V)	0.9	—	1.25	W

Notes:

1. Outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity
2. Power values are calculated using the formula:

$$\text{Power} = \sum i(VDD \times IDD)$$

Where i denotes all the various power supplies on the device, VDD is the voltage for supply i in accordance with the condition, and IDD is the current for supply.

Table 22 Conditions For Power Requirements

	Typical	Power For Thermal Calulations	Maximum Current
Process	Nominal	Nominal +2 sigmas of process variation*	Nominal +6 sigmas of process variation
Voltage	Nominal Vdd	Maximum Operating Vdd	Maximum Vdd
Temperature	Tj=25C	Tj=105C	Temperature that yields the highest current

15.2 Power Supply Decoupling

V_{DD} should be decoupled as close to the pins as possible. The recommended decoupling capacitor size is 0402 or 0603. The ground for the capacitors should be a solid ground plane.

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One 0.1 µF decoupling capacitor should be used for every two VDD, VDDS and VDDQ pins

One 10 µF filtering cap should be used on each of the VDD and VDDQ power rails. Taiyo Yuden PN # LMK325BJ106MN or Panasonic PN # ECJ-3YB0J106K are the recommend components.

In order to minimize the intrinsic jitter on the TDO outputs, RC filtering of the VDDA supply voltage is required. The values shown in Figure 25 were chosen to minimize the IR drop on the VDDA supply voltage, yet provide sufficient filtering of power supply noise at low frequencies.

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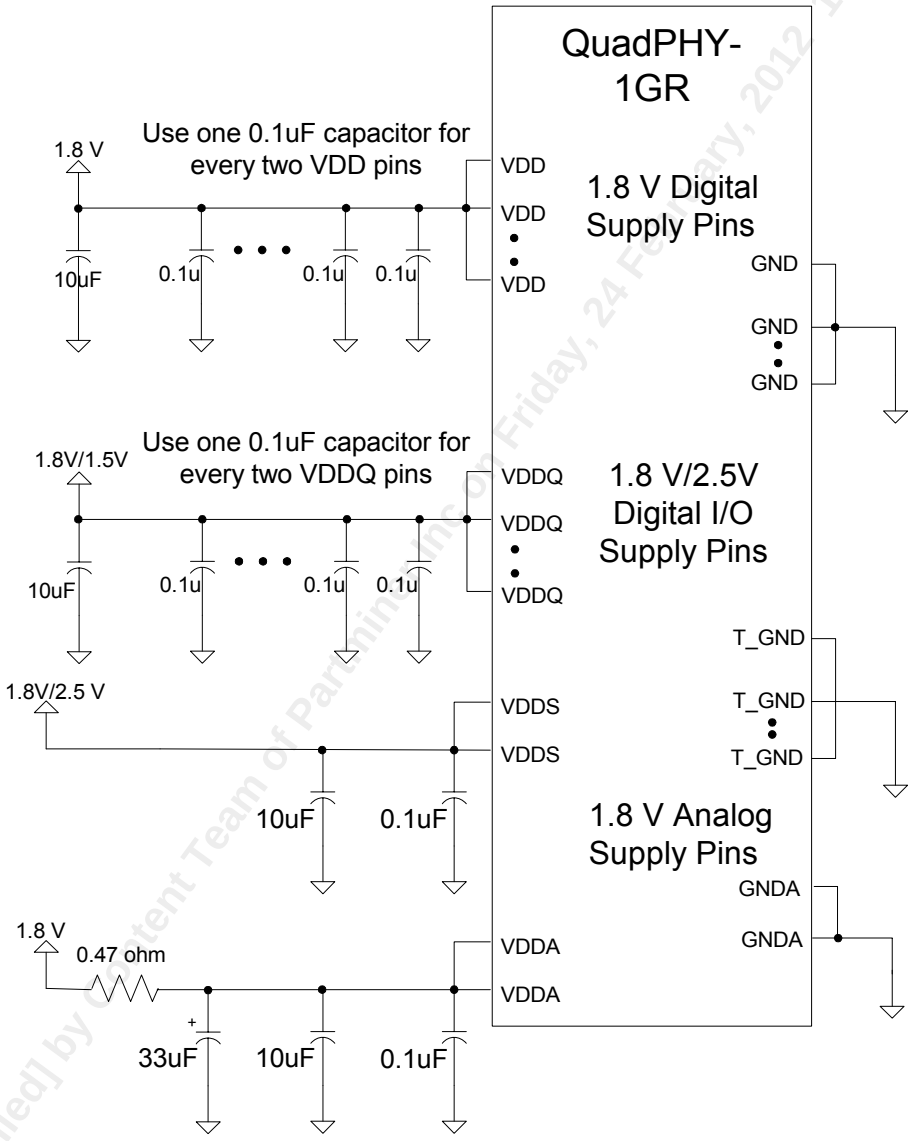
Figure 25 Recommended Power Supply Decoupling



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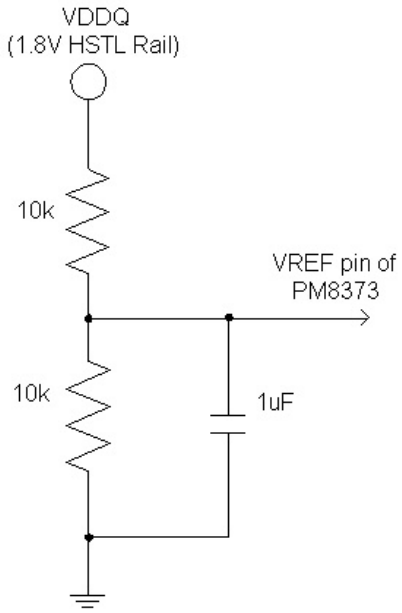
15.3 VREF Decoupling

PMC-Sierra recommends filtering the VREF input of the PM8373 using a 1uF ceramic capacitor X5R (X7R) type (not tantalum or Y5V's) to achieve the best frequency response and lowest ESR. Recommended capacitors are Panasonic PN# ECJ-2YB1A105K or Kemet PN# C0805C105K8RACTU. VREF has a requirement that the noise on at this pin does not exceed 5% of the DC voltage present at the VREF pin. Figure 26 shows the recommended filtering circuit for the VREF pin. 1% tolerance resistors are required to set the HSTL VREF voltage.

Figure 26 VREF Filtering Circuit



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16 D.C. Characteristics

Unless otherwise stated, the following parameters are provided given the following conditions: Ta = -40° C to Tj = 125° C, V_{DD} = 1.8 V ±5%, $V_{DD}Q$ = 1.8 V ±5% or 1.5 V ±5%, $V_{DD}S$ = 1.8 V ±5% or 2.5 V ±5%, $V_{DD}A$ = 1.8 V ±5%

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Table 23 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Core power supply	1.71	1.80	1.89	V	
V_{DDQ}	HSTL I/O power supply					
	VDDQ = 1.5 V	1.425	1.50	1.575	V	
	VDDQ = 1.8 V	1.71	1.80	1.89	V	
V_{DDS}	LVCMOS I/O power supply					
	VDDS = 1.8 V	1.71	1.80	1.89	V	
	VDDS = 2.5 V	2.375	2.50	2.625	V	
V_{DDA}	Analog power supply	1.71	1.80	1.89	V	
VREF	HSTL reference Voltage					
	VDDQ = 1.5 V	0.7	0.75	0.79	V	
	VDDQ = 1.8 V	0.86	0.90	0.95	V	
LVCMOS V_{IL}	Input Low Voltage					Guaranteed Input LOW Voltage
	VDDS = 1.8 V			0.59	V	
	VDDS = 2.5 V			0.87		
LVCMOS V_{IH}	Input High Voltage					Guaranteed Input HIGH Voltage
	VDDS = 1.8 V	1.24			V	
	VDDS = 2.5 V	1.63				
HSTL V_{IL}	Input Low Voltage					VREF min – 0.1
	VDDQ = 1.5 V			0.60	V	
	VDDQ = 1.8 V			0.76	V	
HSTL V_{IH}	Input High Voltage					VREF max + 0.1
	VDDQ = 1.5 V	0.89			V	
	VDDQ = 1.8 V	1.05			V	
LVCMOS V_{OL}	Output or Bidirectional Low Voltage				V	I_{OL} = -1.0 mA all outputs
	VDDS = 1.8 V			0.3		
	VDDS = 2.5 V			0.4		
LVCMOS V_{OH}	Output or Bidirectional High Voltage				V	I_{OH} = 0.5 mA all outputs
	VDDS = 1.8 V	VDDS – 0.2				
	VDDS = 2.5 V	VDDS – 0.3				
HSTL V_{OL}	Output or Bidirectional Low Voltage					I_{OL} = 8 mA
	VDDQ = 1.5 V			0.4	V	
	VDDQ = 1.8 V			0.4	V	

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Symbol	Parameter	Min	Typ	Max	Units	Conditions
HSTL V_{OH}	Output or Bidirectional High Voltage VDDQ = 1.5 V VDDQ = 1.8 V	 1.0 1.31			 V V	I_{OH} = 6 mA
I_{ILPUH}	HSTL Input Low Current (pull-up terminals)			50	µA	V_{IL} = 0 V (note 1)
I_{IHPUH}	HSTL Input High Current (pull-up terminals)			10	µA	$V_{IH} = V_{DDQ}$ (note 1)
I_{ILPD}	Input Low Current (LVCMOS pull-down terminals)			20	µA	V_{IL} = 0 V (note 3)
I_{IHPD}	Input High Current (LVCMOS pull-down terminals)			50	µA	$V_{IH} = V_{DDQ}$ (note 3)
I_{OLPOH}	HSTL Output Low Leakage Current (no pull-up terminals)			10	µA	
I_{OHPH}	HSTL Output High Leakage Current (no pull-up terminals)			10	µA	
LVCMOS I_{IL}	Input Low Current			100	µA	V_{IL} = 0 V (note 2)
LVCMOS I_{IH}	Input High Current			100	µA	$V_{IH} = V_{DDQ}$ (note 2)
HSTL I_{IL}	Input Low Current			10	µA	V_{IL} = 0 V (note 2)
HSTL I_{IH}	Input High Current			10	µA	$V_{IH} = V_{DDQ}$ (note 2)
C_{IN}	Input Capacitance (MDC/MDIO TDI TCK REFCLK and control terminals)	—	1.5	—	pF	T_A = 25 C, f = 1 MHz (note 7)
C_{IO}	Output and Bidirectional Capacitance (MDIO/TDO and control terminals)	—	1.8	—	pF	T_A = 25 C, f = 1 MHz (note 7)
C_{INH}	HSTL Input Capacitance (parallel interface)			4	pF	
C_{IOH}	HSTL Output and Bidirectional Capacitance (parallel interface)			4	pF	
C_{INHS}	Input Capacitance (RDI terminals)	—	1.0	—	pF	T_A = 25 C, f = 1 MHz (note 7)

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Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{OUTHS}	Output Capacitance	—	1.0	—	pF	T_A = 25 C, f = 1 MHz (note 7)
L_{PIN}	Pin Inductance	—	2.5	—	nH	T_A = 25 C, f = 1 MHz (note 7)

Notes:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Input pin or bi-directional pin with internal pull-down resistor.
4. Input peak-to-peak differential voltage specified as RDI[D:A]_P minus RDI[D:A]_N.
5. Output peak-to-peak differential voltage specified as TDO[D:A]_P minus TDO[D:A]_N.
6. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
7. Typical values are given as a design aid. The product is not tested to the typical values given in the data sheet.

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17 Interface Timing Characteristics

Unless otherwise stated, the following parameters are provided given the following conditions: Ta = -40° C to Tj = 125° C, V_{DD} = 1.8 V ±5%, V_{DD}Q = 1.5 V ±5% or 1.8 V ±5%, V_{DD}S = 1.8 V ±5% or 2.5 V ±5%, V_{DD}A = 1.8 V ±5%

17.1 Reference Clock

Table 24 Reference Clock Timing

Symbol	Description	Min	Typ	Max	Units
REFCLK	REFCLK frequency for 933 Mbit/s operation.	93.2907	–	93.3093	MHz
REFCLK	REFCLK frequency for 1.0625 Gbit/s operation.	106.2394	–	106.2606	MHz
REFCLK	REFCLK frequency for 1.25 Gbit/s operation.	124.9875	–	125.0125	MHz
DCrefclk	REFCLK duty cycle	40	–	60	%
Peak to peak jitter on REFCLK	Wideband Peak to peak jitter on REFCLK (10 Hz–20 MHz) (RMS jitter is peak to peak jitter divided by 7) Narrowband peak to peak jitter on REFCLK (12 KHz –20 MHz)	– –	– –	50 20	ps
T_r/T_f, Refclk	REFCLK rise/fall time, 10% - 90% (maximum)	–	1000	–	ps
REFCLK to TXCKy phase deviation	Maximum phase deviation between REFCLK and TXCKy [1]	- 500	–	500	ps
F_lock	Frequency lock after reset	–	–	2.5	ms

Note:

1. The TXCLKy and the REFCLK must be synchronous. Once an arbitrary phase relationship is established, the phase deviation must not vary by more than ±500 ps. Should the phase change more than ±500ps, momentary corruption of data may occur.

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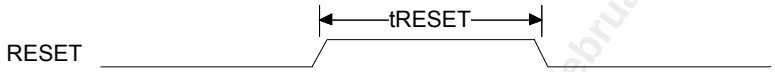
17.2 Asynchronous Reset

Table 25 QuadPHY 1GR Reset Timing

Symbol	Description	Min	Max	Units
t_{RES}	RESET High Pulse Width	500	—	ns
$t_{RESFALL}$	RESET Fall Time	—	10	ns

Figure 27 QuadPHY 1GR Reset Timing



17.3 MII Management Interface (MDC/MDIO)

Table 26 MDIO Timing

Symbol	Description	Min	Max	Units
f_{MDCMAX}	Clock Frequency (MDC)	0	10	MHz
$t_{MDCHIGH}$	MDC High Pulse Width	45	—	ns
t_{MDCLOW}	MDC Low Pulse Width	45	—	ns
$t_{MDCRISE}$	MDC Rise Time [1]	—	5	ns
$t_{MDCFALL}$	MDC Fall Time [1]	—	5	ns
$t_{MDIORISE}$	MDIO Input Rise Time [1]	—	5	ns
$t_{MDIOFALL}$	MDIO Input Fall Time [1]	—	5	ns
t_{MDIO_S}	MDIO Setup Time	10	—	ns
t_{MDIO_H}	MDIO Hold Time	10	—	ns
t_{pMDIO}	MDC to MDIO valid data	0	15	ns
t_{zMDIO}	MDC to MDIO high-impedence	—	10	ns

Notes:

1. MDC or MDIO rise times and fall times are measure from 10% to 90%.
2. For proper operation at the specified maximum MDC frequency, the MDIO load capacitance must not exceed 470 pf while operating up to 2.5 MHz and 100 pF while operating up to 10 MHz.

Figure 28 MDIO Timing Diagram

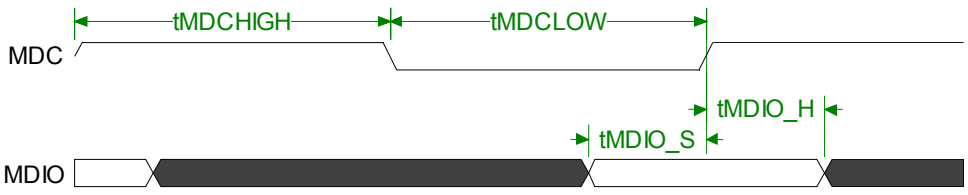


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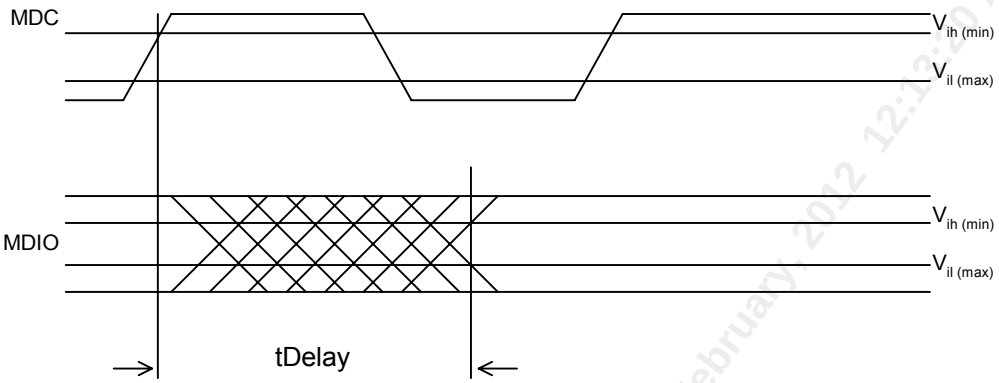
Figure 29 MDIO Sourced by PHY



17.4 JTAG

Table 27 JTAG Port Interface

Symbol	Description	Min	Max	Units
—	TCK Frequency	—	1	MHz
—	TCK Duty Cycle	40	60	%
t_{STMS}	TMS Set-up time to TCK	50	—	ns
t_{HTMS}	TMS Hold time to TCK	50	—	ns
t_{STDI}	TDI Set-up time to TCK	50	—	ns
t_{HTDI}	TDI Hold time to TCK	50	—	ns
t_{PTDO}	TCK Low to TDO Valid	2	50	ns
t_{VTRSTB}	TRSTB Pulse Width	100	—	ns
$t_{TRSTBRISE}$	TRSTB Rise Time	—	10	ns

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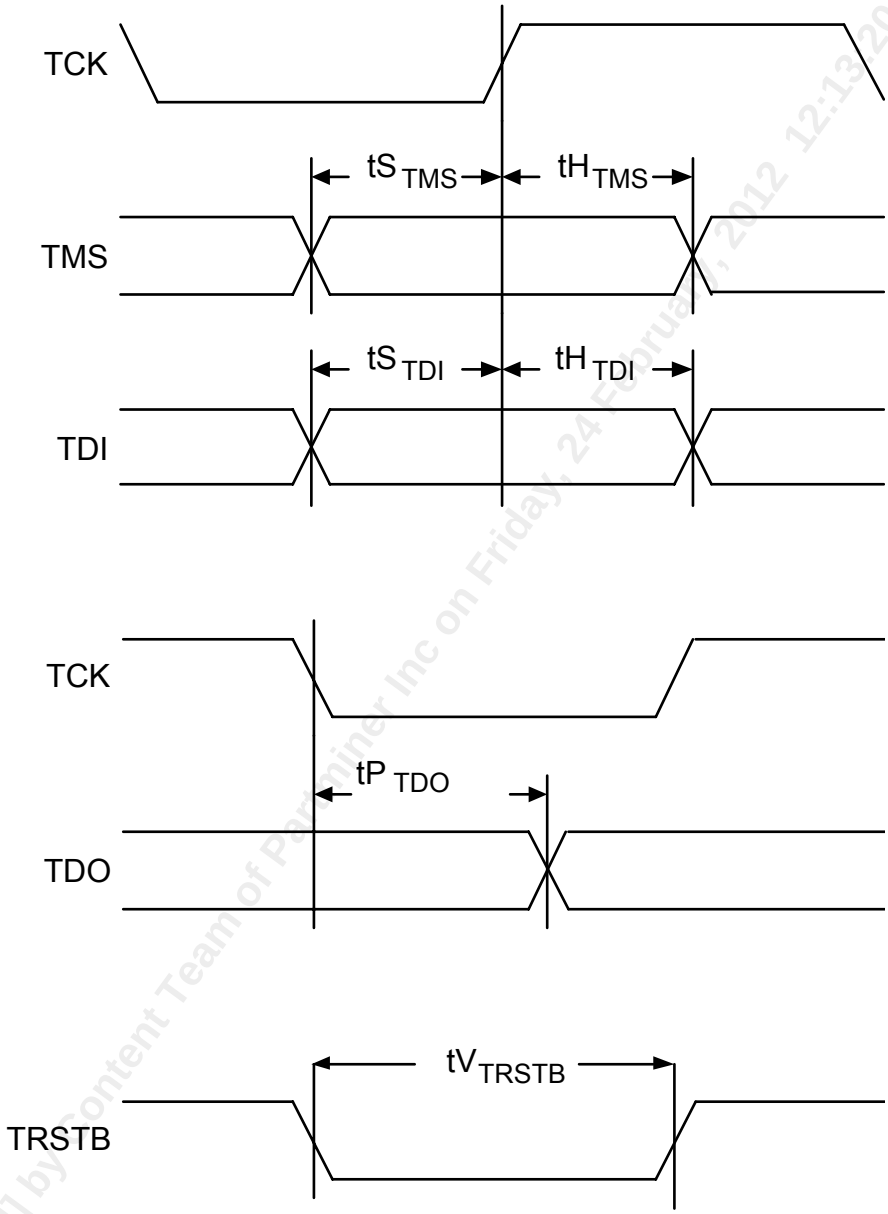
Figure 30 JTAG Port Interface Timing



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Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the VDD/2 Volt point of the input to the VDD/2 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the V_{DD}/2 Volt point of the clock to the V_{DD}/2 Volt point of the input.

Notes on Output Timing

1. Output propagation delay time is the time in nanoseconds from the VDD/2 Volt point of the reference signal to the VDD/2 Volt point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs

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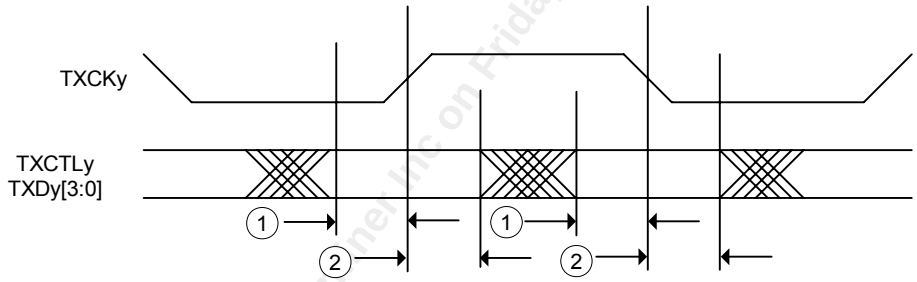
17.5 Transmit Timing

Table 28 Center Aligned DDR Transmit Timing

Number	Symbol	Parameter	Min	Typ	Max	Unit
		Tx Min Pulse Width				ns
1	t_{TS}	TXD setup time to TXCK (TCLKSEL = 1)	0.6	—	—	ns
		TXD setup time to TXCK (TCLKSEL = 0)	1.1	—	—	ns
2	t_{TH}	TXD hold time from TXCK (TCLKSEL = 1)	0.6	—	—	ns
		TXD hold time from TXCK (TCLKSEL = 0)	0.9	—	—	ns

Figure 31 Center Aligned DDR Transmit Timing



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17.6 Receive Timing

Table 29 Receive Timing (Center Aligned) [3]

Number	Symbol	Parameter	Min	Typ	Max	Unit
	D_{CRX}	Rx Clock Duty Cycle	40%		60%	
5	t_{RDV}	RXDy valid before RXCKy 106 MHz 125 MHz	 1.7 1.3	 — —	 — —	 ns ns
6	t_{RDH}	RXD hold after RXCKy 106 MHz 125 MHz	 0.9[4] 0.9[4]	 — —	 — —	 ns ns
—	t_{RDR}	Output rise time, 10%–90%, 10pF load for RXCKy	—	—		ns
—	t_{RDF}	Output fall time, 90%–10%, 10pF load for RXCKy	—	—		ns
—	B_sync	Time for Receive channel to lock to incoming data [2]	—	—	5	ms
—	t_{RXFTOL}	REFCLK/input data frequency difference	-200	—	200	ppm

Notes:

1. The outputs are 50 ohm source series internally terminated and are designed to drive a 50 ohm unterminated transmission line. The specifications are provided for reference when driving capacitive loads. Capacitive loads should be consistent across all data and clock pins on the Receive interface. PMC-Sierra strongly recommends that all trace lengths be matched on the Receive interface.
2. B_sync has been verified by design. Please refer to Clock and Data Recovery description in section 9.2.4 for conditions which impact B_sync.
3. The usage of internal delay to implement the center aligned clock-to-data relationship is referred to as RGMII-ID in RGMII v2.0.
4. Hold time can be extended (reducing valid time) by introducing some clock-to-data trace skew. To extend the hold time to 1.2ns (reducing valid time by 0.3ns) you must ensure that the clock trace is 1.8 inches longer (assuming FR4 dielectric) than the associated data traces.

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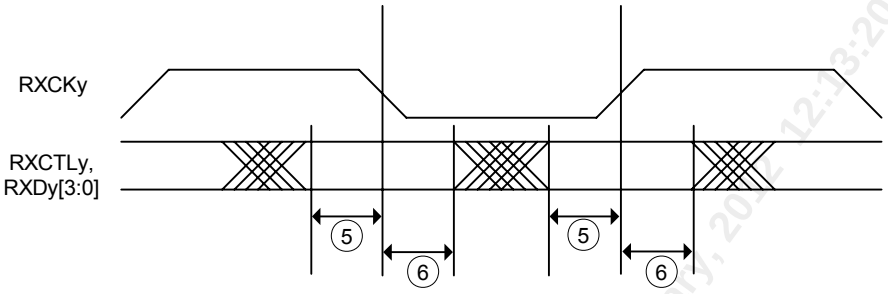
Figure 32 Parallel Receive Timing Diagram



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17.7 Receive Latency

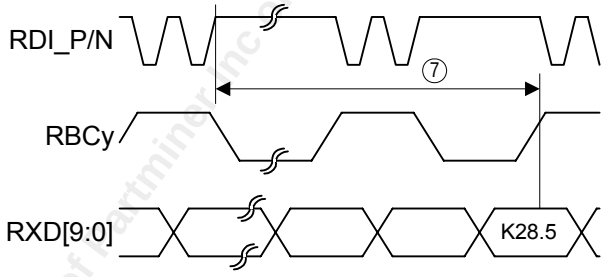
Table 30 Receive Latency Timing

Number	Symbol	Parameter	Min	Typ	Max	Unit
7	t_{RXLAT}	Receiver latency				
		decoder enabled, PCS on, Clock compensation enabled	165	—	345	Bits
		decoder enabled, PCS on, without clock compensation	110		134	Bits
		decoder disabled, PCS off, without clock compensation	30		50	Bits

Note:

1. The receiver latency, as shown in Figure 33 is defined as the time between receiving the first serial bit of a word and the clocking out of that parallel word (defined by the rising edge of REFCLK) when in Nibble Mode. If the FIFO is used, latency may increase.

Figure 33 Receive Latency



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17.8 Transmit Latency

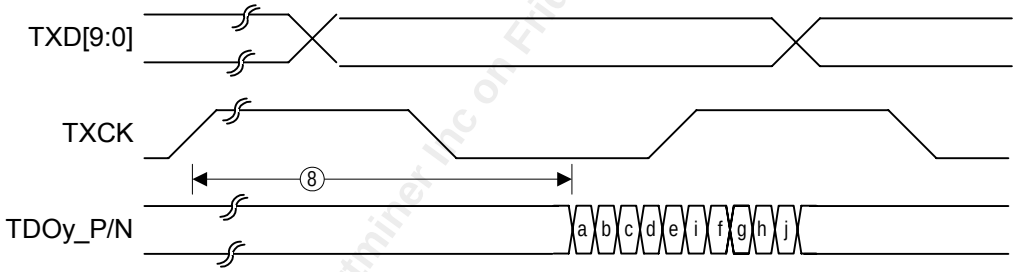
Table 31 Transmit Latency Timing

Number	Symbol	Parameter	Min	Typ	Max	Unit
8	t_{TXLAT}	Transmitter latency [1]				
		- encoder disabled, PCS off	66	—	92	Bits
		- encoder enabled, PCS on	106	—	141	Bits

Note:

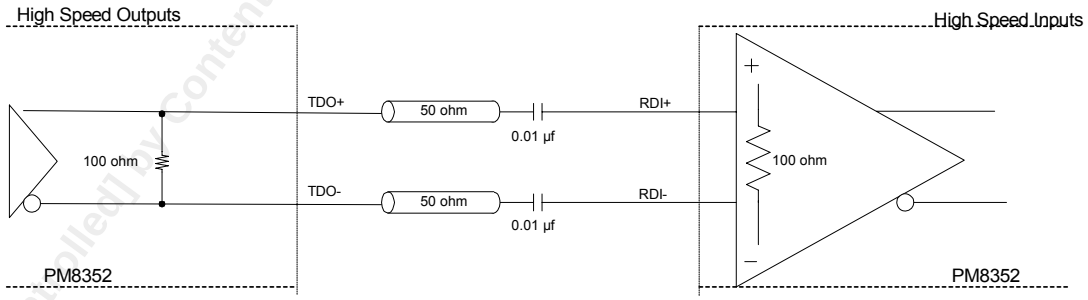
1. Independent of operating mode (channel interleave, trunking, nibble).
2. The transmitter latency, as shown in Figure 34, is defined as the time between the latching in of the parallel data word and the transmission of the first serial bit of that parallel word (defined byte the leading edge of the first bit transmitted.

Figure 34 Transmit Latency



17.9 High-speed Serial Timing Characteristics

Figure 35 933Mbit/s to 1.25 Gbit/s Serial I/O Block Diagram



Note:

1. The differential (100 Ω) terminating resistors have been implemented on-chip within the high-speed input buffer and should not be placed on the PC board. The capacitors are DC blocking caps. The TDO and RDI do not have the same common mode bias.

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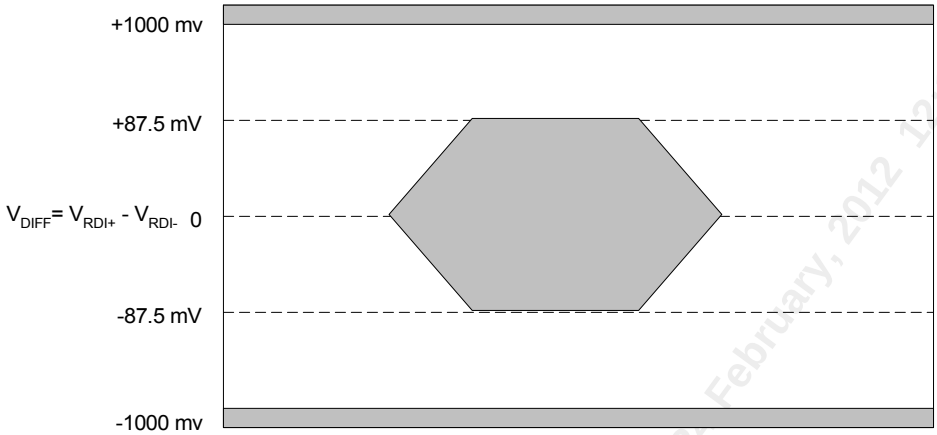
Figure 36 Differential Peak-Peak Receiver Eye Diagram



Note:

1. Minimum differential sensitivity (peak to peak) is 2x the magnitude of the minimum physical potential that can be expected across the differential pair.

   V_{DIFF} can be +100 mV for logic 1 or –100 mV for logic 0.

When viewing a data eye on an oscilloscope using a differential probe across terminals A and B, the top and bottom of the eye has a maximum separation of $V_{diff\ peak\ to\ peak}$. If the same signal is measured using a single ended probe attached to terminal A and referenced to GND, the top and bottom of the eye has a maximum vertical separation of $|V_{diff}|$. The single ended measurement technique yields a vertical eye opening equal to ½ the vertical eye opening of the differential measurement technique.

Definitions

Vdiff	Voltage of terminal A – Voltage of terminal B. Vdiff swings both positive and negative in value.
|Vdiff|	The magnitude of Vdiff. Vdiff is always a positive number and represents the maximum voltage that can exist between terminals A and B.
Vdiff peak-to-peak	Represents the peak to peak difference of the differential voltage Vdiff. Vdiff p-p is always be twice the magnitude of the maximum voltage that can exist between terminals A and B.

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Table 32 High-speed I/O Characteristics (V_{DD} = 1.8 V)

Symbol	Parameter	Min	Typ.	Max	Unit
$\|V_{RDI+} - V_{RDI-}\|$	High-speed input differential voltage magnitude	87.5	—	1000	mV pk differential
$V_{ID(ppk)}$	High-speed input peak-peak differential voltage	175	—	2000	mV pk – pk differential
$V_{OD(ppk)}$ [1]	High-speed output peak-peak differential voltage (High Amplitude Mode)	1070	—	1405	mV pk – pk differential
$V_{OD(ppk)}$ [1]	High-speed output peak-peak differential voltage (Low Amplitude Mode)	646	—	839	mV pk – pk differential
t_r, t_f [2]	High-speed output rise and fall times, 20 % – 80 %	100	—	200	ps
t_{SKEW}	Differential Output Skew between high-speed output terminals TDOx_P/_N	—	—	30	ps

Notes:

1. High-speed output peak-peak differential voltages are measured with 100 ohm external differential termination at the pin of the device.
2. Rise and Fall times (tr, tf) measured with board trace, connector and approximately 2.5pf load.

Table 33 Gigabit Ethernet Jitter Specifications[2]

T_J	Total output jitter	—	—	0.240	UI pk-pk
T_{DJ}	Deterministic output jitter	—	—	0.100	UI pk-pk
R_{RJT} [1]	Total Jitter Tolerance	—	—	0.749	UI pk-pk
R_{DJT}	Deterministic Jitter Tolerance	—	—	0.462	UI pk-pk

Table 34 Fibre Channel Jitter Specifications[3]

T_J	Total output jitter	—	—	0.21	UI pk-pk
T_{DJ}	Deterministic output jitter	—	—	0.10	UI pk-pk
R_{RJT}	Total Jitter Tolerance	—	—	0.70	UI pk-pk
R_{DJT}	Deterministic Jitter Tolerance	—	—	0.38	UI pk-pk
R_{SJT}	Sinusoidal Jitter Tolerance	—	—	0.10	UI pk-pk

Notes:

1. Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter.
2. The jitter values that are specified in Table 33 assume the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For the Gigabit Ethernet Standard the lower cutoff frequency for jitter is 750 kHz.
3. The jitter values that are specified in Table 34 assume the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For the Fibre Channel Standard the lower cutoff frequency for jitter is 637 kHz for 1.0625 Gbit/s operation.

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18 Thermal Information

Table 35 Outside Plant Thermal Information

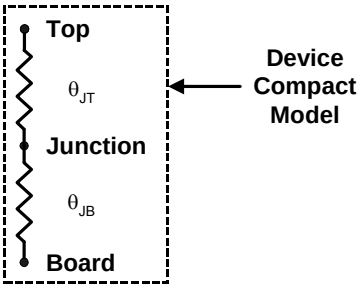
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition is typically reached when local ambient reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 36 Thermal Resistance vs. Air Flow[3]

Airflow	Natural Convection	200 LFM	400 LFM
θ_{JA} (°C/W)	35	29.6	27

Table 37 Device Compact Model[4]

Junction-to-Top Thermal Resistance, θ_{JT}	7 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	21.8 °C/W



Power depends upon the operating mode. To obtain power information, refer to Thermal power values in section 15 Power Requirements.

Notes:

1. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core; for more information about this standard, see [9].
2. θ_{JA}, the total junction to ambient thermal resistance, is measured according to JEDEC Standard JESD51 (2S2P); for more information about this standard, see [1].
3. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8 (for more information about this standard, see [8]) and θ_{JT}, the junction-to-top thermal resistance, is obtained by simulating conditions described in SEMI Standard G30-88 (for more information about this standard, see [10]).

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for use in outside equipment.

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Table 38 Outside Plant Thermal Information

Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 39 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	7 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	18 °C/W

Table 40 Heat Sink Requirements

θ_{SA}+ θ_{CS}[4]	The sum of θ_{SA} + θ_{CS} must be less than or equal to: [(105 - T_A) / P_D] - θ_{JC}] °C/W where: T_A is the ambient temperature at the heatsink location P_D is the operating power dissipated in the package
θ_{SA} and θ_{CS} are required for long-term operation[4]	

Power depends upon the operating mode. To obtain power information, refer to Thermal power values in section 15 Power Requirements.

Notes:

1. The minimum ambient temperature requirement for Outside Plant Equipment approximates the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core
3. The junction-to-case thermal resistance, θ_{JC}, is a measured nominal value plus two sigma. The junction-to-board thermal resistance, θ_{JB}, is obtained by simulating conditions described in JEDEC Standard JESD 51-8
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place

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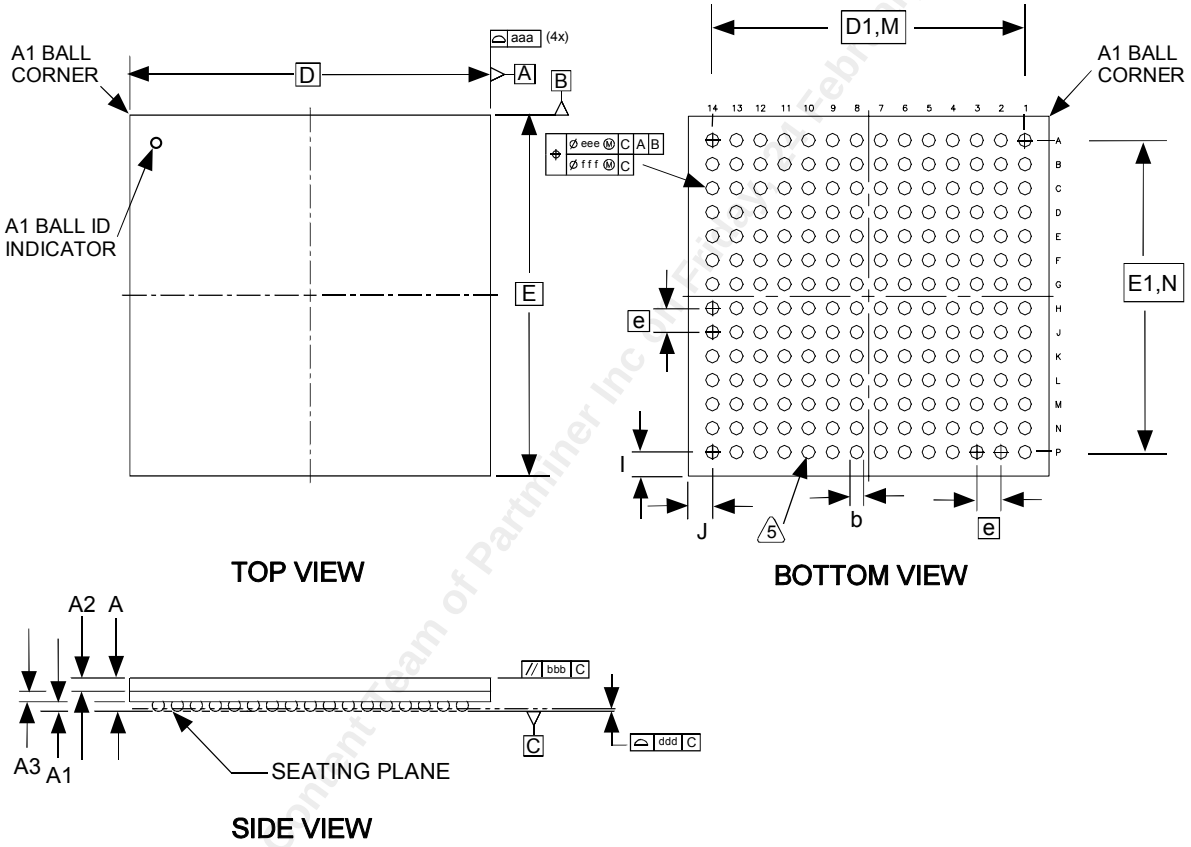
19 Mechanical Information

The package conforms to JEDEC JESD51 (2S2P).

Figure 37 196 PIN CABGA -15x15 MM BODY - (N SUFFIX)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) SOLDER MASK OPENING 0.435 +/- 0.03 MM DIAMETER (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MO-192, VARIATION AAE-1.

PACKAGE TYPE : 196 CHIP ARRAY BALL GRID ARRAY - CABGA																		
BODY SIZE : 15 x 15 x 1.40 MM																		
Dim.	A	A_1	A_2	A_3	D	D_1	E	E_1	M,N	I	J	b	e	aaa	bbb	ddd	eee	f f f
Min.	1.30	0.31	0.65	0.34	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Nom.	1.40	0.36	0.70	0.34	15.00 BSC	13.00 BSC	15.00 BSC	13.00 BSC	14x14	1.00	1.00	0.46	1.00 BSC	-	-	-	-	-
Max.	1.50	0.41	0.75	0.34	-	-	-	-	-	-	-	-	-	0.10	0.10	0.12	0.15	0.08

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20 Ordering Information

Table 41 Ordering Information

Part No.	Description
PM8363-NI	196-Pin CABGA, 15 x 15 x 1.62 mm, 1.00 mm BP
PM8363-NGI	196-Pin CABGA, 15 x 15 x 1.62 mm, 1.00 mm BP (RoHS-compliant)

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Notes

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